

VSC9187

VSC9187 Bromley - 3045 x 3045 VT1.5 TSI Switch Fabric



FEATURES:

- (3024x3024 (5 G) Non-Blocking VT1.5 TSI, 6048x6048 (10 Gb/s) VT1.5 TSI with 2:1 UPSR Input Pre-selection
- (2x9x622 Mb/s STS-12 LVDS Backplane Inputs with Integrated Retiming and Alignment
- (Working and Protection 2 x 9 x 622 Mb/s STS-12 LVDS Outputs
- (Supports 2:1 Hardware VT1.5 UPSR Selection when used in Conjunction with VSC9188 VT1.5 Pointer Processor and Column Aligner
- (6 Service & 6 Protection STS-1 like Serial 51.84 Mb/s Interfaces for Local Drop Interfaces
- (Integrated STS-1 Frame Delay Management on Output for use in Subtended STS-1 Switch Fabrics

KEY SPECIFICATIONS:

PARAMETERS	DESCRIPTION	Min	Max	Conditions
Vdd_core	Voltage for Core	1.65V	1.95V	Recommended 1.8V
Vdd_IO	Voltage of IO cells	2.3V	2.7V	Recommended 2.5V
POWER DISSIPATION				
IDD_2.5	Peak power supply current from 2.5V VDD		0.4 A	
IDD_1.8	Peak power supply current from 1.8V VDD		2.25 A	
PD_typical	Typical power dissipation		4 W	
PD_peak	Peak power dissipation		5 W	
Data STS-12 Inputs I/O	622Mb/s LVDS	–	–	Nominal
Service Data STS-1 Inputs I/O	51.84Mb/s LVDS	–	–	Nominal
STS1 Reference Clock Input	51.84MHz LVDS	51.83MHz	51.85MHz	Nominal

- (Compliant with SONET Requirements as Stated in ANSI T1.105 and Bellcore GR-253-CORE
- (Facilitates Hardware Based UPSR Switching in Accordance with Telcordia GR-1400-CORE
- (Thermally Enhanced 360 CCGA Package
- (IEEE P1149.1 Test Access Port

SPECIFICATIONS:

- (2.5/1.8V Power Supply; 0.18um Technology

APPLICATIONS:

- (VT1.5 Time Slot Interchange (TSI)

BENEFITS:

- (Low cost, low power, VT1.5 switching

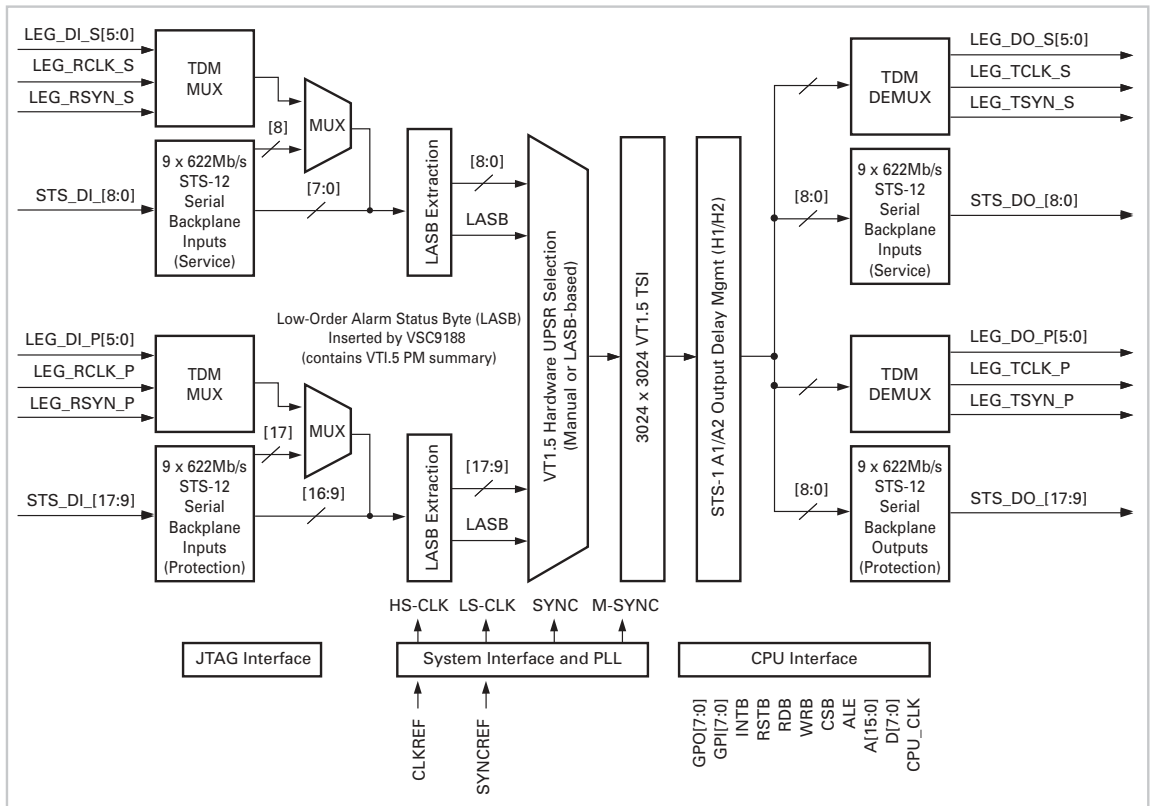
GENERAL DESCRIPTION:



The VSC9187 is a VT1.5 Time Slot Interchange (TSI) Device. It provides a fully non blocking cross connect for 3024 VT1.5's that are all frequency, phase and column aligned in addition to a pre-grooming 2:1 UPSR selection. The device receives 9 x 622 Mb/s STS-12 working and protection backplane inputs and performs all necessary functions to retime and align these signals from the backplane. VT1.5 tributaries are then pre-selected with a hardware 2:1 UPSR switch from the working

and protection timeslot with programmable holdover and pre-hold switch timers. The results of the 2:1 hardware selection are then made available to an internal 3024x3024 VT1.5 non-blocking grooming switch, allowing a 5G UPSR ring to be terminated. Alternatively, the 9 protection STS-12 backplane inputs can remain unused and the VSC9187 can act as a 5G VT1.5 switch. Output STS-1 delay management following the crossconnect allows the VSC9187 to be used in subtended switch applications with large scale STS-1 crossconnects such as the VSC9182 40Gb/s STS-1 TSI.

VSC9187 BLOCK DIAGRAM:



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