Vanguard Semiconductor

VSO030C04MC

40V N+P Channel Advanced Power MOSFET

Features

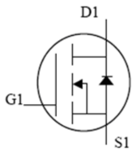
- N+P Channel
- Enhancement mode
- Very low on-resistance
- Fast Switching
- Pb-free lead plating; RoHS compliant

V_{DS}	40	-40	V
$R_{DS(on),TYP}$@ V_{GS}=±10 V	18	32	mΩ
$R_{DS(on),TYP}$@ V_{GS}=±4.5V	24	38	mΩ
I_D	8	-6	A

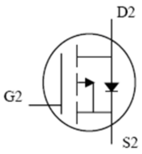
Pb-Free RoHS HF Halogen-Free

SOP8

Part ID	Package Type	Marking	Tape and reel information
VSO030C04MC	SOP8	030C04MC	3000pcs/Reel



N-Channel



P-Channel

Absolute Maximum Ratings

Symbol	Parameter		Rating		Unit
			NMOS	PMOS	
Common Ratings (T_C=25°C Unless Otherwise Noted)					
V_{GS}	Gate-Source Voltage		±20	±20	V
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage		40	-40	V
T_J	Maximum Junction Temperature①		150		°C
T_{STG}	Storage Temperature Range		-50 to 150		°C
I_S	Diode Continuous Forward Current	T_A=25°C	2.4	-2.4	A
Mounted on Large Heat Sink					
I_{DM}	Pulse Drain Current Tested②	T_A=25°C	32	-24	A
I_D	Continuous Drain Current	T_A=25°C	8	-6	A
		T_A=100°C	4.7	-3.5	
P_D	Power dissipation for Dual Operation	T_A=25°C	2		W
$R_{\theta JL}$	Thermal Resistance-Junction to Lead		50		°C/W
$R_{\theta JA}$	Thermal Resistance Junction-Ambient		62.5		°C/W

N-Channel Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=250μA	40	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current(T_A =25℃)	V_{DS}=40V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T_A =125℃)	V_{DS}=40V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.8	2.3	3.2	V
$R_{DS(ON)}$	Drain-Source On-State Resistance②	V_{GS}=10V, I_D=5A	--	18	25	mΩ
		V_{GS}=4.5V, I_D=3A	--	24	30	mΩ
Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
C_{iss}	Input Capacitance	V_{DS}=20V,V_{GS}=0V, f=1MHz	--	840	--	pF
C_{oss}	Output Capacitance		--	90	--	pF
C_{rss}	Reverse Transfer Capacitance		--	75	--	pF
R_g	Gate Resistance	f=1MHz	--	1.7	--	Ω
Q_g	Total Gate Charge	V_{DS}=20V,I_D=4A, V_{GS}=10V	--	12	--	nC
Q_{gs}	Gate Source Charge		--	2.3	--	nC
Q_{gd}	Gate Drain Charge		--	3.9	--	nC
Switching Characteristics						
$t_{d(on)}$	Turn on Delay Time	V_{DD}=20V, I_D=4A, R_G=3.3Ω, V_{GS}=10V	--	7	--	nS
t_r	Turn on Rise Time		--	12	--	nS
$t_{d(off)}$	Turn Off Delay Time		-	21	--	nS
t_f	Turn Off Fall Time		--	9	--	nS
Source Drain Diode Characteristics						
V_{SD}	Forward on voltage	I_{SD}=5A,V_{GS}=0V	--	0.82	1.2	V
t_{rr}	Reverse Recovery Time	T_j=25℃,I_{sd}=4A, V_{GS}=0V di/dt=-100A/μs	--	33	--	nS
Q_{rr}	Reverse Recovery Charge		--	20	--	nC

P-Channel Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=-250μA	-40	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current(T_A =25℃)	V_{DS}=-40V,V_{GS}=0V	--	--	-1	μA
	Zero Gate Voltage Drain Current(T_A =125℃)	V_{DS}=-40V,V_{GS}=0V	--	--	-100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=-250μA	-1.0	-1.7	-2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance②	V_{GS}=-10V, I_D=-5A	--	32	40	mΩ
		V_{GS}=-4.5V, I_D=-3A	--	38	45	mΩ
Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
C_{iss}	Input Capacitance	VDS=-20V,VGS=0V, f=1MHz	--	1520	--	pF
C_{oss}	Output Capacitance		--	155	--	pF
C_{rss}	Reverse Transfer Capacitance		--	110	--	pF
R_g	Gate Resistance	f=1MHz	--	24	--	Ω
Q_g	Total Gate Charge	VDS=-20V,ID=-3A, VGS=-10V	--	29	--	nC
Q_{gs}	Gate Source Charge		--	5	--	nC
Q_{gd}	Gate Drain Charge		--	11	--	nC
Switching Characteristics						
$t_{d(on)}$	Turn on Delay Time	VDD=-20V, ID=-3A, RG=3.3Ω, VGS=-10V	--	13	--	ns
t_r	Turn on Rise Time		--	38	--	ns
$t_{d(off)}$	Turn Off Delay Time		-	67	--	ns
t_f	Turn Off Fall Time		--	21	--	ns
Source Drain Diode Characteristics						
V_{SD}	Forward on voltage	I_{SD}=-5A,V_{GS}=0V	--	-0.83	-1.2	V
t_{rr}	Reverse Recovery Time	T_j=25℃,Isd=-3A, VGS=0V di/dt=-100A/μs	--	49	--	nS
Q_{rr}	Reverse Recovery Charge		--	35	--	nC

Notes: ① Repetitive rating; pulse width limited by max. junction temperature.

② Pulse width ≤ 300μs; duty cycle≤ 2%.

N-Channel Typical Characteristics

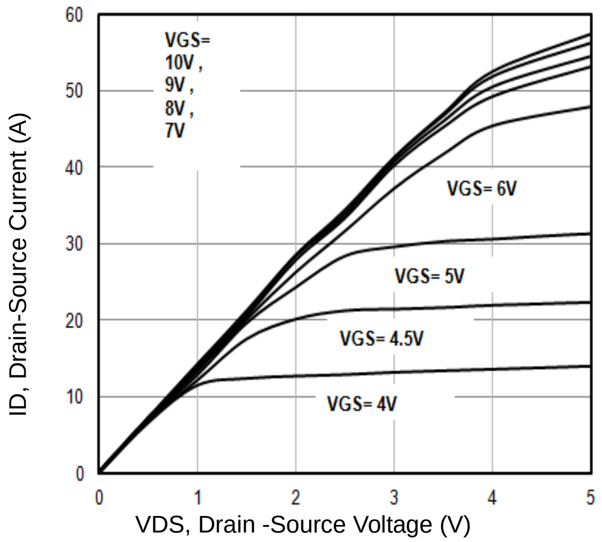


Fig1. Typical Output Characteristics

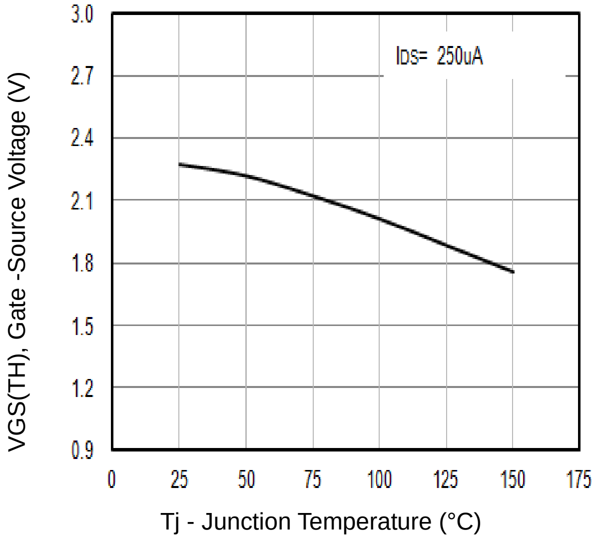


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs. Tj

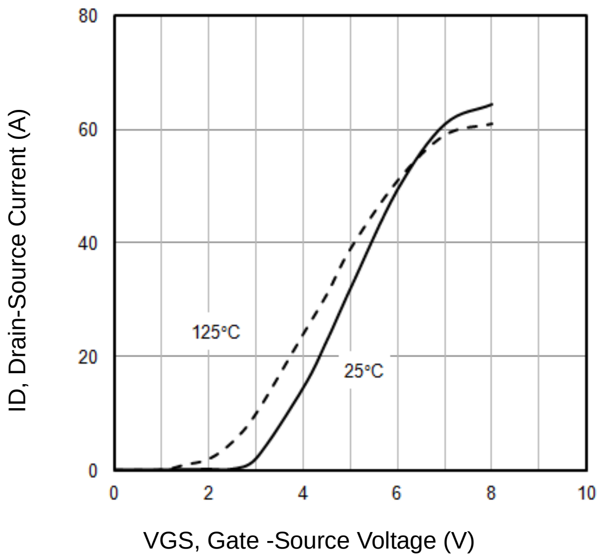


Fig3. Typical Transfer Characteristics

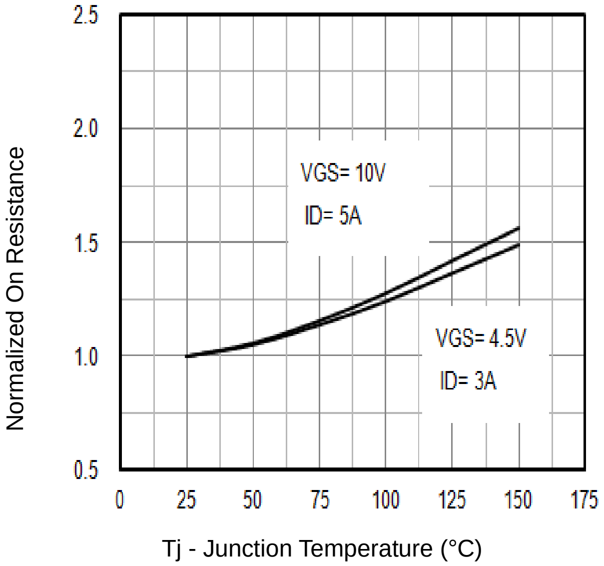


Fig4. Normalized On-Resistance Vs. Tj

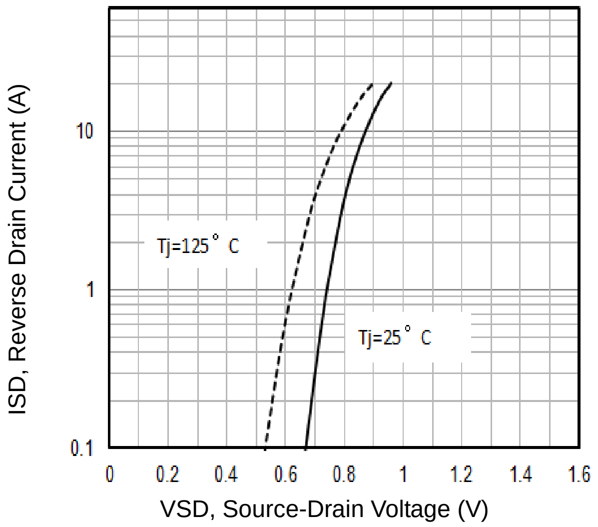


Fig5. Typical Source-Drain Diode Forward Voltage

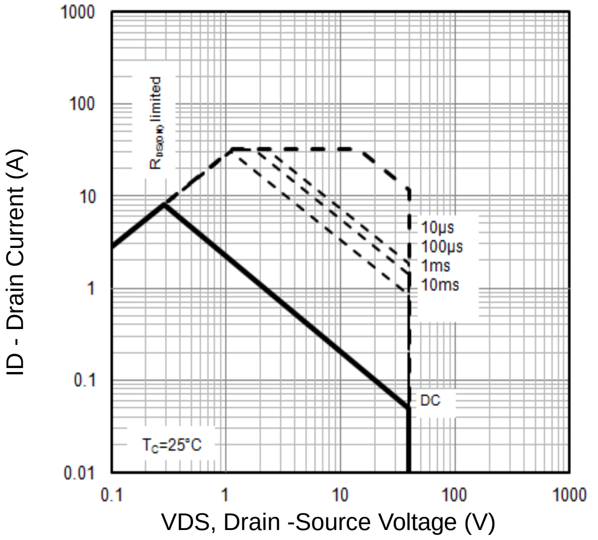


Fig6. Maximum Safe Operating Area

N-Channel Typical Characteristics

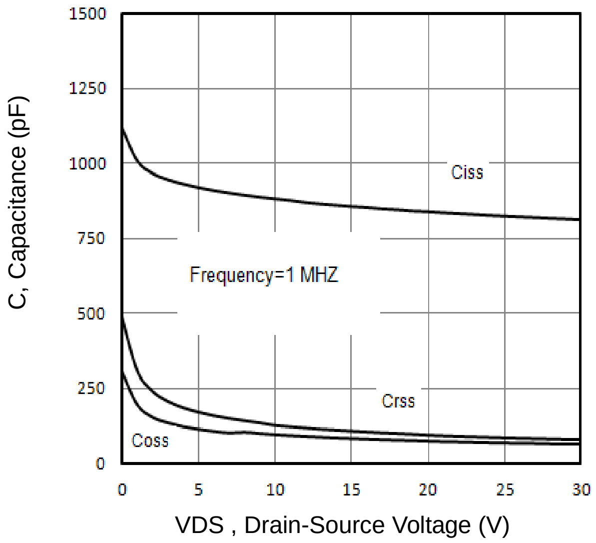


Fig7. Typical Capacitance Vs.Drain-Source Voltage

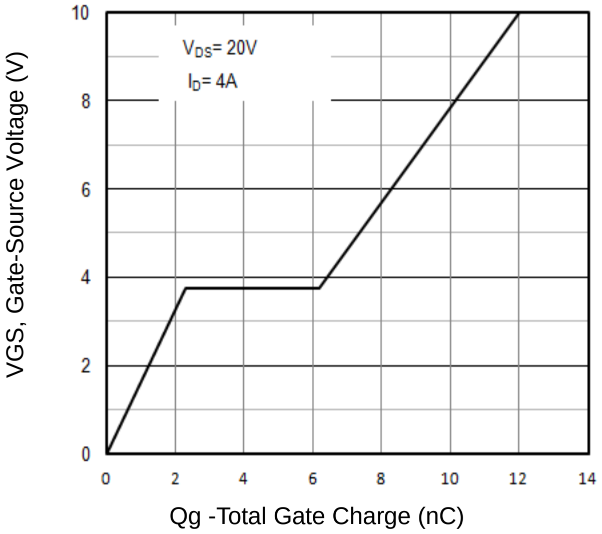


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

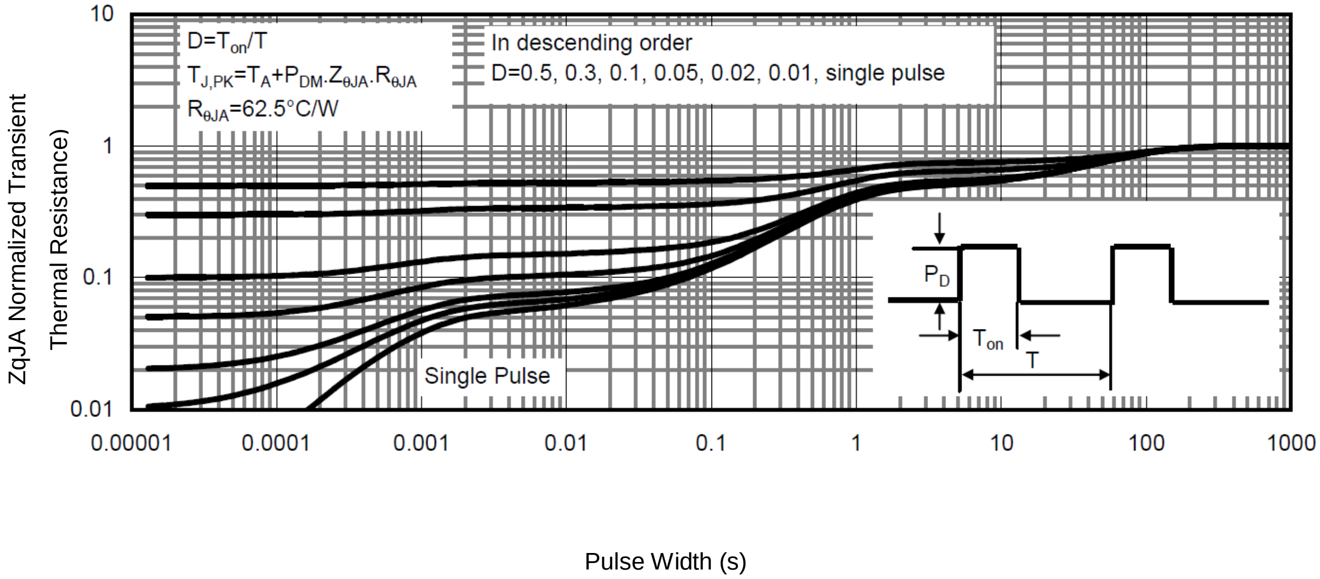


Fig 9 .Normalized Maximum Transient Thermal Impedance

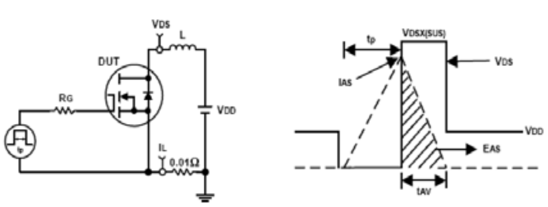


Fig10. Unclamped Inductive Test Circuit and waveforms

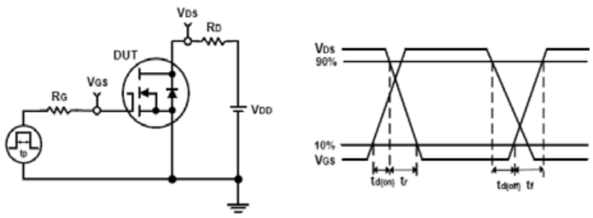


Fig11. Switching Time Test Circuit and waveforms

P-Channel Typical Characteristics

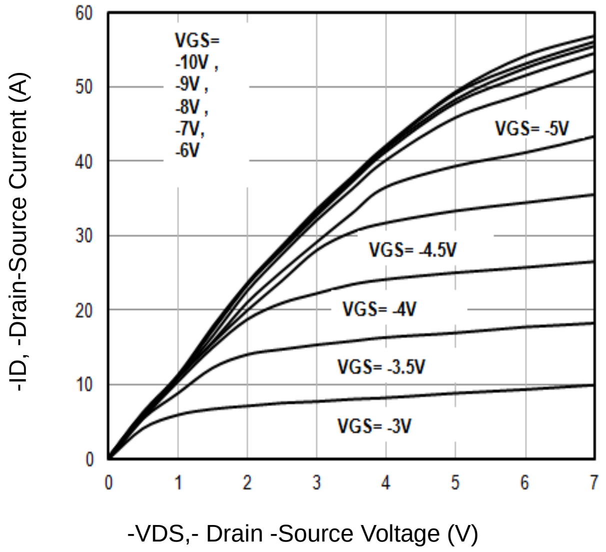


Fig1. Typical Output Characteristics

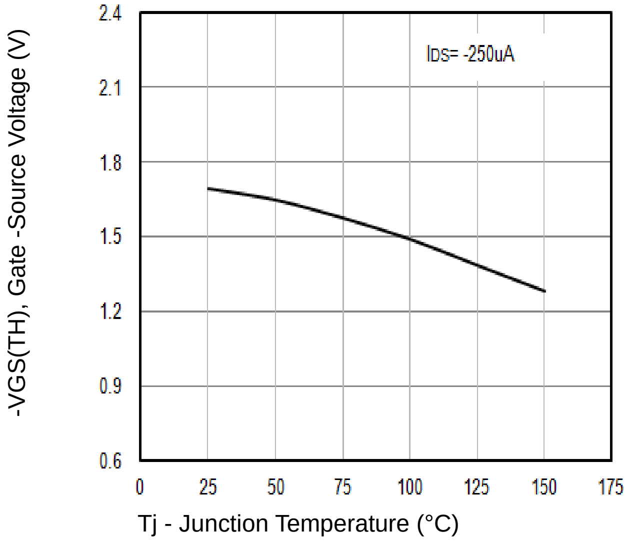


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs. Tj

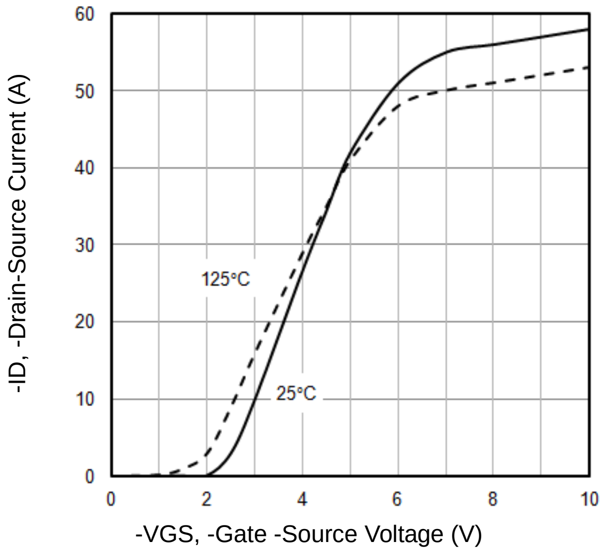


Fig3. Typical Transfer Characteristics

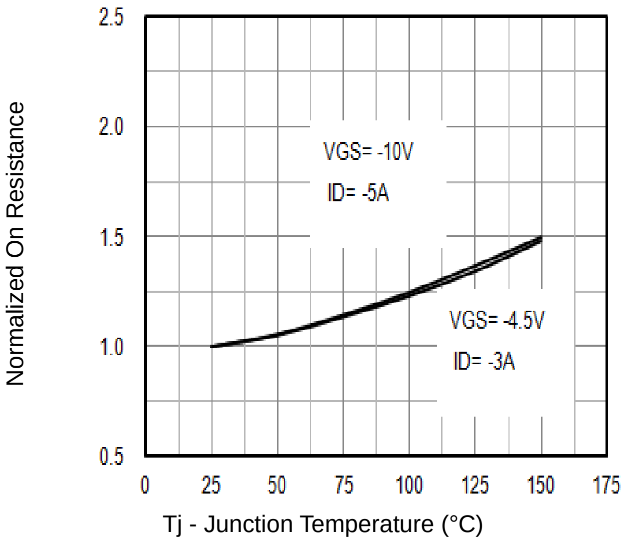


Fig4. Normalized On-Resistance Vs. Tj

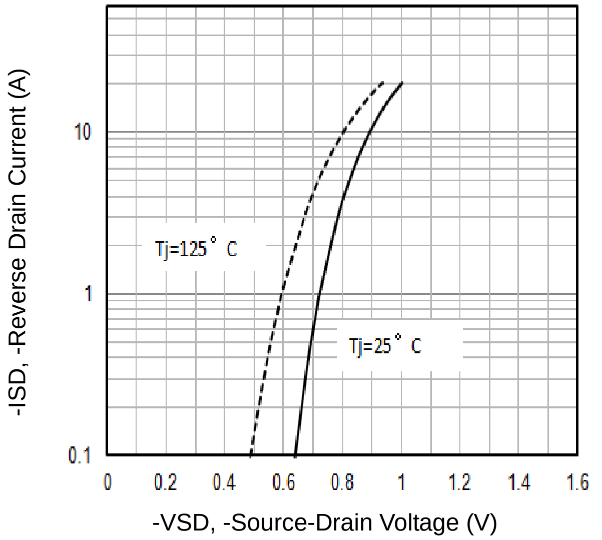


Fig5. Typical Source-Drain Diode Forward Voltage

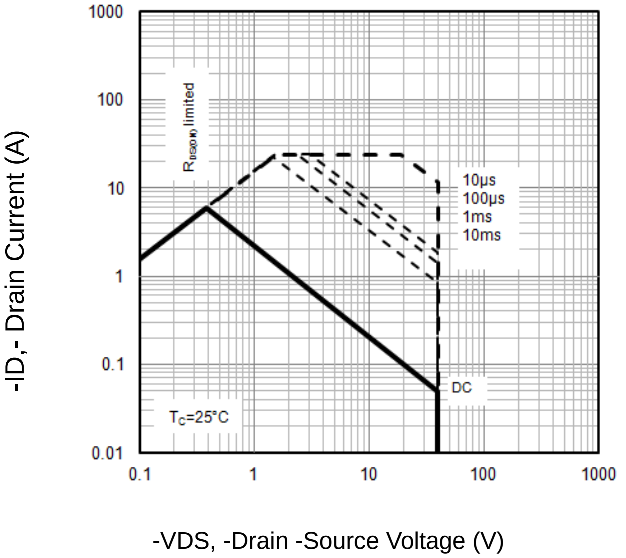


Fig6. Maximum Safe Operating Area

P-Channel Typical Characteristics

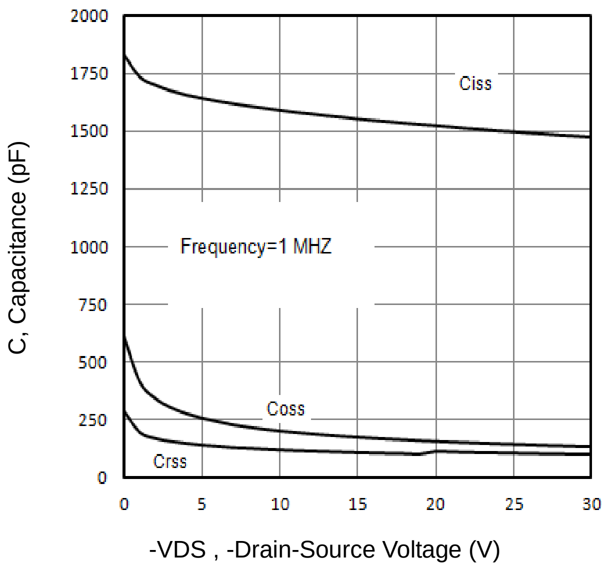


Fig7. Typical Capacitance Vs.Drain-Source Voltage

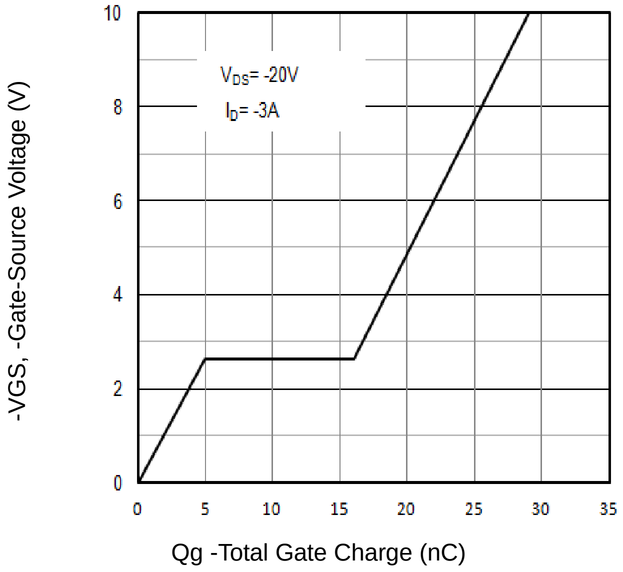


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

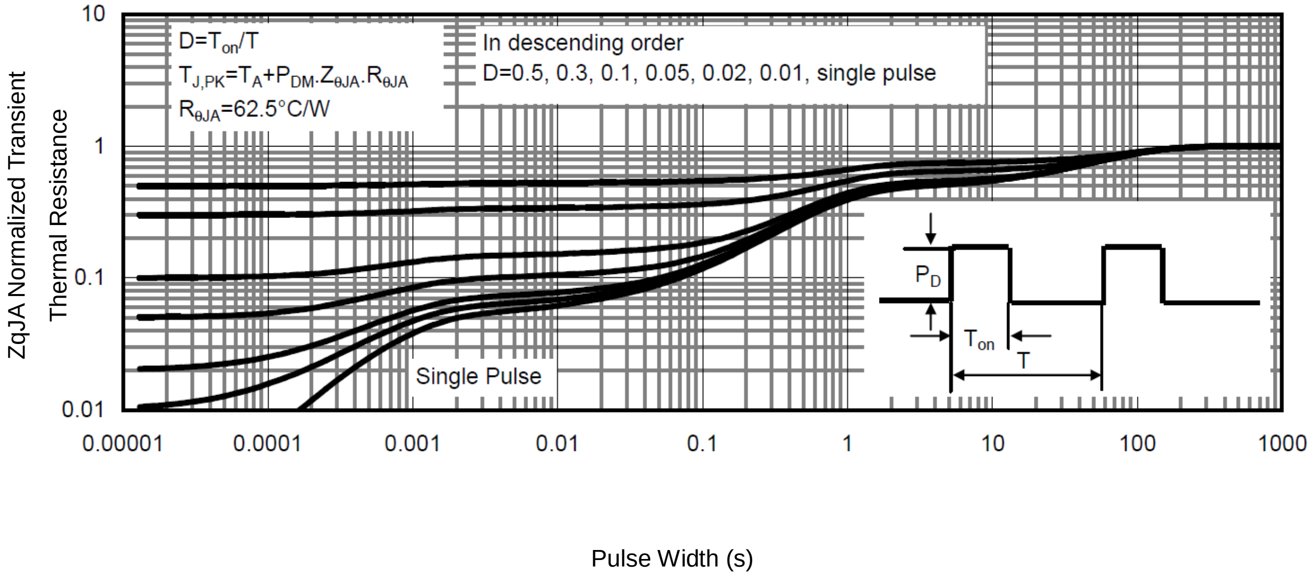


Fig9. Normalized Maximum Transient Thermal Impedance

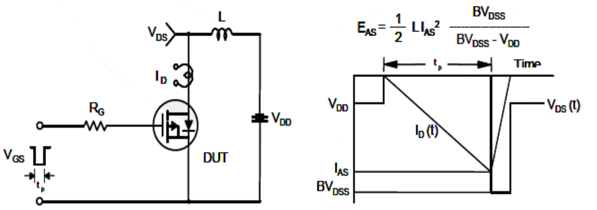


Fig10. Unclamped Inductive Test Circuit and Waveforms

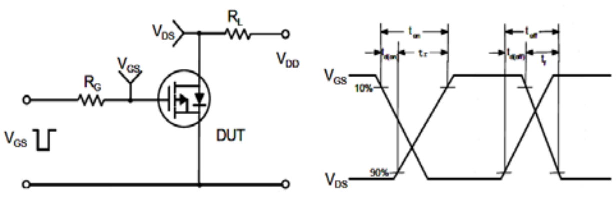
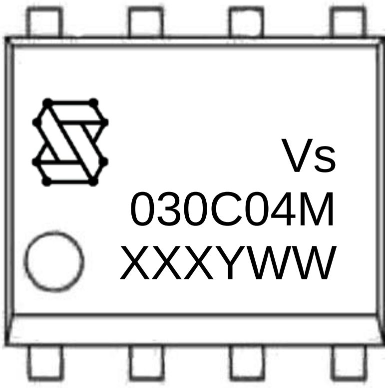


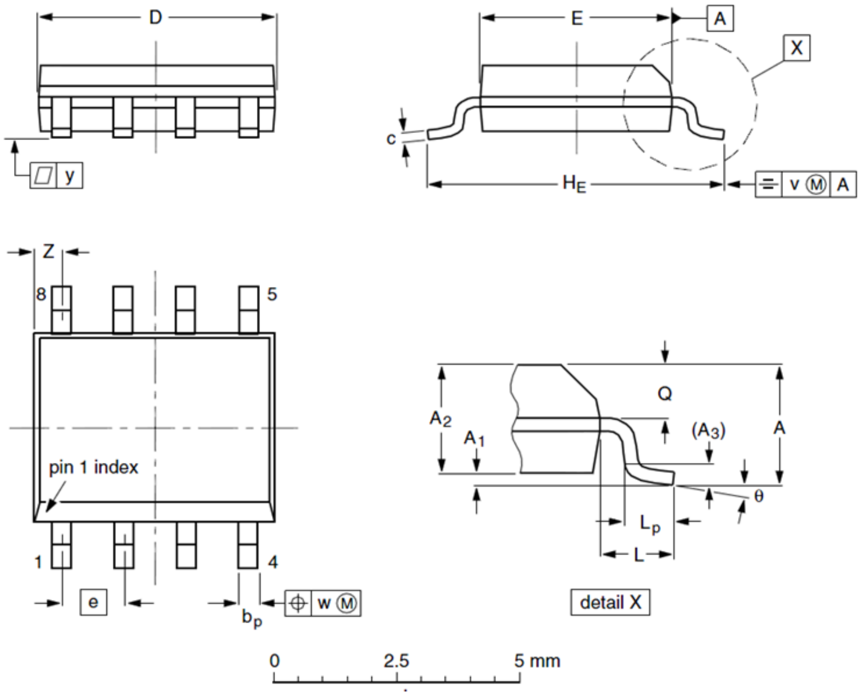
Fig11. Switching Time Test Circuit and waveforms

Marking Information



1st line：Company Code（Vs），Company Logo
2nd line：Part Number（030C04M）
3rd line：Date code （XXXYWW）
XXX：Wafer Lot Number
Y：Year Code，e.g. E means 2017
WW：Week Code

SOP8 Package Outline Data



Label	Dimensions (unit: mm)		
	Min	Typ	Max
A	--	--	1.75
A_1	0.10	0.18	0.25
A_2	1.25	1.35	1.50
A_3	--	0.25	--
b_p	0.36	0.42	0.51
c	0.19	0.22	0.25
D	4.80	4.92	5.00
E	3.80	3.90	4.00
e	--	1.27	--
H_E	5.80	6.00	6.20
L	--	1.05	--
L_p	0.40	0.68	1.00
Q	0.60	0.65	0.725
v	--	0.25	--
w	--	0.25	--
y	--	0.10	--
Z	0.30	0.50	0.70
θ	0°		8°

Notes:

1. Follow JEDEC MS-012.
2. Dimension "D" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension "E" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
4. Dimension "bp" does NOT include dambar protrusion. Allowable dambar protrusion shall be 0.1mm total in excess of "bp" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.

Customer Service

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