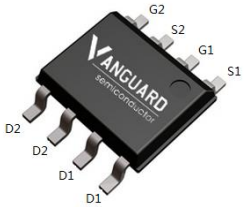
Features

- Dual N-Channel，5V Logic Level Control
- Enhancement mode
- Fast Switching
- High Effective
- Pb-free lead plating; RoHS compliant; Halogen-Free

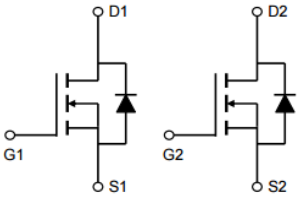
V_{DS}	100	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	76	mΩ
$R_{DS(on),TYP}$@ V_{GS}=4.5 V	81	mΩ
I_D	3.7	A

SOP8



Pb-Free RoHS HF Halogen-Free

Part ID	Package Type	Marking	Tape and reel information
VSO100N10MD	SOP8	100N10MD	3000pcs/reel



Maximum ratings, at T_j=25 °C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		100	V
I_S	Diode continuous forward current	T_A=25°C	2.4	A
I_D	Continuous drain current @V_{GS}=10V	T_A=25°C	3.7	A
		T_A=100°C	2.4	A
I_{DM}	Pulse drain current tested ①	T_A=25°C	15	A
P_D	Maximum power dissipation	T_A=25°C	2	W
V_{GS}	Gate-Source voltage		±20	V
T_{STG}	Storage temperature range		-55 to 175	°C
T_J	Maximum Junction Temperature		150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JL}$	Thermal Resistance-Junction to Lead	40	°C/W
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	62.5	°C/W

Typical Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	100	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current(Tc=25℃)	V_{DS}=100V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(Tc=125℃)	V_{DS}=100V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1	1.7	2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance ②	V_{GS}=10V, I_D=4A	--	76	95	mΩ
$R_{DS(ON)}$	Drain-Source On-State Resistance ②	V_{GS}=4.5V, I_D=2A	--	81	100	mΩ
Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
C_{iss}	Input Capacitance	V_{DS}=30V,V_{GS}=0V, f=1MHz	--	555	--	pF
C_{oss}	Output Capacitance		--	40	--	pF
C_{rss}	Reverse Transfer Capacitance		--	35	--	pF
R_g	Gate Resistance	f=1MHz	--	2.1	--	Ω
Q_g	Total Gate Charge	V_{DS}=50V,I_D=4A, V_{GS}=10V	--	8.5	--	nC
Q_{gs}	Gate-Source Charge		--	3.5	--	nC
Q_{gd}	Gate-Drain Charge		--	3.5	--	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=50V, I_D=4A, R_G=3Ω, V_{GS}=10V	--	6	--	nS
t_r	Turn-on Rise Time		--	4	--	nS
$t_{d(off)}$	Turn-Off Delay Time		--	17	--	nS
t_f	Turn-Off Fall Time		--	4	--	nS
Source- Drain Diode Characteristics@ T_J = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=4A,V_{GS}=0V	--	0.8	1.2	V
t_{rr}	Reverse Recovery Time	T_j=25℃,I_{sd}=4A, V_{GS}=0V di/dt=500A/μs	--	18	--	nS
Q_{rr}	Reverse Recovery Charge			46		nC

NOTE:

① Repetitive rating; pulse width limited by maximum junction temperature.

② Pulse width ≤ 300μs; duty cycle≤ 2%.

Typical Characteristics

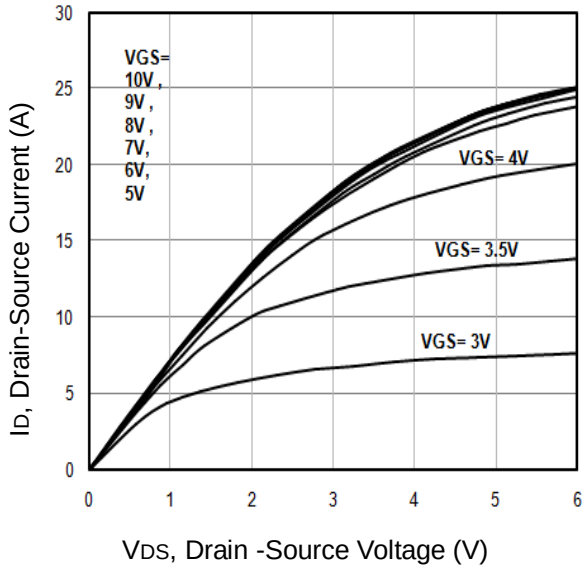


Fig1. Typical Output Characteristics

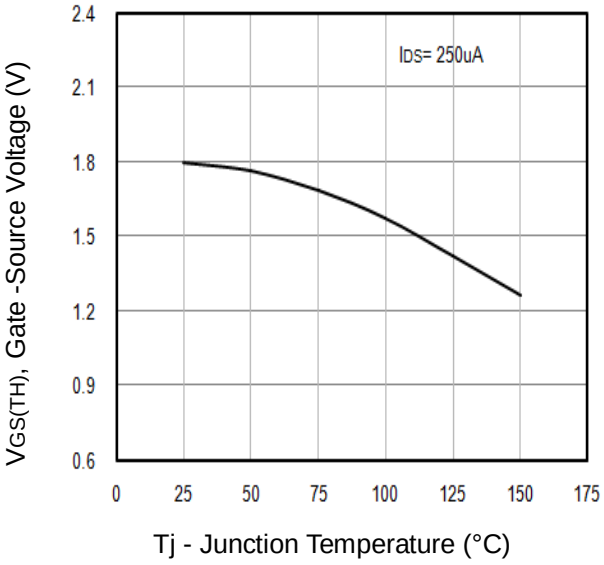


Fig2. Threshold Voltage Vs. Temperature

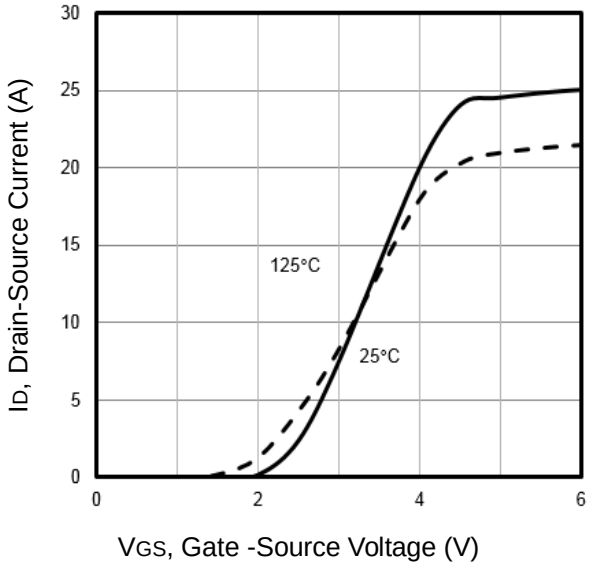


Fig3. Typical Transfer Characteristics

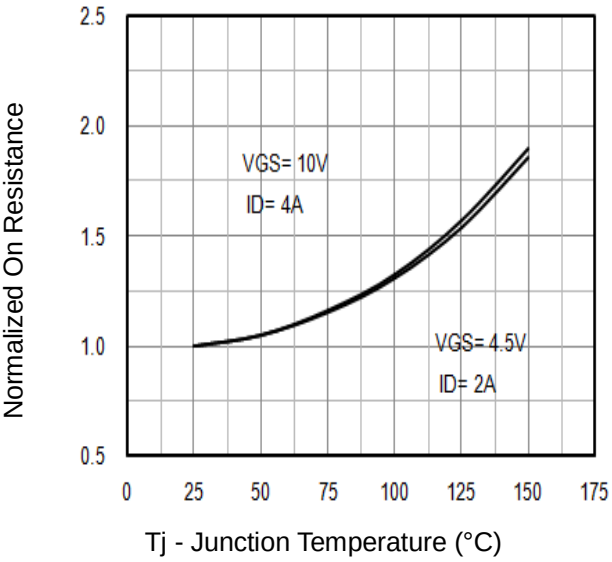


Fig4. Normalized On-Resistance Vs. Temperature

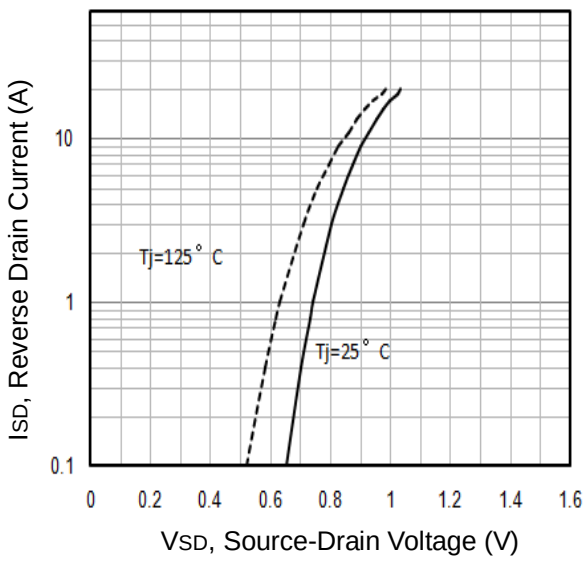


Fig5. Typical Source-Drain Diode Forward Voltage

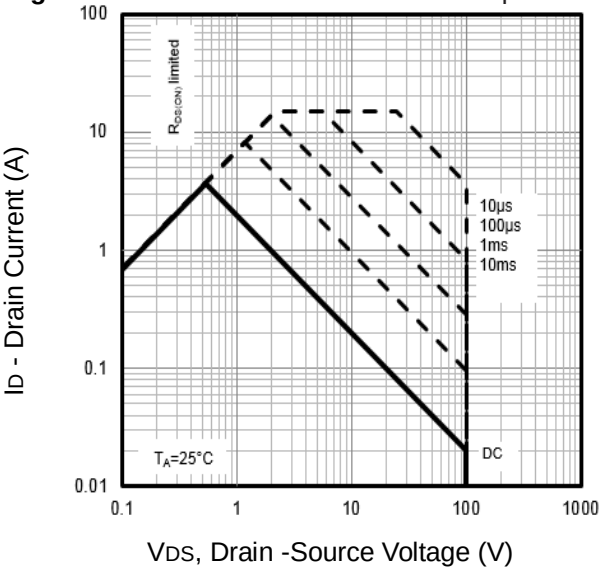


Fig6. Maximum Safe Operating Area

Typical Characteristics

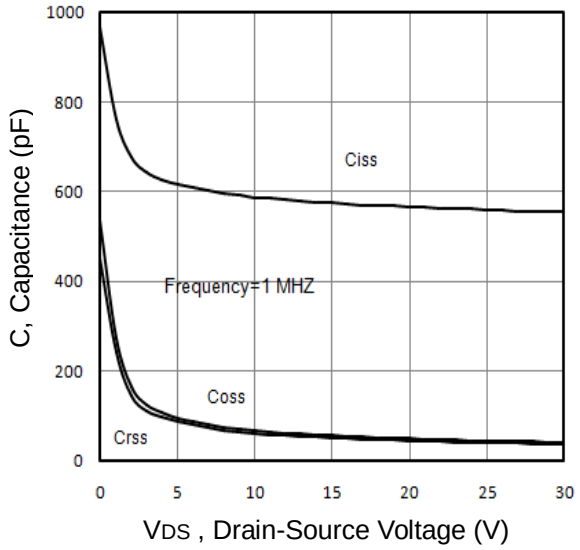


Fig7. Typical Capacitance Vs.Drain-Source Voltage

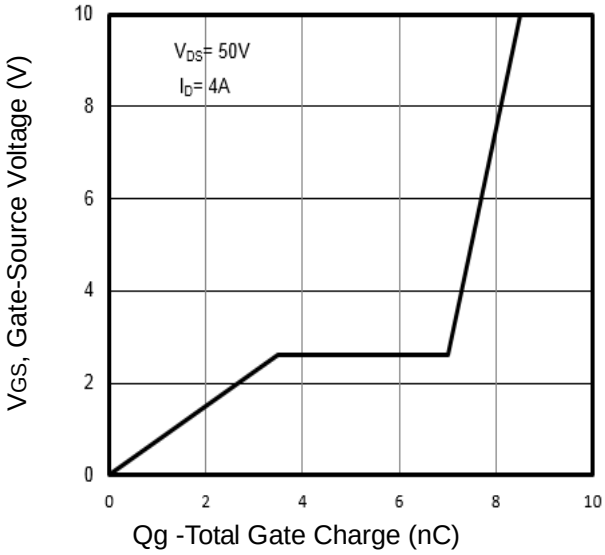
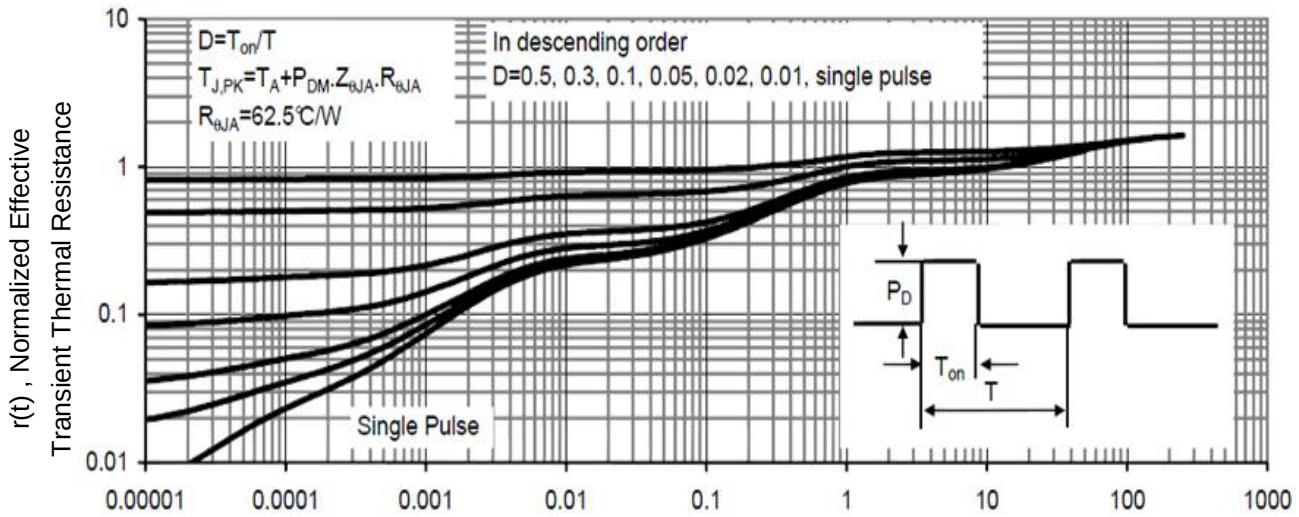


Fig8. Typical Gate Charge Vs.Gate-Source Voltage



T1, Square Wave Pulse Duration(sec)

Fig9. T1 ,Transient Thermal Response Curve

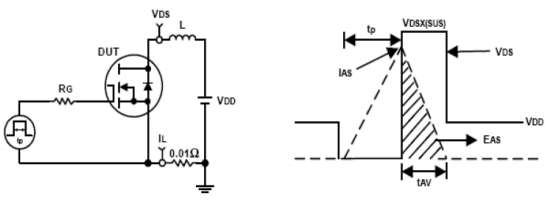


Fig10. Unclamped Inductive Test Circuit and waveforms

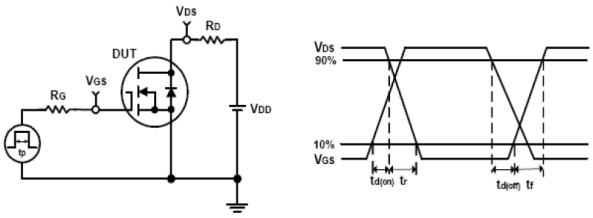
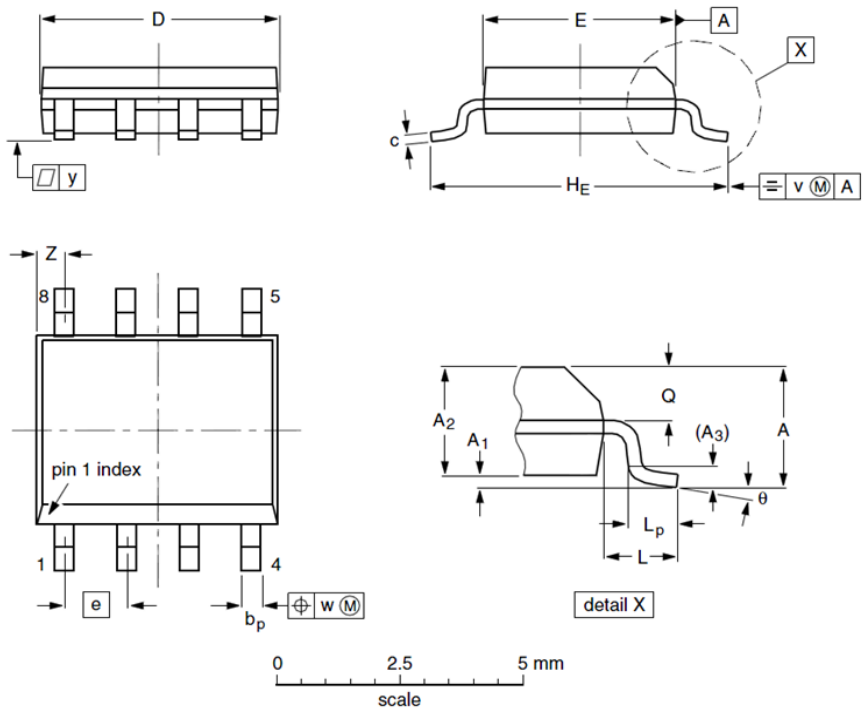


Fig11. Switching Time Test Circuit and waveforms

SOP8 Package Outline Data



Label	Dimensions (unit: mm)		
	Min	Typ	Max
A	--	--	1.75
A_1	0.10	0.18	0.25
A_2	1.25	1.35	1.50
A_3	--	0.25	--
b_p	0.36	0.42	0.51
c	0.19	0.22	0.25
D	4.80	4.92	5.00
E	3.80	3.90	4.00
e	--	1.27	--
H_E	5.80	6.00	6.20
L	--	1.05	--
L_p	0.40	0.68	1.00
Q	0.60	0.65	0.725
v	--	0.25	--
w	--	0.25	--
y	--	0.10	--
Z	0.30	0.50	0.70
θ	0°		8°

Notes:

1. Follow JEDEC MS-012.
2. Dimension "D" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension "E" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
4. Dimension "bp" does NOT include dambar protrusion. Allowable dambar protrusion shall be 0.1mm total in excess of "bp" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.

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