

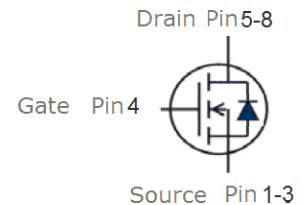
Features

- N-Channel
- Enhancement mode
- Very low on-resistance @ $V_{GS}=4.5\text{ V}$
- Fast Switching
- Pb-free lead plating; RoHS compliant


Halogen-Free

Part ID	Package Type	Marking	Tape and reel information
VSO100N10MS	SOP8	100N10M	3000pcs/reel

V_{DS}	100	V
$R_{DS(on),typ@V_{GS}=10V}$	78	mΩ
$R_{DS(on),typ@V_{GS}=4.5V}$	85	mΩ
I_D	6	A



Maximum ratings, at $T_j=25\text{ }^{\circ}\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	100	V
V_{GS}	Gate-Source voltage	± 16	V
I_D	Continuous drain current@ $V_{GS}=10V$	$T_C=25^{\circ}\text{C}$	6 A
		$T_A=100^{\circ}\text{C}$	3.8 A
I_{DM}	Pulse drain current tested ①	$T_C=25^{\circ}\text{C}$	24 A
P_D	Maximum power dissipation	$T_C=25^{\circ}\text{C}$	1.6 W
I_S	Diode Continuous Forward Current	$T_C=25^{\circ}\text{C}$	6 A
T_j	Maximum Junction Temperature	150	$^{\circ}\text{C}$
T_{STG}	Storage temperature range	-55 to 175	$^{\circ}\text{C}$
Thermal characteristics			
$R_{\theta JA}$	Thermal Resistance Junction-Ambient	75	$^{\circ}\text{C/W}$
$R_{\theta JC}$	Thermal Resistance-Junction to Case	43	$^{\circ}\text{C/W}$

Typical Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T _J = 25°C (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V I _D =250μA	100	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current(Tc=25°C)	V _{DS} =100V,V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(Tc=125°C)	V _{DS} =100V,V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±16V,V _{DS} =0V	--	--	±100	nA
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} ,I _D =250μA	1.0	1.5	2.5	V
R _{DS(ON)}	Drain-Source On-State Resistance②	V _{GS} =10V, I _D =6A	--	78	90	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance②	V _{GS} =4.5V, I _D =3A	--	85	100	mΩ
Dynamic Electrical Characteristics @ T _J = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =30V,V _{GS} =0V, f=1MHz	--	435	--	pF
C _{oss}	Output Capacitance		--	45	--	pF
C _{rss}	Reverse Transfer Capacitance		--	30	--	pF
Q _g	Total Gate Charge	V _{DS} =50V,I _D =1A, V _{GS} =10V	--	9	--	nC
Q _{gs}	Gate-Source Charge		--	1.7	--	nC
Q _{gd}	Gate-Drain Charge		--	1.6	--	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =30V, I _D =1A, R _G =6.8Ω, V _{GS} =4.5V	--	6	--	nS
t _r	Turn-on Rise Time		--	15	--	nS
t _{d(off)}	Turn-Off Delay Time		--	16	--	nS
t _f	Turn-Off Fall Time		--	10	--	nS
Source- Drain Diode Characteristics@ T _J = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =4 A,V _{GS} =0V	--	0.82	1.20	V

NOTE:

- ① Repetitive rating; pulse width limited by max. junction temperature
 ② Pulse width ≤ 300μs; duty cycles ≤ 2%.



Typical Characteristics

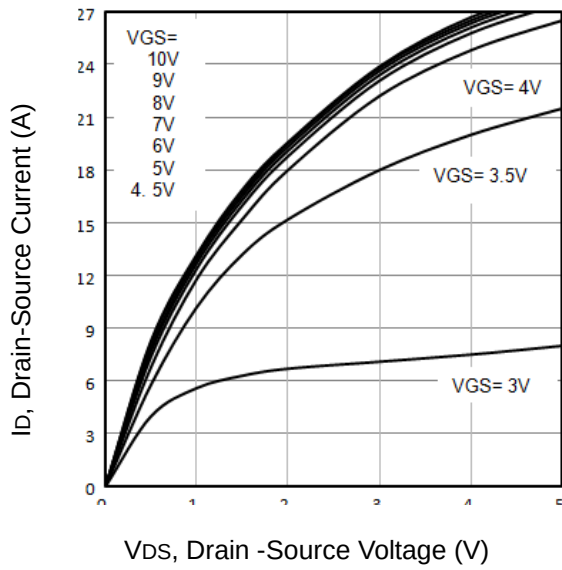


Fig1. Typical Output Characteristics

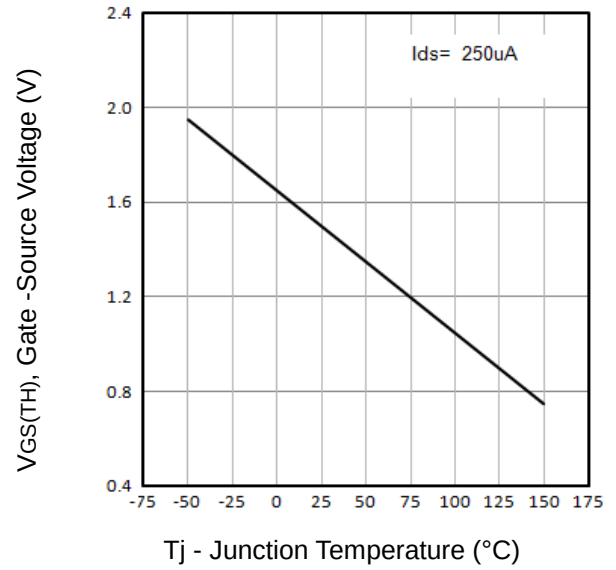


Fig2. Threshold Voltage Vs. Temperature

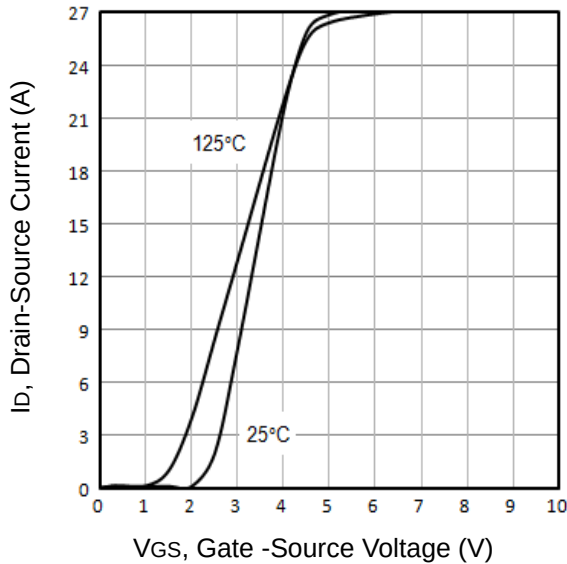


Fig3. Typical Transfer Characteristics

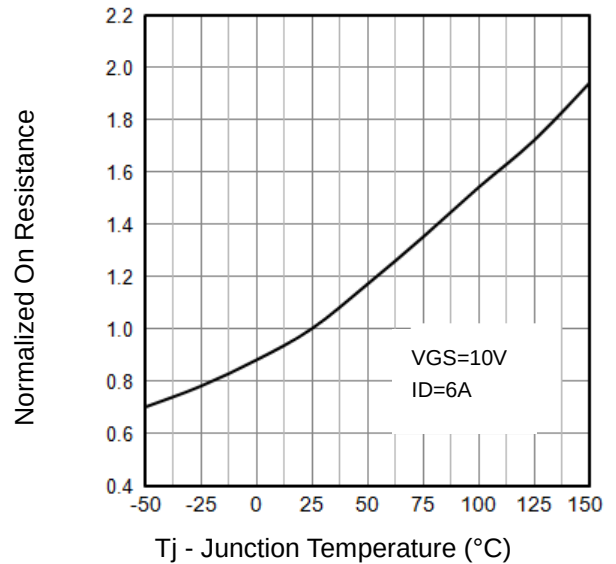


Fig4. Normalized On-Resistance Vs. Temperature

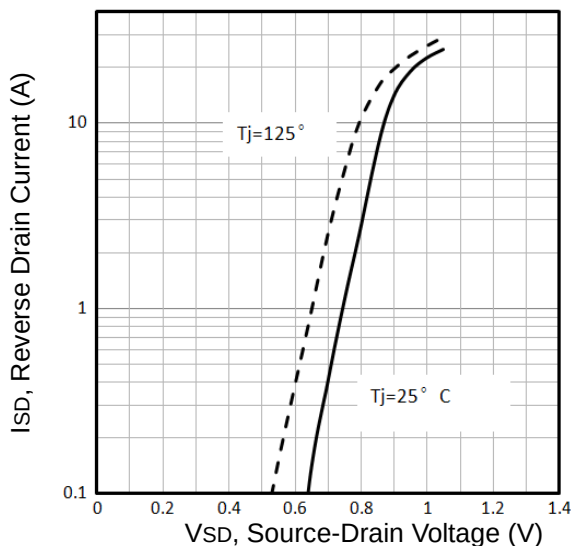


Fig5. Typical Source-Drain Diode Forward Voltage

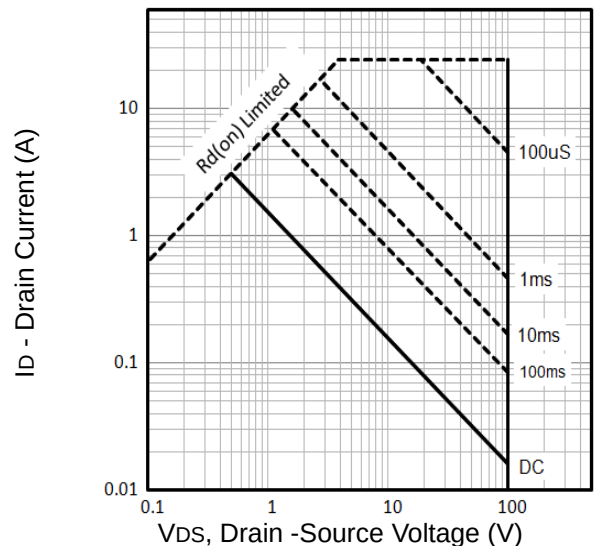


Fig6. Maximum Safe Operating Area

Typical Characteristics

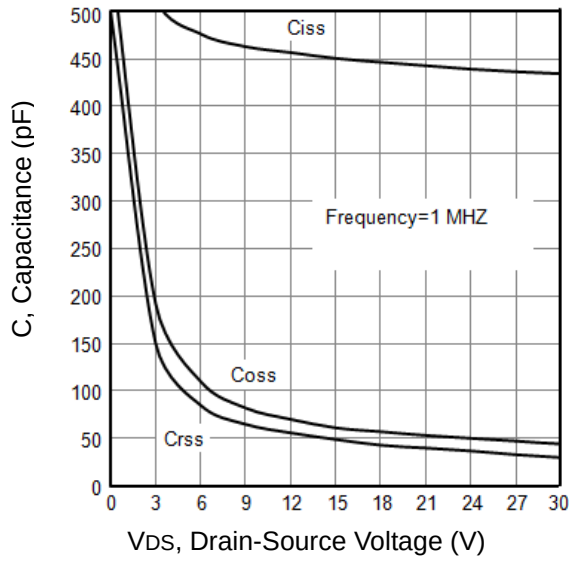


Fig7. Typical Capacitance Vs. Drain-Source Voltage

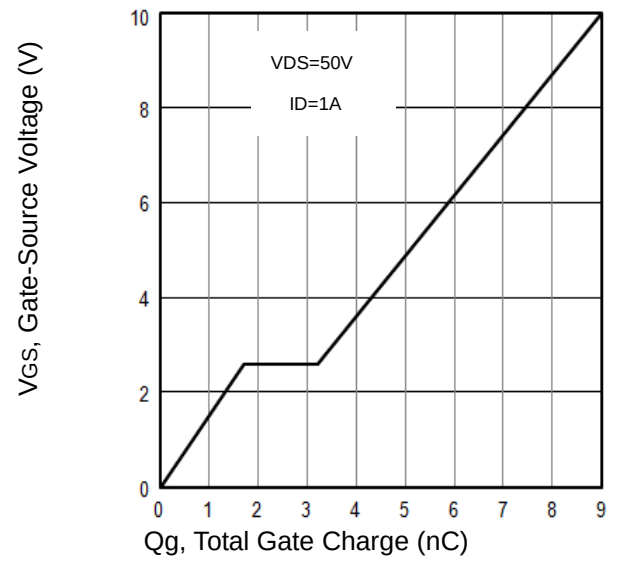


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

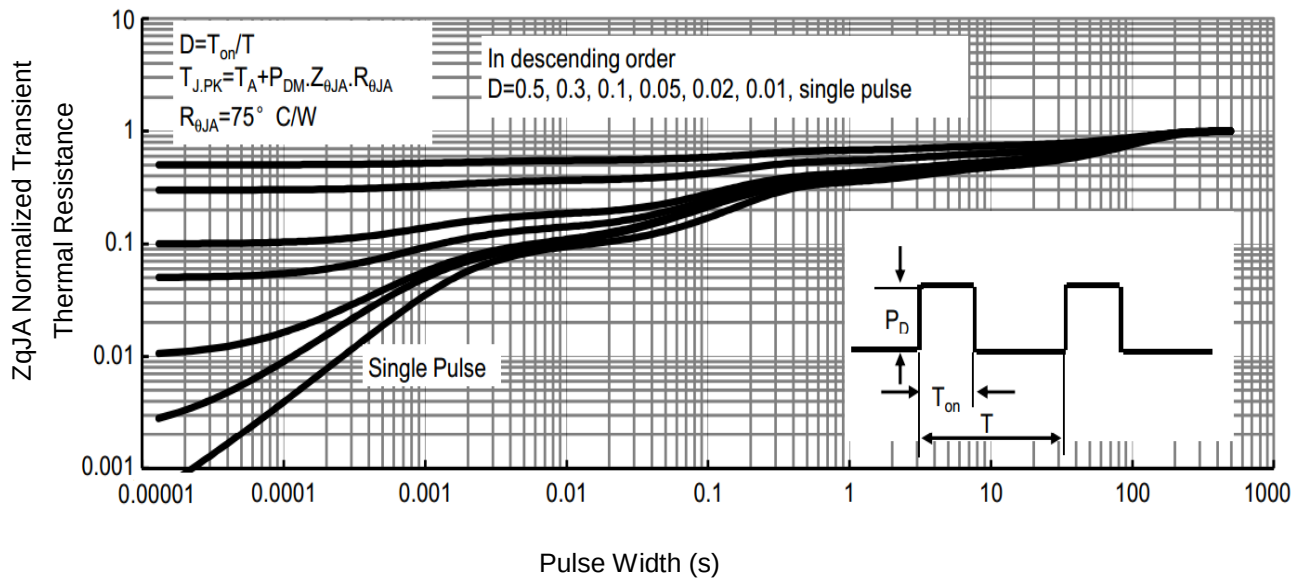


Figure 9: Normalized Maximum Transient Thermal

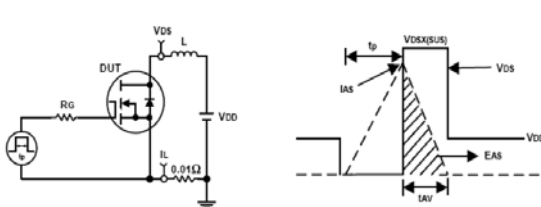


Fig10. Unclamped Inductive Test Circuit and waveforms

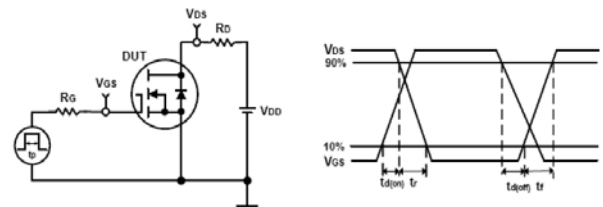
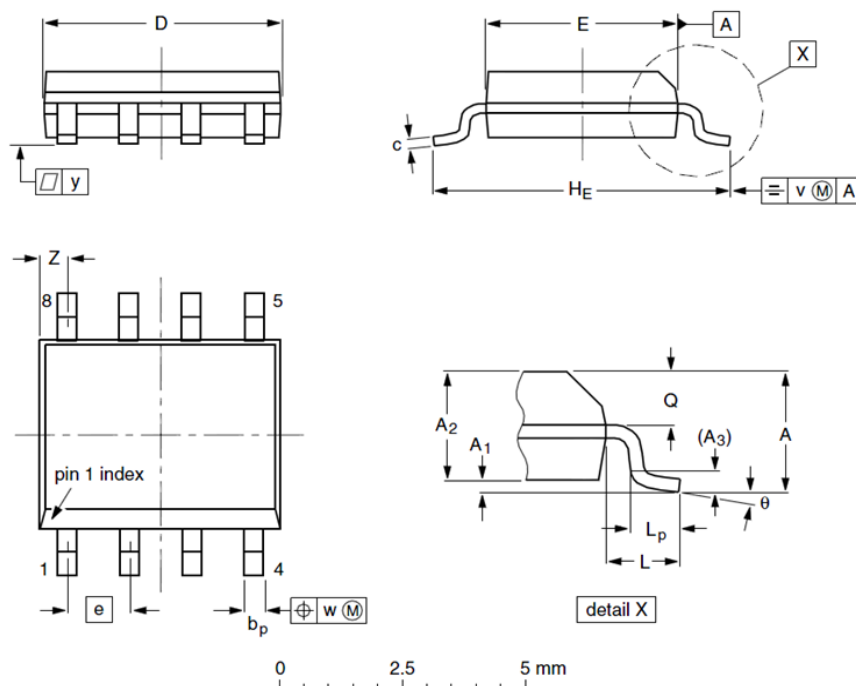


Fig11. Switching Time Test Circuit and waveforms

SOP8 Package Outline Data



Label	Dimensions (unit: mm)		
	Min	Typ	Max
A	--	--	1.75
A ₁	0.10	0.18	0.25
A ₂	1.25	1.35	1.50
A ₃	--	0.25	--
b _p	0.36	0.42	0.51
c	0.19	0.22	0.25
D	4.80	4.92	5.00
E	3.80	3.90	4.00
e	--	1.27	--
H _E	5.80	6.00	6.20
L	--	1.05	--
L _p	0.40	0.68	1.00
Q	0.60	0.65	0.725
v	--	0.25	--
w	--	0.25	--
y	--	0.10	--
Z	0.30	0.50	0.70
θ	0°		8°

Notes:

1. Follow JEDEC MS-012.
2. Dimension "D" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension "E" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
4. Dimension "b_p" does NOT include dambar protrusion. Allowable dambar protrusion shall be 0.1mm total in excess of "b_p" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.

Customer Service

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