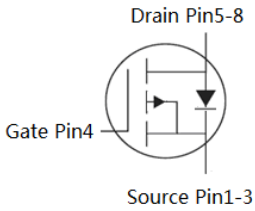
Features

- P-Channel，-5V Logic Level Control
- Very low on-resistance RDS(on) @ V_{GS}=-4.5 V
- Fast Switching
- Enhancement mode
- Pb-free lead plating; RoHS compliant

V_{DS}	-100	V
$R_{DS(on),TYP}$@ V_{GS}=-10 V	88	mΩ
$R_{DS(on),TYP}$@ V_{GS}=-4.5V	92	mΩ
I_D	-4	A

SOP8

Pb-Free RoHS HF Halogen-Free



Part ID	Package Type	Marking	Tape and reel information
VSO100P10MS	SOP8	100P10M	3000pcs/Reel

Maximum ratings, at T_j=25 °C, unless otherwise specified

Symbol	Parameter		Rating	Unit
Common Ratings				
V_{GS}	Gate-Source Voltage		±20	V
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage		-100	V
T_{STG} T_J	Storage and operating temperature range①		-55 to 150	°C
I_S	Diode Continuous Forward Current	T_A=25°C	-3	A
Mounted on Large Heat Sink				
I_D	Continuous Drain current @V_{GS}=-10V	T_A=25°C	-4	A
		T_A=100°C	-2.5	A
I_{DM}	Pulse Drain Current Tested ②	T_A=25°C	-16	A
P_D	Maximum Power Dissipation	T_A=25°C	3.1	W
$R_{\theta JC}$	Thermal Resistance-Junction to Case		25	°C/W
$R_{\theta JA}$	Thermal Resistance Junction-Ambient		40	°C/W
Drain-Source Avalanche Ratings				
EAS	Avalanche Energy, Single Pulsed ③		210	mJ

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=-250μA	-100	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-100V,V_{GS}=0V	--	--	-1	μA
	Zero Gate Voltage Drain Current(T_j=125℃)	V_{DS}=-100V,V_{GS}=0V	--	--	-100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=-250μA	-1.0	-1.8	-2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance ②	V_{GS}=-10V, I_D=-4A	--	88	100	mΩ
$R_{DS(ON)}$	Drain-Source On-State Resistance ②	V_{GS}=-4.5V, I_D=-2A	--	92	110	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
C_{iss}	Input Capacitance	V_{DS}=-30V,V_{GS}=0V, f=1MHz	--	2575	--	pF
C_{oss}	Output Capacitance		--	90	--	pF
C_{rss}	Reverse Transfer Capacitance		--	75	--	pF
Q_g	Total Gate Charge	V_{DS}=-50V,I_D=-2A, V_{GS}=-10V	--	37	--	nC
Q_{gs}	Gate-Source Charge		--	8	--	nC
Q_{gd}	Gate-Drain Charge		--	9	--	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=-50V, I_D=-2A, R_G=6.8Ω, V_{GS}=-10V	--	11	--	nS
t_r	Turn-on Rise Time		--	16	--	nS
$t_{d(off)}$	Turn-Off Delay Time		--	38	--	nS
t_f	Turn-Off Fall Time		--	15	--	nS
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=-4A,V_{GS}=0V	--	-0.83	-1.0	V
t_{rr}	Reverse Recovery Time	T_j=25℃,I_{sd}=-2A, V_{GS}=0V di/dt=-100A/μs	--	25	--	nS
Q_{rr}	Reverse Recovery Charge			135		nC

NOTE:

① Repetitive rating; pulse width limited by max. junction temperature.

②Pulse width ≤ 300μs; duty cycle≤ 2%.

③Limited by TJmax, starting TJ = 25°C, L = 0.5mH,RG = 25Ω, IAS = -29A, VGS =-10V. Part not recommended for use above this value

Typical Characteristics

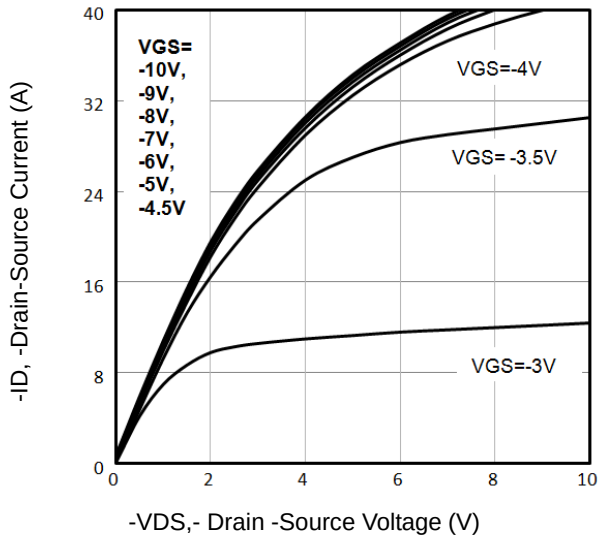


Fig1. Typical Output Characteristics

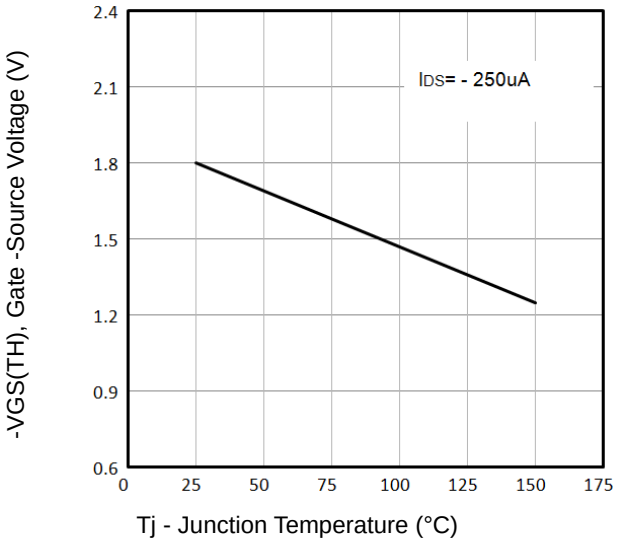


Fig2. $-V_{GS(TH)}$ Gate -Source Voltage Vs.Tj

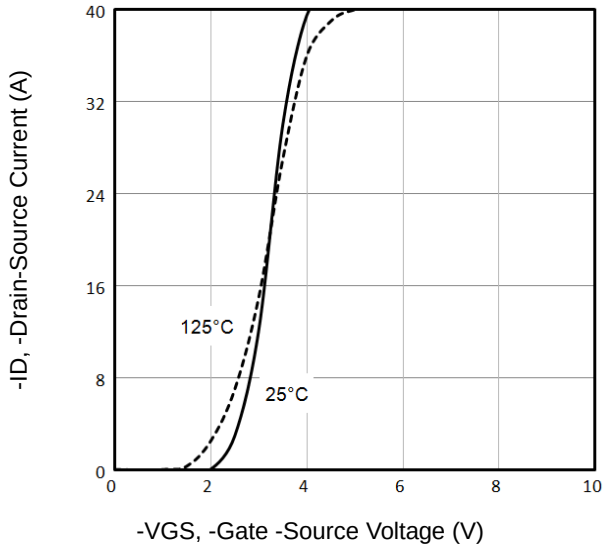


Fig3. Typical Transfer Characteristics

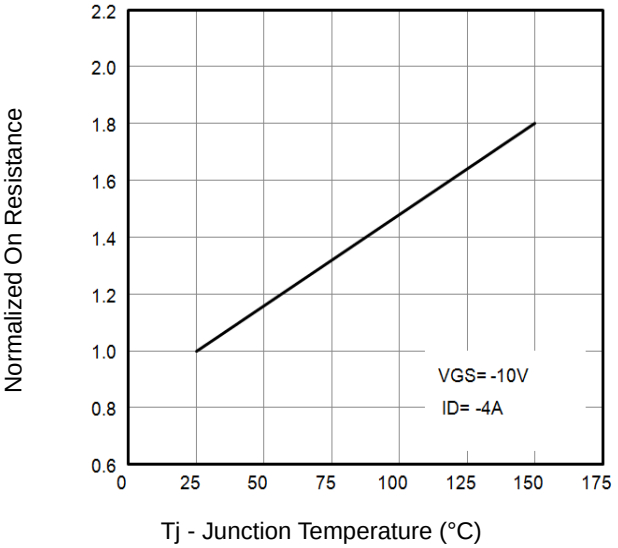


Fig4. Normalized On-Resistance Vs. Tj

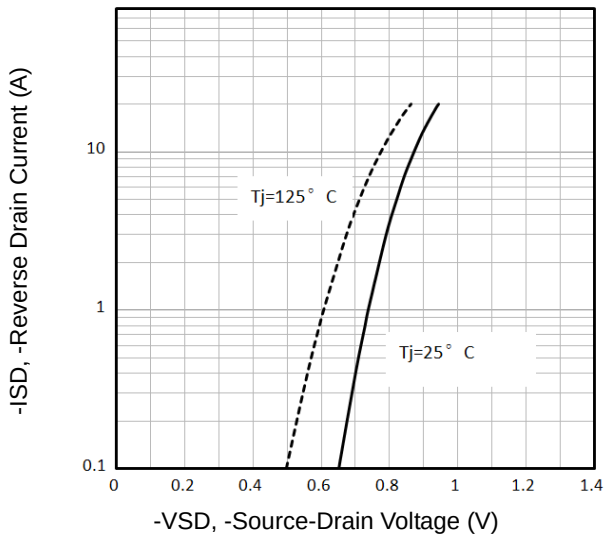


Fig5. Typical Source-Drain Diode Forward Voltage

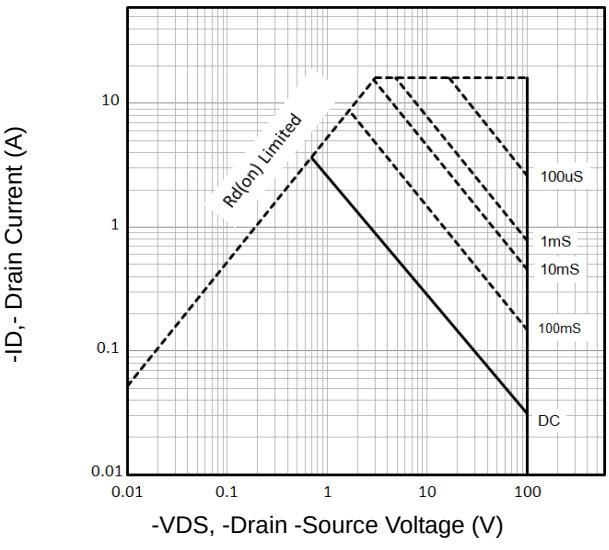


Fig6. Maximum Safe Operating Area

Typical Characteristics

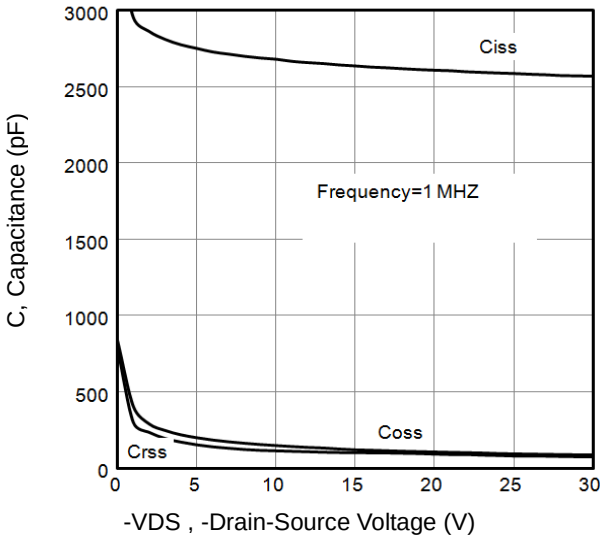


Fig7. Typical Capacitance Vs.Drain-Source Voltage

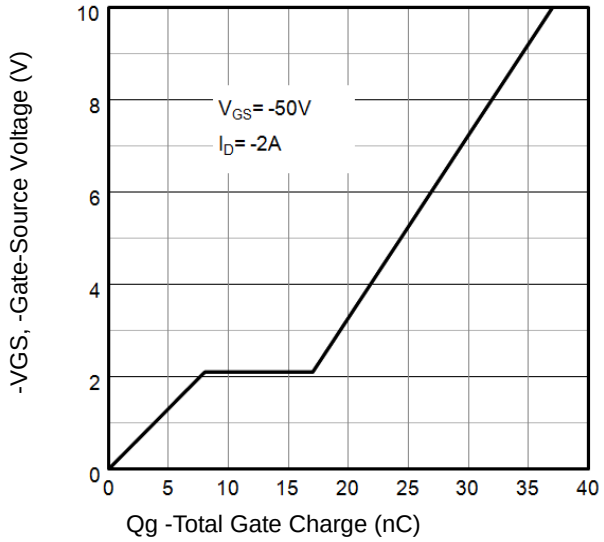


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

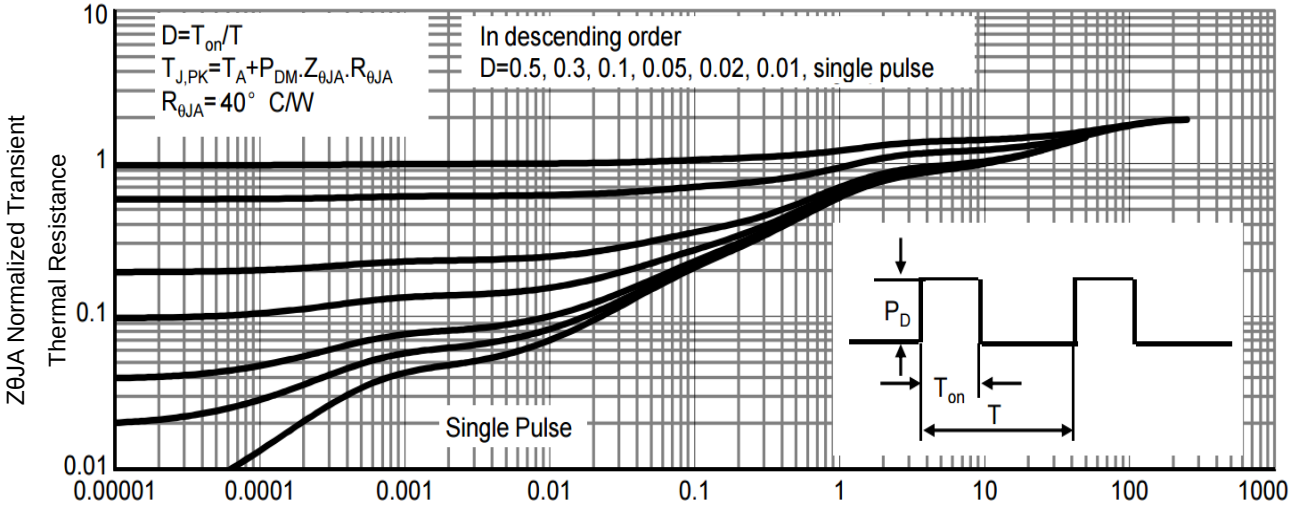


Fig9. Normalized Maximum Transient Thermal Impedance

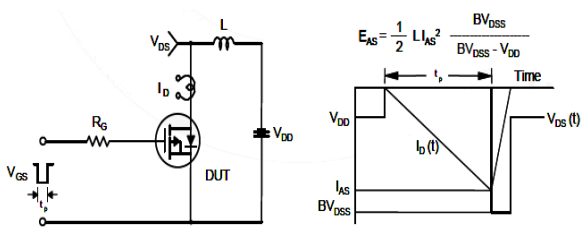


Fig10. Unclamped Inductive Test Circuit and Waveforms

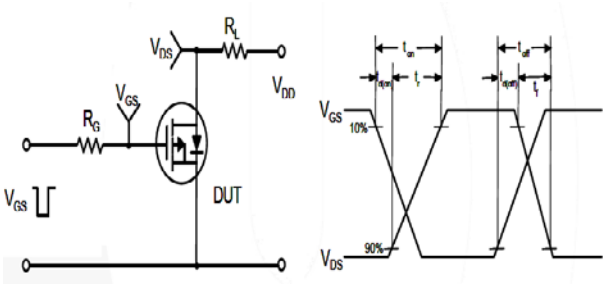
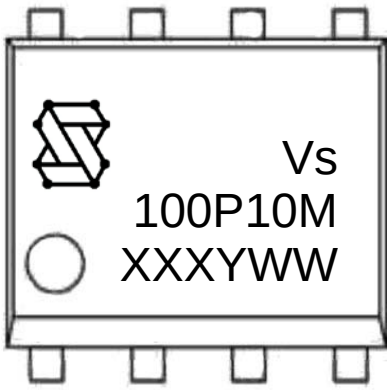


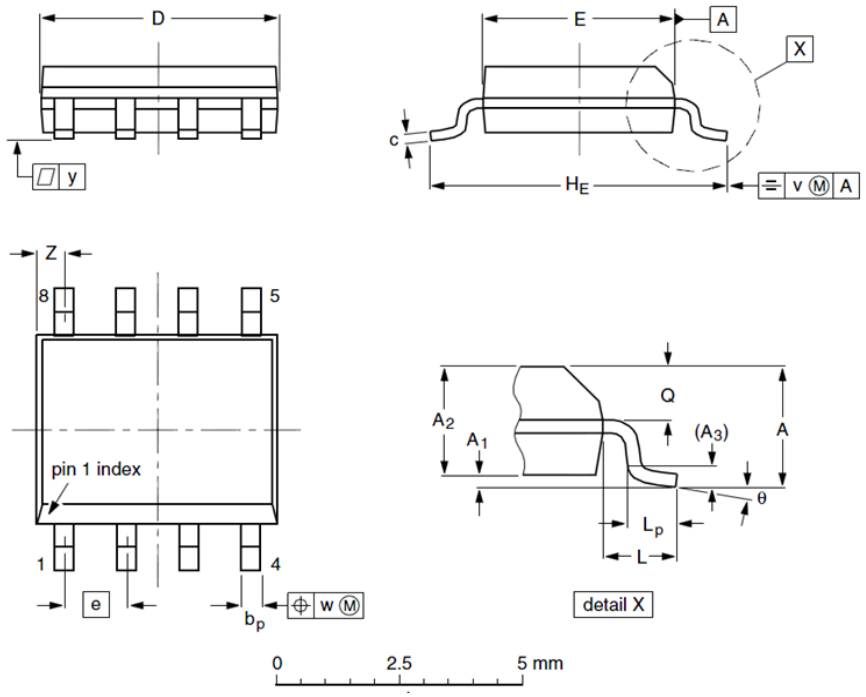
Fig11. Switching Time Test Circuit and waveforms

Marking Information



1st line：Company Code（Vs），Company Logo
2nd line：Part Number（100P10M）
3rd line：Date code （XXXYWW）
XXX：Wafer Lot Number
Y：Year Code，e.g. E means 2017
WW：Week Code

SOP8 Package Outline Data



Label	Dimensions (unit: mm)		
	Min	Typ	Max
A	--	--	1.75
A_1	0.10	0.18	0.25
A_2	1.25	1.35	1.50
A_3	--	0.25	--
b_p	0.36	0.42	0.51
c	0.19	0.22	0.25
D	4.80	4.92	5.00
E	3.80	3.90	4.00
e	--	1.27	--
H_E	5.80	6.00	6.20
L	--	1.05	--
L_p	0.40	0.68	1.00
Q	0.60	0.65	0.725
v	--	0.25	--
w	--	0.25	--
y	--	0.10	--
Z	0.30	0.50	0.70
θ	0°		8°

Notes:

1. Follow JEDEC MS-012.
2. Dimension "D" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension "E" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
4. Dimension "bp" does NOT include dambar protrusion. Allowable dambar protrusion shall be 0.1mm total in excess of "bp" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.

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