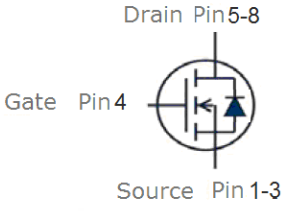
Features

- N-Channel
- Enhancement mode
- low on-resistance @ V_{GS}=4.5 V
- Fast Switching
- Pb-free lead plating; RoHS compliant

V_{DS}	150	V
$R_{DS(on),typ@VGS=10V}$	125	mΩ
$R_{DS(on),typ@VGS=4.5V}$	115	mΩ
I_D	6	A

SOP8

Pb-Free RoHS HF Halogen-Free



Part ID	Package Type	Marking	Tape and reel information
VSO140N15MS	SOP8	140N15M	3000pcs/reel

Maximum ratings, at T_j=25 °C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		150	V
V_{GS}	Gate-Source voltage		±20	V
I_D	Continuous drain current@V_{GS}=10V	T_C=25°C	6	A
		T_A=100°C	3.8	A
I_{DM}	Pulse drain current tested ①	T_C=25°C	24	A
P_D	Maximum power dissipation	T_C=25°C	2	W
I_S	Diode Continuous Forward Current	T_C=25°C	6	A
MSL			Level 3	
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage temperature range		-55 to 175	°C
Thermal characteristics				
$R_{\theta JA}$	Thermal Resistance Junction-Ambient		62.5	°C/W
$R_{\theta JC}$	Thermal Resistance-Junction to Case		45	°C/W

Typical Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=250μA	150	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current(Tc=25℃)	V_{DS}=150V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(Tc=125℃)	V_{DS}=150V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.0	2.0	3.0	V
$R_{DS(ON)}$	Drain-Source On-State Resistance②	V_{GS}=10V, I_D=6A	--	125	140	mΩ
$R_{DS(ON)}$	Drain-Source On-State Resistance②	V_{GS}=4.5V, I_D=3A	--	115	140	mΩ
Dynamic Electrical Characteristics @ T_J= 25°C (unless otherwise stated)						
C_{iss}	Input Capacitance	V_{DS}=75V,V_{GS}=0V, f=1MHz	--	1780	--	pF
C_{oss}	Output Capacitance		--	165	--	pF
C_{rss}	Reverse Transfer Capacitance		--	85	--	pF
Q_g	Total Gate Charge	V_{DS}=75V,I_D=6A, V_{GS}=10V	--	39	--	nC
Q_{gs}	Gate-Source Charge		--	10	--	nC
Q_{gd}	Gate-Drain Charge		--	13	--	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=75V, I_D=1A, R_G=6.8Ω, V_{GS}=4.5V	--	18	--	nS
t_r	Turn-on Rise Time		--	10	--	nS
$t_{d(off)}$	Turn-Off Delay Time		--	30	--	nS
t_f	Turn-Off Fall Time		--	6	--	nS
Source- Drain Diode Characteristics@ T_J= 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=2 A,V_{GS}=0V	--	0.75	1.20	V
t_{rr}	Reverse Recovery Time	T_j=25℃,I_{sd}=4A, V_{GS}=0V di/dt=100A/μs	--	45	--	nS
Q_{rr}	Reverse Recovery Charge			385		nC

NOTE:

① Repetitive rating; pulse width limited by max. junction temperature

② Pulse width ≤ 300μs; duty cycle≤ 2%.

.

Typical Characteristics

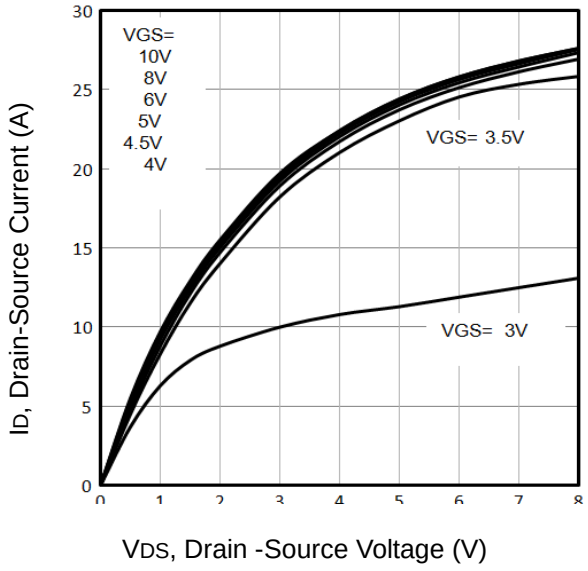


Fig1. Typical Output Characteristics

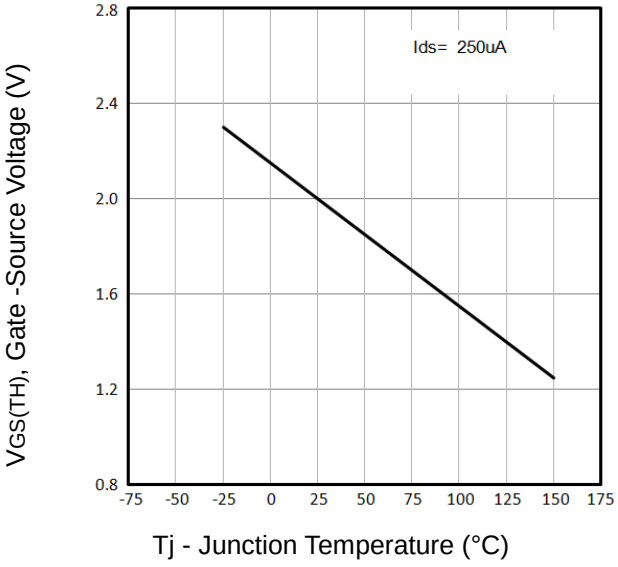


Fig2. Threshold Voltage Vs. Temperature

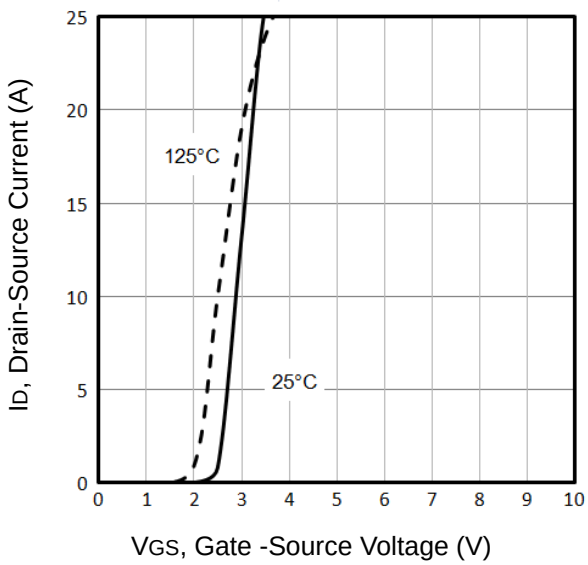


Fig3. Typical Transfer Characteristics

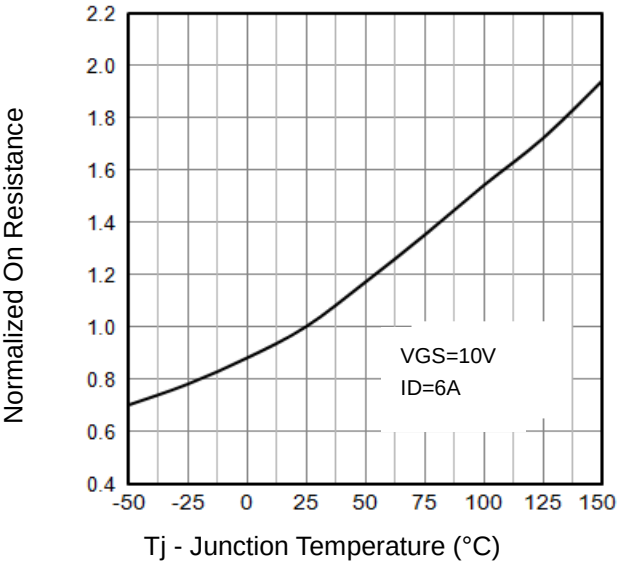


Fig4. Normalized On-Resistance Vs. Temperature

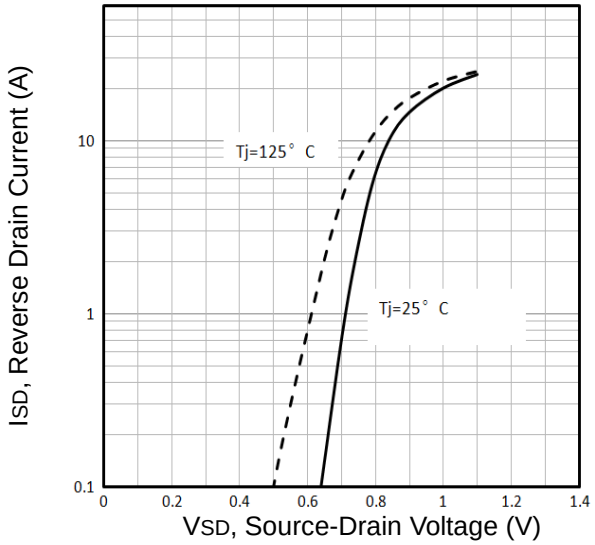


Fig5. Typical Source-Drain Diode Forward Voltage

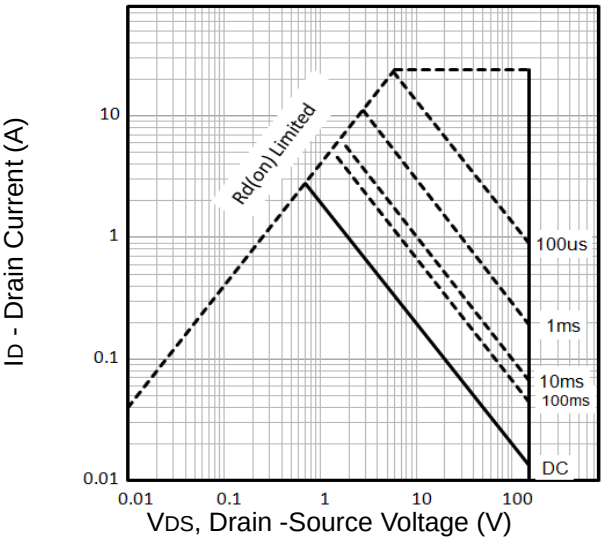


Fig6. Maximum Safe Operating Area

Typical Characteristics

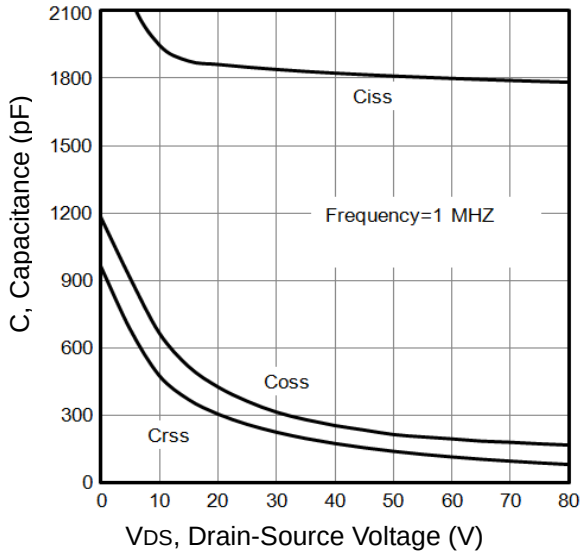


Fig7. Typical Capacitance Vs. Drain-Source Voltage

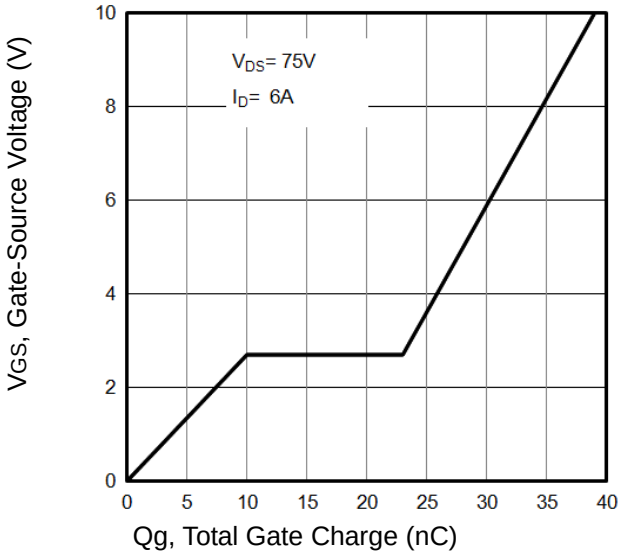


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

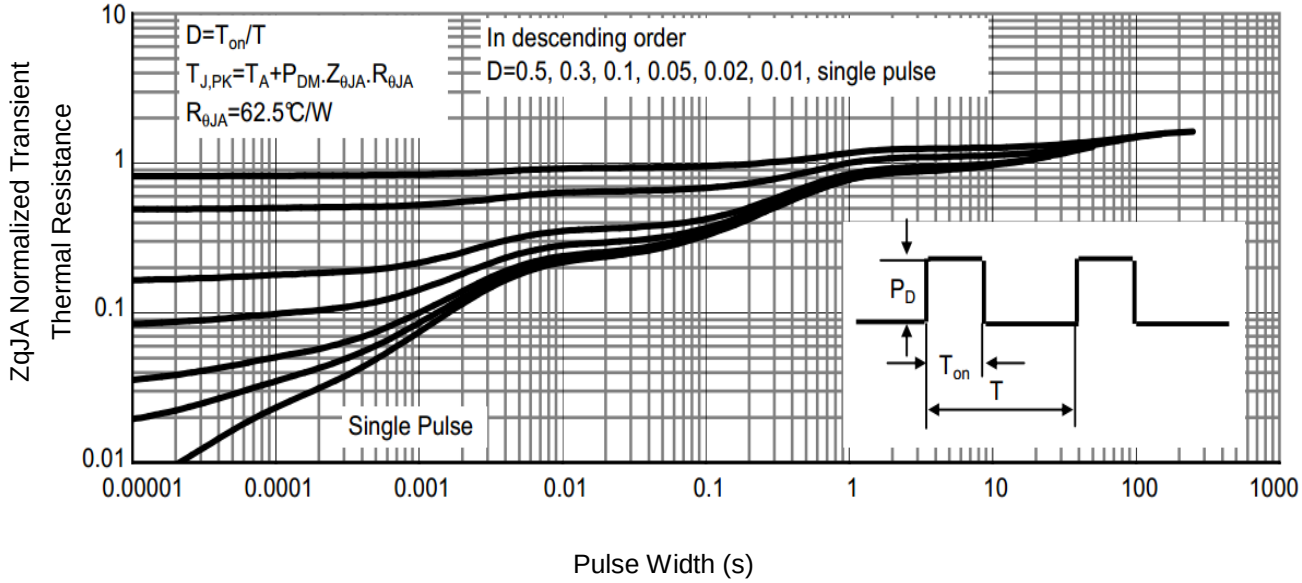


Fig 9: Normalized Maximum Transient Thermal

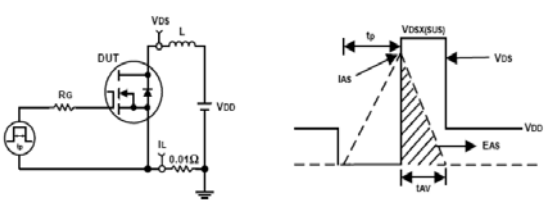


Fig10. Unclamped Inductive Test Circuit and waveforms

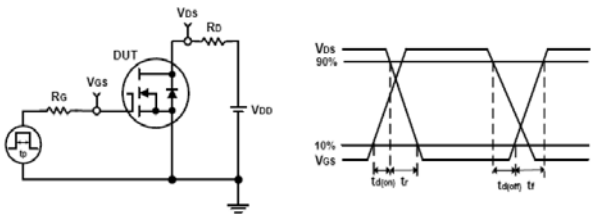
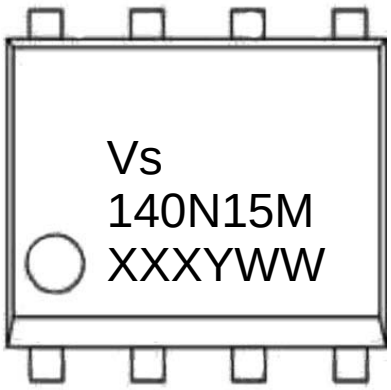


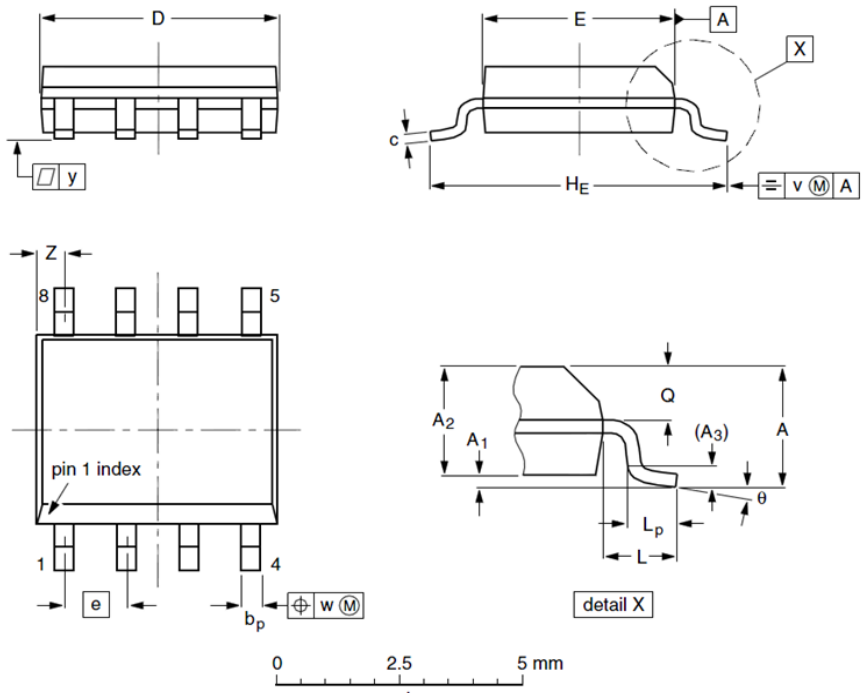
Fig11. Switching Time Test Circuit and waveforms

Marking Information



1st line：Company Code（Vs），Company Logo
2nd line：Part Number（140N15M）
3rd line：Date code （XXXYWW）
XXX：Wafer Lot Number
Y：Year Code，e.g. E means 2017
WW：Week Code

SOP8 Package Outline Data



Label	Dimensions (unit: mm)		
	Min	Typ	Max
A	--	--	1.75
A_1	0.10	0.18	0.25
A_2	1.25	1.35	1.50
A_3	--	0.25	--
b_p	0.36	0.42	0.51
c	0.19	0.22	0.25
D	4.80	4.92	5.00
E	3.80	3.90	4.00
e	--	1.27	--
H_E	5.80	6.00	6.20
L	--	1.05	--
L_p	0.40	0.68	1.00
Q	0.60	0.65	0.725
v	--	0.25	--
w	--	0.25	--
y	--	0.10	--
Z	0.30	0.50	0.70
θ	0°		8°

Notes:

1. Follow JEDEC MS-012.
2. Dimension "D" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension "E" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
4. Dimension "bp" does NOT include dambar protrusion. Allowable dambar protrusion shall be 0.1mm total in excess of "bp" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.

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