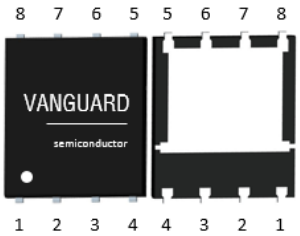
V_{DS}	60	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	2.1	mΩ
I_D	190	A

Features

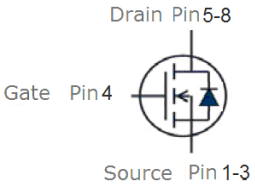
- Enhancement mode
- Low on-resistance $R_{DS(on)}$ @ V_{GS}=10 V
- VitoMOS® Ⅱ Technology
- 100% Avalanche test
- Pb-free lead plating; RoHS compliant

Pb-Free RoHS HF Halogen-Free

PDFN5060X



Part ID	Package Type	Marking	Tape and reel information
VSP002N06HS-G	PDFN5060X	002N06HG	3000PCS/Reel



Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		60	V
V_{GS}	Gate-Source voltage		±20	V
I_S	Diode continuous forward current	T_C =25°C	190	A
I_D	Continuous drain current @VGS=10V	T_C =25°C	190	A
		T_C =100°C	120	A
I_{DM}	Pulse drain current tested ①	T_C =25°C	760	A
I_{DSM}	Continuous drain current @VGS=10V	T_A=25°C	35	A
		T_A=70°C	28	A
EAS	Avalanche energy, single pulsed ②		320	mJ
P_D	Maximum power dissipation	T_C =25°C	125	W
		T_C =100°C	50	W
P_{DSM}	Maximum power dissipation ③	T_A=25°C	4.2	W
		T_A=70°C	2.7	W
T_{STG},T_J	Storage and Junction Temperature Range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1	1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	30	36	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	60	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T_j=125℃)	V_{DS}=60V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	2.3	3	4	V
$R_{DS(on)}$	Drain-Source On-State Resistance ④	V_{GS}=10V, I_D=40A	--	2.1	2.9	mΩ
		T_j=100℃	--	2.5	--	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
Ciss	Input Capacitance	V_{DS}=30V,V_{GS}=0V, f=1MHz	3815	5085	6765	pF
Coss	Output Capacitance		2170	2890	3845	pF
Crss	Reverse Transfer Capacitance		25	35	50	pF
Rg	Gate Resistance	f=1MHz	0.2	0.9	3	Ω
Qg	Total Gate Charge	V_{DS}=30V,I_D=40A, V_{GS}=10V	--	76	101	nC
Qgs	Gate-Source Charge		--	24	32	nC
Qgd	Gate-Drain Charge		--	18	27	nC
Switching Characteristics						
Td(on)	Turn-on Delay Time	V_{DD}=30V, I_D=40A, R_G=3Ω, V_{GS}=10V	--	19	--	ns
Tr	Turn-on Rise Time		--	63	--	ns
Td(off)	Turn-Off Delay Time		--	41	--	ns
Tf	Turn-Off Fall Time		--	26	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=40A,V_{GS}=0V	--	0.8	1.2	V
Trr	Reverse Recovery Time	T_j=25℃,I_{sd}=40A, V_{GS}=0V di/dt=100A/μs	--	66	132	ns
Qrr	Reverse Recovery Charge		--	69	138	nC

NOTE: ① Repetitive rating; pulse width limited by max junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.1mH, R_G = 25Ω, I_{AS} = 80A, V_{GS} =10V. Part not recommended for use above this value

③ The power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C.

④ Pulse width ≤ 380μs; duty cycle≤ 2%.

Typical Characteristics

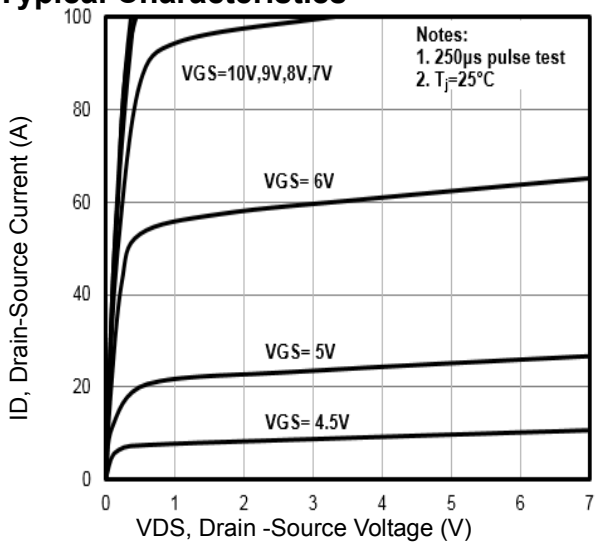


Fig1. Typical Output Characteristics

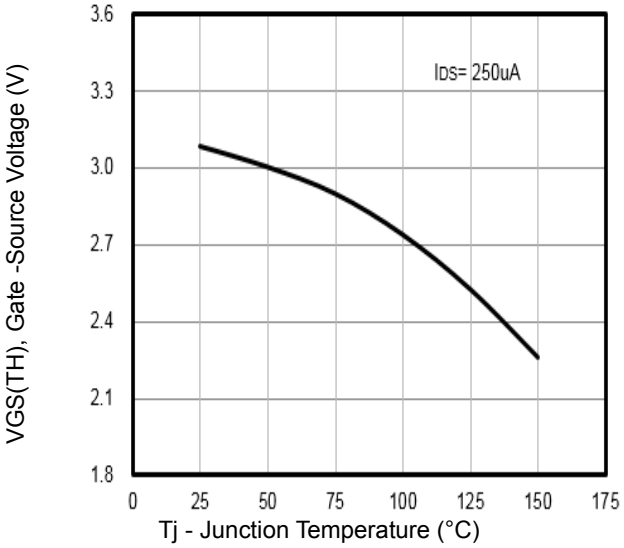


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs. Tj

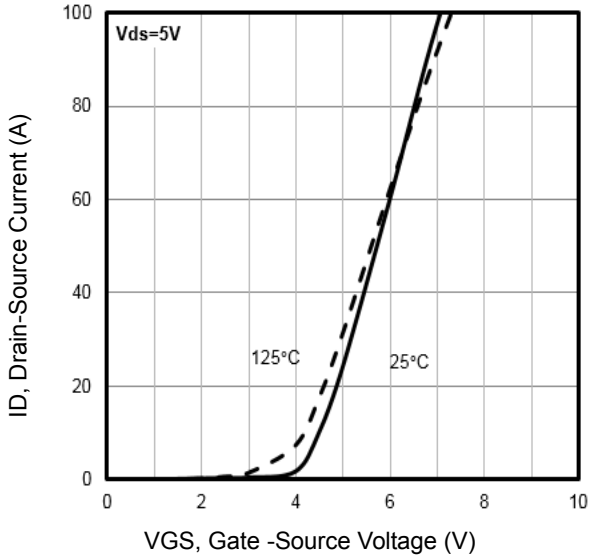


Fig3. Typical Transfer Characteristics

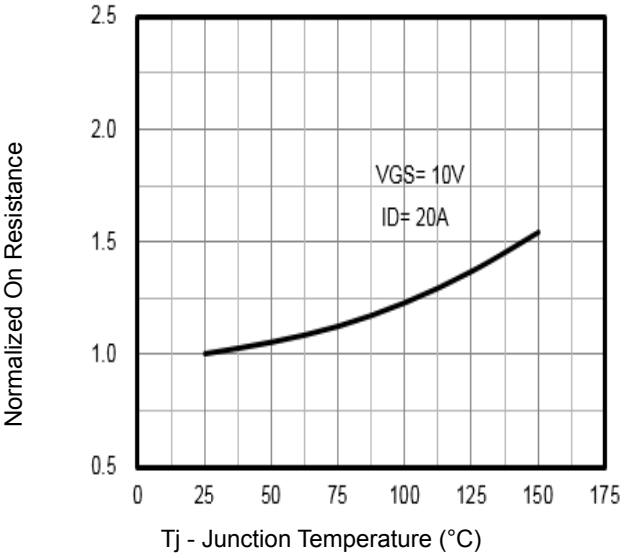


Fig4. Normalized On-Resistance Vs. Tj

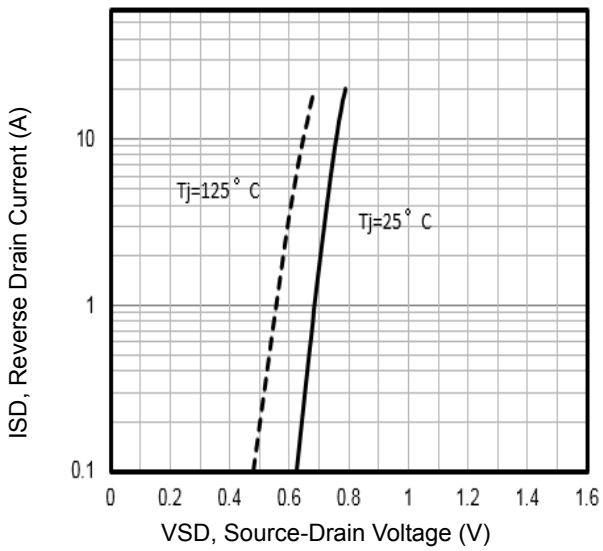


Fig5. Typical Source-Drain Diode Forward Voltage

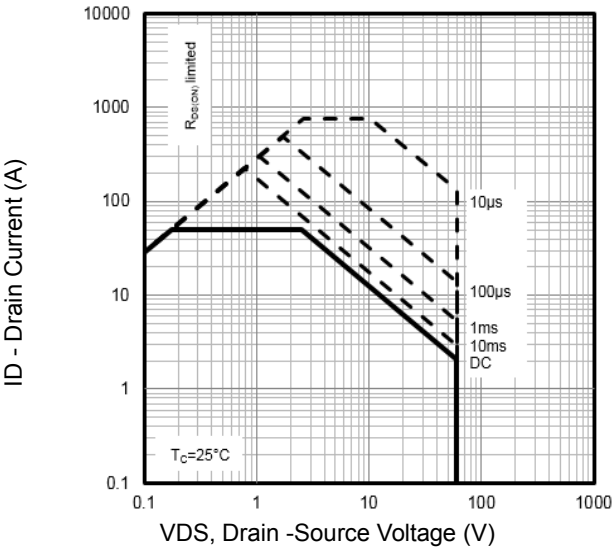


Fig6. Maximum Safe Operating Area

Typical Characteristics

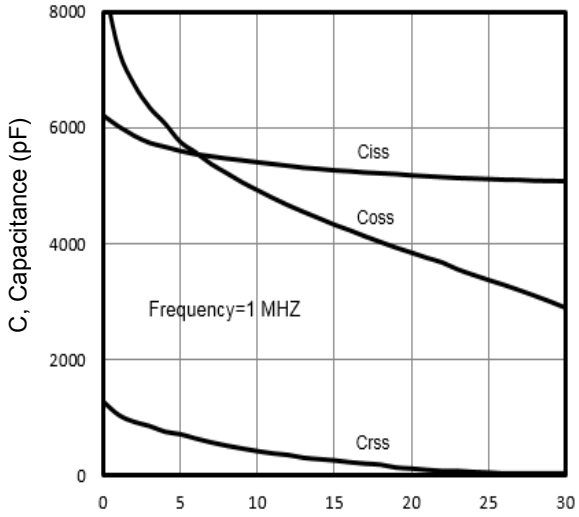


Fig7. Typical Capacitance Vs. Drain-Source Voltage

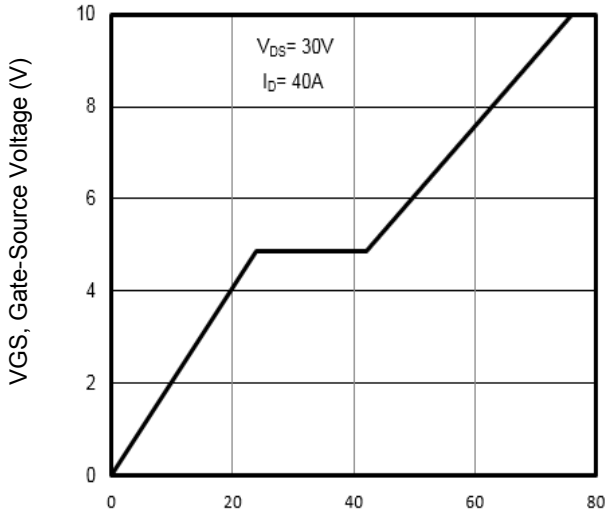


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

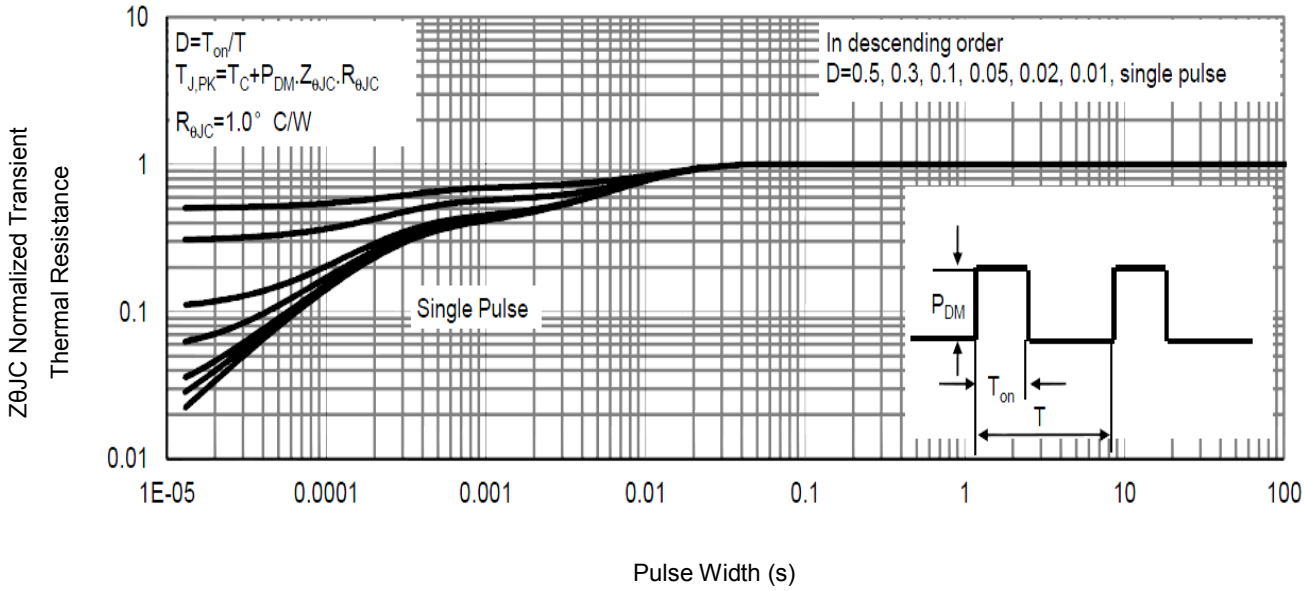


Fig9. Normalized Maximum Transient Thermal Impedance

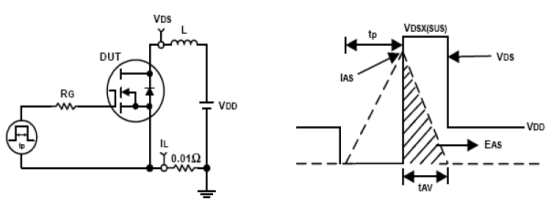


Fig10. Unclamped Inductive Test Circuit and waveforms

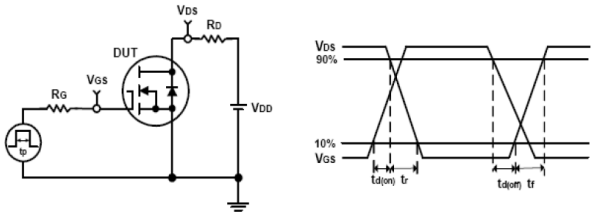
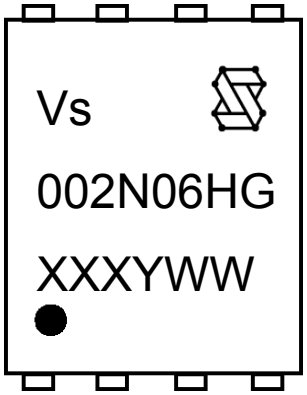


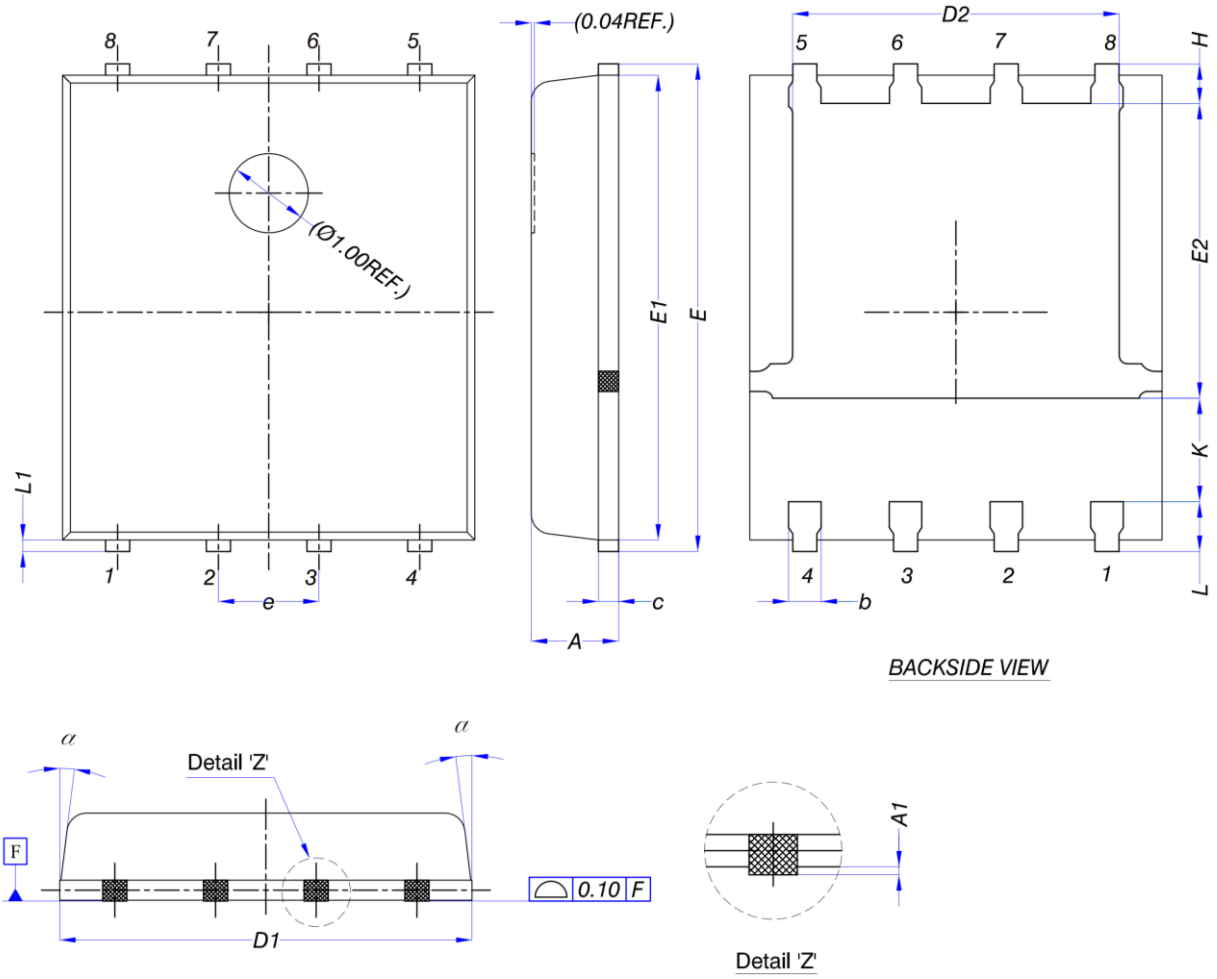
Fig11. Switching Time Test Circuit and waveforms

Marking Information



1st line： Vanguard Code（Vs）， Vanguard Logo
2nd line： Part Number（002N06HG）
3rd line： Date code （XXXYWW）
XXX： Wafer Lot Number Code , code changed with Lot Number
Y： Year Code，(e.g. E=2017, F=2018, G=2019, H=2020, etc)
WW： Week Code (01 to 53)

PDFN5060X Package Outline Data



Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
A	1.00	1.10	1.20
A1	0.00	--	0.05
b	0.30	0.40	0.50
c	0.20	0.25	0.30
D1	5.00	5.20	5.40
D2	3.80	4.10	4.25
E	5.95	6.15	6.35
E1	5.66	5.86	6.06
E2	3.52	3.72	3.92
e	1.27 BSC		
H	0.40	0.50	0.60
K	1.10	--	--
L	0.50	0.60	0.70
L1	0.08	0.15	0.22
α	0°	--	12°

Notes:

1. Refer to JEDEC MO-240 variation AA.
2. Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D1" and "E1" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.

Customer Service

Sales and Service:
sales@vgsemi.com
Vanguard Semiconductor CO., LTD
TEL: (86-755) -26902410
FAX: (86-755) -26907027
WEB: **www.vgsemi.com**