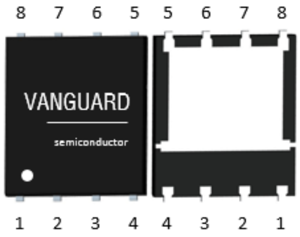
Features

- Enhancement mode
- Low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V
- VitoMOS® Ⅱ Technology
- 100% Avalanche test
- Pb-free lead plating; RoHS compliant

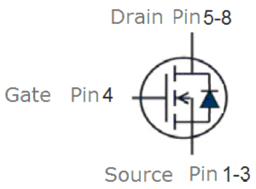
V_{DS}	40	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	2.3	mΩ
$R_{DS(on),TYP}$@ V_{GS}=4.5 V	3.4	mΩ
I_D	110	A

PDFN5x6



Pb-Free RoHS HF Halogen-Free

Part ID	Package Type	Marking	Tape and reel information
VSP003N04MS-G	PDFN5x6	003N04M	3000PCS/Reel



Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	**Parameter**		**Rating**	**Unit**
$V_{(BR)DSS}$	Drain-Source breakdown voltage		40	V
V_{GS}	Gate-Source voltage		±20	V
I_S	Diode continuous forward current	T_C =25°C	110	A
I_D	Continuous drain current @VGS=10V	T_C =25°C	110	A
		T_C =100°C	69	A
I_{DM}	Pulse drain current tested ①	T_C =25°C	440	A
I_{DSM}	Continuous drain current @VGS=10V	T_A=25°C	34	A
		T_A=70°C	27	A
EAS	Avalanche energy, single pulsed ②		45	mJ
P_D	Maximum power dissipation	T_C =25°C	44	W
		T_C =100°C	17.5	W
P_{DSM}	Maximum power dissipation ③	T_A=25°C	4.2	W
		T_A=70°C	2.7	W
T_{STG},T_J	Storage and Junction Temperature Range		-55 to 150	°C

Thermal Characteristics

Symbol	**Parameter**	**Typical**	**Max**	**Unit**
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.85	3.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	30	36	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	40	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T_j =125℃)	V_{DS}=40V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.3	1.7	2.5	V
$R_{DS(on)}$	Drain-Source On-State Resistance④	V_{GS}=10V, I_D=40A	--	2.3	3	mΩ
		T_j =100℃	--	2.8	--	mΩ
$R_{DS(on)}$	Drain-Source On-State Resistance④	V_{GS}=4.5V, I_D=30A	--	3.4	4.4	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
Ciss	Input Capacitance	V_{DS}=20V,V_{GS}=0V, f=1MHz	1830	2440	3245	pF
Coss	Output Capacitance		615	820	1090	pF
Crss	Reverse Transfer Capacitance		65	85	115	pF
Rg	Gate Resistance	f=1MHz	0.2	1.9	3	Ω
Qg(10V)	Total Gate Charge	V_{DS}=20V,I_D=40A, V_{GS}=10V	--	47	62.5	nC
Qg(4.5V)	Total Gate Charge		--	24	32	nC
Qgs	Gate-Source Charge		--	7.8	10.4	nC
Qgd	Gate-Drain Charge		--	10.6	16	nC
Switching Characteristics						
Td(on)	Turn-on Delay Time	V_{DD}=20V, I_D=40A, R_G=3Ω, V_{GS}=10V	--	8.2	--	ns
Tr	Turn-on Rise Time		--	78	--	ns
Td(off)	Turn-Off Delay Time		--	37	--	ns
Tf	Turn-Off Fall Time		--	28	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=40A,V_{GS}=0V	--	0.8	1.2	V
Trr	Reverse Recovery Time	T_j=25℃,I_{sd}=40A, V_{GS}=0V di/dt=100A/μs	--	32	64	ns
Qrr	Reverse Recovery Charge		--	16	32	nC

NOTE: ① Repetitive rating; pulse width limited by max junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.1mH, R_G = 25Ω, I_{AS} = 30A, V_{GS} =10V. Part not recommended for use above this value

③ The power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C.

④ Pulse width ≤ 380μs; duty cycle≤ 2%.

Typical Characteristics

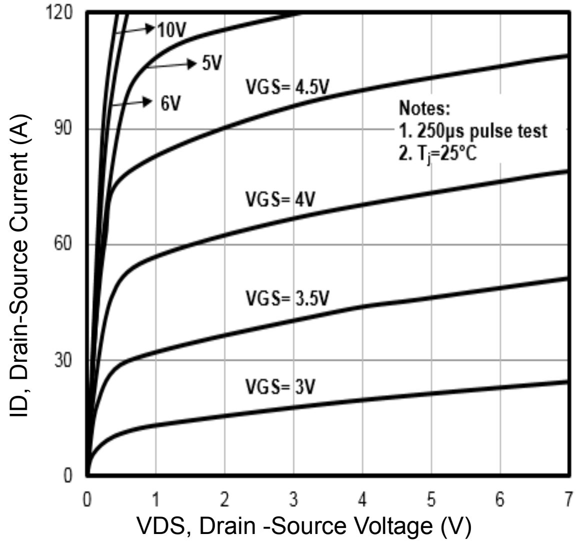


Fig1. Typical Output Characteristics

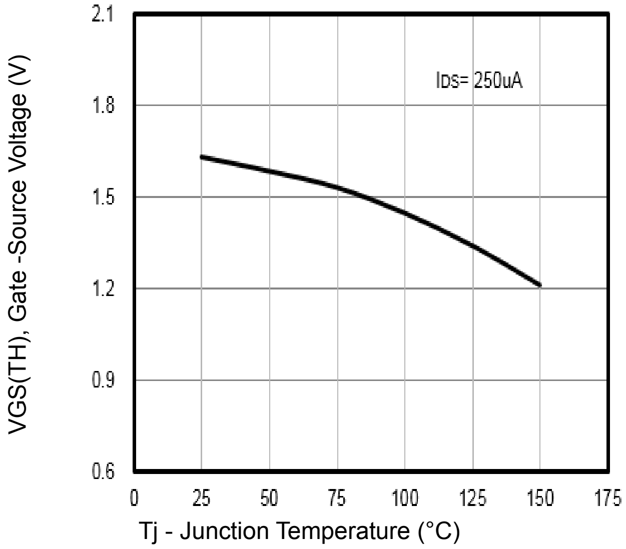


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs. Tj

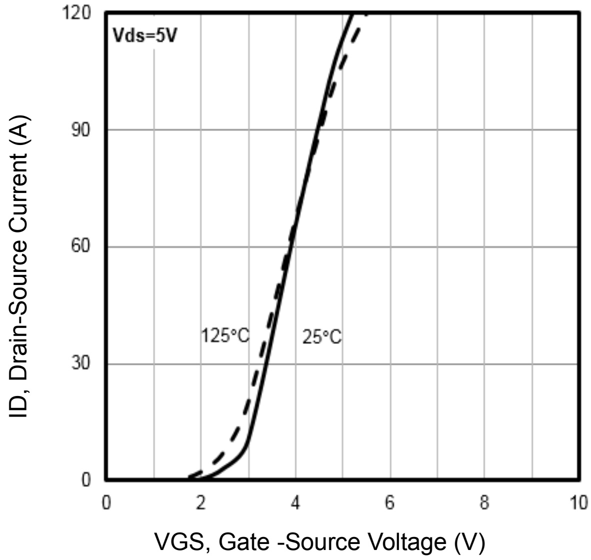


Fig3. Typical Transfer Characteristics

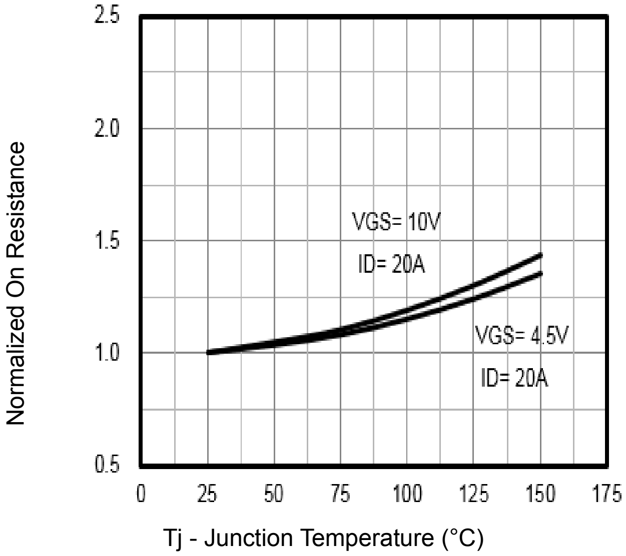


Fig4. Normalized On-Resistance Vs. Tj

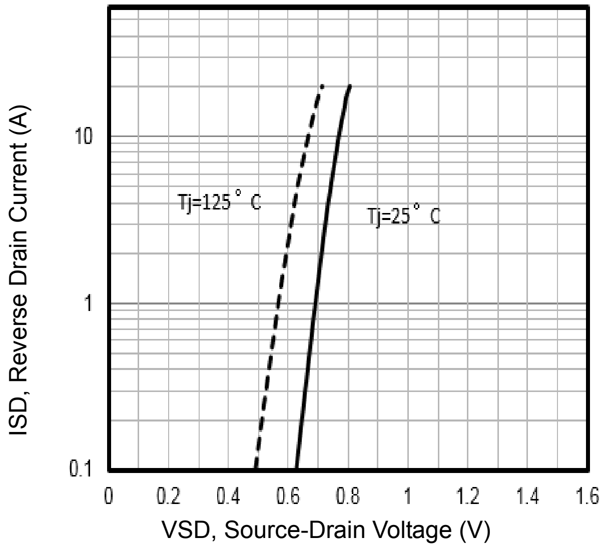


Fig5. Typical Source-Drain Diode Forward Voltage

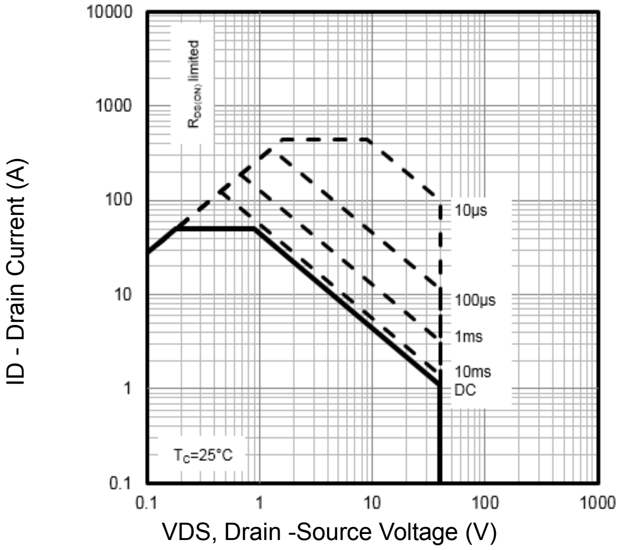


Fig6. Maximum Safe Operating Area

Typical Characteristics

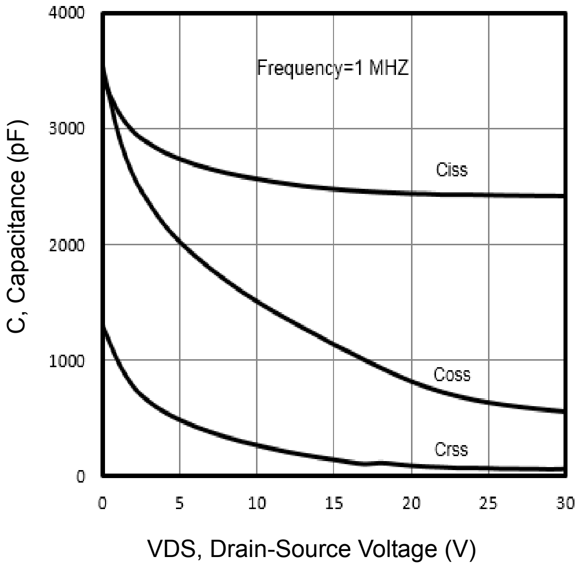


Fig7. Typical Capacitance Vs. Drain-Source Voltage

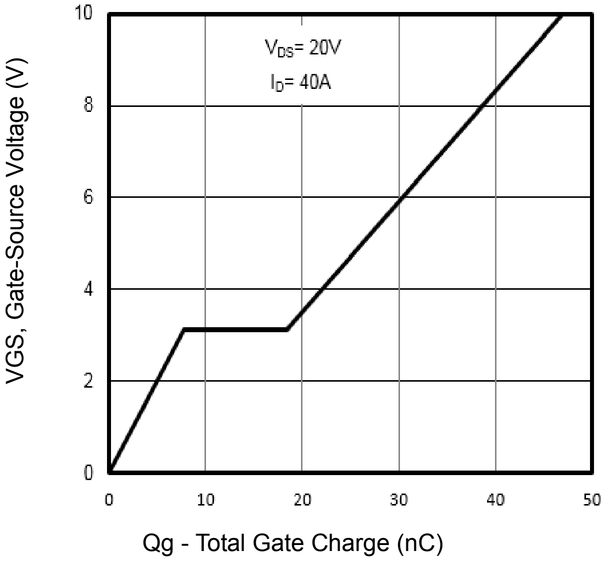


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

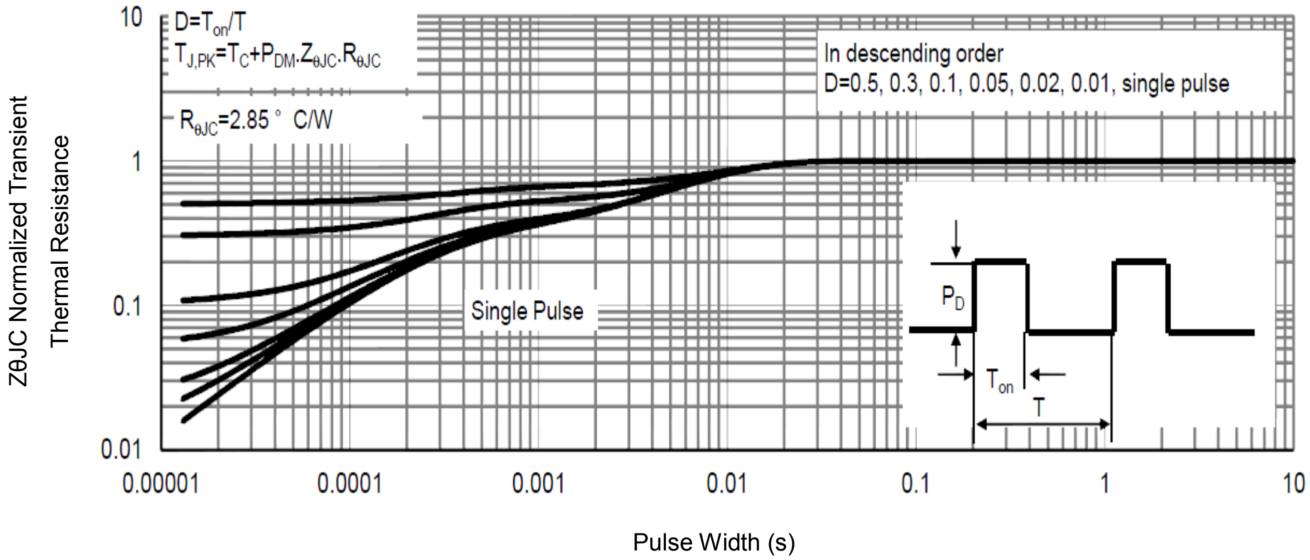


Fig9. Normalized Maximum Transient Thermal Impedance

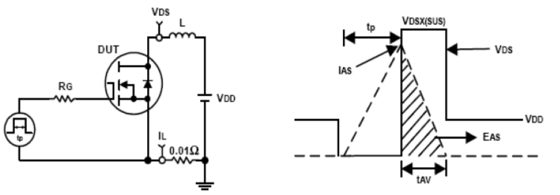


Fig10. Unclamped Inductive Test Circuit and waveforms

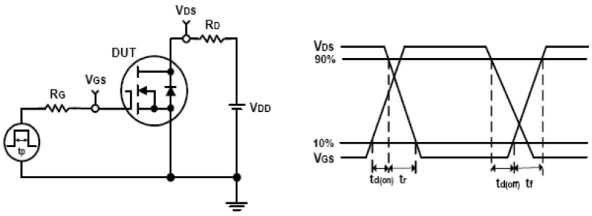
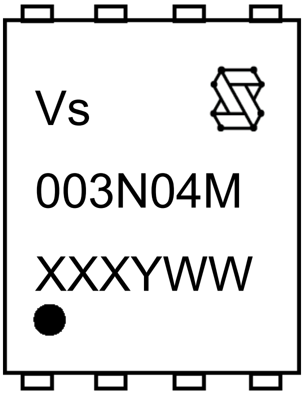


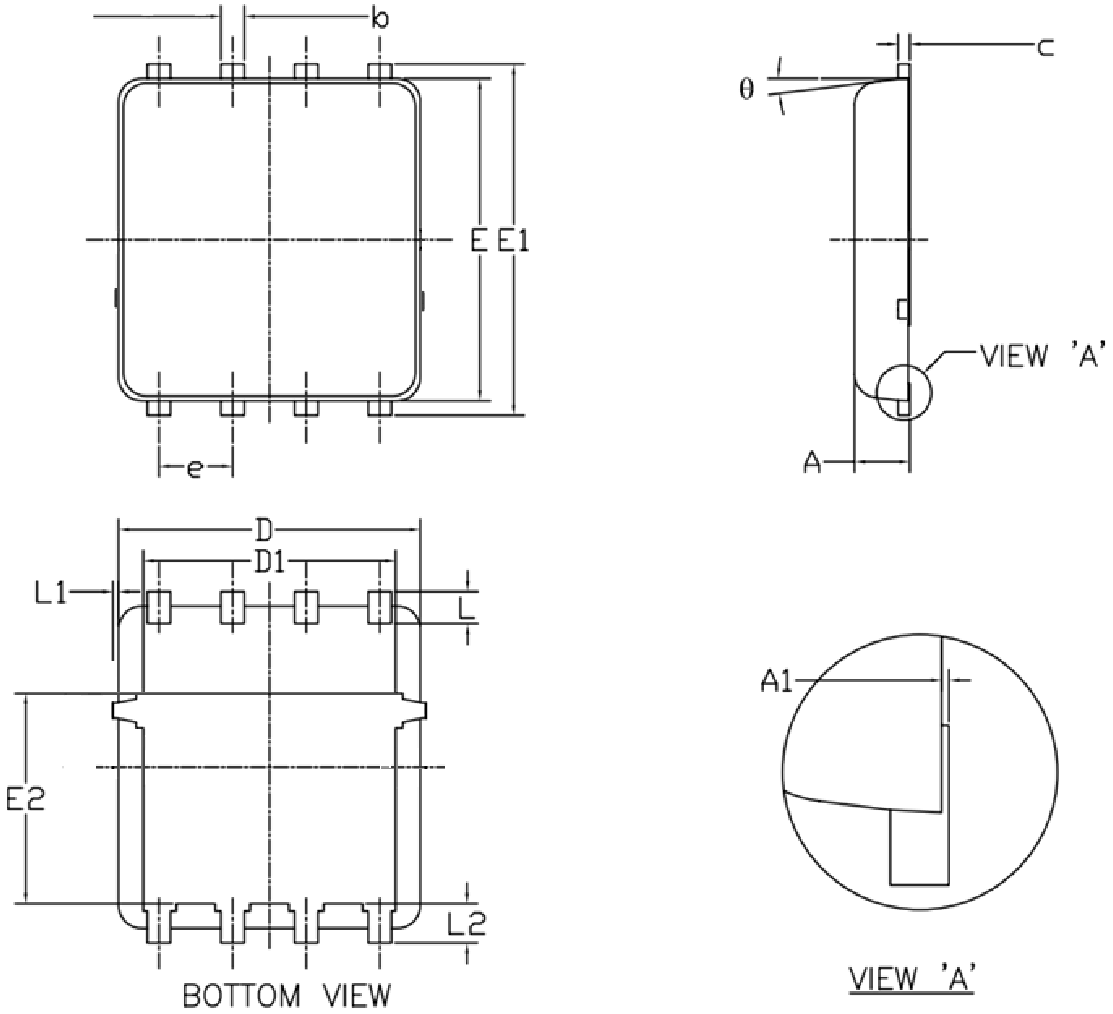
Fig11. Switching Time Test Circuit and waveforms

Marking Information



1st line：　Vanguard Code（Vs），　Vanguard Logo
2nd line：　Part Number（003N04M）
3rd line：　Date code　（XXXYWW）
　XXX：　Wafer Lot Number Code , code changed with Lot Number
　Y：　Year Code，(e.g. E=2017, F=2018, G=2019, H=2020, etc)
　WW：　Week Code (01 to 53)

PDFN5x6 Package Outline Data



Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
A	0.90	1.00	1.20
A1	0.00	--	0.05
b	0.30	0.40	0.51
c	0.20	0.25	0.33
D	4.80	4.90	5.40
D1	3.61	4.00	4.25
E	5.65	5.80	6.06
E1	5.90	6.10	6.35
E2	3.38	3.58	3.92
e	1.27 BSC		
L	0.51	0.61	0.71
L1	--	--	0.15
L2	0.41	0.51	0.61
θ	0°	--	12°

Notes:

1. Refer to JEDEC MO-240 variation AA.
2. Dimensions "D" and "E" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D" and "E" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.

Customer Service

Sales and Service:

sales@vgsemi.com

Vanguard Semiconductor CO., LTD
TEL: (86-755) -26902410
FAX: (86-755) -26907027
WEB: www.vgsemi.com