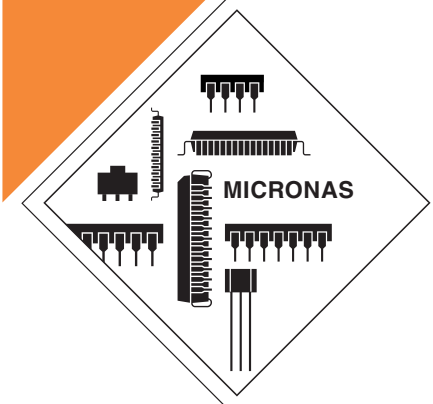


PRELIMINARY DATA SHEET

VSP 94x5B, VSP 94x7B
OPTIMUS
Color Decoder and Scan-Rate Converter
Version Cx

Edition Nov. 28, 2002
6251-576-3PD

MICRONAS

Contents

Contents, continued

Contents, continued

Color Decoder and Scan-Rate Converter

Release Note: Revision bars indicate significant changes to the previous edition. The hardware and software description in this document is valid for the VSP 94x5B/VSP 94x7B version Cx.

1. Introduction

The VSPB family supports 15/32 kHz systems and is available with different options. VSP 94xxB has one channel only. VSP 94x5B supports two channels, including PiP, double-window etc. The VSP 942xB versions come in a MQFP144 package, whereas all other versions come in a MQFP80 package, pin compatible to other VSP 94xx devices (e.g. VSP 94x2A). The VSP 943xB and VSP 944xB come without scan-rate-converter and a single-scan (50i/60i) signal is output. Table 1–1 and Table 1–2 give an overview of the VSPB single-chip family.

Table 1–1: Optimus family for double-scan application

Type	Package	PiP	Digital Input	Analog Input	Digital Output	Analog Output
VSP 94**05B**	MQFP80		ITU656[1)]	7xCVBS/YC, 2xRGB/YUV	DS656[1),2)]	1xYUV/RGB, 3xCVBS
VSP 94**15B**	MQFP80		ITU656	7xCVBS/YC, 2xRGB/YUV	DS656	3xCVBS
VSP 94**25B**	MQFP144		ITU656	9xCVBS/YC, 2xRGB/YUV	ITU601, DS656, RGB/YUV(27bit)	1xYUV/RGB, 3xCVBS
VSP 94**07B**	MQFP80	✓	ITU656[1)]	7xCVBS/YC, 2xRGB/YUV	DS656[1)]	1xYUV/RGB, 3xCVBS
VSP 94**17B**	MQFP80	✓	ITU656	7xCVBS/YC, 2xRGB/YUV	DS656	3xCVBS
VSP 94**27B**	MQFP144	✓	ITU656	9xCVBS/YC, 2xRGB/YUV	ITU601, DS656, RGB/YUV(27bit)	1xYUV/RGB, 3xCVBS

[1)] Input and output can not be used at same time (pin sharing)
[2)] DS656 is an ITU656 like, double-scan interface for connection to DDP 3315C

Table 1–2: Optimus family for single-scan applications

Type	Package	PiP	Digital Input	Analog Input	Digital Output	Analog Output
VSP 94**35B**	MQFP80		ITU656[1)]	7xCVBS/YC, 2xRGB/YUV	ITU656[1)]	1xYUV/RGB, 3xCVBS
VSP 94**45B**	MQFP80		ITU656	7xCVBS/YC, 2xRGB/YUV	ITU656	3xCVBS
VSP 94**37B**	MQFP80	✓	ITU656[1)]	7xCVBS/YC, 2xRGB/YUV	ITU656[1)]	1xYUV/RGB, 3xCVBS
VSP 94**47B**	MQFP80	✓	ITU656	7xCVBS/YC, 2xRGB/YUV	ITU656	3xCVBS
VSP 94**25B**[2)]	MQFP144		ITU656	9xCVBS/YC, 2xRGB/YUV	ITU601, DS656, RGB/YUV(27bit)	1xYUV/RGB, 3xCVBS
VSP 94**27B**[2)]	MQFP144	✓	ITU656	9xCVBS/YC, 2xRGB/YUV	ITU601, DS656, RGB/YUV(27bit)	1xYUV/RGB, 3xCVBS

[1)] Input and output can not be used at same time (pin sharing)
[2)] VSP 9425B and 9427B can be used in single-or double-scan applications.

Table 1–3: Compatibility and suited backend ICs

Hardware Compatible[1)]	DDP 3315C	SDA 9380
VSP 94**02A**, VSP 94**32A** VSP 94**05B**, VSP 94**35B** VSP 94**07B**, VSP 94**37B**	✓ (no ITU656 input possible)	✓
VSP 94**12A,** VSP 94**42A** VSP 94**15B**, VSP 94**45B** VSP 94**17B,** VSP 94**47B**	✓	
VSP 94**25B** VSP 94**27B**	✓	✓
[1)] With some restrictions. Please refer to pin description and/or respective application note		

1.1. Feature Overview

– Different application modes
  - FSM: Frame based high performance master with PiP
  - SSC: Split screen ("Double Window")
  - MUP: Multi pictures, several still and 2 live pictures possible
  - PC: PC signal in combination with TV signal (TV in PC or PC in TV)

– Data acquisition connectivity
  - Up to seven (VSP 9425B/9427B: nine) CVBS inputs, up to two Y/C inputs
  - Up to three CVBS outputs (even when Y/C input)
  - ITU-R 656 compatible digital input
  - RGB/FBL or YUV or YUV-H-V input
  - 9 bit amplitude resolution for CVBS/Y/C A/D converter
  - 8 bit amplitude resolution for RGB/FBL A/D converter

– Multi-standard color decoder with 4H comb-filter
  - PAL/NTSC/SECAM including all substandard
  - Automatic recognition of chroma standard
  - AGC (Automatic Gain Control)

– Second multi-standard color decoder for slave channel (VSP 94x7B only)

– Processing of two input channels independently: Master and slave channel

– Temporal noise reduction for master and slave channel
  - Field or frame based temporal noise reduction for luminance and chrominance

– Pre-scaling of the $1f_H$ signal (master and slave channel)
  - Horizontal scaling factors: 3/2...1...1/28
  - Vertical scaling factors: 1...1/30

– Horizontal and vertical scaling of the $2f_H$ signal (master and slave channel)
  - Horizontal Scaling factors: 3...0.75
  - 5 zone horizontal panorama generator

– Vertical scaling of the $2f_H$ signal (master channel)
  - Vertical scaling factors: 8...0.92
  - 5 zone vertical panorama generator

– Detection circuits
  - Global motion and global still detection
  - Film mode and phase detection (PAL, NTSC; 2-2, 3-2 pull down)
  - Measurement of the noise level (blanking)
  - Detection of letter box formats

– Embedded memory
  - On-chip memory controller
  - Embedded DRAM core for field memory
  - SRAM for delay lines

– Data format 4:2:2

– Data slicer for closed caption ("V-chip") and WSS

– Flexible clock and synchronization concept
  - Horizontal line-locked or free-running mode

– Scan-rate-conversion (version dependent)
  - Motion adaptive frame based 100/120 Hz interlaced scan-rate conversion
  - Motion adaptive frame based 50/60 Hz progressive scan-rate conversion
  - Special treatment for film material ("Inverse 3-2 pull down")
  - Large area and line flicker reduction
  - Simple progressive modes: AB, AA*
  - Simple interlaced modes (100/120 Hz): ABAB, AABB, AAAA, BBBB
  - No scan-rate-conversion modes (50/60 Hz): AB, AA, BB
– Signal manipulations
  - Still field or still frame
  - Insertion of colored background
  - 2D and 3D frames for master and slave channel
  - Snapshot
  - Windowing
  - Temporal overblending between master and slave
  - Vertical chrominance shift for improved VCR picture quality
  - Mosaic-mode generator
  - Test pattern generator
  - Demo mode
  - Contrast, brightness and saturation control
– Sharpness improvement
  - Digital color transition improvement (DCTI)
  - Adaptive horizontal and vertical peaking (luminance)
  - Digital luminance transition improvement (DLTI)
  - Digital contrast improvement (DCI, master channel only)
– (S) VGA support
  - Synchronization to external (S)VGA source possible
  - Scaling of VGA picture, including TV picture and VGA display "side-by-side"
– Three D/A converters
  - 9 bit amplitude resolution for YUV, RGB output
  - (Nominal) 72 MHz clock frequency with two-fold oversampling
– Digital output (version dependent)
  - 4:4:4 YUV or RGB output with 24 or 27 bit
  - 4:2:2 YUV output with 24 or 27 bit
  - $2f_H$-8bit (656 like) digital output
  - ITU-R 656 compatible digital output
– I^2C bus control (400 kHz)
– 1.8 V± 5% and 3.3 V ± 5% supply voltages
– P-MQFP-80 or P-MQFP-144 package
– Only one crystal necessary for whole IC and all color standards

1.2. Block Diagram

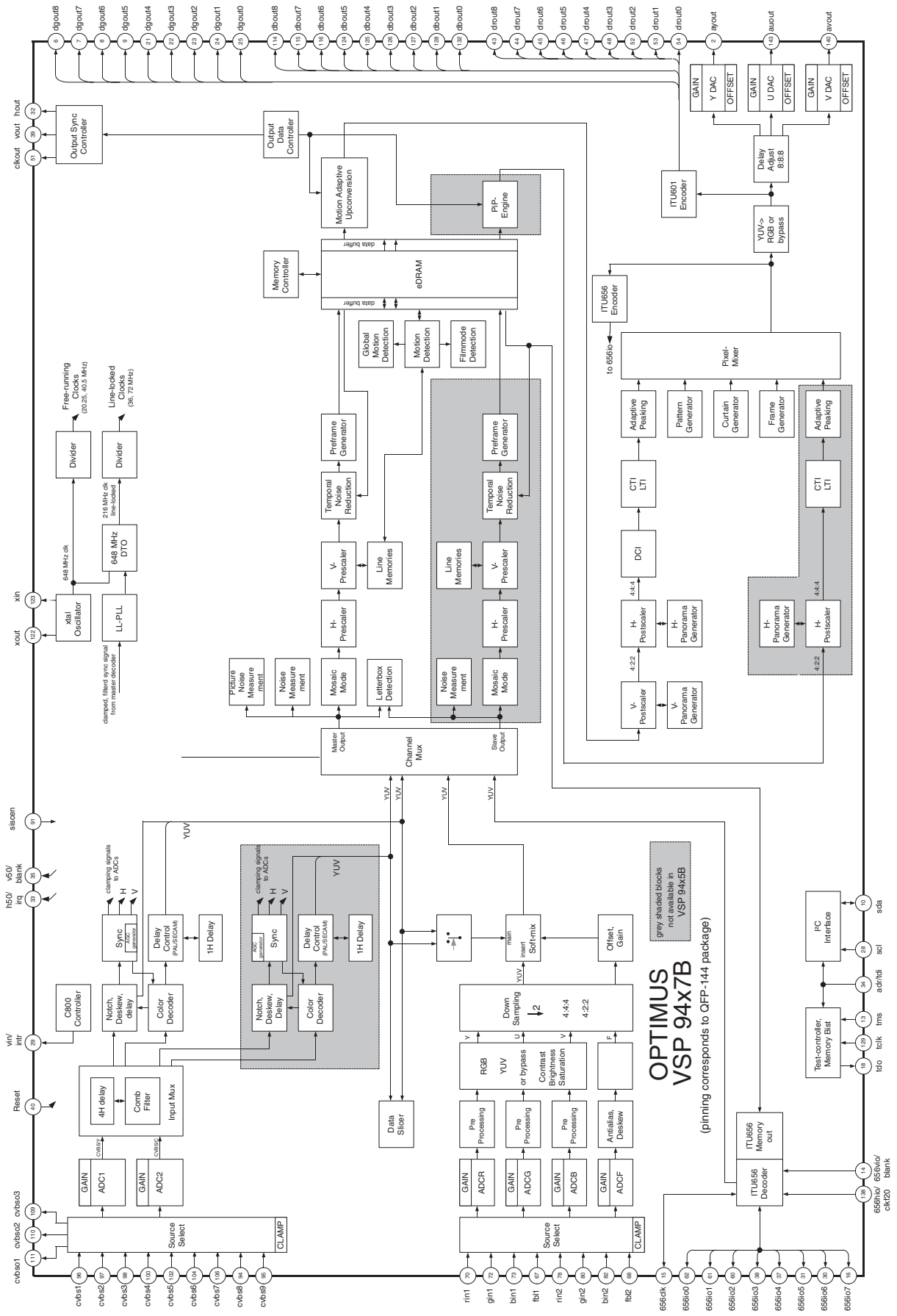


Fig. 1–1: Block diagram (MQFP144 package)

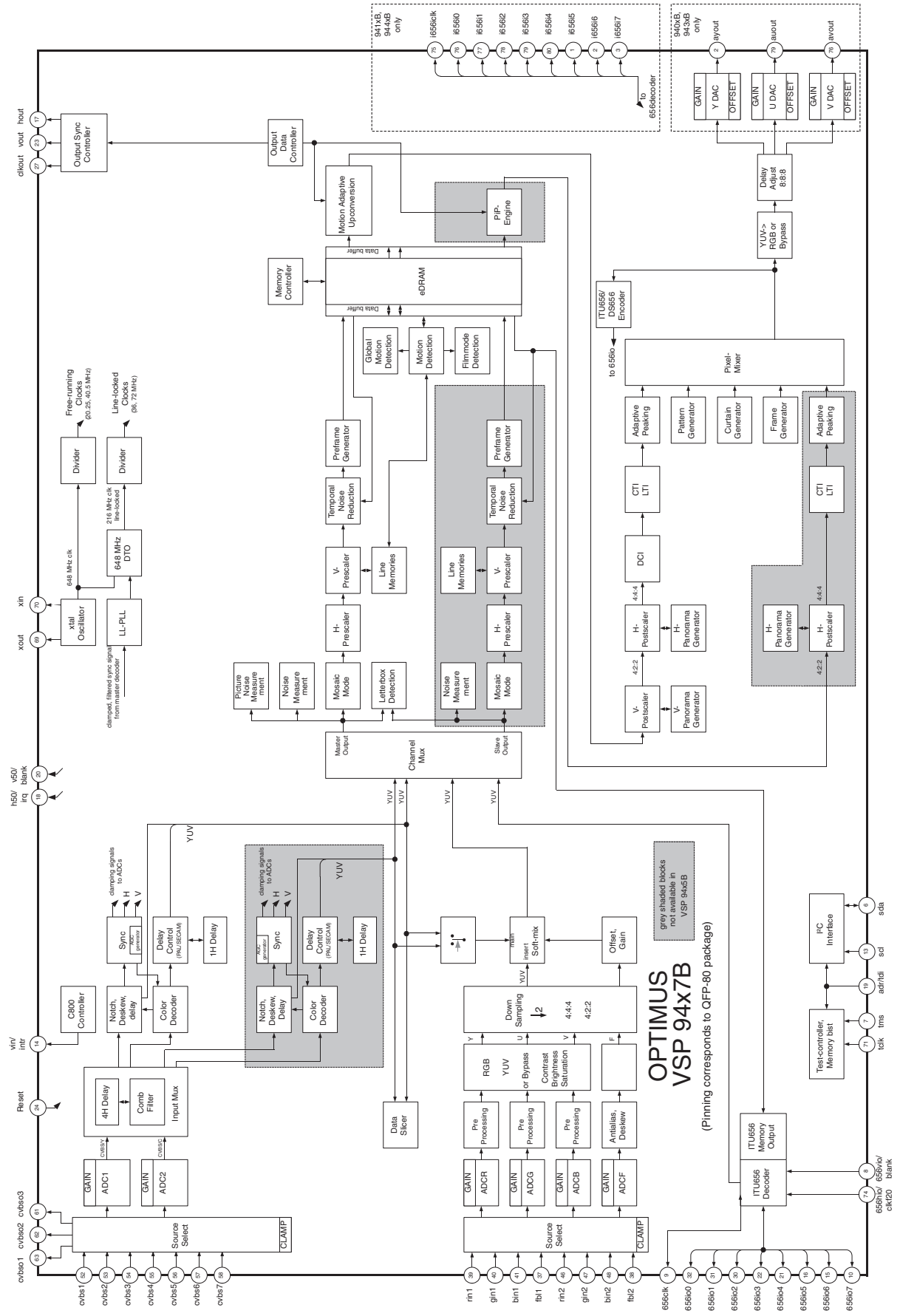


Fig. 1–2: Block diagram (MQFP80 package)

2. Functional Description

2.1. General Description

The VSP 94xxB (OPTIMUS) is a new component of the Micronas MEGAVISION® single-chip-IC family. The VSP 94xxB family comprises all main functions of a digital featurebox in one monolithic IC. The amount of features is splitted up to different levels from mid to high end, always giving highest picture quality. The family is ideally suited to work in conjunction with the deflection processors SDA 9380 or DDP 3315C (dependent on VSP 94xxB version). In combination with the “digital TV decoder” MDE 9500 double-scan iDTV are possible. 50/60 Hz derivatives are also available. The device comprises digital multistandard color decoder for master and slave channel, a RGB interface with fast-blank capability (SCART), scaling units including panorama, embedded DRAM for upconversion, high performance frame based upconversion algorithms, picture improvements, temporal noise reduction as well as A/D and D/A converter.

2.2. Chip Architecture

The OPTIMUS contains many blocks which are dedicated to master channel only (e.g. vertical postscaler) which can only be used with master channel. Some blocks are twice implemented (e.g. noise reduction). Some blocks are only once available but can be selected to work in master or slave channel (e.g. data-slicer). VSP 94xxB does not contain dedicated slave blocks. All items mentioned for slave channel in the data sheet are not valid for VSP 94xxB (see Table 2–2 on page 11).

All I²C bus registers mentioned are printed in bold and italics (e.g. ***YCDEL***).

2.3. Data Acquisition

The “Data Acquisition Processing” provides two independent data streams (master and slave) for the input processing. They either come from a CVBS, Y/C, RGB or YUV input or from a CCIR 656 compatible digital input signal. For RGB and YUV, interlace and progressive signals up to XGA can be connected. High resolution PC signals (SVGA, XGA etc.) may only be reproduced with limited picture quality (see Table 2–3 on page 11).

Table 2–1: Versions available

Version	Scan-rate Conversion	Output Format	PiP	Package
9405B	50p/60p/100i/120i	Analog, DS656	-	QFP80
9415B	50p/60p/100i/120i	DS656	-	QFP80
9425B	50i/60i/50p/60p/100i/120i	Analog, DS656, digital RGB/YUV	-	QFP144
9435B	50i/60i	Analog, ITU656	-	QFP80
9445B	50i/60i	ITU656	-	QFP80
9407B	50p/60p/100i/120i	Analog, DS656	PiP	QFP80
9417B	50p/60p/100i/120i	DS656	PiP	QFP80
9427B	50i/60i/50p/60p/100i/120i	Analog, DS656, digital RGB/YUV	PiP	QFP144
9437B	50i/60i	Analog, ITU656	PiP	QFP80
9447B	50i/60i	ITU656	PiP	QFP80

Table 2–2: Master/Slave building blocks

Function	Defined for Master	Defined for Slave	Defined for Master or Slave
Color decoder	✓	✓	
Letterbox			✓
Temporal noise reduction	✓	✓	
Film mode detector	✓		
Data-slicer			✓
Comb-filter			✓
CTI/LTI/adaptive peaking	✓	✓	
Noise measurement (blanking)	✓	✓	
Noise measurement (picture content)			✓
H/V-prescaler	✓	✓	
H-panorama postscaler	✓	✓	
V-panorama postscaler	✓		
Preframe generator	✓	✓	
Mosaic mode generator	✓	✓	
Global motion detection	✓		
Global still detection	✓		
Digital contrast improvement	✓		

Table 2–3: Allowed analog and digital input signals

Input Signals	f_H [kHz]	Remark
CVBS/Y/C	15.6	Standard TV (PAL, NTSC, SECAM)
YUV (sync on Y)	15.6	DVD (EIA770.1)
	31.2	Progressive DVD (EIA770.2)
RGB+CVBS/ RGB+sync	15.6	DVD
RGB+H+V	31.5	VGA
	37.9	SVGA
	48.3	XGA
Limit values for analog inputs	53	
Digital 656	15.6	(Only single-scan possible)

2.3.1. Double CVBS Frontend

The CVBS and Y/C decoding is done by two CVBS-frontends working in parallel. Normally, the comb-filter is connected to the first frontend, giving the main picture whereas the second frontend generates an uncombed picture for the PiP channel.

The input of frontend 1 is selected by ***COMBUSEM***, the input for frontend 2 is selected by ***COMBUSES*** (refer to Figure 2–1).

As two CVBS-ADC are not sufficient for any combination of input signals, RGB-ADCs can be used as well for CVBS, Y/C conversion. When using these ADCs, the signal must be switched/connected on the PCB accordingly.

At least two solutions are possible:

– When using Y/C for main channel, PiP channel can be connected to G_ADC. An external device must be used to switch one CVBS output and the G-signal to GIN1. If only one RGB/YUV input is required, one CVBS out can be directly connected to GIN2.

– When two Y/C inputs are required, Y1 and Y2 can be connected to CVBSIN4 and CVBSIN6, C1 and C2 can be connected to RIN1 and RIN2 (please refer to "Source Select" on page 20).To make use of the 'Y/C to CVBS adder', C1 and C2 should be additionally connected to CVBSIN5 and CVBSIN7.

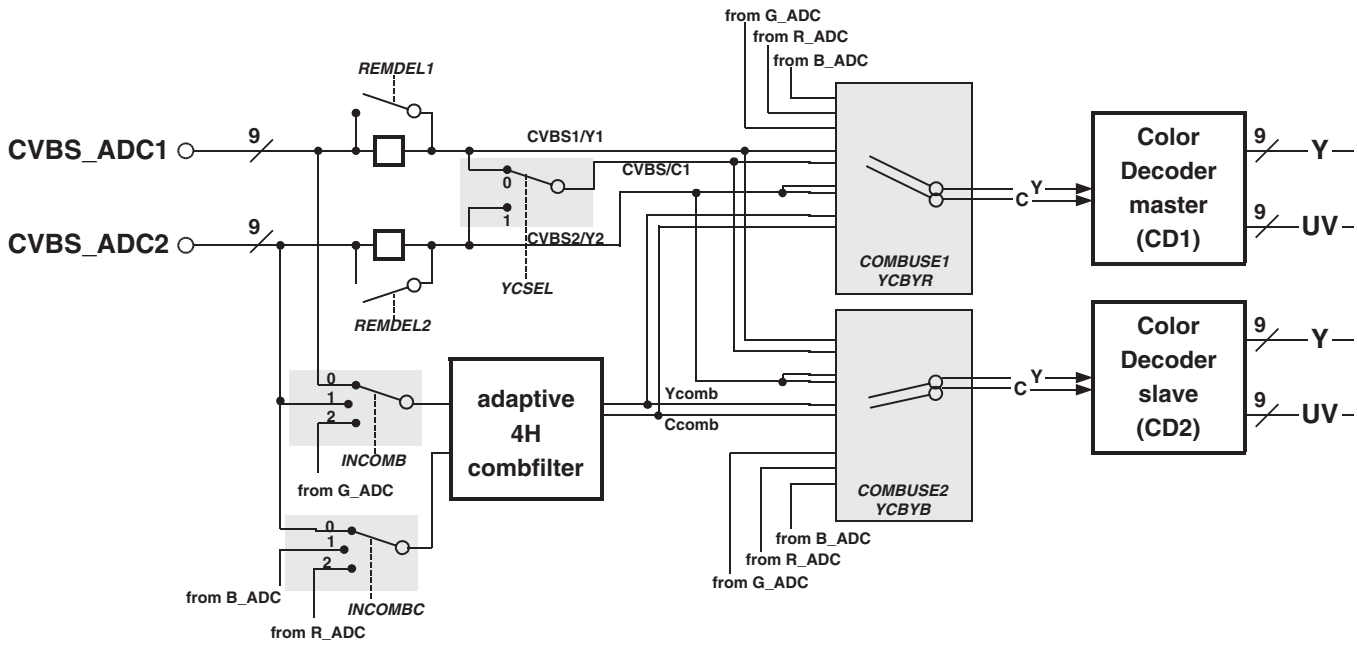


Fig. 2–1: Double CVBS frontend

Table 2–4: Input signal combinations

COMBUSEM	**Y_CD1**	**C_CD1**
0	CVBS1	CVBS/C (***YCBYR***=0)
		R_ADC (***YCBYR***=1)
1	CVBS2	CVBS2 (***YCBYR***=0)
		B_ADC (***YCBYR***=1)
2[1)]	Ycomb	Ccomb
3	G_ADC	G_ADC (***YCBYR***=0)
		R_ADC (***YCBYR***=1)
COMBUSES	**Y_CD2**	**C_CD2**
0	CVBS1	CVBS/C (***YCBYB***=0)
		R_ADC (***YCBYB***=1)
1	CVBS2	CVBS2 (***YCBYB***=0)
		B_ADC (***YCBYB***=1)
2[2)]	Ycomb	Ccomb
3	G_ADC	G_ADC (***YCBYB***=0)
		B_ADC (***YCBYB***=1)

[1)] When using COMBUSEM=2, BGSHIFTM must be set to 1, otherwise 0.
[2)] When using COMBUSES=2, BGSHIFTS must be set to 1, otherwise 0

2.3.2. Analog CVBS and Y/C Inputs

Source Select

The analog CVBS signal can be fed to the inputs CVBS1...7 (or 3x CVBS and 2x Y/C) of VSP 94x7B (amplitude 0.5...1.5 V_{pp}). In P-MQFP144 package, 9 CVBS inputs (or 5x CVBS and 2x Y/C) are possible and 3 CVBS outputs are available. One signal is selected via ***CVBSEL1*** and fed to first ADC. A second signal is selected via ***CVBSEL2*** and fed to the other ADC. Although every input CVBS1...CVBS9 can handle CVBS/Y or C signals, CVBS4&5 or CVBS6&7 are intended to be used as separate Y/C inputs (***YCSEL***).

After clamping to the back porch (switchable to sync-tip clamping by ***CLPSTGY***) both signals are AD-converted with an amplitude resolution of 9 bit. The conversion is done using a 20.25 MHz free-running crystal stable clock. Before this the signals are lowpass filtered by antialias filter.

Three inputs can be looped back to output CVBSO1-3 (***CVBOSEL1***, ***CVBOSEL2***, ***CVBSELO3***). A signal addition is performed to output a CVBS signal even when separate Y/C signals are used at input. Inputs that are not used by ADC are roughly clamped to fit in the allowed voltage region. For stand-by operation (power-save mode), A/D and D/A converter can be switched off by ***STANDBYxxx*** keeping the source-selector operational.

If ***CVBSEL1*** and ***CVBSEL2*** are switched to the same input, a superimposing of clamping pulses and clamping values occur. This case must be avoided. If it is desired to display one source on both channels, disable ADC2 (***CVBSEL2***='1111') and distribute output from ADC1 to master and slave CD by ***COMBUSEM*** and ***COMBUSES***.

Figure 2–3 shows the analog frontend.

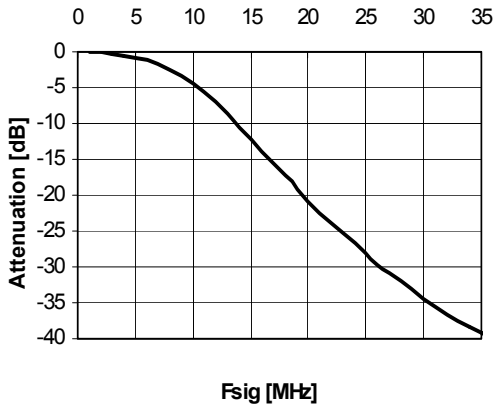


Fig. 2–2: Default characteristic of analog CVBS/Y/C antialias filter

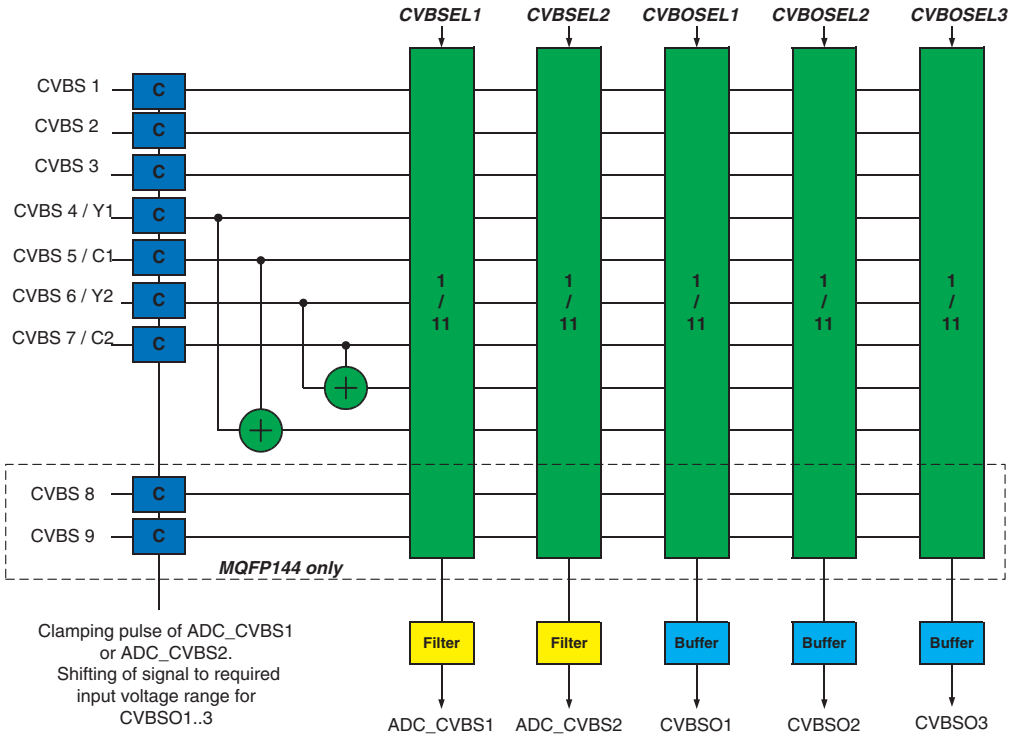


Fig. 2–3: Input selection

2.3.2.1. Signal Magnitudes and Gain Control

To adjust to different CVBS input voltages a digitally working automatic gain control is implemented. Input voltages in the range between 0.6 to 1.8 V_{pp} can be applied to the CVBS inputs. The AGC behavior can be chosen from four possible ***AGCMD*** modes (see Table 2–5).

When using the sync height, the A/D gain rises or falls depending on the sync-height of the incoming signal. When using overflow detection only, the gain is set to maximum and is reduced whenever an "overflow" occurs. The signal is lowpassed so that chrominance and noise are not used for detection.

The threshold can be adjusted by ***PWTHD***. A setting of '11' equals 511 and means an overflow of the ADC. Other settings react for a lower level. The gain only becomes higher when a change of the channel is detected or is manually reset by ***AGCRES***. ***AGCFRZE*** holds the current AGC value. With ***AGCADJ1*** and ***AGCADJ2***, both ADCs are gain controlled manually.

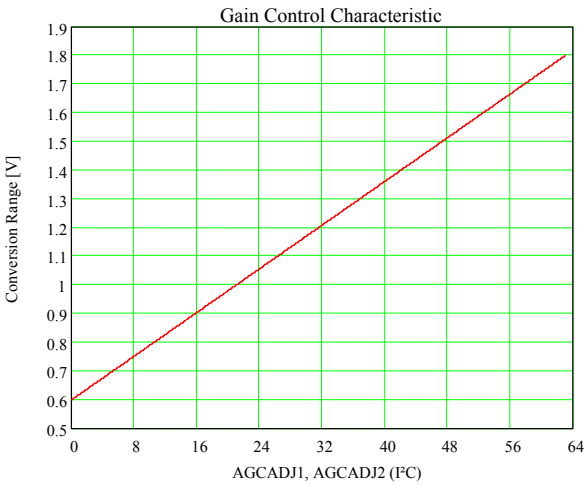


Fig. 2–4: CVBS, Y and C amplitude characteristics

Table 2–5: AGC modes

AGCMD	AGC Operation Mode
00	AGC uses the height of the sync pulse as a reference and additionally reduces amplification when ADC overflows
01	AGC uses the height of the sync pulse as a reference
10	AGC uses only ADC overflows
11	AGC is disabled and the ADC fits to the values given in ***AGCADJ***

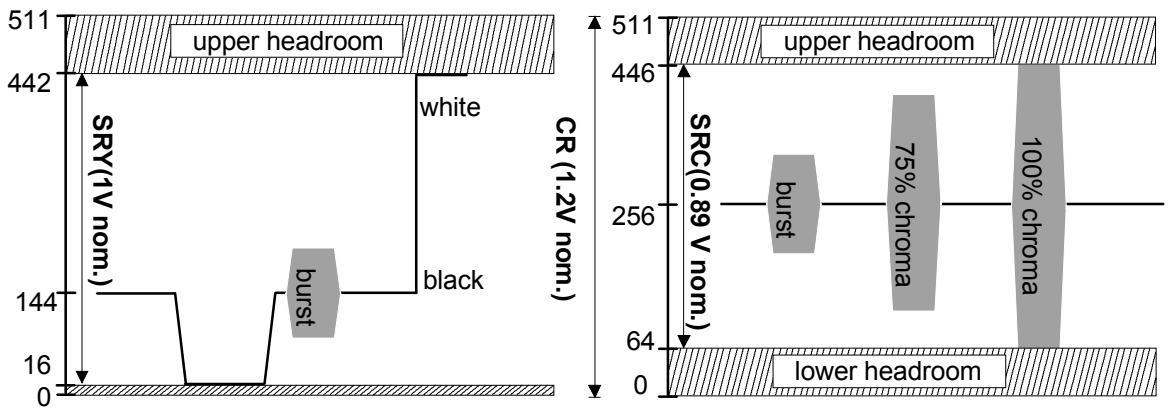


Fig. 2–5: CVBS ADC characteristic

2.3.2.2. Clamping

The clamp timing for the analog inputs is generated from its corresponding CVBS/sync signal. Clamping can be suppressed for some lines by ***CLMPLOW*** and ***CLMPHIGH*** to ignore copyprotection information. Both color-decoder generate two sets of clamping signals each (signals 1 and signals 2). Signals 1 are intended to be used for CVBS ADCs, signals 2 are intended to be used for RGBF ADCs. The start and length of each signal is adjustable. For adjustment, please refer to application note.

2.3.2.3. Double Frontend Adjustments

CVBS and RGBF ADCs receive gain and clamping signals from the color decoder. For flexibility reasons, these can be selected according to the following figures:

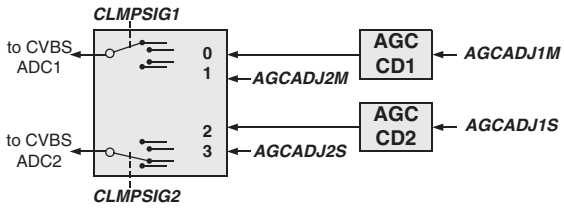


Fig. 2–6: Selection of cvbs gain control

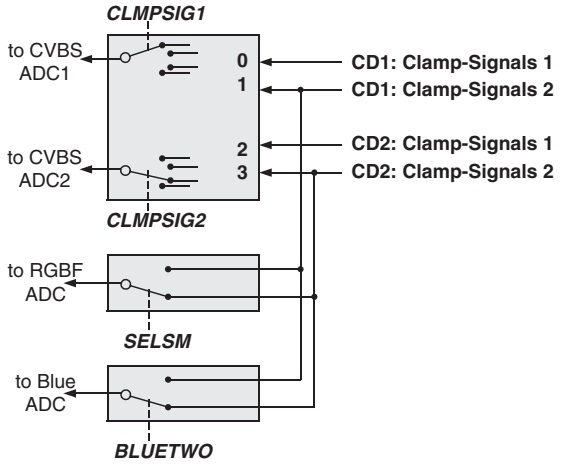


Fig. 2–7: Selection of clamp signals

For normal conditions, ***CLMPSIG1***=0 and ***CLMPSIG2***=2 allow to select "signals1" from master and slave color-decoder. To connect CVBS ADC1 with CD2 and CVBS ADC2 with CD1, use ***CLMPSIG1***=2 and ***CLMPSIG2***=0***.*** For "Chrominance on Blue", the clamping for this ADC must be selected separately (***BLUETWO***), dependent on whether Y is on CD1 or CD2.The separate clamp-signal for blue ADC is only used when this mode is selected by ***BLUESEL***.

2.3.3. CVBS Frontend

The CVBS frontend consists of the color-decoding circuit itself, a sync processing circuit for separating H/V sync out of the CVBS signal, and the luminance processing. Separated H/V syncs are given to pins H50 and V50. In contrast to previous versions of VSP 94xxB, H50 pin can be used to synchronize other ICs (e.g. text controller), if ***H50SKEW*** is set to 1. The main task of the luminance processing is to remove the color carrier by means of a notch filter (no comb mode). For PAL and SECAM operation a baseband delay line is used for U and V signals. This can be used as comb filter in NTSC operation (only for chrominance). The RGB input can either be used as an overlay for the CVBS channel (RGB+FBL) or as a full master channel (RGB+H/V, $RG_{sync}B$). The overlay is done by means of a soft-mix and can be used e.g. for "SCART" connector. This block contains a matrix (for RGB signals) which is switched off for YUV (e.g. $Y_{sync}PbPr$) input signals. A CBS (contrast, brightness, saturation) control makes the input signal adjustable.

2.3.4. Synchronization

After elimination of the high frequency components of the CVBS signal by a low pass filter, horizontal and vertical sync pulses are separated. Horizontal sync pulses are generated by a digital phase locked loop. The time constant can be adjusted between fast and slow behavior in four steps (***PLLTC***) to accommode different input sources (e.g. VCR). The time-constant can be changed during normal operation without visible picture degradation. Additionally weak input signals from a satellite dish ("fish") become more stable when ***SATNR*** is enabled. Vertical sync pulses are separated by integration of equalizing pulses. A vertical flywheel mode improves vertical sync separation for weak signals (***VFLYWHL, VFLYWHLMD***). Additionally, v-syncs may be gated by to reject invalid v-syncs, separately adjustable for 50 Hz ***(VTHRL50, VTHRH50)*** and 60 Hz ***(VTHRL60, VTHRH60)*** signals.

If no input signal is connected the device switches to a free-running mode. The device can be configured to switch-on background color when no or only a weak signal is applied (***NOSIGB***). 50 Hz or 60 Hz operation for sync separation may be forced separately (e.g NTSC only chassis) or selected to work automatically (***FLNSTRD***).

The center frequency of the frontend PLL can be adjusted in a range up to 52 kHz with ***FHFRRN***.

$$f = \frac{20250kHz}{384 + 4 \cdot FHFRRN}$$

2.3.5. Color Decoder

The digital multistandard chroma decoder is able to decode NTSC and PAL signals with a subcarrier frequency of 3.58 MHz and 4.43 MHz (PAL B[1)]/M/N/60[2)], NTSC M/44) as well as SECAM signals with automatic standard detection. Alternatively a standard can be forced. The demodulation is done with a regenerated color-carrier.

For use of non-standard crystals or factory adjustment, the frequency of the free-running regenerated subcarrier can be adjusted between ±270 ppm via ***SCADJ***. For this purpose the crystal deviation (***SCDEV***) can be read out via I²C after chroma PLL locking (indicated by ***SCOUTEN***) and can be stored in µC ROM for ***SCADJ***. For test purposes, ***CPLLOF*** allows a loop opening of the chroma PLL. The delay between Y and C is well aligned and can also be adjusted in steps of 50ns (***YCDEL***).

No picture shifting occurs when switching between different color standards (e.g. SECAM → PAL). A delay-line is implemented for PAL and SECAM signals. It acts as a simple chrominance comb-filter for NTSC and can be disabled by ***COMB.*** This improves the vertical chroma resolution, but cross-color remains.

2.3.6. IF-Compensation

With off-air or mistuned reception, any attenuation at higher frequencies or asymmetry around the color subcarrier is compensated. Five different settings (***IFCOMP***) of the IF-compensation are possible:

– Flat (no compensation)

– 6 dB/octave

– 12 dB/octave

– 4.4 MHz prefiltering (with or without prefiltering)

1 PAL B is representative for PAL B/G/H/I/N

2 PAL60 and NTSC44 are nonstandard signals which are generated by some VCR or DVD player

2.3.7. Chrominance Filter

The demodulation is followed by a lowpass filter for the color difference signals for PAL/NTSC. SECAM requires a modified lowpass function with bell filter characteristic. For SECAM mode, the de-emphasis filter can be adjusted by ***DEEMPFIR*** and ***DEEMPIIR***. The bell filter can be adjusted by ***BELLFIR*** and ***BELLIIR***. A wide band chroma filter can be selected. This filter is intended for high bandwidth chroma signals, e.g. S-VHS signal or when comb-filter is enabled. The chroma bandwidth can be adjusted by ***CHRF***. The value of ***CHRF*** has no linear dependency on effective bandwidth. The proper constellations are shown in Figure 2–8.

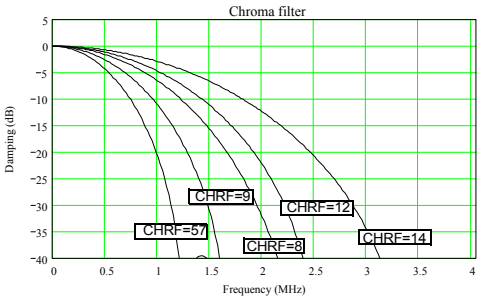


Fig. 2–8: Chroma filter characteristics

2.3.8. Automatic Standard Recognition

For adjustment to the specific operational area an automatic norm detection is selectable. Available 50 Hz color standards are PAL B, PAL N and SECAM. Available 60 Hz color standards are NTSC M, PAL M, PAL60 and NTSC44.

For each line standard, one or more color standards can be chosen for automatic standard detection. In addition, a standard can be forced as well. Within each line standard, the standard is detected by consequently switching from one to another. This standard detection process can be set to slow or fast behavior **(*LOCKSP*).** In slow behavior, 25 fields are used to detect the standard, whereas 15 fields are used in fast behavior. If unsuccessful within this time period the system tries to detect another standard. ***AMSTD50*** selects whether PAL B or SECAM is tried first in the automatic routine. ***AMSTD60*** selects whether NTSC44/PAL60 or NTSC M is tried first. Both bits can also be set for automatic detection, then the last detected chroma standard will be used.

For SECAM detection, a choice between different recognition levels is possible (***SCMIDL, SCMREL***) and the evaluated burst position is selectable (***BGPOS***).

Color standard (***STDET***), line standard (***LNSTDRD***) and color killer status (***CKSTAT***) can be read out.

Table 2–6: Allowed combinations for 60 Hz standards

Standard	CSTAND			
(60 Hz)	D6	D5	D4	D3
None	0	0	0	0
PAL60	0	0	0	1
PAL M	0	0	1	0
NTSC M	0	1	0	0
NTSC44	1	0	0	0
Automatic PAL M/NTSC M	0	1	1	0
Automatic NTSC M/NTSC44/PAL60	1	1	0	0(!)

Table 2–7: Allowed combinations for 50 Hz standards

Standard	CSTAND		
(50 Hz)	D2	D1	D0
None	0	0	0
PAL N	0	0	1
PAL B	0	1	0
SECAM	1	0	0
Automatic PAL B/SECAM	1	1	0

2.3.9. Color Saturation Control

In the PAL/NTSC system the burst is the reference for the color signal. An Automatic Chroma Control (ACC) produces a stable output for input chroma variations from (approximately) -30 dB to +6 dB compared to nominal burst value. The ACC reference value is programmable for NTSC and PAL independently (***NTSCREF***, ***PALREF***) to ensure correct color saturation.

With ***ACCFIX***, the ACC is disabled and a constant value (dependent on ***NTSCREF*** and ***PALREF***) is used instead. ***ACCFRZ*** holds the current ACC value. The maximum amplification of the ACC can be limited by ***ACCLIM.*** This results in a smooth attenuation of color intensity for weak color carrier (see Fig. 2–9).

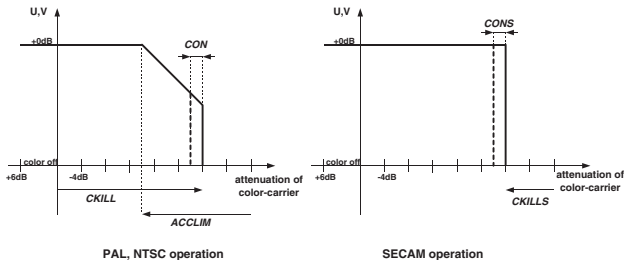


Fig. 2–9: Color killer adjustment

2.3.10. Color Killer

If the chrominance signal is below an adjustable threshold (***CKILL*** (PAL; NTSC) or ***CKILLS*** (SECAM)) the color is switched off. To prevent on/off switching, a hysteresis is given by ***CON*** or ***CONS*** which is the value of switching on the color. ***COLON*** switches on the color under any circumstance. The output of the color decoder can be set to UV or CrCb data by ***CRCB.*** For NTSC only, the color impression (tint) can be adjusted by the huecontrol between –88° and 90° in steps of 0.7° (***HUE***).

2.3.11. Luminance Processing

A luminance notch filter is implemented to reject the chroma information from luminance. Depending on the color standard, one of three different notch characteristics is chosen (PAL, NTSC, SECAM). For PAL and SECAM standards, five different characteristics are available. For NTSC standard, four different characteristics are available. They can be selected by ***NTCHSEL***. Alternatively, when ***NOTCHOFF*** is set to 1, notch is disabled or enabled when necessary automatically. ***TNOTCHOFF*** disables notch-filter under any circumstance.

A simple lowpass-filter can be enabled by ***LPPOST*** to further reduce high-frequency noise component from the CVBS signal.

For applications for which a black offset is not desired, controlling may be done using ***LMOFST***. The positive or negative offset is added to the Y signal before scaling.

The filter characteristics can be found in Fig. 2–10 to Fig. 2–11 and Fig. 2–13 to Fig. 2–14.

Table 2–8: Notch-filter

NOTCHOFF	TNOTCHOFF	Notch-filter
0	0	Always enabled
0	1	Always disabled
1	0	Dependent on mode
1	1	Always disabled

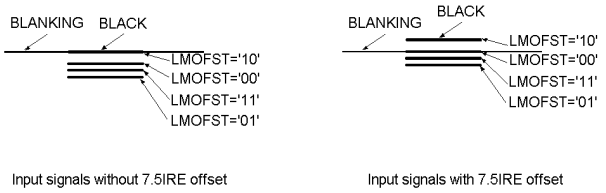


Fig. 2–12: Adjustment of Black- to Blankingvalue at analog output

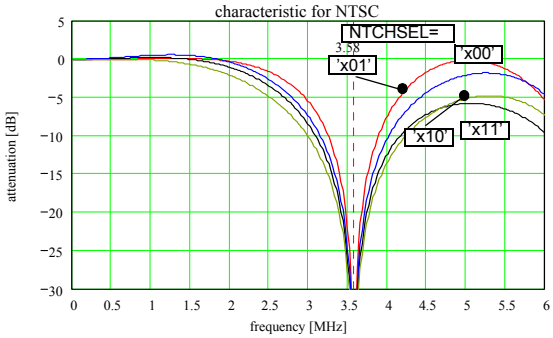


Fig. 2–10: Filter characteristics for NTSC, PAL M and PAL N

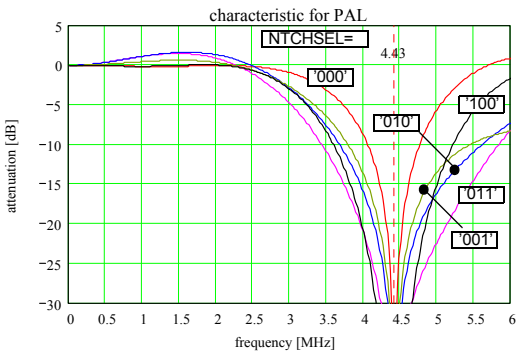


Fig. 2–11: Filter characteristics for PAL B/G, NTSC44 and PAL60

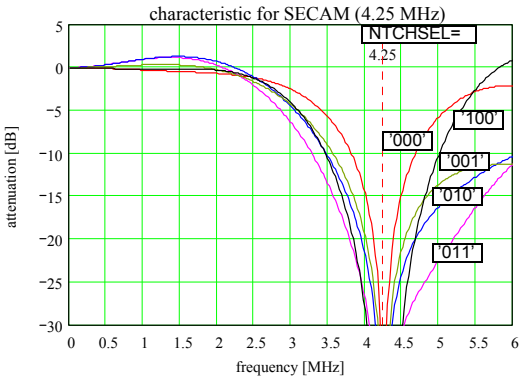


Fig. 2–13: Filter characteristics for SECAM (*SECNTCH*='01', 4.25 MHz)

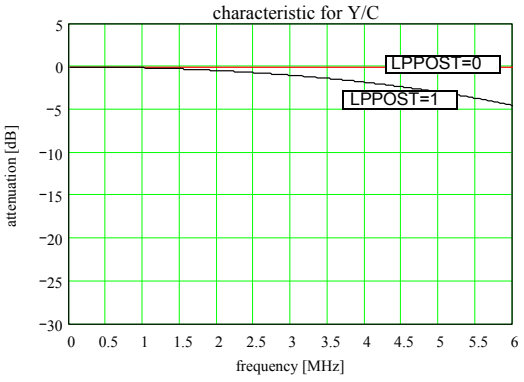


Fig. 2–14: Filter characteristics for Y/C mode

2.3.12. Adaptive Comb-filter

As only one comb-filter is included, the selection whether master or slave color decoder uses the comb-filter is done by ***SELCOMB***. The comb-filter input can be selected by ***INCOMB.*** First or second CVBS ADC or green ADC can be used. ***DISCOMB*** disables the comb-filter without changing the vertical or horizontal delay. The benefit is, that on/off switching of comb-filter can be done without picture jumping. When setting ***YCTCOMB***, a Y/C signal is fed through line delays without combing, allowing same vertical delay for Y/C signals also. The origin of C signal is given by ***INCOMBC*** (refer to Fig. 2–1 on page 12).

The comb-filter incorporates a detection circuit, whether standard TV sources or unstable non-standard sources (e.g. VCR) are applied. Although the adaption logic does not allow combing for unstable signals, it is recommended to disable comb-filter by ***DISCOMB*** when ***TVMODE*** indicates a non-standard signal.

The 4H adaptive comb-filter is used for high quality luminance/chrominance separation for PAL or NTSC composite video signals. The comb-filter improves the luminance resolution (bandwidth) and reduces interferences like cross-luminance and cross-color. The adaptive algorithm eliminates most of the mentioned errors without introducing new artifacts or noise.

The filter uses four line delays to process the information of three video lines. To have a fixed phase relationship of the color subcarrier in the three channels, the digital data is fractionally locked to the color subcarrier. This allows the processing of all color standards and sub-standards using a single crystal frequency.

The CVBS signal in the three channels is filtered at the subcarrier frequency by a set of bandpass/notch filters. The output of the three channels is used by the adaption logic to select the weighting that is used to reconstruct the luminance/chrominance signal from the 4 bandpass/notch filter signals. By using soft mixing of the 4 signals switching artifacts of the adaption algorithm are completely suppressed.

The comb-filter uses the middle line as reference, therefore, the comb-filter delay is two lines. If the comb-filter is switched off, the delay lines are used to pass the luma/chroma signals from the A/D converters to the luma/chroma outputs. Thus, the processing delay is always two lines.

In order to obtain the best-suited picture quality, the user has the possibility to influence the behavior of the adaption algorithm going from moderate combing to strong combing. Therefore, the following three parameters may be adjusted:

– ***HDG*** (horizontal difference gain)

– ***VDG*** (vertical difference gain)

– ***DDR*** (diagonal dot reducer)

HDG typically defines the comb strength on horizontal edges. It determines the amount of the remaining cross-luminance and the sharpness on edges respectively. As HDG increases, the comb strength, e. g. cross luminance reduction and sharpness, increases.

VDG typically determines the comb filter behavior on vertical edges. As ***VDG*** increases, the comb strength, e. g. the amount of hanging dots, decreases.

After selecting the comb-filter performance in horizontal and vertical direction, the diagonal picture performance may further be optimized by adjusting ***DDR***. As ***DDR*** increases, the dot crawl on diagonal colored edges is reduced.

2.3.13. Analog RGB/YUV Inputs

2.3.13.1. Source Select

Two RGB/YUV inputs are available. The choice between the first or second input is made by ***RGBSEL***. Additionally, RIN1 and RIN2 (or RIN1 and BIN1 or RIN2 and BIN2) can be used as two separate C inputs for Y/C operation.

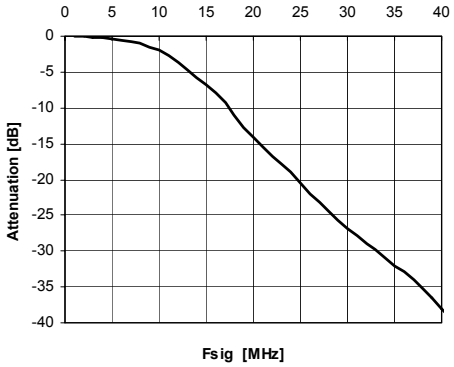


Fig. 2–15: Default characteristic of analog RGB/FBL antialiasfilter

Table 2–9: RGB input selection

RGBSEL	**0**	**1**	**0**	**1**
BLUESEL	**0**	**0**	**1**	**1**
R_ADC	RIN1	RIN2	RIN1	RIN1
G_ADC	GIN1	GIN2	GIN1	GIN2
B_ADC	BIN1	BIN2	RIN2	RIN2
F_ADC	FIN1	FIN2	FIN1	FIN2
	RGB/ YUV input 1 or C	RGB/ YUV input 2 or C	C1 and C2	C1 and C2

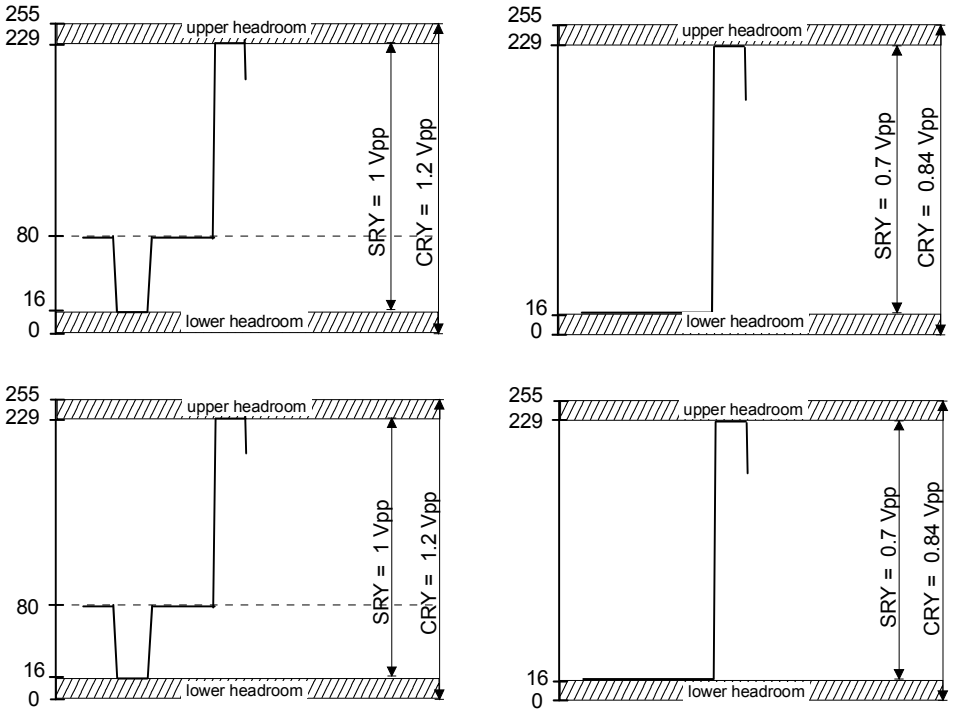


Fig. 2–16: Y/RGBF (w/ or w/o sync) and UV amplitude characteristics

2.3.13.2. Signal Magnitudes and Gain Control

Each ADC can be gain adjusted by ***AGCADJR***, ***AGCADJG***, ***AGCADJB***, ***AGCADJF***.

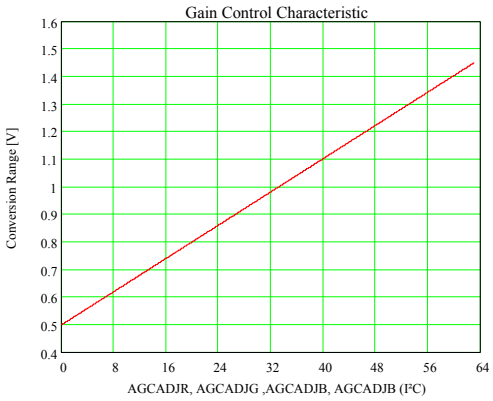


Fig. 2–17: RGBF ADC characteristic

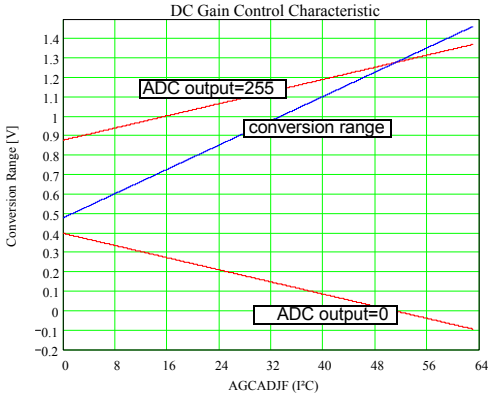


Fig. 2–18: Fast-blank ADC characteristic without clamping (*DCLMPF*=1)

2.3.13.3. Clamping

When using the dynamic softmix-mode with fast-blank, clamping of fast-blank input must be disabled by ***DCLMPF***. The analog clamping value of red and blue input (V and U resp.) can be adjusted by ***CLMPVRB***. The analog clamping value of green input (Y resp.) can be adjusted by ***CLMPVG***. Depending on the input signal format (YUV, RGB, sync signal or not) these bits must be set accordingly. On the digital side, a correction of the analog clamping value must be performed to reconstruct the blacklevel. This is achieved by ***RBOFST*** and ***GOFST***.

Table 2–10: Configurations of input signals

Mode	CLMPVG	CLMPVRB	GOFST	RBOFST	DCLMPF
YUV, sync on Y	80	128	64	128	Don’t care
YUV, sync on H,V, or CVBS	16	128	0	128	0
RGB, sync on G	80	16	64	0	Don’t care
RGB, sync on RGB	80	80	64	64	Don’t care
RGB, sync on H,V, or CVBS	16	16	0	0	0
RGB with fast-blank, synchron to CVBS	16	16	0	0	1

2.3.14. RGB-Frontend

An analog RGB input port for an external RGB or YUV source is available. The incoming signal is clamped to the back porch by a clamping pulse. As the memory is only able to store a 4:2:2 picture, the YUV input signal is downconverted to 4:2:2 format. There are two operation modes available. The first one uses this input as an overlay input (soft mix). The RGB or YUV signal must then be synchronized to the main CVBS signal.

The so called independent mode uses RGB / YUV including sync or H/V signals. This can be used, for example, for a DVD player or set-top-box. When using H sync from a non CVBS input (e.g. separate H-sync) this must be indicated by ***HINP***. The usage of separate V-sync must be set by ***VINP***.

With the readable information of number-of-lines (***LPFLD***), pixel-per-line (***NRPIXEL***), H and V polarity (***DETHPOL***, ***DETVPOL***), the applied PC-signals can be distinguished. The delay of luminance and fast-blank can be adjusted by ***YFDEL***, and chrominance can be delay adjusted by ***UVDEL***. If necessary, fast-blank can be adjusted fine by ***FBLDEL***.

Table 2–11: Possible input signals for RGB frontend

Input Signal	FBL_{IN}	V_{IN}	Sync Separation	*HINP*	*VINP*
RGB / YUV	CVBS[1)]		Sync on CVBS	0	0
RGB / YUV	H[a]	V	Sync on H	1	1
RGB	FBL		Synchron to CVBS	0	0
RGB			Sync on G	1	0
YUV			Sync on Y	1	0
[1)] Instead of FBL input, CVBS input can be used					

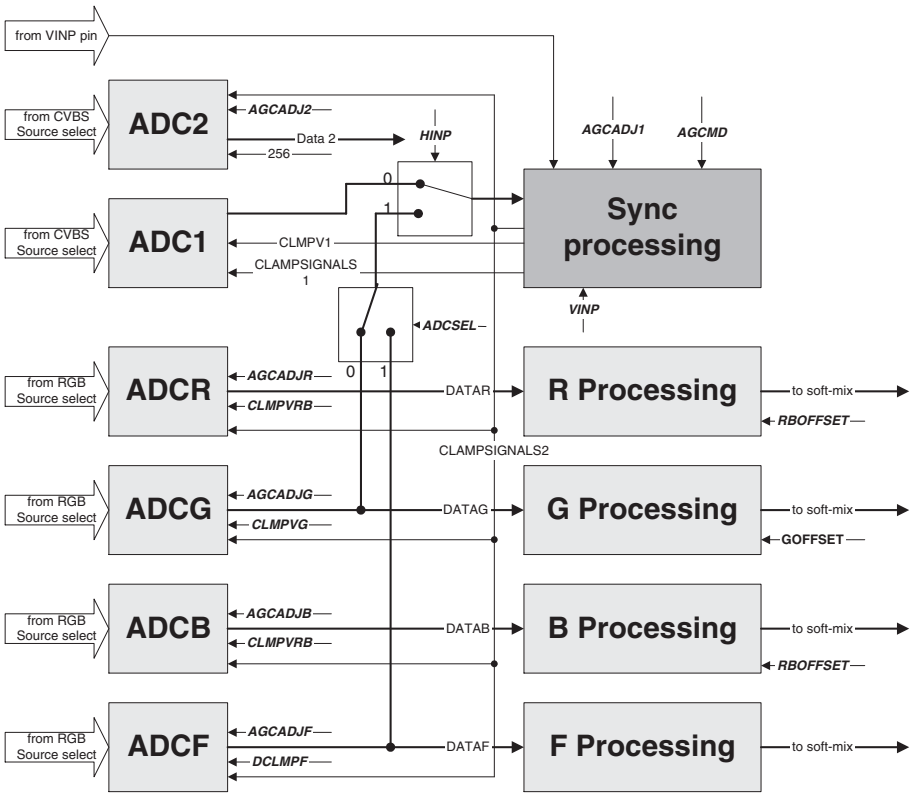


Fig. 2–19: Signal and clamping organization

2.3.15. Digital Prefiltering

A digital prefiltering can be enabled. This reduces the bandwidth of very steep input signals, such as a display of characters. A band limitation is required, because the succeeding de-skewing filter performs best below 14 MHz. The filtering is performed in all four channels and frequency characteristic can be selected by ***AASEL***. It can be disabled by ***AABYP***. For signal conversion to 4:2:2, an additional chrominance lowpass can be enabled by ***CHRSF***.

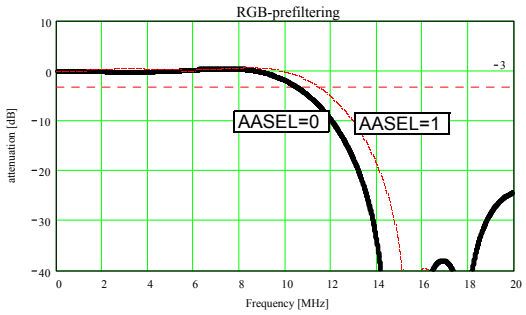


Fig. 2–20: Digital prefiltering of RGB input

2.3.16. RGB/YPbPr to YCrCb Matrix

RGB or YPbPr signals are converted to the YCrCb format by a matrix operation (***YUVMAT***). In case of YCrCb input the matrix is bypassed (***YUVSEL***).

$$\begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix} = \begin{bmatrix} R \\ G \\ B \end{bmatrix} \cdot \begin{bmatrix} 0{,}299 & 0{,}587 & 0{,}114 \\ -0{,}147 & -0{,}289 & 0{,}436 \\ 0{,}615 & -0{,}515 & -0{,}100 \end{bmatrix}$$

Fig. 2–21: RGB to YCrCb matrix (CCIR)

$$\begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix} = \begin{bmatrix} Pr \\ Y \\ Pb \end{bmatrix} \cdot \begin{bmatrix} 0{,}191 & 1 & 0{,}075 \\ -0{,}108 & 0 & 0{,}991 \\ 0{,}991 & 0 & -0{,}054 \end{bmatrix}$$

Fig. 2–22: YPbPr to YCrCb matrix (BTA)

$$\begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix} = \begin{bmatrix} Pr \\ Y \\ Pb \end{bmatrix} \cdot \begin{bmatrix} 0{,}196 & 1 & 0{,}102 \\ -0{,}111 & 0 & 0{,}991 \\ 0{,}988 & 0 & -0{,}073 \end{bmatrix}$$

Fig. 2–23: YPbPr to YCrCb matrix (CCIR)

2.3.17. Component YCrCb Control

The VSP 94xxB supports the following picture adjustment parameters on the component signal:

- 0 ≤ contrast ≤63/32 (***CONADJ)***
- –128 ≤ brightness ≤ 127 (***BRTADJ)***
- 0 ≤ saturation C_r ≤ 63/32 (***VSAT***)
- 0 ≤ saturation C_b ≤ 63/32 (***USAT***)
- -45° ≤ tint ≤ +45° (***TINT***)

2.3.18. Soft Mix

The softmixer circuit consists of a Fast Blank (FB) processing block supplying a mixing factor k (0... 128) to a high quality signal mixer achieving the output function:

$$YUVmix = \frac{YUV_{main} \cdot (128 - k) + YUV_{inserted} \cdot k}{128}$$

k="0" means that only the main signal is fed through to the output. k="128" means that only the inserted signal becomes visible. The mixing is done once for the luminance and once for the chrominance in the subsampled domain (4:2:2). The softmixer supports four modes that are selected by ***MIXOP*** and ***SMOP.***

Table 2–12: RGB operation modes

MIXOP	SMOP	Softmix-mode
00	0	Dynamic Soft-Mix (***DECTWO*** must be set to "1")
00	1	Static Soft-Mix (***DECTWO*** must be set to "1")
01	x	Only RGB/YUV path visible
10	x	Only CVBS path visible
11	x	(Reserved)

2.3.18.1. Static Switch Mode

In its simplest and most common application the softmixer is used as a static switch between YUVmain and YUVinsert. This is for instance, the adequate way to handle a DVD component signal. By using ***MIXOP***, k is internally set to 0 or 128 respectively.

2.3.18.2. Static Mixer Mode

The signal YUVmain and the component signal YUVinsert may also be statically mixed. In this environment, k is manually controlled via ***FBLOFFSET*** and ***MIXGAIN***.

$$k = MIXGAIN \cdot (31 - FBLOFFST) + 32$$

All necessary limitation and rounding operations are built-in to fit the range: $0 \le k \le 128$.

Considering ***MIXGAIN***=3, k is obtained by:

$$k = 158 - 3 \cdot FBLOFFST$$

k limited to 0 and 128

The mixing is only controlled by ***FBLOFFST***.

In the static mixer mode as well as in the previously mentioned static switch mode, the softmixer operates independently of the analog fast blank input.

2.3.18.3. Dynamic Mixer Mode

In the dynamic mixer mode, the mixer is controlled by the Fast Blank signal. The VSP 94xxB provides a linear mixing coefficient.

$$k = \frac{MIXGAIN(FB - FBLOFFST \cdot 2)}{2} + 64$$

The dynamic mode is used for mixing which is dependent on FB input. FB is the preprocessed digitized fastblank input in the range from 0...127. FBL manipulation is done both for luminance and chrominance FBL signal.

Fast blank is delay adjustable by ***FBLDEL*** in the range of –2...4 clock cycles.

2.3.19. Fast Blank Activity and Overflow Detection

It is important to know whether the FBL input is used or not. Therefore a detection circuit gives information via the I²C bus to the microcontroller. The circuit uses the digitized FBL as input. If it is greater than a threshold for one or five clock cycles (***FBLCONF***), the I²C bit ***FBLACTIVE*** is set. This bit is reset when it is read by the microcontroller.

For a detailed SCART signal ident analysis by the microcontroller, the fast blank monitor provides additional status information (see Fig. 2–24):

– ***FBSTAT***: FB status at register read

– ***FBRISE***: set by FB rising edge, reset by register read

– ***FBFALL***: set by FB falling edge, reset by register read

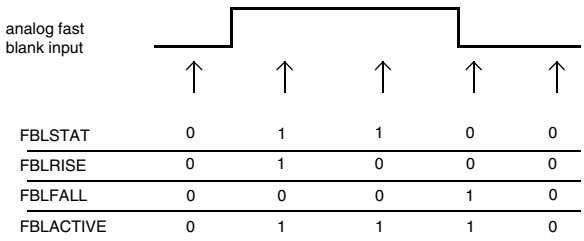


Fig. 2–24: Fast Blank Monitor

PFBL, ***PG***, ***PR***, ***PB*** indicate an overflow of the corresponding ADC (upper limit: ADC=511) exceeding 5 clock cycles duration.

2.3.20. Digital 656-Input/-Output

The IC decodes a digital 8bit@27 MHz data stream according to ITU.BT656 standard. Four modes are supported:

Table 2–13: 656 modes

IMODE	656 Operation
00	Full ITU mode (automatic). Information about active picture is taken from data-stream.
01	Full ITU mode (manual). Information about active picture is taken from ***APPLIPI***, ***NAPPLIPI***, ***ALPFIPI***, ***NALPFIPI.***
10	ITU656 only data, H/V-sync according PAL/NTSC.
11	ITU656 only data, H/V-sync according ITU656.

To adjust the input to sources, which deviate from the standard, the field information may be inverted (***FPOL***) and the chrominance format can be chosen between unsigned and 2's complement format (***CFORMAT***).

The polarity of H an V can be inverted by ***HPOL*** and ***VPOL*** respectively. The port selection (pin 656ioX or i656iX) is done by ***ITUPRTSEL***.

2.3.21. Data-Slicer

Two slicer working in parallel are implemented. One can be selected to slice either CC or WSS625, the other is only capable of WSS525.

Depending on ***SERVICE***, Closed Caption data ("Line 21") or WSS (Widescreen signalling) is sliced. Sliced data can be read out from I²C interface (***DATA_CCWSS*** and ***DATAUSWSS***). The line number of the sliced data is selectable with ***SLNCW*** (CC and WSS625) and ***SLNRUW*** (WSS525). Therefore WSS and CC can be processed in different regions (e.g. CC with PAL M). The Closed Caption data is assumed to conform with the ITU standards EIA-608 and EIA-744-A. WSS data is assumed to conform with ETS 300 294 (2nd edition, May 1996) for 625 lines or IEC61880 for 525 lines standards. ***SLSRC*** selects between slicing of master or slave data.

Table 2–14: Data slicer configuration

I²C Commands	Configuration each Data Service		
	CC (NTSC)	WSS625 (PAL, SECAM)	WSS525 (NTSC)
XDSCLS	As required	x	x
XDSTPE	As required	0	2
SERVICE	0	1	1
SLNCW	16 (=line 21)	21 (=line 23)	x
SLNRUW	x	x	15 (=line 20)
DATA_CCWSS	Data	Data	(Not valid)
DATA_USWSS	(Not valid)	(Not valid)	Data

2.3.22. Indication of New Data

The sliced and possibly filtered data is available in ***DATA_USWSS1/DATA_USWSS2/DATAUS_WSS3*** (closed-caption and WSS625) and ***DATA_CCWSS1/ DATACCWSS2*** (WSS525). The corresponding status bits are ***DATAVUSWSS/DATAVCCWSS*** and ***SLFIEL-DUSWSS/SLFIELDCCWSS***. When new data were received, ***DATAVxx*** becomes "1" and the controller must read ***DATA_xx1***, ***DATA_xx2 (DATA_xx3)*** and the status information. After the data bytes were read ***DATAVxx*** becomes "0" until new data arrives. It must be ensured that the data polling is activated once per field (16.7 or 20 ms) or every second field (33.3 or 40 ms), depending on the slicer configuration and line standard. The data in ***DATA_xx*** is not deleted after reading. If the slicer does not get new data, the old data is still readable in ***DATA_xx***, even if this is not valid any more. The field number of the data in ***DATAxxx*** can be found in ***SLFIELDxx***. If one or more XDS-class filter are activated for closed caption, ***SLFIELDxx*** contains always "1".

Additionally pin h50/irq may flag that new data is received. At default this pin outputs the 50 Hz separated h-sync. It can be configured by ***IRQCON*** to output a single short pulse when new data is available or behave equal to ***DATAV***. In the last case the output remains active until the two data registers ***DATA1/ DATA2*** are read. Both modes are useful to avoid continuos polling of the I²C bus. The micro-controller then initiates I²C transfers only when required.

```
while (1){
   i2c_read VSP94xxB_adr, status_reg_adr, status
   if (status & data_valid_mask) {
      i2c_read_inc VSP94xxB_adr, data_reg_adr,
                           data1, data2, status
      process_data data1, data2, status
   }
 }
```

Fig. 2–25: Example in pseudo-code for reading data

2.3.23. Closed Caption

The closed caption data stream contains different data services. In field 1 (line 21) the captions CC1 and CC2 and the text pages T1 and T2 are transmitted whereas in field 2 (line 284) caption CC3, CC4, text T3, T4 and the XDS data are transmitted. For more information please refer to the above mentioned standards.

Raw CC as well as prefiltered data is provided alternatively. With the built-in programmable XDS-Filter (***XDSCLS***), the program rating information (V-chip) as well as others can be filtered out. The XDS filter reduce traffic on the I²C bus and save calculation power of the main controller. If no class filter is selected, all incoming data (both fields) is sliced and provided by the I²C interface.

If one or more class filters are chosen, only data in field 2 is sliced. Any combination of class filters is allowed. Each "CLASS" is divided into "TYPES" which can be sorted out by the XDS-secondary filter (***XDSTPE***). Any combination of type filter is allowed. Some type filter require an appropriate class filter.

2.3.24. Violence Protection

The rating information is sent in the program rating packet of the current (sometimes future) class in the XDS data stream. If only this information is desired the corresponding XDS filter (class 01h, type 05h) should be used to suppress other data. The class/packet bytes (0105h) precede the 2 bytes rating information. Each sequence is closed by the end-of-packet byte (0fh) and a checksum. This checksum complements the byte truncated sum of all bytes to 00h. Except comparison of the received rating with the adjusted user rating threshold the micro-controller should check the parity of each byte and validate the checksum to avoid miss-interpretation of wrong received data.

The IC offers some alternatives to blocking the master or slave channel completely by switching it off (see Fig. 2–26 on page 26).

The Mosaic mode (***FRCMMOD***) hides details of the picture by reduced sharpness and increased aliasing. The picture looks scrambled and is less perceptible.

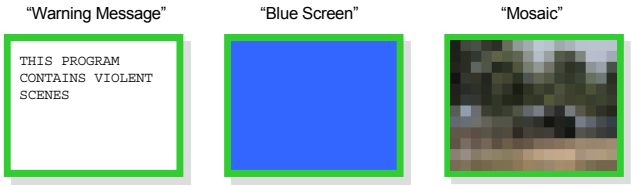


Fig. 2–26: Possibilities of master or slave channel blocking ("warning message" from external OSD controller)

2.3.25. Widescreen Signalling (625 lines WSS)

In WSS mode (***SERVICE***="1"), no content filtering is possible. All sliced data is passed to the output registers. In this case ***XDSTPE*** selects the field number of the data to be sliced (usually ***XDSTPE***=0 for first field). In Europe WSS (ETS 300 294) carries for instance information about aspect ratio and film-mode.

Table 2–15: WSS-625 bit coding (according to ETS 300 294)

IIC read		Group	WSS bit	Code	Meaning
DATA_CCWSS1 (low byte)	D0	Aspect ratio	b0	[b0 b1 b2 b3]	[0001] = Full format 4:3
					[1000] = Letterbox 14:9 centre
	D1		b1		[0100] = Letterbox 14:9 top
					[1101] = Letterbox 16:9 centre
	D2		b2		[0010] = Letterbox 16:9 top
					[1011] = Letterbox > 16:9 centre
	D3		b3		[0111] = Full format 4:3 (shoot and protect 14:9 centre)
					[1110] = Full format 16:9 (anamorphic)
	D4	Enhanced services	b4	0	Camera mode
				1	Film mode
	D5		b5	0	Standard PAL
				1	Motion adaptive coding
	D6		b6	0	No helper
				1	Modulated helper
	D7		b7		(Reserved)
DATA_CCWSS1 (high byte)	D0	Subtitles	b8	0	No subtitles (Teletext)
				1	Subtitles (Teletext)
	D1		b9	[b9 b10]	[00] = No open subtitles
					[01] = Subtitles on active image area
	D2		b10		[10] = Subtitles out of image area
					[11] = (Reserved)
	D3	Others	b11	0	No surround sound information
				1	Surround sound mode
	D4		b12		(Reserved)
	D5		b13		(Reserved)
	D6	(Not defined)			
	D7				

2.3.26. Widescreen Signalling (525 lines WSS)

Processed data can be read out by ***DATAVUSWSS***

Table 2–16: WSS-525 bit coding (according to IEC61880)

IIC read		Group	WSS bit	Code	Meaning
DATA_USWSS1	D0	Word 0 Aspect Ratio	1	[b1 b2]	[00] = 4:3 normal display format
					[01] = 16:3 normal display format
	D1		2		[10] = 16:9 letter box
					[11] = (Reserved)
	D2	Word 1 Copy Control	3	[b3 b4 b5 b6]	[0000] copy control information in Word 2
	D3		4		
	D4		5		[1111] no copy control
	D5		6		
	D6	Word 2 Copy Control	7	[b7 b8]	[00] = Copying is permitted without restriction
					[01] = No used
	D7		8		[10] = One generation of copies may be made
					[11] = No copying is permitted
DATA_CCWSS2	D0		9	[b9 b10]	[00] = PSP off
					[01] = PSP on, split burst off
	D1		10		[10] = PSP on, 2-line split burst on
					[11] = PSP on, 4-line split burst on
	D2		11	0	Not analogue pre-recorded packaged medium
				1	Analogue pre-recorded packaged medium
	D3		12		(Reserved)
	D4		13		
	D5		14		
	D6	CRCCC	15	[b15 b16 b17 b18 b19 b20]	CRCC error check
	D7		16		
DATA_CCWSS3	D0		17		
	D1		18		
	D2		19		
	D3		20		
	D4	Not defined			
	D5				
	D6				
	D7				

2.3.27. Channel Mux

Any input signal can be connected to master channel and slave channel independently. ***SELMASTER*** and ***SELSLAVE*** select whether CD1 (colordecoder 1), CD2, 656 decoder of soft-mixed signal is connected to master and slave. If the softmix output is used, ***SELSM*** selects between CD1 and CD2 for combination with the RGB input. Which color decoder is used as master can be found in the Table 2–17.

The linelocked display PLL (LL-PLL) is connected to the color decoder input or color decoder output (parallel or serial operation) or to ITU656 input, see Table 2–17 and Table 2–47 on page 67). Automatic switching to freerun (***AUTOFRRN***) and automatic switching to colored background (***NOSIGB***) must be disabled for the channel, which uses ITU656 input.

Table 2–17: Master input and reference for LL_PLL and automatic freerun

ARTSYNC	ITUSYNC	SELMASTER	SELSM	Signal on Master	Reference for *AUTOFRRN* and *NOSIGBM* (LL_PLL operation)
0 / 1	0	00	x	CD1	CD1 (parallel / serial)
0 / 1	0	01	x	CD2	CD2 (parallel / serial)
0 / 1	0	10	0	Softmix RGB/CD1	CD1 (parallel / serial)
			1	Softmix RGB/CD2	CD2 (parallel / serial)
1	1	11	x	ITU656	set ***AUTOFRRN***=***NOSIGBM***=0 (ITU656)

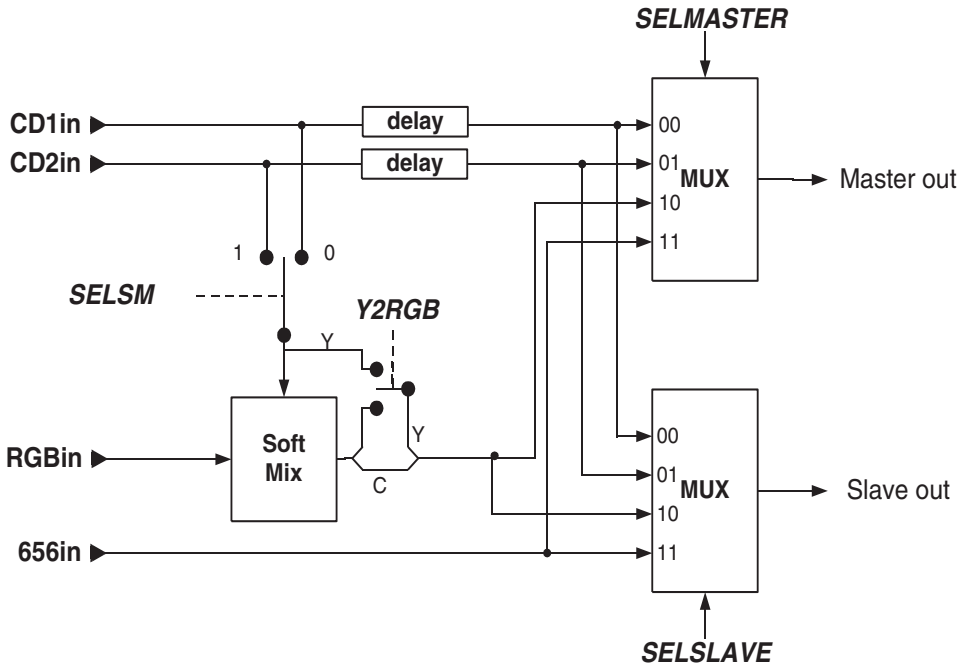


Fig. 2–27: Channelmux

2.4. Input Processing

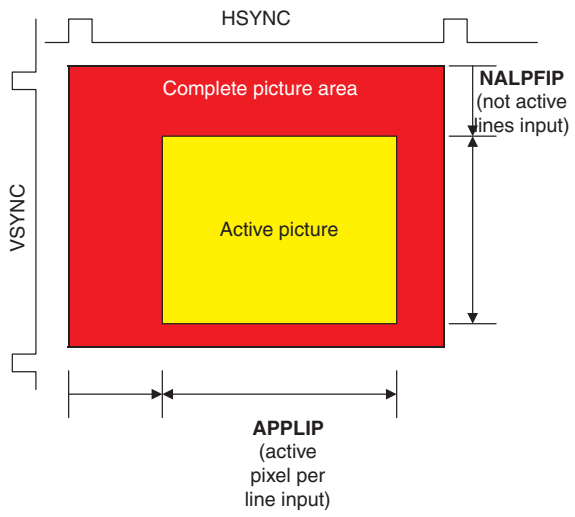


Fig. 2–28: Image format before memory

2.4.1. Mosaic Mode Generator

The mosaicmode generator scrambles the displayed picture. The main application is the conversion of the fine input resolution to a very crude output resolution. This may be used in combination with violence protection systems (V-chip) or conditional access systems (pay-per-view). The segmentation of the picture suppresses fine details and thus makes the recognition of the picture content very vague.

The input picture is divided into very few segments compared to the large amount of input pixels. The mosaicmode generator is enabled by ***FRCMMOD***.

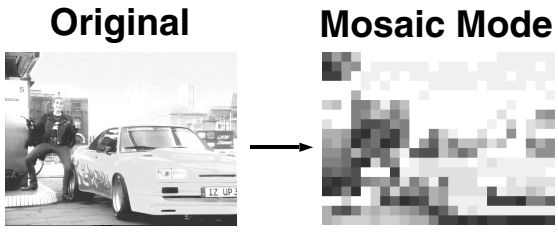


Fig. 2–29: Example of scrambled picture

2.4.2. Horizontal Prescaler

The main application is the conversion of the data coming from the 40.5/20.25 MHz pixel clock domain down to the number of pixels stored in the memory (factor 2/3). Generally the number of incoming pixels can be decimated by a factor between 1 and 64 in a granularity of 2 output pixels. The horizontal scaler reduces the number of incoming pixels by subsampling. To prevent the introduction of alias distortion low pass filters are used for luminance and chrominance processing controlled by ***HAAPRESC*** (bypass, weak, strong and automatic). Fig. 2–30 shows the luminance characteristic. In case of automatic the filter characteristic is calculated in relation to ***HSCPRESC*** and ***HDCPRESC***.

The horizontal prescaler is controlled by ***HSCPRESC*** (fine steps from 1 to 2) and ***HDCPRESC*** (integer decimation factors 1, 2, 3, ...). For full-screen display of digital 656 input, the scaler must be bypassed (***HSCPRESC***=0 and ***HDCPRESC***=0).

The start of the horizontal prescaler is defined by the ***NAPPLIP*** (Not Active Pixel Per Line Input) register, the amount of pixels is defined by the ***APPLIP*** (Active Pixel Per Line Input) register.

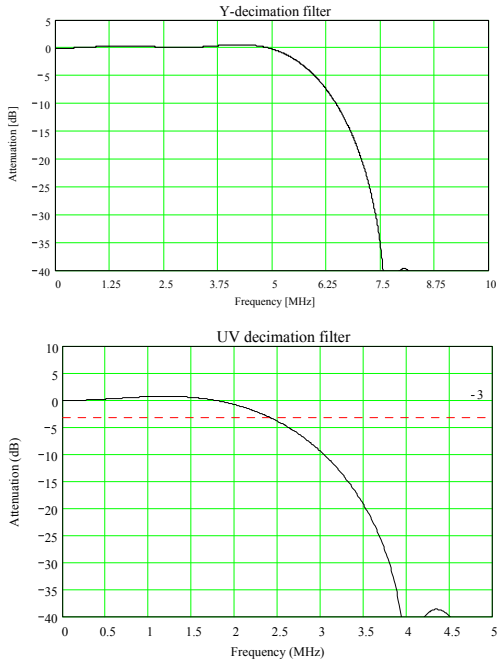


Fig. 2–30: Y and C decimation filter characteristic for standard operation (1.5)

2.4.3. Vertical Prescaler

The vertical prescaler is controlled by ***VSCPRESC*** (fine steps from 1 to 2) and ***VDCPRESC*** (integer decimation factors 1, 2, 3, ...). The number of output lines after the scaling process can be controlled with the use of the ***ALPFIP*** (active lines per field input) signal.

The vertical scaler allows to shift the picture content in vertical direction. The I²C register ***NALPFIP*** (not active lines per field input) controls the shift in vertical direction. The delay elements needed for integer decimation are shared with the motion detector. In case of active motion detection (***MOTON***=1), only weak filtering or line-dropping for master channel is possible. An optional prefiltering can be disabled by ***VAAPRESC***. (***VAAPRESC*** enables or disables an anti alias filter by adding a zero in the Y channel). ***VPKPRESC*** allows to adjust the amount of vertical peaking. The chrominance may be shifted one line upwards by ***VCRPRESC***. This may give a better picture for VCR sources. Prescaler can be bypassed by ***VPREBYP*** to overcome limited capacity of line delays in slave channel (usable for stockticker mode).

2.4.4. Filmmode Detection

Image sequences occur at various picture rates. Source material exists in 24p, 25p, 30p, 50i and 60i Hz formats, whereas video is broadcasted at 50 and 60 Hz, respectively. If the content is shot and broadcasted at 50i Hz or 60i Hz, it is called “video mode”. If the video is shot at 24p, 25p or 30p Hz and broadcasted as 50i or 60i Hz, it is called “film mode”.

For video mode and film mode different scan rate conversion algorithms are required. Therefore the information about video mode or film mode is necessary to adapt the processing. The information is provided by the ***FILMMODE*** signal. Film mode means, that the signal source was progressive e.g. 25p Hz, which was translated into a e.g. 50i Hz interlaced signal (2-2 pull down). Therefore two consecutive fields called A and B have the same motion phase. Normally field “An” and field “Bn” belong to the same phase. But it is also possible, depending on the translation process, that field “Bn-1” and field “An” belong to the same motion phase (***FILMMODE***=1 or 2). The translation process is different for 50i or 60i Hz output signals. For 60i Hz the signal looks like: An Bn An Bn+1 An+1 Bn+2 An+2 Bn+2 An+3 Bn+3 etc. This is also called 3-2 pull down. So always three and two fields belong to the same motion phase (***FILMMODE***=3, 4, 5, 6 or 7). For video mode ***FILMMODE*** = 0. Fig. 2–31 and Figure 2–32 on page 32 show the film scanning process for the 2-2 (3-2) pulldown.

The detected ***FILMMODE*** information is a four bit signal. The 4th bit gives a security information about the detected filmmode (means whether the ***FILMMODE*** is generated synthetically or is really detected). If it is set to 1, the ***FILMMODE*** value is insecure. That means the film mode detector can not recognize a stable mode and the integrated mode generator is switched on. If it is set to 0, the ***FILMMODE*** value is secure. That means the film mode detector can find a defined mode. The 3 LSB of the ***FILMMODE*** value define the detected mode (see Table 2–18).

This ***FILMMODE*** value will be used in the frame rate conversion block to switch between different algorithms. Furthermore this value can be read by the I²C bus. ***FMSTATUS*** indicates new data for ***FILMMODE***. When one of the film mode read registers contains updated data which was not read so far, ***FMSTATUS*** is set. ***FMSTATUS*** is reset when read.

Table 2–18: Filmmode detection results

FILMMODE	Description
0000	Video mode
0001	Film mode PAL, Phase 0
0010	Film mode PAL, Phase 1
0011	Film mode NTSC, Phase 0
0100	Film mode NTSC, Phase 1
0101	Film mode NTSC, Phase 2
0110	Film mode NTSC, Phase 3
0111	Film mode NTSC, Phase 4
1xxx	Insecure, (3 LSB still show the current detected mode)

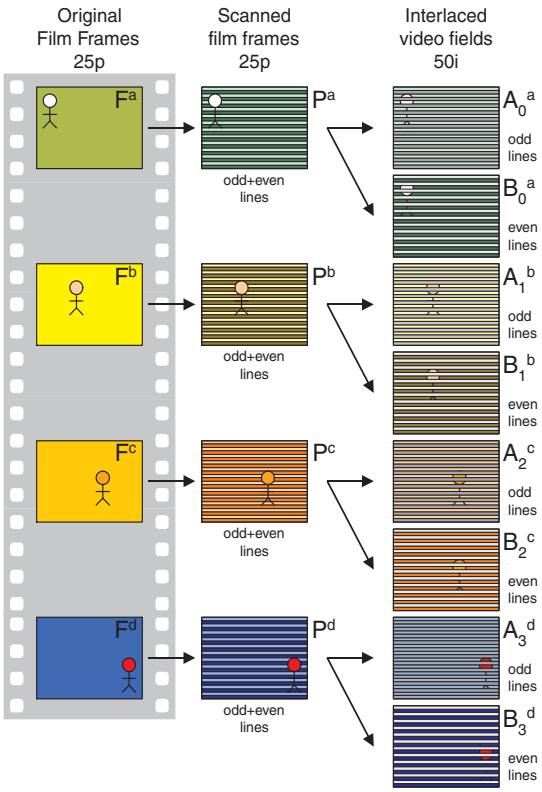


Fig. 2–31: Scan process from 25p to 50i (2-2 pulldown)

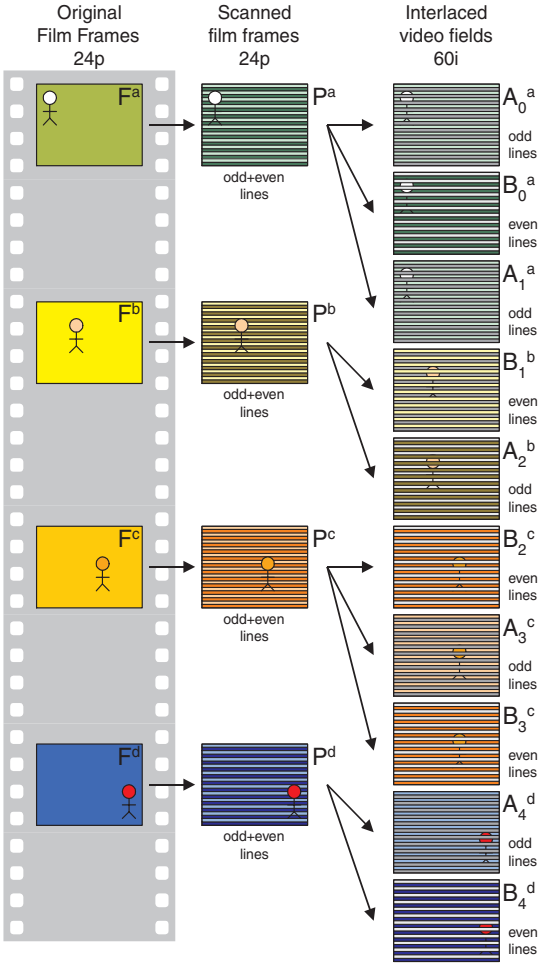


Fig. 2–32: Scan process from 24p to 60i (3-2 pulldown)

2.4.5. Motion Detection for Scan-Rate Conversion

The motion detection calculates a motion value for each pixel. The motion values are stored in the main memory block and used for the scan rate conversion. The motion detection works by comparing different fields of the input signal.

2.4.6. Global Motion and Global Still Detection

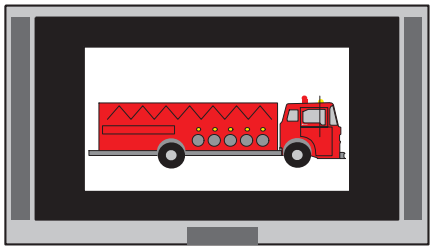
The result of the global motion detection block are I²C readable signals ***GMOTION*** and ***GSTILL***.

GMOTION (***GSTILL***) equal zero means, the complete picture is not moving (not still), ***GMOTION*** (***GSTILL***) equal one means, there is motion in the picture or the complete picture is moving (there is a still picture). These values are used internally to switch between different scan rate conversion algorithms. They may additionally be used, to control parameters adaptively per software, e.g. noisereduction.

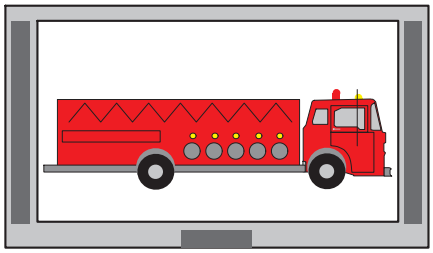
When one of the global motion and still read registers contains updated data which was not read so far, ***GMDSTATUS*** is set. ***GMDSTATUS*** is reset when read.

2.4.7. Letterbox Detection

A drawback of wide screen 16:9 TV sets are the black bars at the left and the right side on the screen, if displaying a 4:3 source on a 16:9 screen with correct aspect ratio. In case of letter box source material, black bars at the top and bottom also exist. With the help of an expansion algorithm it is possible to expand the letter box picture vertically and horizontally in such a way, that the letter box picture will fill the complete screen without loosing information. To do so, the information about the active part of the letter box picture is necessary. Active part means the information about the first active line and the last active line of the letter box picture. The figure below shows the principle of this idea.



4:3 Letterbox Picture



Expanded Letterbox Picture

Fig. 2–33: Handling of letterbox pictures on 16:9 tubes

The WSS (Wide Screen Signal) signal contains some information about the picture format (4:3 or 14:9 or 16:9), but not all existing formats are covered and not all signals contain WSS. Therefore, it is necessary a separate algorithm, which delivers the necessary information. The Fig. 2–34 on page 33 shows the concept of the letter box detection algorithm. One part of the algorithm is dedicated hardware and located in the VSP 94x5B, another part is software and located in the RAM of the TV microcontroller. The part located in VSP 94x5B is called measurement part. The measurement part delivers 5 signals to the controller part. Based on the delivered information the controller part calculates an expansion and a vertical pan factor and sends these values back to the VSP 94x5B for manipulation of the video signal.

The I²C bus parameter ***LBMASLA*** can be used to switch between the master and slave channel for the letter box analysis.

The letter box detection block works only at a data rate of 13.5 MHz. Due to the fact, that the input data rate at channelmux output can be 13.5 MHz, 20.25 MHz or 40.5 MHz, the input signal has to be downsampled. Depending on the I²C bus register ***LBSUB*** different modes are possible (Downsample 1, 1.5, 3).

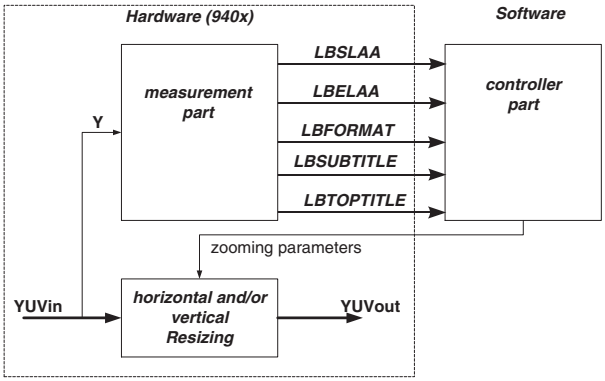


Fig. 2–34: HW/SW partitioning of letterbox detection

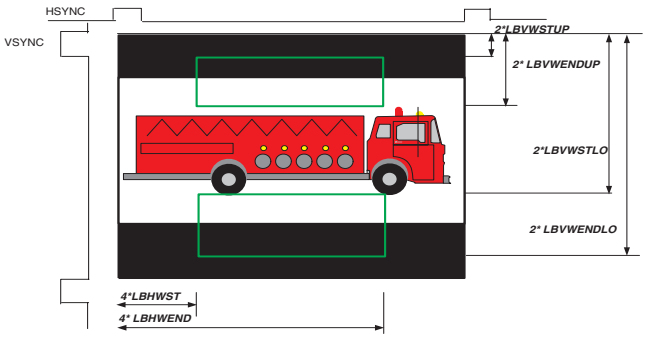


Fig. 2–35: Measurement windows

As digital 656input data is already in 13.5 MHz format, no downsampling should be used (***LBSUB***=0). For CVBS, YUV and RGB signals (if ***DEC2***=1) a downsampling of 1.5 (***LBSUB***=2) is required.

In principle the input picture is separated in one upper and one lower part. The measurement windows are defined by the parameters ***LBVWSTUP***, ***LBVWENDUP*** (upper vertical measurement window), ***LBVWSTLO***, ***LBVWENDLO*** (lower measurement window) and ***LBHWST***, ***LBHWEND*** (horizontal measurement window).

Note: A controller software and its description is available upon request.

2.4.7.1. Visualization of Letterbox Results

For optimizing of the parameters, it is advantageous to make the decision of the algorithm visible. The figure below shows different possibilities. The visibility can be switched on or off with the I²C bus parameter ***LBVISUON***.

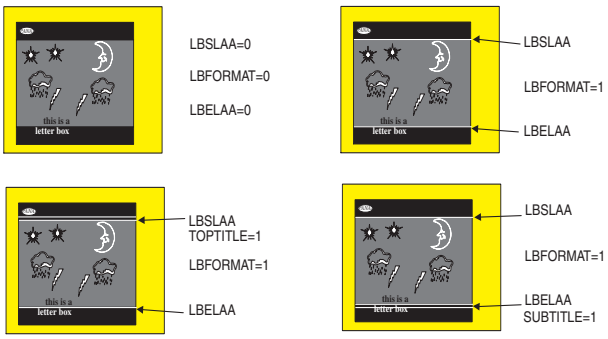


Fig. 2–36: Visibility of LBX detection parameters

2.4.8. Preframe Generator

The preframe generator's task is to fill the memory with a colored background before storing of decimated pictures into the memory. The parameter ***FRC_BGND*** enables the preframe generator. The color is given by the parameters ***YBORDER***, ***UBORDER*** and ***VBORDER***.

The preframe generator is able to add up to 30 active pixels with background color at the end of every picture line. The number of pixels to be added is calculated with the use of a "modulo 16 operation" applied to the number of input pixels ***APPL***. Additionally with the parameter ***MPFBPR*** (multi picture force background pixels right) up to 3 blocks of 16 colored pixels can be appended to the input picture (or 32 colored pixels if ***DISPMODEM*** is "0", "1", "6" or "7". 16 is always valid for slave channel).

The parameter ***MPFBPL*** (multi picture force background pixels left) with a resolution of 2 pixels allows to overwrite 0...62 pixels of the active picture content from the left of the picture.

In vertical direction up to 15 lines can be appended to the active area of the input picture colored with background color. This is controlled via ***MPFBLB*** (multi picture force background lines bottom). In vertical direction up to 15 lines of the active area of the input picture can be overwritten with background color. This is controlled via ***MPFBLT*** (multi picture force background lines top). Where "0" means that no lines are appended and "15" means that 15 lines are appended with background color. Fig. 2–37 on page 34 gives an overview of the possible adjustments.

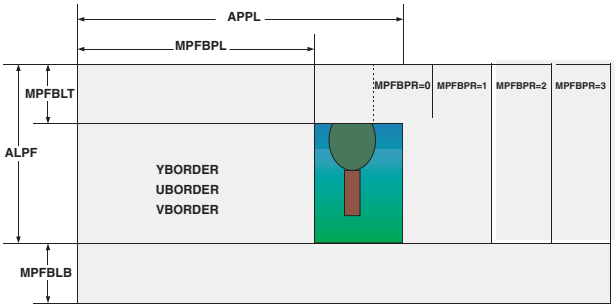


Fig. 2–37: Overview of background settings

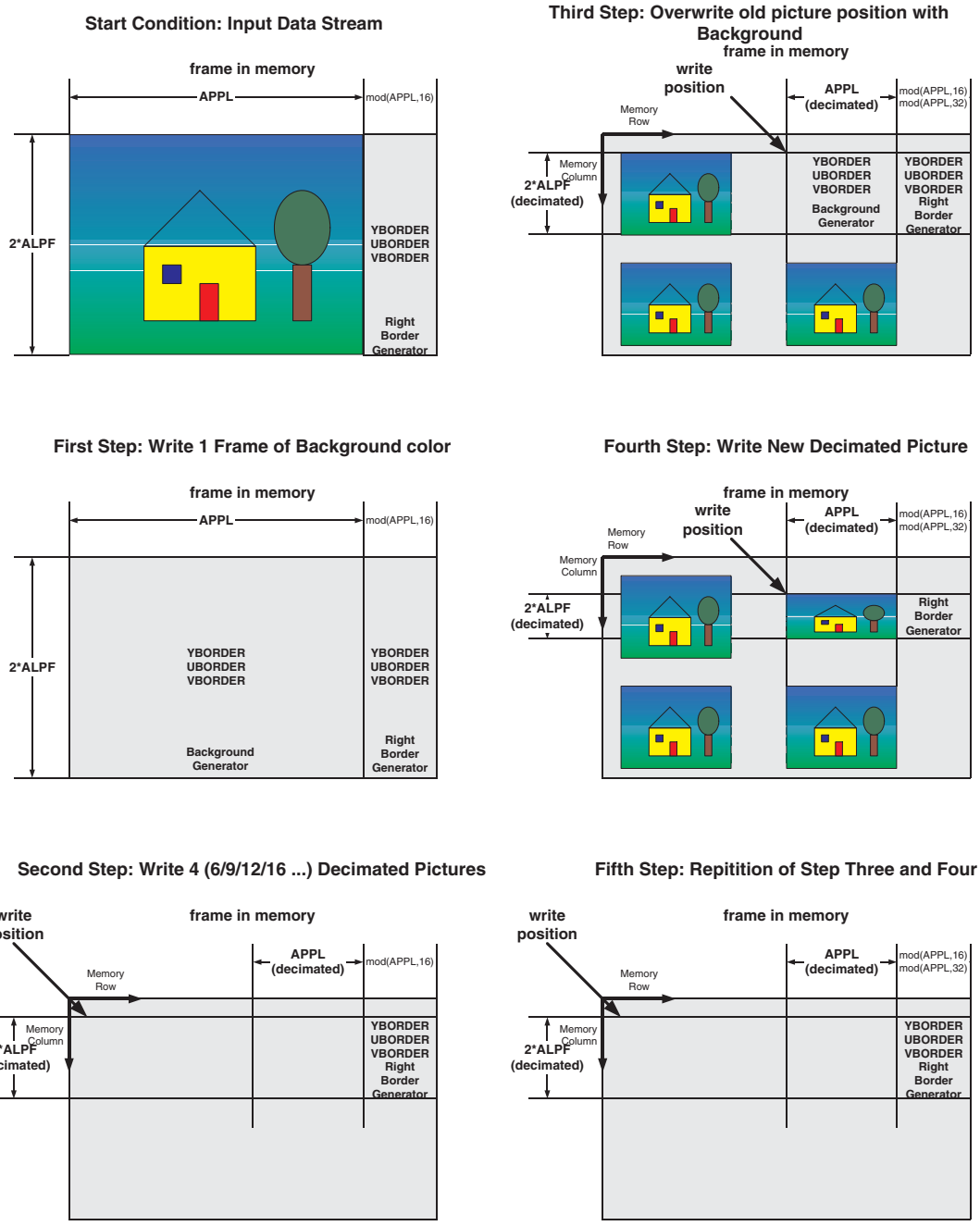


Fig. 2–38: Multipicture generation with colored background/frame

2.4.9. Noise Measurement

As noise reduction algorithms usually decrease the quality of pictures with little noise, it is highly desirable to apply a noise adaptive mechanism, which makes strong corrections in pictures with poor quality, and little corrections in pictures with good quality. To control this mechanism, it is necessary to measure the extent of noise.

The noise measurement algorithm can be used to change the parameters of the temporal noise reduction processing depending on the actual noise level of the input signal. This is done by the TV- microcontroller which reads the noise level (***NOISEME***) and sends different parameter sets to the temporal noise reduction registers of the VSP 94x2A depending on this value (0=no noise, 126=strong noise). Value 127 indicates an overflow status which means that the measurement failed.

The value is determined by averaging several fields. The line taken for noise measurement is selected by ***NMLINE***. If ***NOISEME*** contains updated data which was not read so far, ***NMSTATUS*** is set. ***NMSTATUS*** is reset when read.

The ***NMLINE*** parameter determines the line, which is used in the VSP 94x5B for the measurement. In case ***NMLINE***=0, line 2 of the field A and line 315 of the field B is chosen. In case of ***NMLINE=3***, line 5 of the field A and line 318 of the field B is chosen. The measurement position can be adjusted (***NMPOS***) as well as the sensitivity (***NMSENSE***).

2.4.10. Noise Reduction

The Fig. 2–39 shows a block diagram of the motion adaptive temporal noise reduction. The structure of the temporal motion adaptive noise reduction is the same for luminance as for chrominance signal. Noise reduction is enabled by ***NRON***.

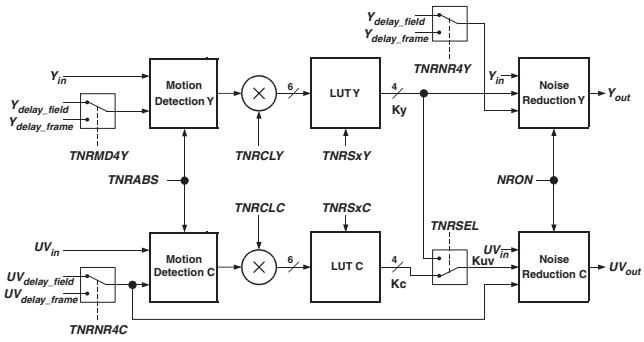


Fig. 2–39: Temporal noise reduction

Depending on the motion in the input signal, the K-factor Ky (Kuv) is adjustable between 0 (no motion) and 15 (motion) by the motion detector. The K-factor for the chrominance filter can be either Ky (output of the luminance motion detector, ***TNRSEL***=0) or Kuv (output of the chrominance motion detector, ***TNRSEL***=1). The delay of the feedback path is a field or frame delay (***TNRNR4YM***, ***TNRNR4CM***).

The motion detector for master channel of luminance and chrominance can be field or frame based (***TNRMD4YM***). The recursive filtering should be set to the **same** algorithm (***TNRNR4YM,*** field- or frame-based filtering). The chrominance motion detection uses always the delay of the noise reduction (***TNRNR4CM***). For slave channel, delay of motion detection and noise reduction can not be selected separately for luminance and chrominance. ***TNRNR4YS*** selects whether field or frame delay is used.

Table 2–19: Allowed combinations for Master NR

Y Noise Reduction	C Noise Reduction	Settings Y	C uses C Motion Detection	C uses Y Motion Detection
Field based	Field based	***TNRMD4YM***=1 ***TNRNR4YM***=1	***TNRNR4CM***=1 / ***TNRSELM***=1	***TNRNR4CM***=1 / ***TNRSELM***=0
Field based	Frame based		***TNRNR4CM***=0 / ***TNRSELM***=1	Not available
Frame based	Field based	***TNRMD4YM***=0 ***TNRNR4YM***=0	***TNRNR4CM***=1 / ***TNRSELM***=1	
Frame based	Frame based		***TNRNR4CM***=0 / ***TNRSELM***=1	***TNRNR4CM***=0 / ***TNRSELM***=0

Table 2–20: Allowed combinations for Slave NR

Y Noise Reduction	C Noise Reduction	Settings Y	C uses C Motion Detection	C uses Y Motion Detection
Field based	Field based	***TNRNR4YS***=1	***TNRSELS***=1	***TNRSELS***=0
Field based	Frame based	Not allowed		
Frame based	Field based			
Frame based	Frame based	***TNRNR4YS***=0	***TNRSELS***=1	***TNRSELS***=0

The output of the motion detector is weighted using the parameters ***TNRCLC*** and ***TNRCLY***. The look-up table input value range is separated into 8 segments.

It is possible to define a predefined curve characteristic for each segment. The curve characteristics can be programmed by the parameters ***TNRYSx*** for luminance and ***TNRCSx*** for chrominance. The curve-start is defined by ***TNRYSS*** (***TNRCSS***) at the end of the last segment. The overall curve is now constructed by connecting the end of segment 6 to the beginning of segment 7 and so on. Negative values of Ky (Kuv) are not possible and clipped to zero. A continuous mapping of 64 motion values to 16 Ky (Kuv) values is the result.

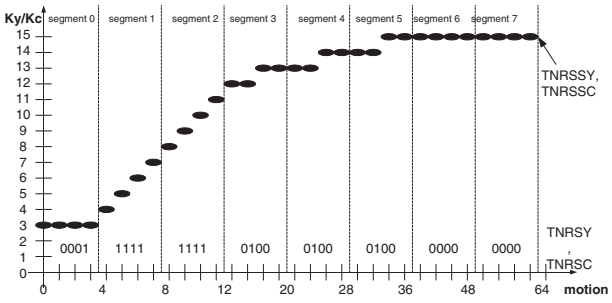


Fig. 2–40: Predefined curve characteristics for LUT

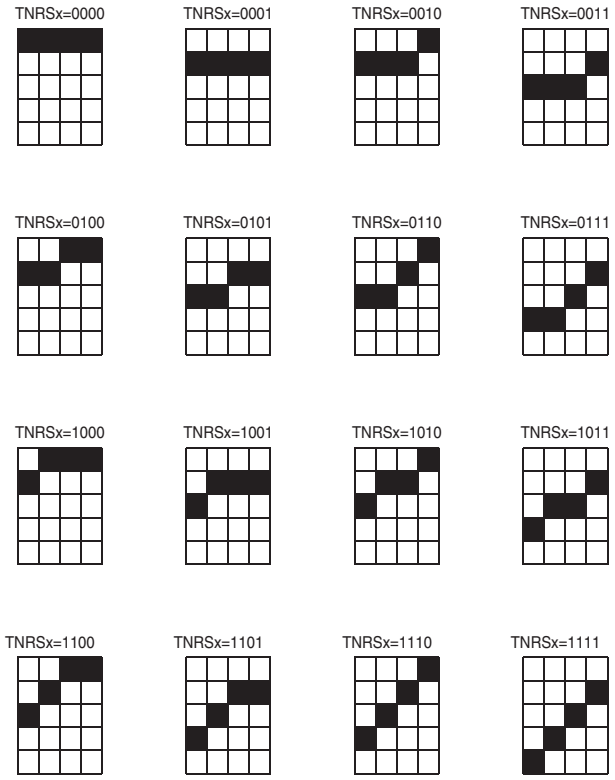


Fig. 2–41: Segments of LUT

2.5. Output Processing

2.5.1. Vertical Postscaler

The main task of the vertical postscaler is the expansion or decimation of the master channel in vertical direction. That means rational subsampling and upsampling factors.

The vertical post scaler is able to operate in progressive scan or interlace mode. The range of the vertical distortion is from 0.5 to 32 in relation to the original vertical picture size. The scaling of the picture is controlled via the value of ***VSCPOSC***.

When displaying a progressive picture in interlace format (e.g. 480p → 960i) it might be necessary to adjust ***VOFPOSC*** to prevent interlace flickering. In case of interlace output, ***VDOUBLE*** should be set to 0. ***VDOUBLE***=1 should be used in case of progressive output. Dependent on the operation mode, some restrictions are given for vertical postscaling (picture distortions will occur outside these ranges).

Table 2–21: Allowed vertical expansion factors

	VSCPOSC	Vertical Filter Expansion
Interlace output (***FMODE***=0)	256	32
	8192	1
	8900	0.92
Progressive output (***FMODE***=1)	256	32
	8192	1
	16383	0.5
Field-jam mode	8192	1

2.5.1.1. Vertical Panorama Mode

For the adjustment of the expansion process, the picture is divided into 5 segments. For each of these segments the increment value for the expansion factor can be defined separately. Each end of a segment can be defined individually. For every segment an increment value can be defined (***VINC0***...***VINC4***) which indicates the amount of decimation/expansion. One LSB is equivalent to an offset of 0.125 to ***VSCPRESC*** per lines. This means that with ***VINC***, ***VSCPRESC*** is altered in the range from -32...31.875 per line. The segments (equal or unequal sizes) are distributed among the number of lines available. The first four segments are defined by (***VSEG1***...***VSEG4***). The last one goes from ***VSEG4*** until the end of the picture.

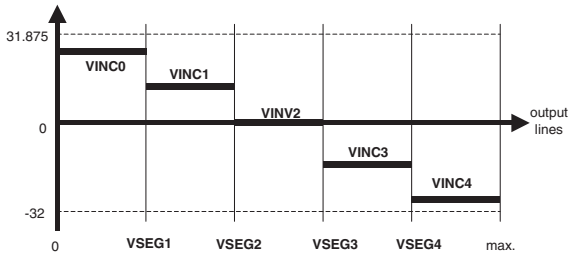


Fig. 2–42: Visualization of vertical panorama segments

Table 2–22: Examples of vertical panorama modes

Input→ Output	288 →576i/576p		240 i →480i/480p	
	Panorama	Lens	Panorama	Lens
VSCPOSC	5200	7050		
VSEG1	58	58	48	48
VSEG2	115	115	96	96
VSEG3	173	173	144	144
VSEG4	230	230	192	192
VINC0	-128	128	-128	128
VINC1	-64	64	-64	64
VINC2	0	0	0	0
VINC3	64	-64	64	-64
VINC4	128	-128	128	-128

2.5.2. Horizontal Postscaler

After the main memory, the display processing is performed using a different clock.The conversion to the display clock is done by an interpolation filter. This can be used for horizontal expansion in the range of 1...4 in steps of 2 pixels (***HSCPOSC***). Due to increased clock frequency in the backend part, the realized horizontal scaling factor depends on backend clock frequency.

$$HSCALE = \frac{4095}{HSPOSC} \cdot \frac{27MHz}{CLKB36}$$

Usually (36 MHz operation), the horizontal expansion factors result as 0.75...16. This ensures that the factor 0.75 gives no loss of resolution (to show a 4:3 picture on a 16:9 tube). When using DS656 output, neither horizontal compression nor horizontal panorama is possible due to 27 MHz clock.

Because of the nonlinear characteristic and integer number of pixel, sometimes different ***HSCPOSC*** values result in the same decimation factors.

Table 2–23: Horizontal expansion factors

HSCPOSC	Horizontal Filter Expansion	Overall Expansion	
		CLKB36= 27 MHz	CLKB36= 36 MHz
256 (minimum)	16	16	12
3072	1.33	1.33	1
4095 (maximum)	1	1	0.75

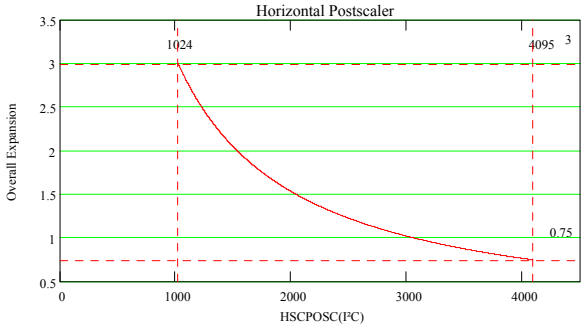


Fig. 2–43: Expansion factor of horizontal postscaler dependent on *HSCPOSC*

2.5.2.1. Horizontal Panorama Mode

For an improved impression in the case of expansions of 4:3 pictures to a 16:9 ratio tube, the picture can be geometrically distorted in horizontal direction. It is enabled by ***HPANON***. The idea behind this panorama mode is to keep the middle part of the picture in a 4:3 ratio and to stretch the left and the right to fill the entire width of the 16:9 screen.

The picture is divided into 5 segments of selectable size, in order to adjust the expansion process. The increment value for the expansion factor can be defined separately for each of these segments.

Each end of a segment can be defined individually in a granularity of two output pixels. For every segment an increment value can be defined (***HINC0***...***HINC4***) which indicates the amount of decimation/expansion. One LSB is equivalent to an offset of 0.125 to ***HSCPRESC*** per double pixel. This means that with ***HINC***, ***HSCPRESC*** is altered in the range from -32...31.875 per double pixel. The first four segments are defined by (***HSEG1***...***HSEG4***). The last one goes from ***HSEG4*** to ***HORWIDTH***. Examples are given in Table 2–24 on page 40.

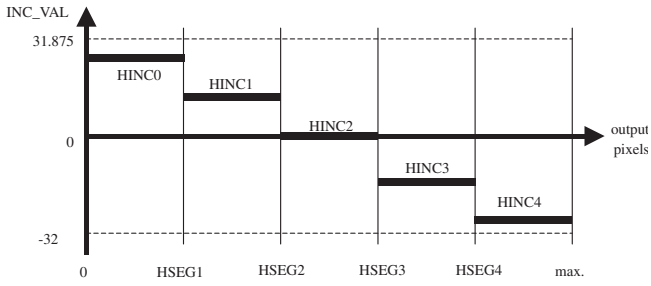


Fig. 2–44: Visualization of horizontal panorama segments

Table 2–24: Examples of horizontal panorama modes

Function	Panorama	Extreme Panorama	Lens
HSCPOSC	2099	1023	3999
HSEG1	96	96	96
HSEG2	192	192	192
HSEG3	288	288	288
HSEG4	384	384	384
HINC0	40	85	472
HINC1	20	43	492
HINC2	0	0	0
HINC3	492	469	20
HINC4	472	427	40
HORWIDTH	960	960	960

2.5.3. Application Modes

A still field can be displayed using ***FREEZE*** command. Dependent on the desired picture arrangement, an appropriate display (or application) mode has to be chosen. One of 9 display modes can be chosen by ***DISPMODE***:

1. **FSM mode (Full-Screen-Mode)**: In Full-screen-mode, two independent asynchronous input channels (master and slave channel) are processed. The master channel is displayed with a frame-based upconversion algorithm. The slave channel shows a high resolution PiP.

Fig. 2–45: FSM mode

By means of ***PIXPLINS***, the slave picture size can be modified to enable stock-ticker mode. In this case, a stock-ticker from one channel is displayed in another channel

Fig. 2–46: Stock-ticker application in FSM mode

2. **SSC1 mode (Split-Screen)**: In split-screen mode, two pictures can be shown side by side. Alternatively, a multi-PiP display with two live sources is possible. Both channels are displayed with field based upconversion algorithms.
3. **SSC2 mode (Split-Screen)**: Same functionality like SSC1 mode. In this case only the memory configuration is different. This enables Joint Line Free Display of 50i and 60i input sources at 50/60p output display frequency.

Fig. 2–47: SSC1 mode

4. **SPS mode (SnaP-Shot)**: In snap-shot-mode, a still field can be hidden in the memory. A switch between running picture and still field can be done. This may be used to store a picture (e.g. displayed phone number). This picture can then be shown at any time later. Before snapshot, a frame-based display is possible, after snapshot a field-based display is possible only. The slave channel shows a high resolution PiP.
5. **PCE mode (PC extern mode)**: In PC extern mode, a PiP is generated, which is synchronized to an external signal. E.g. when a PC or HDTV signal is directly connected to the backend IC, the PiP can be overlaid to this.

6. **PCF mode (PC Full Screen mode)**: In PC fullscreen mode, a PC signal is shown as master channel. No PiP is available. The display raster is locked to the PC signal or is freerunning to achieve a decoupling between input and display (e.g. to display a XGA signal on a VGA screen).
7. **PCP mode (PC + PIP mode)**: The PC PiP mode is equal to the PCF mode, but the displayed picture size for master is smaller in order to have memory capacity for the slave channel.

Fig. 2–48: PCE mode

8. **MUP1 mode (Multipicture mode 1)**: MUP1 is the recommended multi-picture mode for most applications. It is possible to show up to 2 live pictures. If interlace output, the master live picture should not be decimated in vertical direction to avoid joint-lines. The slave picture size is limited to 256 pixels x 106 lines and is jointline-free. The display is frame-based in master and slave with high resolution.
9. **MUP2 mode (Multipicture mode 2)**: Multi-picture display with up to two live and manifold still pictures. The display is field-based without restriction in picture size. Jointlines in live-pictures are not rejected. The display is only field-based.

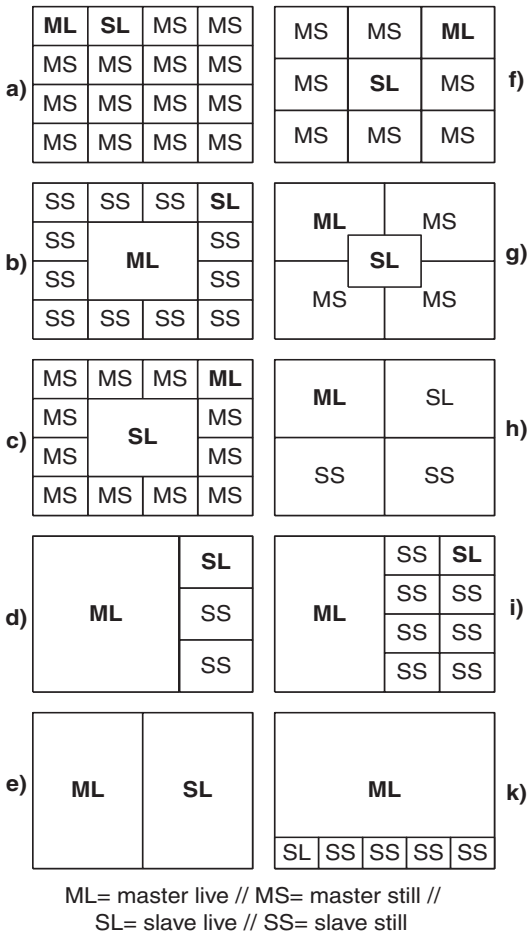


Fig. 2–49: Some multipicture examples

Similar arrangements for 16:9 tubes are possible.

Table 2–25: Preferred modes for multi-picture examples

Picture	Preferred Mode	Remark
a	MUP1	
b	SSC1	This configuration can be achieved by horizontal expansion of slave picture over whole screen by postscaler. A slightly reduced horizontal resolution in slave channel occurs.
c	MUP2	Master jointlinefree for progressive output. Jointline visible in master channel, when interlace output
d	SSC1	
e	SSC1	
f	MUP1	
g	MUP1	
h	MUP1	
i	SSC1	
k	FSM	Stock-ticker-application with still pictures. ***INTPROGS*** must be set to "1"

Table 2–26: Display modes: Picture sizes

Display Mode	Master Channel			Slave Channel		
	Stored Fields YC	Supplied Fields YC	Max. Picture Size [Pixels x Lines]	Stored Fields YC	Supplied Fields YC	Max.Picture Size [Pixels x Lines]
FSM (0)	2	2	704 x 288 (***PIXPLINM***=0) 832 x 240 (***PIXPLINM***=1)	3	2	256 x 106 (***PIXPLINS***=0) 432 x 60 (***PIXPLINS***=1) 768 x 34 (***PIXPLINS***=2)
SPS (1)	1 live / 1 shot	1	768 x 288	3	2	256 x 106 (***PIXPLINS***=0) 432 x 60 (***PIXPLINS***=1)
SSC1 (2)	2	1	448 x 292	2	1	432 X 292
MUP1 (3)	2	2	768 x 288	3	2	256 x 106 (***PIXPLINS***=0) 432 x 60 (***PIXPLINS***=1)
MUP2 (4)	1	1	768 x 288	1	1	768 x 288 (***PIXPLINS***=0) 432 x 60 (***PIXPLINS***=1)
PCE (5)	Not available			3	2	256 x 106 (***PIXPLINS***=0) 432 x 60 (***PIXPLINS***=1)
PCF (6)	2	2	768 x 340 (***PIXPLINM***=2) 864 x 292 (***PIXPLINM***=0)	Not available		
PCP (7)	2	2	768 x 288	3	2	256 x 106 (***PIXPLINS***=0) 432 x 60 (***PIXPLINS***=1)
SSC2 (8)	1	1	448 x 292	3	2	432 x 292

Table 2–27: Capabilities of display modes

Mode	Input Master[1)]	Input Slave	Output Display[2)3)4)]	MC Jointline Free	SC Jointline Free	Comment
FSM/SPS/ MUP1	50i	50i	100i, 50p, (50i)	✓	✓	
		60i		✓	✓	
		PC signal		✓		
	60i	50i	120i, 60p, (60i)	✓	✓	
		60i		✓	✓	
		PC signal		✓		
SSC1	50i	50i	100i, 50p, (50i)	✓	✓	
		60i		✓		Strong flickering in slave
		PC signal		✓		
	60i	50i	120i, 60p, (60i)	✓		
		60i		✓	✓	Strong flickering in slave
		PC signal		✓		Master channel is joinlinefree only, if NOT decimated or expanded vertically.
SSC2	50i	50i	50p, (50i)	✓	✓	
		60i		✓	✓	
		PC signal		✓		
		50i	100i	✓	✓	
		60i		✓	✓	
		PC signal		✓		
	60i	50i	60p, (60i)	✓	✓	
		60i		✓	✓	
		PC signal		✓		
		50i	120i	✓	✓	
		60i		✓	✓	
		PC signal		✓		

Table 2–27: Capabilities of display modes, continued

Mode	Input Master[1)]	Input Slave	Output Display[2)3)4)]	MC Jointline Free	SC Jointline Free	Comment
MUP2	50i	50i	50p, (50i)	✓		Master channel is joinlinefree only, if NOT decimated or expanded vertically.
		60i		✓		
		PC signal		✓		
		50i	100i	✓		
		60i		✓		
		PC signal		✓		
	60i	50i	60p, (60i)	✓		
		60i		✓		
		PC signal		✓		
		50i	120i	✓		
		60i		✓		
		PC signal		✓		
FSM/PCP/ SPS/MUP1/ SSC1	PC signal	50i, 60i	Allowed PC standards	✓		
PCF	PC signal	–	Allowed PC standards	✓		Slave channel not available
PCE	PC signal (not visible)	50i, 60i	Allowed PC standards			Master channel not visible

1) 50i=625 lines / 50 Hz interlaced (normal PAL), 60i=525 lines / 60 Hz interlaced (normal NTSC)
50p=625 lines / 50 Hz progressive, 60p=525 lines / 60 Hz progressive (e.g. progressive YPbPr from DVD)

2) Values in brackets belong to single-scan version,

3) No single-scan output possible with double-scan input //

4) Please refer to Table 2–33 on page 53 for upconversion details

Table 2–28: Application mode capabilities

		FSM		SPS		SSC		MUP1		MUP2		PCE		PCF		PCP	
		MC	SC	MC	SC	MC	SC	MC	SC	MC	SC	MC	SC	MC	SC	MC	SC
Frame rate conversion																	
Motion adaptive		✓															
Simple frame based		✓	✓						✓				✓	✓		✓	✓
Simple field based		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Image analysis																	
Motion adaptive temporal noise reduction	Field	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓		✓	✓
	Frame	✓	✓		✓	✓	✓	✓	✓	✓			✓	✓		✓	✓
Film mode detector		✓												✓		✓	
Global motion detector		✓												✓		✓	
Motion detector		✓												✓		✓	
Image Scaler																	
DCI		✓		✓		✓		✓		✓		✓		✓		✓	
V pre-scaler (linear)			✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓		✓
V post-scaler (nonlinear)		✓ [1)]	✓	✓		✓		✓		✓		✓		✓		✓	

[1)] Not usable in “Inverse 3-2 pull down” mode

2.5.4. Write/Read Positioning

The picture position, where the picture is written into the memory is given by ***WRPOSX*** for horizontal and ***WRPOSY*** for vertical direction. The accuracy of positioning is one line in vertical direction. The slave can be positioned horizontally in 16 pixel, whereas the master is positioned only in MUP-modes with 16 pixel resolution. All other modes allow only bigger steps.

The picture position, where the picture is read out of the memory is given by ***RDPOSX*** for horizontal and ***RDPOSY*** for vertical direction. The accuracy of reading is one line in vertical direction, whereas in horizontal direction the accuracy is 2 pixel (master) or 32 pixel (slave)

2.5.5. Multi-Picture Display

For the programming of a multi picture display it must be considered that the addressing of horizontal positions is restricted to a raster of 16 pixels. Therefore only a few configurations have an exact symmetrical structure. The following figures Fig. 2–50 and Fig. 2–51 on page 46 show two alternative configurations for 9 x 1/9 and 16 x 1/16 multi picture displays, respectively. The Fig. 2–52 on page 46 deals with the configurations for 24 x 1/24 and 36 x 1/36 multi picture displays.

Configurations with other picture sizes or combinations of different picture sizes are also possible, when the mentioned addressing restrictions are considered. Corresponding considerations must be done for 16:9 picture tubes. In Fig. 2–50 on page 46 symmetrical borders on the left and right side are achieved for a border width of 32 pixels when the active line length is enlarged to 720 pixels.

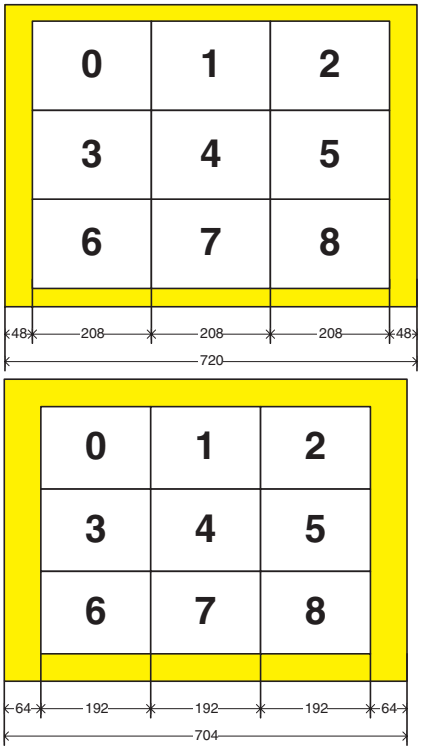


Fig. 2–50: Examples of 9 x 1/9 multi picture

Using 704 active pixels the border width becomes 64 pixels when symmetry is desired.

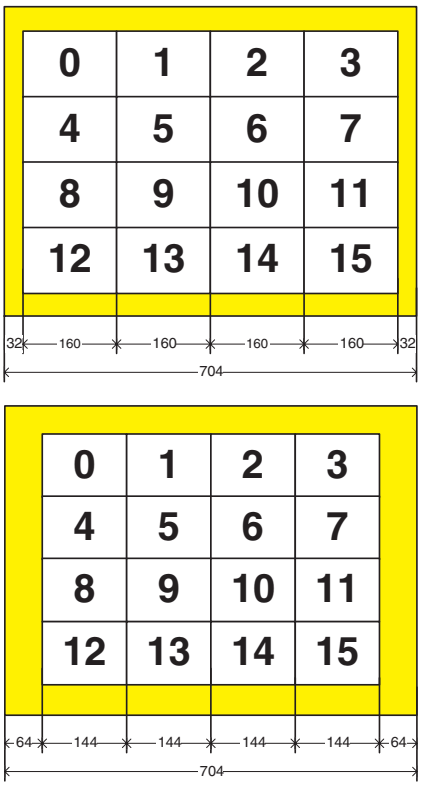


Fig. 2–51: Examples of 16 x 1/16 multi picture

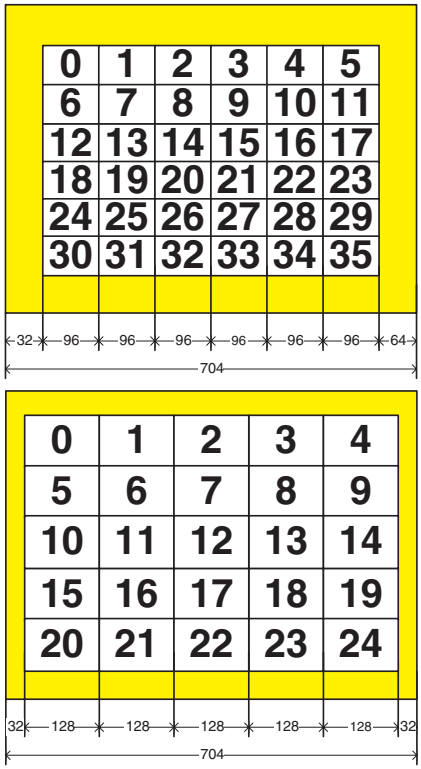


Fig. 2–52: Example of 25 x 1/25 and 36 x 1/36 multi picture

2.5.6. PiP Processing

The PIP engine performs the upconversion of the slave data path. For a multitude of modes joint line free display is possible. In Table 2–29 and Table 2–30 on page 48) all supported display modes are listed.

Table 2–29: Supported interlaced display modes

DISPMODE	STOPMOS	Display Raster	Displayed Fields	Joint Line Free
FSM (0) SPS (1) MUP1 (3) PCE (5) PCP (7) SSC2 (8)	001	αβαβ	ABAB, frame repetition	X
	010	ααββ	AABB, field repetition	
	011	αβαβ	AAAA, field repetition	
	100	ααββ		
	101	αβαβ	BBBB, field repetition	
	110	ααββ		
	111	αβαβ	AA*B*B, intra field interpolation	
SSC1 (2)	000/001/010	ααββ	AABB, field repetition	
	011	αβαβ	AAAA, field repetition	
	100	ααββ		
	101	αβαβ	BBBB, field repetition	
	110	ααββ		
	111	αβαβ	AA*B*B, intra field interpolation	X
MUP2 (4)	000/001/011/101/111		AABB, field repetition (αβαβ)	
	010/100/110		AABB, field repetition (ααββ)	

Table 2–30: Supported progressive display modes

DISPMODE	STOPMOS	Display Raster	Displayed Fields	Joint Line Free
FSM (0) SPS (1) MUP1 (3) PCE (5) PCP (7) SSC2 (8)	001	a+b	A+B, A+B, frame repetition	X
	010		A+A, B+B, line doubling	
	011		A+A, A+A, line doubling, field repetition	
	100		A+A*, A+A*, intra field interpolation, field repetition	
	101		B+B, B+B, line doubling, field repetition	
	110		B+B*, B+B*, intra field interpolation, field repetition	
	111		A+A*, B*+B, intra field interpolation	
SSC1 (2)	000/001/010		A+A, B+B, line doubling	
	011		A+A, A+A, line doubling, field repetition	
	100		A+A*, A+A*, intra field interpolation, field repetition	
	101		B+B, B+B, line doubling, field repetition	
	110		B+B*, B+B*, intra field interpolation, field repetition	
	111		A+A*, B*+B, intra field interpolation	X
MUP2 (4)	X		A+A B+B, line doubling	

2.5.7. Basic Upconversion Concept

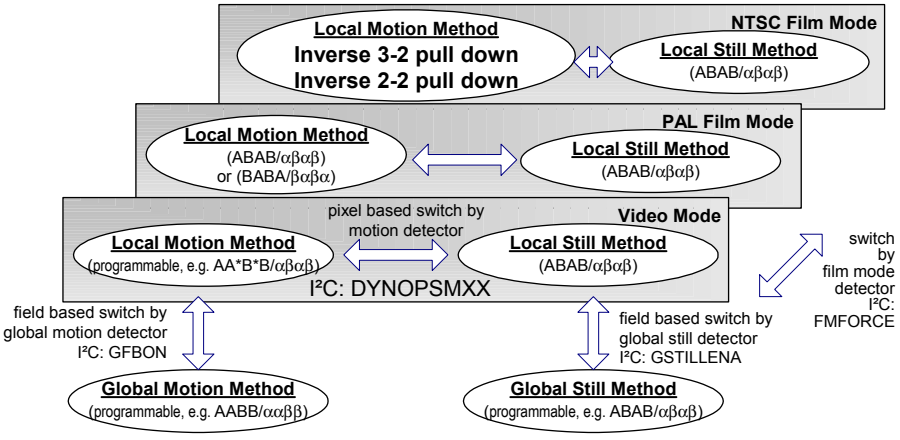
The upconversion creates a temporary progressive output image. This progressive output is used afterwards for vertical scaling. The scaled image now can be interlaced again or remains progressive.

The upconversion itself can be divided into three steps. In the first step the decision is made which of the two available motion phases (motion phase from field A or from field B) should be displayed. This process is called motion phase selection. The original lines from the selected field are copied into the progressive output. In a second step the missing lines for the progressive output are created. Several interpolation methods are available. Now, the progressive image is ready to be scaled vertically. After the scaling the decision about the line scan pattern is made. Interlaced outputs or progressive outputs are possible.

The scan rate conversion algorithm concept is based on the assumption that the video input signal can be in video mode (two consecutive fields belong **not** to the same motion phase) or film mode (means two consecutive fields belong to the same motion phase for 2-2 pull down mode or two and three consecutive fields belong to the same motion phase for 3-2 pull down mode. Please refer to "Filmmode Detection" on page 31.

The video mode material can be further separated. The separation is based on the motion range of the picture content, which is displayed. For the different source materials optimized scan rate conversion methods exists. Film mode material created by 2-2 pulldown (25p to 50i) is converted to 100i should be displayed in ABAB or BABA mode depending on the film mode phase. 60i film mode sources (3-2 pulldown) normally are converted to 60p whereas the "inverse 3-2 pulldown" is the best way for creating the progressive output.

For the video mode material the optimized scan rate conversion method depends on the picture content.



XX = GM = Global Motion
XX = GS = GLOBAL STILL
XX = V = VIDEO
XX = P0-1 = FILM PAL PHASE 0-1
XX = N0-4 = FILM NTSC PHASE0-4

Fig. 2–53: Upconversion concept

2.5.8. General Upconversion Parameters

Fig. 2–54 explains the used wording for the following explanations.

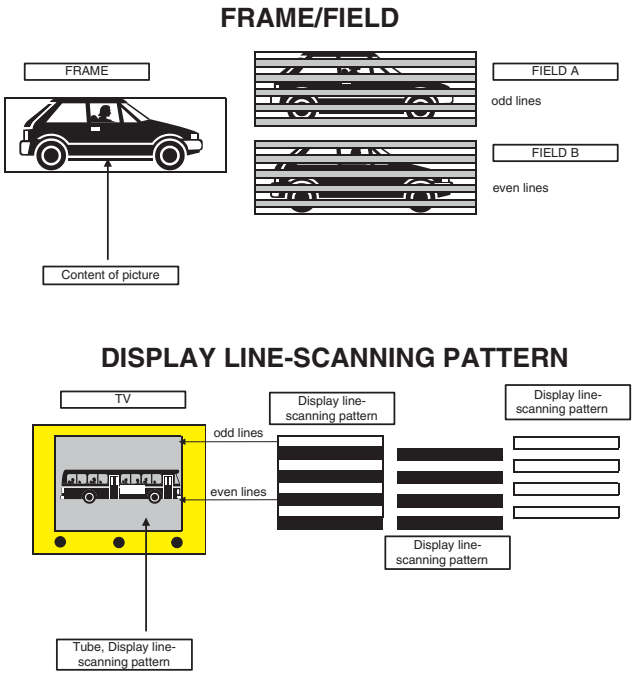


Fig. 2–54: Explanation of field and display line-scanning pattern

The interlaced input signal (e.g. 50 Hz PAL/SECAM or 60 Hz NTSC) is composed of a field A (odd lines) and a field B (even lines).

A^n - Input signal, field A at time n,

B^n - Input signal, field B at time n

The field information describes the picture content. The output signal, which could contain different picture contents (e.g. field A, field B), can be displayed with the display line-scanning pattern α or β.

Examples:

(A^n, α) - Output signal, field A at time n, displayed as line-scanning pattern α,

(A^n, β) - Output signal, field A at time n, displayed as line-scanning pattern β,

($(A^*)^n$, β) - Output signal, field A raster interpolated into field B at time n, displayed as line- scanning pattern β

($A^n B^{n-1}$, $\alpha+\beta$) – Output signal, frame AB at time n, displayed as progressive line-scanning pattern $\alpha+\beta$

The figure below describes the data flow in the VSP 94x5B. The input fields are stored in the internal memory. Maximum two fields (three fields in case of inverse 3-2 pull down) are available for upconversion. The generated output fields belong to four different phases in case of interlaced output or two different phases in case of progressive output, respectively. The delay between the input field and the corresponding output fields depends on the ***OPDEL*** parameter. If ***OPDEL*** is not set correctly, a static jointline may occur in the picture.

Two input fields are used to generate one output field or frame. Therefore first an internal progressive frame is generated. The motion phase of this internal progressive frame is programmed by the parameter DYNOP**MS**XX (MS - Motion Sequence value, XX is the abbreviation as defined in Fig. 2–52 on page 46).

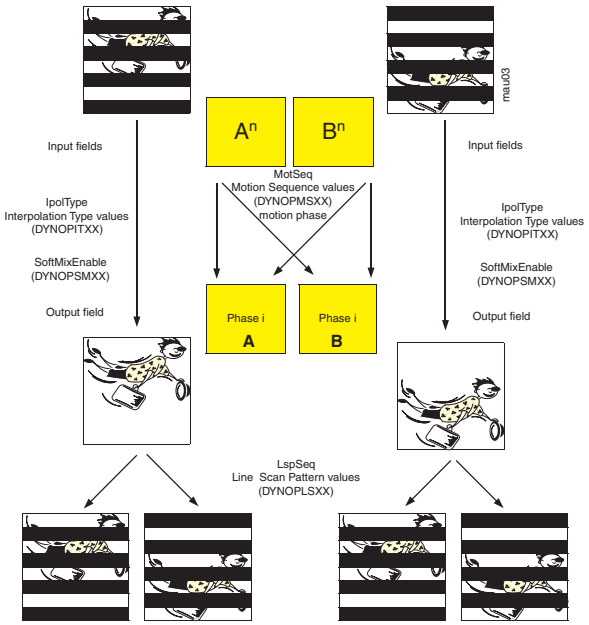


Fig. 2–55: Explanation of output field generation

The interpolation of the missing lines for the internal frame can be programmed by the parameters DYNOP**IT**XX and DYNOP**SM**XX. The first parameter defines the Interpolation Type (e.g. linear filter) and the second enables the Soft Mix method. Soft Mix means using the motion values from the Motion Detector to switch soft between the programmed Interpolation Type mode and the local fall back Interpolation Type Frame display. The Line Scan Pattern of the generated output fields are programmed using the parameter DYNOP**LS**XX.

2.5.8.1. Motion Phase (MotPh) and Motion Sequence (MotSeq)

The input signal usually contains two different fields, an A field with a line scan pattern (Aa) and a B field with b line scan pattern (Bb). The field content (A or B) called motion phase (called MotPh) and the line scan pattern (a or b) are separately handled. E.g. the content of an input Aa field can be displayed as Aa or can be displayed in a b line scan pattern Ab. The formerly coupling of A/a and B/b is now broken.

The continuous output signal can be defined as a sequence of motion phases. The worst case is the 100i output: Four motion phases must be generated from two consecutive input field motion phases A and B. For each output field it has to be decided which motion phase (A or B) should be generated. i.e. for a still input the sequence ABAB is a good 100i output.

The VSP 94x7B has a full frame memory for the chrominance. It is possible to define a static Motion sequence for chrominance by the parameter ***StatOpMsC***.

Table 2–31: MotSeq and LspSeq description (xx is placeholder for the specific dynamic operation case)

		100/120 Hz Interlaced 2V/2H Output **Phase** **0 1 2 3**	**50/60 Hz Progressive 1V/2H** **50/60 Hz Interlaced 1V/2H** **50/60 Hz Interlaced 1V/1H** **Phase** **0 2**
Motion Sequence (MotSeq) **DYNOPMSxx**	0 - MotSeqAAAA	A A A A	AA
	1 - MotSeqBBBB	B B B B	BB
	2 - MotSeqAABB	A A B B	AB
	3 - MotSeqABBA	A B B A	AB
	4 - MotSeqBBAA	B B A A	BA
	5 - MotSeqBAAB	B A A B	BA
	6 - MotSeqABAB	A B A B	AA
	7 - MotSeqBABA	B A B A	BB
Line scan pattern sequence (LspSeq) **DYNOPLSxx**	0 - LspSeqAAAA	$\alpha\ \alpha\ \alpha\ \alpha$	$\alpha\alpha$ (progressive)
	1 - LspSeqBBBB	$\beta\ \beta\ \beta\ \beta$	$\beta\beta$ (progressive)
	2 - LspSeqAABB	$\alpha\ \alpha\ \beta\ \beta$	$\alpha\beta$ (interlaced)
	3 - LspSeqABBA	$\alpha\ \beta\ \beta\ \alpha$	$\alpha\beta$ (interlaced)
	4 - LspSeqBBAA	$\beta\ \beta\ \alpha\ \alpha$	$\beta\alpha$ (interlaced)
	5 - LspSeqBAAB	$\beta\ \alpha\ \alpha\ \beta$	$\beta\alpha$ (interlaced)
	6 - LspSeqABAB	$\alpha\ \beta\ \alpha\ \beta$	$\alpha\alpha$ (progressive)
	7 - LspSeqBABA	$\beta\ \alpha\ \beta\ \alpha$	$\beta\beta$ (progressive)

2.5.8.2. Line Scan Pattern (Lsp) and Line Scan Pattern Sequence (LspSeq)

According to the motion phase each output image will be assigned an line scan pattern (Lsp). The combination of 4 line scan patterns is called Line Scan Pattern Sequence (LspSeq). The line scan pattern sequence can be adjusted by a list of parameters including the key word ***DYNOPLS*** followed by the sequence. The combination of four motion phases is called Motion Sequence (in the following marked as MotSeq). The motion sequence can be adjusted by a list of parameters including the key word ***DYNOPMS*** followed by the indicator of the dynamic operation case (e.g. DYNOPMSGM for the motion sequence for the global motion case). 8 (progressive: 4) different motion sequences are allowed which represent all necessary combinations.

2.5.8.3. Interpolation Type Values (IpolType)

If the picture content does not fit to the line scan pattern or in case of de-interlacing (creation of missing lines in the progressive output frame), these picture content or missing lines must be created by interpolation. Four different techniques can be selected by setting the interpolation type value IpolType. The interpolation type can be adjusted by a list of parameters including the key word ***DYNOPIT*** followed by the indicator of the dynamic operation case (e.g. DYNOPITP0 for the IpolType for the first 2-2 pulldown case). The different values are described in the following table.

Table 2–32: IpolType description

DynOpIt	Description
0 - IpolTypeAB	Frame based de-interlacing using original A and B lines for displaying still sequences
1 - IpolTypeLineDb1	Field based de-interlacing using line doubling
2 - IpolTypeLin2	Field based de-interlacing using linear interpolation
4 - IpolTypeLin4	Field based de-interlacing using modified line doubling

2.5.8.4. SoftBlend Enable Switch (SoftBlendEna)

In still areas of the input fields the upconversion uses the SoftBlend functionality to switch soft and pixelwise the interpolation type from the adjusted IpolType to the IpolTypeAB. The SoftBlend feature can be enabled by the ***SoftBlendEna*** switch. If disabled, the selected IpolType is used for the whole picture. The soft blend switch can be adjusted by a list of parameters including the key word ***DYNOPSM*** followed by the indicator of the dynamic operation case (e.g. DYNOPSMGS for the SoftBlendEna for the global still case).

2.5.8.5. Filmmode Handling

The I²C bus read register ***FILMMODE*** consists of 4 bits. The 3 LSBs indicate the current film type and phase, the MSB indicates whether the 3 LSBs were generated synthetically inside the film mode detector (phase flywheel mode on unsecure input sources) or if the film mode detection result was securely detected (see chapter 2.4.4. "Filmmode Detection" on page 31 for details). This signal is used as input for the Upconversion-Modified Filmmode Generator (UMF). The generator is controlled by the I²C bus ***FmForce*** and ***FmForceTrig*** signals and has as output a modified filmmode signal.

Three general possibilities exist to modify the incoming ***FILMMODE*** signal. Please refer to Table 2–33 on page 53). ***FmForce*** = 15 disables the UMF and uses the original unmodified ***FILMMODE*** signal for further processing. It is also possible to discard the original information and to generate (“force”) an artificial filmmode signal. This is helpful for test purposes or when having film type and phase information available from external. Three different film types can be forced: Video mode (formerly called Camera mode), 2-2 pulldown mode (**FM PAL**) or 3-2 pulldown mode (**FM NTSC**).

Adjusting 2-2 pulldown mode the two film phases A_nB_n (***FmForce*** = 1) or B_nA_{n+1} (***FmForce*** = 2) can be adjusted. Forcing a mode requires to set ***FmForceTrig***. Switching to ***FmForce*** = 3…7, the film phases 0, 1, 2, 3 and 4 are generated cyclically starting with the adjusted ***FmForce***. To change the 3-2 pulldown mode film phase again, ***FmForce*** must be changed and at the same time ***FmForceTrig*** must be set (and released). A usually used modification restricts the ***FILMMODE*** signal to selected film types.

It is possible to limit the allowed film types only to Video mode, to 2-2 pulldown mode, or only to 3-2 pulldown mode. A combination of two modes can also be selected.

Table 2–33: Upconversion modified film mode generator

Fm Force	UMF Output	
	Mode	**Phase**
0	Force **VIDEO** mode	
1	Force **FM PAL**	With phase A_nB_n
2		With phase B_nA_{n+1}
3	Force **FM NTSC**	Starting with phase 0
4		Starting with phase 1
5		Starting with phase 2
6		Starting with phase 3
7		Starting with phase 4
8	Allow **VIDEO** only	
9	Allow **FM PAL** only	If secure detection result, synchronize phase, otherwise use internal phase generator
10	Allow **FM NTSC** only	
11	Allow **VIDEO** and **FM PAL** only	
12	Allow **VIDEO** and **FM NTSC** only	
13	Allow **FM PAL** and **FM NTSC** only	
14	Allow all modes	
15		Use unmodified film mode detector result

For all modes ***FmForce*** = 8…14 the following rules are valid:

– Once one of the allowed film types is detected, all excluded film types cannot be reached anymore (until switching to other ***FmForce*** values).

– If the ***FILMMODE*** signal indicates an allowed film type and the detection result is “secure”, the original film phase is used.

– If the ***FILMMODE*** signal indicates any excluded film type, the last detected and allowed film type is hold.

– If the ***FILMMODE*** signal indicates “unsecure” in any film type, the last detected and allowed film type is hold.

– Directly after activating one of the modes ***FmForce*** = 8…14 described above, one of the two scenarios can occur:
  - The current UMF output film type already is one of the allowed film types. In this case the UMF output is transfered seamless to the actual mode.
  - The current UMF output is one of the film types which are not allowed. Now the original ***FILMMODE*** signal is used unmodified, as long as the ***FILMMODE*** signal does not indicate one of the allowed film types. To avoid undetermined behavior after switching, it is recommended to use a two step switching approach. First switch to ***FmForce*** = 0 to force Video mode (to establish a stable state), then switch to your desired mode (e.g. ***FmForce*** = 11).

2.5.8.6. Dynamic Operation Table (DynOpTable)

The DynOpTable transforms the programmed I²C bus parameter into internal signals which determine the current output sequence behavior. The global motion signal ***GMotion***, the global still signal ***GStill*** and the modified film mode signal UMF are generated inside the IC. Depending on these input signals the programmed motion sequence MotSeq, the line scan pattern LspSeq, the interpolation type IpolType the soft blend enable switch SBlendEna and the inverse 3-2 pull down position FJPos are selected. The parameter are coded as follows: DYNOP**YYXX**

The description for YY and XX is described in Table 2–34. For example: ***DYNOPMSGM*** means Motion Sequence value for the Global Motion Fall Back Mode.

Table 2–34: DYNOPYYXX description

YY	XX	Description
MS		Motion Sequence value
IT		Interpolation Type value
SM		Soft Blend Enable value
LS		Line Scan Pattern value
	GM	Global Motion Fall Back mode
	GS	Global Still Fall Back mode
	V	Video mode
	P0	2-2 pulldown mode (FM PAL) (phase 0)
	P1	2-2 pulldown mode (FM PAL) (phase 1)
	N0	3-2 pulldown mode (FM NTSC) (phase 0)
	N1	3-2 pulldown mode (FM NTSC) (phase 1)
	N2	3-2 pulldown mode (FM NTSC) (phase 2)
	N3	3-2 pulldown mode (FM NTSC) (phase 3)
	N4	3-2 pulldown mode (FM NTSC) (phase 4)

Table 2–35: Dynamic operation table

GMotFlag	GStillFlag	UMF	MotSeq	IpolType	SBlendEna	FJPos	LspSeq
1	x	x	DynOpMsGm	DynOpItGm	DynOpSmGm	DynOpFjGm	DynOpLsGm
0	1	x	DynOpMsGs	DynOpItGs	DynOpSmGs	DynOpFjGs	DynOpLsGs
0	0	000	DynOpMsV	DynOpItV	DynOpSmV	DynOpFjV	DynOpLsV
0	0	001	DynOpMsP0	DynOpItP0	DynOpSmP0	DynOpFjP0	DynOpLsP0
0	0	010	DynOpMsP1	DynOpItP1	DynOpSmP1	DynOpFjP1	DynOpLsP1
0	0	011	DynOpMsN0	DynOpItN0	DynOpSmN0	DynOpFjN0	DynOpLsN
0	0	100	DynOpMsN1	DynOpItN1	DynOpSmN1	DynOpFjN1	DynOpLsN
0	0	101	DynOpMsN2	DynOpItN2	DynOpSmN2	DynOpFjN2	DynOpLsN
0	0	110	DynOpMsN3	DynOpItN3	DynOpSmN3	DynOpFjN3	DynOpLsN
0	0	111	DynOpMsN4	DynOpItN4	DynOpSmN4	DynOpFjN4	DynOpLsN

The GMotFlag indicator is the combination of the parameters ***GFBON*** and ***GmFmFbEna*** and the global motion indicator bit ***GMOTION*** (Table 2–36).

Table 2–36: GMotFlag combination

GMOTION	GFBON	GmFmFbEna	UMF	GMotFlag
0	x	x	x	**0**
1	0	x	x	**0**
1	1	0	0	**1**
1	1	0	1...15	**0**
1	1	1	x	**1**

In the same way the GStillFlag is combined.
See Table 2–37 for details.

Table 2–37: GStillFlag combination

GSTILL	GStillEna	GsFmFbEna	UMF	GStillFlag
0	x	x	x	**0**
1	0	x	x	**0**
1	1	0	0	**1**
1	1	0	1...15	**0**
1	1	1	x	**1**

The parameter ***GFBON*** activates the global fall back switch. When activated, the setting for "global motion" is used, if the readable bit ***GMOTION*** is set. This is used to switch for example in case of 100 Hz interlaced to AABB in case of big motion in the picture. If activated the ***GMOTION*** flag has the highest priority. The second priority has the ***GSTILL*** flag, which can be activated with ***GSTILLENA***. This can be used for example in case of 100 Hz interlaced to switch to ABAB mode in case of a complete still picture. The last priority has the UMF flag, which selects between the detected mode camera or the different film phases. By using ***GmFmFbEna*** and ***GsFmFbEna***, the decision for film-mode can be priorized. In this case, the fall back processing is disabled.

2.5.8.7. Inverse 3-2 Pull Down

For progressive output sequence with single V frequency a special mode for displaying film mode sources without interpolation and in frame resolution can be used. This mode is called inverse 3-2 pull down mode. To enable this feature some restrictions are valid.

– Vertical expansion or decimation **can not** be used. For special exceptions, please refer to application-note.

– Vertical locked mode must be used.

– Horizontal locked mode must be used and LL-PLL must be in locked condition (***STABLL***=1).

The inverse 3-2 pull down mode can be activated by the I²C bus register ***FJMode***.

The motion sequence (MotSeq), the line scan pattern (LspSeq), the interpolation type value (IpolType), the softmix enable switch (SoftMixEna), and the inverse 3-2 pull down position switch (FJPos) must be programmed by I²C bus in the dynamic operation table (DynOpTable).

2.6. Display Processing

The display processing part contains an integrated triple 9-bit DAC and performs digital enhancements and manipulations of the digital video component signal. Fig. 2–56 shows the block diagram of the display processing part.

2.6.1. Digital Contrast Improvement (DCI)

There is a strong demand on picture contrast, but each video display has a limited dynamic range. Especially the flat display panels like LCD and PDP (plasma display panel) have a lower dynamic range compared to CRT. The picture contrast can't be increased by simply increasing the video signal amplitude, because exceeding the display dynamic range causes unwanted effects. An efficient use of display dynamic range depending on the picture contents increases picture contrast and quality.

The basic function of DCI is to analyze the picture framewise and adjust the parameters of a dual segment transfer function depending on the analysis results for the best subjective picture quality. Therefore, each image frame is analyzed for three different characteristics. The image average brightness, the dark sample distribution, and the frame peak value. These parameters control the transfer function.

The dual segment transfer function consists of two segments with an adaptive pivot point. A lower segment for dark samples and an upper segment for light

samples. The gain of the lower segment is adaptive to the dark sample distribution. A higher gain results from fewer dark samples and a lower gain from a higher number of dark samples. The gain is limited in the range as given below. The gain of the upper segment is adaptive to the frame peak value. It is computed in the way that the detected peak value lower than the nominal, will be moved to nominal peak value. If the detected peak value is equal or higher than the nominal peak value then, a gain of 1.0 is used (no change). The computed theoretical gain is limited then to a maximum value in order to avoid unnatural effects. ***DCION*** enables or disables DCI function.

When modifying the contrast of the picture (luminance), a chrominance compensation is also performed, in order to avoid wrong color saturation. This feature may be disabled by ***CSCON***. Independent from the actual display region, image analysis is done within a user-defined window. It is defined by start pixel (***SPIXEL***), end pixel (***EPIXEL***), start line (***SLINE***) and end line (***ELINE***).

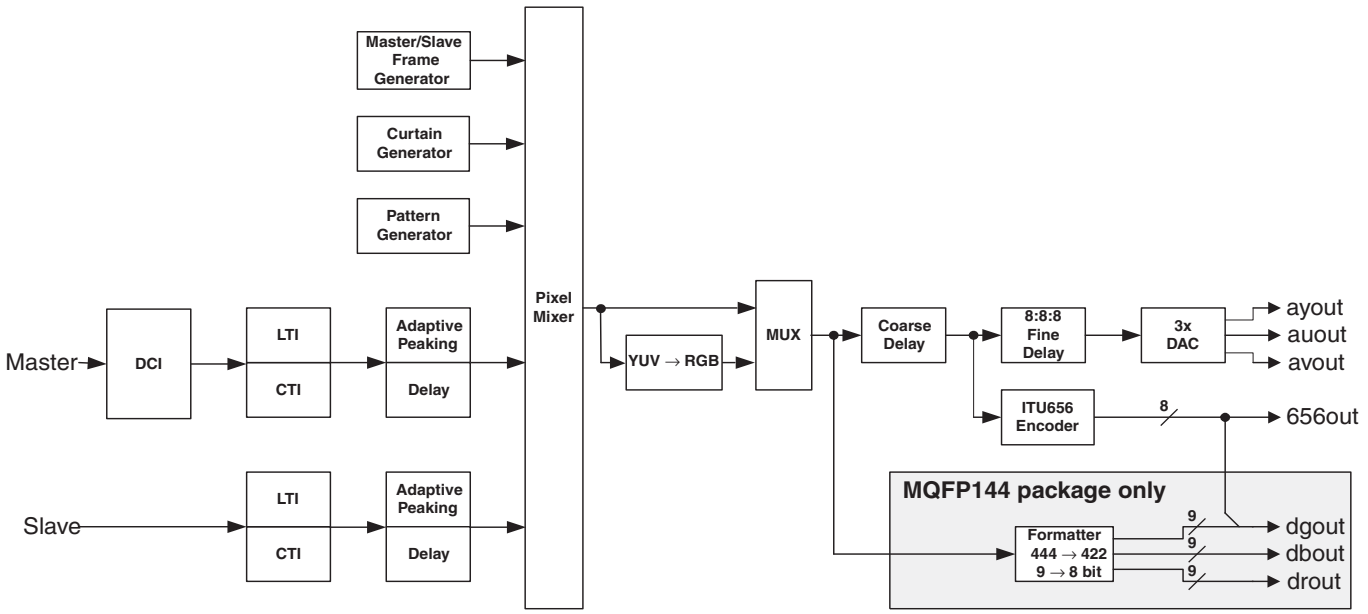


Fig. 2–56: Block diagram of display processing

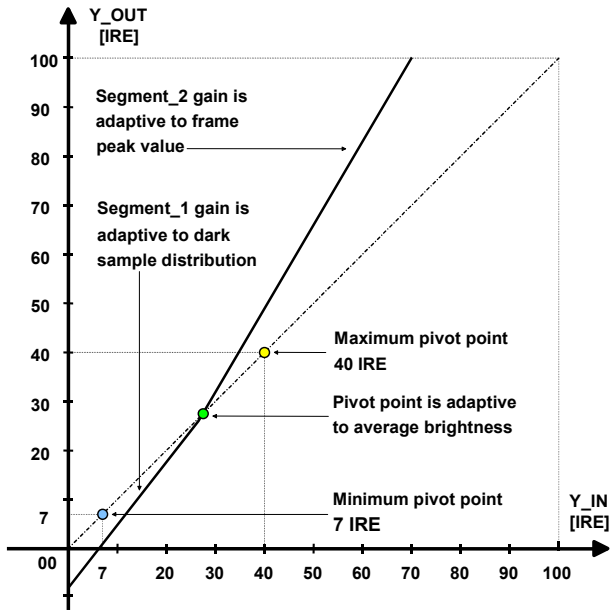


Fig. 2–57: DCI basic function

Each image frame is analyzed for three different characteristics like average brightness, dark sample distribution and peak value. The sensitivity of the average brightness analysis is determined by the setting of ***SENSWS***. A higher value reduces and a lower value increases the sensitivity. The sensitivity is also a function of the analyzed picture size which is defined by analysis window settings. If a desired sensitivity is adjusted and after that the analyzed picture size is changed, then the sensitivity will also be changed. If it is desired to keep the same sensitivity for different analysis window settings, then the ***SENSWS*** value has to be matched by linear interpolation to the new size (see the example given below).

$$SENSWS = \frac{Pixelperline_{analyzed} \cdot Linesperframe_{analyzed}}{9112}$$

$$SENSWS = \frac{680 \cdot 536}{9112} = 40$$

The sensitivity of the dark sample distribution analysis is determined by the setting of ***SENSBS***. A higher value reduces and a lower value increases the sensitivity. The sensitivity is also a function of the analyzed picture size which is defined by analysis window settings. If a desired sensitivity is adjusted and after that the analyzed picture size is changed, then the sensitivity will also be changed. If it is desired to keep the same sensitivity for different analysis window settings then the ***SENSBS*** value has to be matched by linear interpolation to the new size as described for ***SENSWS***.

Dark sample distribution analysis considers for the measurement the size of dark areas related to the total size of analysis window so that small dark parts in the image do not influence the measurement too much. The sensitivity to small dark areas is adjustable by ***DYTC***. Lower value for ***DYTC*** means high sensitivity and higher value low sensitivity.

The basic function of average brightness analysis is the measurement of light sample and dark sample contribution difference. The contribution of light sample is weighted by ***LSWF*** value. The ***LSWF*** setting determines which picture will be considered as light and which as dark. A lower value for ***LSWF*** reduces and a higher value increases the measured result of average brightness. ***LSWF***=0 turns the contribution of light samples off and every picture will be considered as dark. ***SCANID*** gives information about interlace/progressive input and should be set equal to ***FMODE.***

Image analysis is done frame by frame. Depending on the analysis results a suitable transfer function is used for video processing. The analysis results are filtered with a time constant determined by the settings ***ABFTC*** for average brightness, ***DSFTC*** for dark sample distribution and ***PK_FTC*** for peak analysis. A shorter time constant results from a higher setting and a longer time constant from a lower setting for XX_FTC.

ERRORCOMP is used to increase the analysis precision in dark sample distribution part by taking the remainder value in temporal register at the end of analysis into consideration. The value of ***ERRORCOMP*** is determined by the settings of ***SENSBS*** and ***DYTC***. The equation below should be used to determine the proper value.

$$ERRORCOMP = \frac{32 \cdot SENSES}{DYTC}$$

(integer part only)

The contribution of peaks with small size to the total frame peak value is controlled by ***PEAK_SIZE***. A lower value for ***PEAK_SIZE*** increases, and a higher value reduces the contribution of peaks in the image.

2.6.2. Adaptive Peaking

The luminance peaking filter improves the overall frequency response of the luminance channel. It consists of two filters working in parallel. They have high pass (HP) and band pass (BP) characteristics.

The peaking filter clock frequency is CLKB36 (usually 36 MHz). The maximum signal frequency of the picture stored in the memory is 6.75 MHz. Due to a peaking after postscaler, the frequency range of the peaking filter varies with the expansion factor of the postscaler.

Table 2–38: Peaking filter frequencies

Expansion Factor of Postscaler	Corresponding Frequency of Input Signal for Center Frequency	
	Bandpass (BP)	Highpass (HP)
0.75	2.66 MHz	6.75 MHz
...	...	...
1	3.55 MHz	9 MHz
...	...	...
3	10.65 MHz	27 MHz

The peaking is picture-content adaptive.

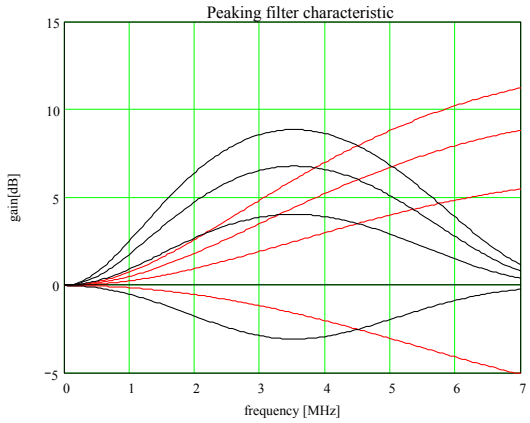


Fig. 2–58: Bandpass/highpass filter characteristic

In a first region, adjustable by ***ATH1BP*** and ***ATH1HP*** for bandpass and highpass, respectively, the signal is damped for to reduce noise (denoising). The second region is adjusted by ***ATH2BP*** (***ATH2HP***). For this region, the amount of peaking is given by ***APK1BP*** (***APK1HP***). The peaking value for the last part is given by ***APK2BP*** (***APK2HP***).

Additional to adaptive peaking, a luminance transition improvement (LTI) circuit may be enabled by ***LTI***.

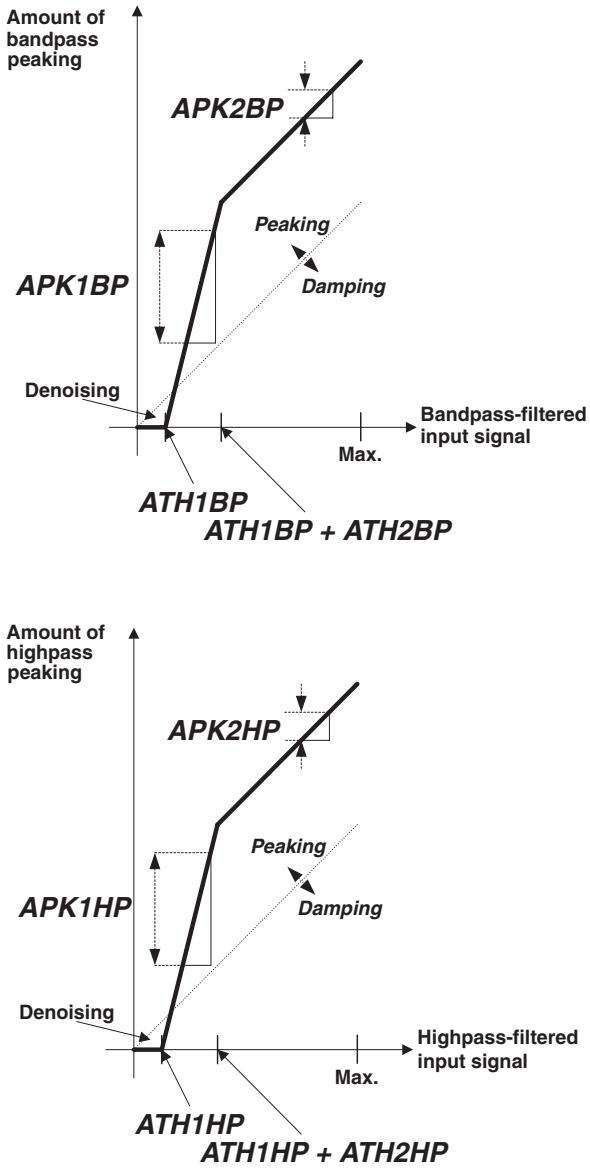
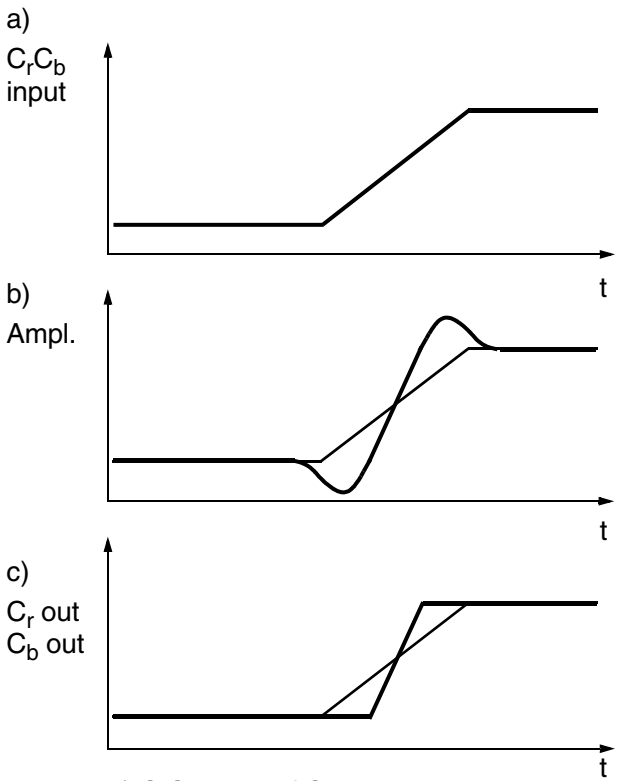


Fig. 2–59: Adaptive peaking segments (BP and HP)

2.6.3. Color Transition Improvement (CTI)

A digital algorithm is implemented to improve horizontal transitions of the chrominance signals resulting in a better picture sharpness. A highpass/bandpass frequency peaking of the signal usually produces broad overshoots. To eliminate “wrong colors”, which are caused by over and undershoots at the chroma transition, the sharpened chroma signals are limited to a proper value automatically. The amount of peaking for the bandpass is adjusted by ***PKCTIBPM***, for the highpass by ***PKCTIHPM***.



a) C_rC_b input of CTI
b) C_rC_b input + correction signal
c) sharpened and limited C_rC_b

Fig. 2–60: Principles of CTI

2.6.4. Pixel Mixer

The aim of the pixel mixer is the combination of the different paths of video sequences to one final video stream being shown by the display unit. Thereby 6 different sources (layer) are possible which are listed in the following table:

Table 2–39: Pixelmixer layer naming conventions

Layer	Suffix
Master channel	M
Slave channel	S
Master frame	G
Slave frame	F
Curtain	C
Background and testpattern	P

The size of the background layer determines the size of the picture. This means, that the background must have at least the size of the picture to be displayed.

Every layer is determined by the position of the upper left edge (***HORPOSx***, ***VERPOSx***) and a stretch in horizontal and vertical direction (***HORWIDTHx***, ***VERWIDTHx***). Additionally, the frame-size is defined by ***HORFRAMEx*** and ***VERFRAMEx***.

While in the default case of interlace (***FMODE***=0), the parameters ***VERPOSx*** and ***VERWIDTHx*** are directly used, in the case of progressive (***FMODE***=1) the parameters ***VERPOSx*** and ***VERWIDTHx*** are multiplied by 2. This is necessary for avoiding additional changes after switching from interlace to progressive or vice versa in order to display all picture elements at the same position.

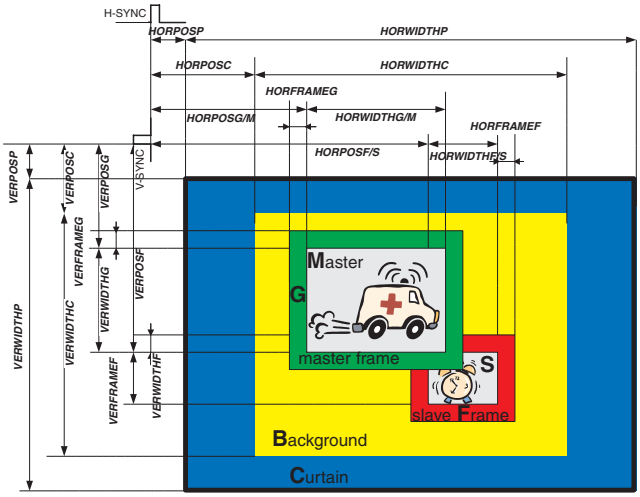


Fig. 2–61: Example of pixel mixer output

2.6.4.1. Priority Decoder

For every layer a priority can be chosen (***PRIOC***, ***PRIOS***, ***PRIOM***, ***PRIOG***, ***PRIOP***, ***PRIOF***). 0 is lowest priority, 15 is highest priority. It is not allowed to give two or more layers same priority. The selectable range is 0, 2, 4, 6, 8, 10, 12, 14. The values between can not be selected but result from the virtual overblending channel.

Fig. 2–62: Overblending

The blending can be enabled by ***OBSOFT***. The temporal dynamic version is enabled by ***OBTEMP***. In this temporal overblending mode ***TBLEND*** specifies how long the soft switching from master components to slave components or vice versa will take. In the static mode (***OBTEMP***=0), ***TBLEND*** gives the proportion of master and slave channel.

Table 2–40: Static and dynamic blending

OBTEMP	TBLEND	Ratio of Lower/Higher Priority
0	00	25/75
	01	50/50
	10	62.5/37.5
	11	75/25
1	00	100/0...fast...0/100
	01	100/0...medium...0/100
	10	100/0...slow...0/100
	11	100/0...very slow...0/100

The components of this virtual overblending channel can be the master and the slave without frame

((***PRIOF***<***PRIOS***)&(***PRIOG***<***PRIOM***)&(***PRIOM***=***PRIOS***±2)).

The master frame and the slave frame can additionally be taken into consideration

(***PRIOG***=***PRIOM***+2=***PRIOF***+4=***PRIOS***+6 or ***PRIOF***=***PRIOS*** +2=***PRIOG***+4=***PRIOM***+6).

Table 2–41: Suggested priorities for pixel mixer

	Show PiP	Hide PiP	Use Curtain
PRIOF	12	8	8
PRIOS	10	6	6
PRIOG	8	12	12
PRIOM	6	10	10
PRIOC	2	2	2
PRIOP	0	0	14

2.6.4.2. Background and Testpattern Component

Displaying the background trivially uses constant values for the Y, U, and V components. However, also nontrivial background images can be generated. How they look like can be seen in the following figure. The used pattern is defined by the IIC-bus parameter ***PATTERN_MODE*** having 3 bits. For the trivial background ’000’ is used.

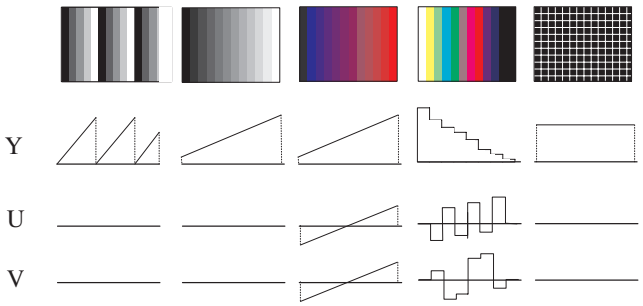


Fig. 2–63: Possible testpattern

All patterns have a length of 288 lines. The chroma is always in 4:4:4 format. In horizontal direction 960 pixels are generated.

If the displayed picture size differs from (288/960), blank picture is added or picture content is cut.

The trivial background pattern takes for Y the constant luminance ***YBAGR***, for U and V the constant chrominance ***UBAGR*** and ***VBAGR***. The *Yramp* gives only a ramp to the luminance channel. The U and V channel are "0". The ramp starts at 0 and with every clock cycle the output increases. After 255 the output starts at 0 again. So nearly four ramps will be seen with 960 pixel resolution. The *Yrampsoft* is only one ramp over the whole screen. It starts at black and is increases every forth pixel. Maximum amplitude is reached after 960 pixel. The *YUVrampsoft* equals the *Yrampsoft* having a ramp on U and V additionally. The *colorbar* equals an ITU100/75/75 color bar. The *crosshatch* is used to adjust the geometry of the picture. Some vertical and horizontal lines with white and are inserted into a black picture. The chroma is always 0.

2.6.4.3. Window Generator

This generator is able to realize an automatic closing and opening of the displayed picture. This means that with every picture the displayed curtain, defined by ***UCUR***, ***VCUR*** and ***YCUR*** will get bigger or smaller. The original picture data will be replaced by the curtain values and vice versa. 4096 different colors are available.

The Fig. 2–64 shows the functionality of the horizontal window function. The window can be closed or opened.

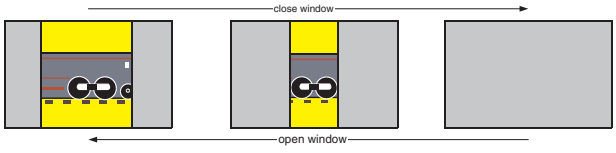


Fig. 2–64: Horizontal windowing

The windowing feature can be enabled by the ***WINDHON*** parameter. The ***WINDHST*** and the ***WINDHDR*** parameter determine, what status (opened or closed) the window has, and what can be done with the window (open or close). With each enabling of the window function by the ***WINDHON*** parameter, the status of the window will be as defined by ***WINDHST*** and ***WINDHDR***. To change from „close“ to „open“ or vice versa only the ***WINDHDR*** parameter has to be toggled. The speed of the window can be defined by the ***WINDHSP*** parameter. The Figure 2–65 shows the functionality of the vertical window function.

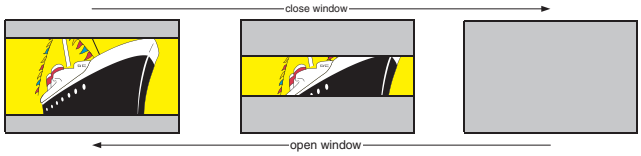


Fig. 2–65: Vertical windowing

All settings are also available in vertical direction. All I²C parameters exist for both directions (e.g. ***WINDHON*** and ***WINDVON*** for horizontal and vertical window enabling). Combinations of both window functions (horizontal and vertical) are also possible.

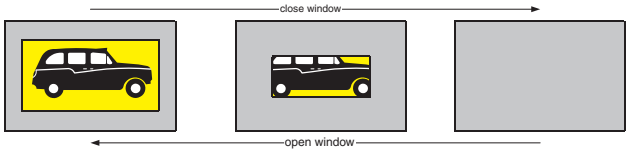


Fig. 2–66: Horizontal and vertical windowing

2.6.5. Coarse and Fine Delay

Before digital-to-analog conversion an adjustment of the phase of the luminance is performed. A coarse delay from -8 to +7 in steps of 1 pixel CLKB36 (~28 ns) are possible (***COARSEDEL***). ***FINEDEL*** shifts the luminance one CLKB72 (~14 ns) pixel. This can be used to compensate delays, when Y and UV are externally processed differently (e.g. lowpass filtered).

2.6.6. YCrCb Control for Digital Output

The VSP 94xxB supports the following picture adjustment parameters on the master and slave signal:

– $0 \leq$ contrast $\leq 63/32$ (***DPCON)***

– $-15 \leq$ brightness ≤ 48(***DPBRT)***

– $0 \leq$ saturation $C_r \leq 63/32$ (***DPVSAT***)

– $0 \leq$ saturation $C_b \leq 63/32$ (***DPUSAT***)

These adjustments should only be used, if there is no other adjustment possible in the system (e.g. flat-panel application). In case of analog display (tube), these adjustments should be done in backend device.

2.6.7. RGB Matrix

The yuv_rgb block converts video data from yuv-format to rgb-format by means of a free programmable matrix. This RGB signal is intended to be used as digital 3*9bit RGB signal, but may also be used on analog outputs. C1...C6 are signed integer values in the range from -511...511. The color saturation may be influenced by "S" in the range about 0.5<S<1.5. The Tint can be adjusted by "α" in the range of -0.14<α<0.14 (resulting in a range of +/- 8°).

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & K_{rb} & K_{rr} \\ 1 & K_{gb} & K_{gr} \\ 1 & K_{bb} & K_{br} \end{bmatrix} \bullet \begin{bmatrix} 1 & 0 & 0 \\ 0 & S & -Sa \\ 0 & Sa & S \end{bmatrix} \bullet \begin{bmatrix} Y \\ C_b \\ C_y \end{bmatrix}$$

RGB-matrix Tint, Saturation

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & (SK_{rb} + SaK_{rr}) & (-SaK_{rb} + SK_{rr}) \\ 1 & (SK_{gb} + SaK_{gr}) & (-SaK_{gb} + SK_{gr}) \\ 1 & (SK_{bb} + SaK_{br}) & (-SaK_{bb} + SK_{br}) \end{bmatrix} \bullet \begin{bmatrix} Y \\ C_b \\ C_r \end{bmatrix}$$

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & \frac{C1}{128} & \frac{C2}{128} \\ 1 & \frac{C3}{128} & \frac{C4}{128} \\ 1 & \frac{C5}{128} & \frac{C6}{128} \end{bmatrix} \bullet \begin{bmatrix} Y \\ C_b \\ C_y \end{bmatrix}$$

The following matrix is obtained by default parameters.

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1,4 \\ 1 & -0,34 & -0,71 \\ 1 & 1,77 & 0 \end{bmatrix} \bullet \begin{bmatrix} Y \\ C_b \\ C_y \end{bmatrix}$$

2.6.8. Oversampling and DAC

After conversion into 8:8:8 format (CLKB72=72 MHz), three 9-bit digital-to-analog converters are used for analog YUV output. This twofold-oversampling generates 1920 active pixels per line (when using recommended settings) and simplifies the external postfiltering. Output voltage is determined by ***PKLY***, ***PKLU*** and ***PKLV*** in a range of 0.4 ...1.9 V (fullscale). The maximum output amplitude calculates as follows:

$$Voltage = \left(1,56V \cdot \frac{PKLx}{256} + 0,36V\right) \cdot signal$$

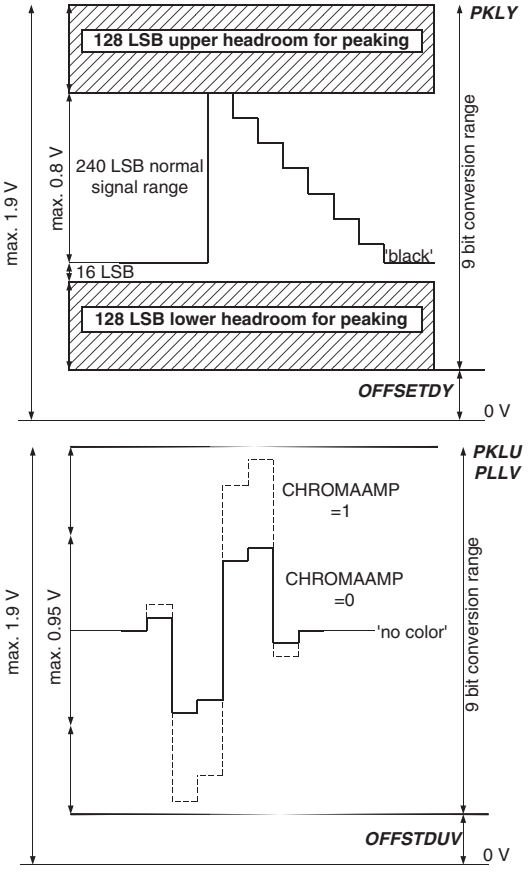


Fig. 2–67: DAC output signals

8 bits of the luminance D/A converter are used for the entire signal. The 9th bit is used for over- and undershoots caused by the peaking to prevent or reduce clipping artifacts. As the CTI block seldomly produces such overshoots, a full-scale operation can be activated by ***CHROMAMP***. For luminance, full-scale operation can be activated by ***LUMAMP***.

2.6.9. Output-Data Controller

The output data controller generates horizontal and vertical syncs. Both sync-generators have a so called “locked-mode” and “freerunning-mode”. The Table 2–42 shows all configurations.

Table 2–42: HOUT and VOUT generator configurations

Mode	HOUTFR	VOUTFR
"H-and-V-locked" mode	0	0
"H-freerunning/ V-locked" mode	1	0
"H-locked/ V-freerunning" mode	0	1
"H- and V-freerunning" mode	1	1

For freerun mode the backend part works stand alone without analyzing the input signal. The clock domains, input data part and output data part of the IC, are not related to each other. If the output processing works in the freerun mode, the output signals of the ODC are generated depending on I²C-bus settings. For locked mode the backend part works with a line locked clock. This means that the frontend and the backend of the IC depend on each other. The generation of the controlling signals depends on output signals from the frontend. This mode will be the default and the most used mode for standard TV applications.

When no or very weak signal is connected to the CVBS input, the IC can be configured to automatically switch into freerunning mode. This stabilizes the display which may contain OSD information, e.g. during channel-tune. The configuration, whether the IC switches to H-freerun, V-freerun or both can be configured by ***AUTOFRRN***.

2.6.9.1. HOUT Generator

The HOUT generator has two operation modes, which can be selected by the parameter **HOUTFR**. The HOUT signal is active high for 64 clock cycles (CLKB36). In the freerunning-mode the HOUT signal is generated depending on the ***PPLOP*** parameter. In the locked-mode the HOUT signal is locked on the incoming H-Sync signal derived from CVBS. The polarity of the HOUT signal is programmable by the parameter ***HOUTPOL***.

2.6.9.2. VOUT Generator

The VOUT generator has two operation modes, which can be selected by the parameter ***VOUTFR***. In the freerunning-mode (***VOUTFR***=1) the VOUT signal is generated depending on the ***LPFOP*** parameter.

In the locked-mode the VOUT signal is synchronized by the incoming V-Sync signal derived from CVBS, delayed by some lines (***OPDEL). OPDEL*** must be adjusted for different input signals and different IC adjustments.

During one incoming V-Sync signal, two VOUT pulses have to be generated. The polarity of the VOUT signal is programmable by the parameter ***VOUTPOL***. The VOUT signal is active high for two output lines

Table 2–43: Display line scanning pattern sequence

Display sequence	1. to 2. (lines)	2. to 3. (lines)	3. to 4. (lines)	4. to 5.(1.) (lines)
α–α–α–α	312	313	312	313
β–β–β–β	313	312	313	312
α–α–β–β	312	312.5	313	312.5
α–β–β–α	312.5	313	312.5	312
β–β–α–α	313	312.5	312	312.5
β–α–α–β	312.5	312	312.5	313
α–β–α–β	312.5	312.5	312.5	312.5
β–α–β–α	312.5	312.5	312.5	312.5
αβ–αβ	625	625	625	625
αβ–αβ	625.5	624.5	625.5	624.5

2.6.9.3. BLANK Generator

The BLANK signal is used to horizontally and vertically mark active picture area. It is enabled by ***BLANEN*** and its polarity can be chosen by ***BLANPOL*** and ***VBLANPOL***. Referred to hsync, the start is given by ***BLANDEL*** and its length is given by ***BLANLEN***, both adjustable in 4 pixel resolution. Referred to vsync, the start is given by ***VBLANDEL*** and its length is given by ***VBLANLEN***, both adjustable in 1 lines resolution.The blank information can be supplied to pin "656vio/blank" (***656BLANK***) or pin "vout50/blank" (***V50BLANK***).

2.6.10. Static Pin Switching

It is possible to set the pin "h50/irq" to static 0 or 1 by ***GPH50***. It is possible to set the pin "vin" to static 0 or 1 by ***CPUIRQ2V***. In 144 package only, three pins (GP0...2) can be controlled individually by I²C commands (***GP0***, ***GP1***, ***GP2***).

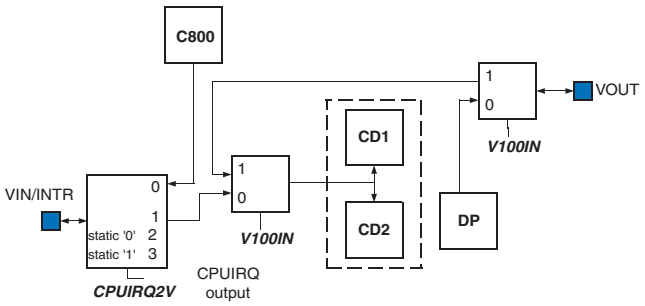


Fig. 2–68: VIN/INTR and VOUT switching

2.6.11. VSP 94xxB in PiP Operation Only

The IC can be used to produce a PiP only (PCE mode), which is synchronized to external H/V signals. This can be used i.e. to insert a PiP into a PC-signal which is directly connected to the RGB/deflection stage. For this, the vout-pin can be set to input by ***V100IN*** and hout to tristate by ***H100TR***. Additionally, the incoming H signal must be connected to any CVBS, GIN or FBLIN pins. The BLANK signal indicates the valid PiP picture in order to switch between the main-signal and the PiP in the backend.

2.6.12. Digital 656 Output

The output data format corresponds to ITU656 (8-bit bus at a data rate of 27 MHz).

Timing reference codes (SAV, EAV) are inserted according to the specification. The output can be enabled by ***DPOUT656***. The display clock should be set to linelocked-clock (***HOUTFR***) with 27 MHz (***PPLIP***) and 720 pixels per line (***HORWIDTHP***). 656 output data is available at pins 656io0...7. In QFP144 versions, 656 output is available at green output (dgout0...7) additionally. The clock output (pin 656clk) is CLKB72 always (usually 27 or 54 MHz) and can be inverted by ***CLK656OUTINV***.

2.6.13. Digital YUV/RGB Output

4:4:4 RGB as well as 4:4:4 and 4:2:2 YUV signals with either 8 or 9 bits are supported.

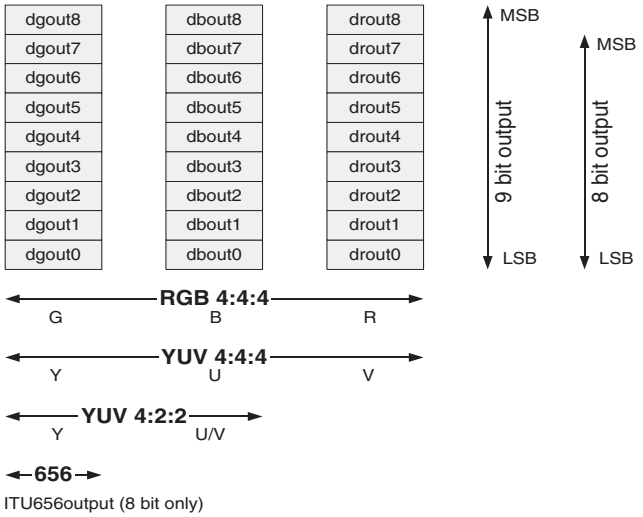


Fig. 2–69: Possibilities of digital output connections

Table 2–44: Digital output configuration in QFP144

		M422	DWO	TO1RGB	DPOUT656
RGB 4:4:4	8 bit	0	0	1	0
	9 bit	0	1	1	0
YUV 4:4:4	8 bit	0	0	0	0
	9 bit	0	1	0	0
YUV 4:2:2	8 bit	1	0	0	0
	9 bit	1	1	0	0
656	8 bit	x	x	x	1

2.7. Clock Concept

A single 20.25 MHz crystal at fundamental mode is used as clock reference. All other clocks are derived from this source. The CVBS frontend works with 20.25 MHz, the RGB frontend and input processing operates at 40.5 MHz, the oversampling DACs use 72.0 MHz and the memory and all parts behind the memory are clocked with 36 MHz.

Three different clock concepts are supported. The difference is the behavior in clocking the memory output. The frontend part of the VSP 94x5B uses a free-running but crystal-stable clock (CLKF). After deskewing, an orthogonal picture is written into the memory. The read out is done using the (CLKB) clock.

The horizontal sync-signal output (HOUT) is derived from a counter running with CLKB. The VOUT is directly derived from the input vertical signal, which is generated by the sync-separation block. This "H-freerunning-V-locked mode" is only possible together with a DC coupled deflection controller.

In "H-and-V-locked mode" CLKB is line-locked to the incoming signal. The freerunning YUV picture data and the internal H signal are converted to the line-locked domain. Now HOUT and the sync signal in the $1f_H$ domain are directly coupled.

In case of "H-and-V-freerunning mode" the HOUT and VOUT signals are derived from counters running with CLKB. There is no connection to the incoming signal. This mode can be used for stable pictures when no signal is applied (e.g. channel search with OSD insertion).

The clock output can be disabled by ***CLKOUTON. CLKOUTINV*** inverts the clock.

HOUT and VOUT are in line with the sampling clock CLKB27, CLKB36 or CLKB72. Even when clkout is not used in the system, ***CLKOUTSEL72***, ***CLKOUT72*** and ***CLKOUTSEL*** must be set properly to obtain correct HOUT, VOUT and BLANK signals.

Table 2–45: Clock output and hout/vout/blank clock reference

CLKOUT SEL72	CLKOUT 72	CLKOUT SEL	CLKOUT (HOUT, VOUT, BLANK derived from)
0	0	0	CLKB27
0	0	1	CLKB36
1	1	0	CLKB72

Table 2–46: Clock output and hout/vout clock reference clock system (FR=free-running; LL=line-locked)

Name	Clock	Nominal Frequency	H- and V-locked Mode	H-freerunning V-locked Mode	H- and V-freerunning Mode
CLKF20	CVBS frontend	20.25 MHz	FR	FR	FR
CLKF40	RGB frontend, input processing	40.5 MHz	FR	FR	FR
CLKB36	Output and display processing	9407: 36 MHz (analog out) 9417: 27 MHz (digital out) 9437: 18 MHz (analog out) 9447: 13.5 MHz (digital out)	LL	FR	FR
CLKB72	Oversampling, DAC	9407: 72 MHz 9417: 54 MHz 9437: 36 MHz 9447: 27 MHz	LL	FR	FR
CLKB27	Pins "clockout", "hout", "vout"	9407: 27 MHz 9417: 20.25 MHz 9437: 13.5 MHz 9447: 10.125 MHz	LL	FR	FR

2.7.1. Line-locked Clock Generator

The clock generation system derives all clocks from one 20.25 MHz crystal oscillator clock source. Line-locked horizontal sync pulses are generated by a digital phase locked loop. The time constant can be adjusted between fast and slow behavior (***KPL, KIL***) to accommodate different backend ICs. The PLL control can be frozen up to 15 lines before v-sync (***FION***) for a duration up to 15 lines (***FILE***). This may be used to reduce disturbances by h-phase errors which are produced by VCR's. The output frequency for the 100/120 Hz version dependent on ***IICINCR*** is

$$f_{display} = IICINC \cdot 103Hz$$

A freerunning frequency is also generated which may be selected alternatively. The freerunning frequency for the double-scan versions dependent on ***FRINC*** is

$$f_{displayfr} = FRINC \cdot 103Hz$$

Normally, ***IICINCR*** and ***FRINC*** are equal or nearly the same. The display frequency is internally divided by two for the single-scan versions.

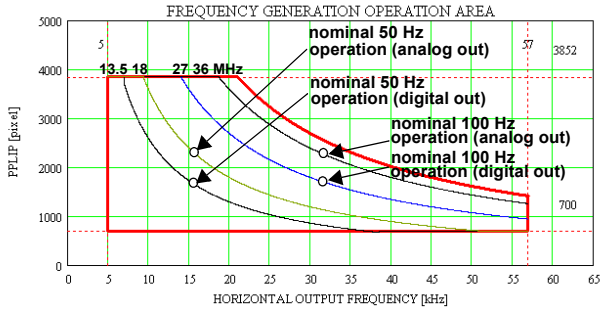


Fig. 2–70: Allowed operation area for clock generation

The number of pixels generated by the PLL is given by ***PPLIP***. For linelocked clock generation the following equation must be fulfilled:

$$PPLIP = PPLOP$$

Dependent on ARTSYNC and ITUSYNC, the LL-PLL input is different (see Table 2–47).

Table 2–47: LL-PLL input

ARTSYNC	ITUSYNC	LL_PLL Input
0	x	CD input (parallel operation)
1	0	CD output (serial operation)
1	1	ITU656 input

Table 2–48: LL-PLL settings

Operation	Input	PPLIP*4	PPLOP*4	IICINCR	FRINCR	CLKB36 [MHz]	f_H[kHz]
Double-scan (analog out)	50 Hz	2304	1152	349525	349525	36	31.250
	60 Hz				351953	36.25	31.468
Double-scan (digital out)	50 Hz	1728	864	262144	262144	27	31.250
	60 Hz				263892	27.18	31.468
Single-scan (analog out)	50 Hz	2304	1152	349525	349525	18	15.625
	60 Hz				351953	18.125	15.734
Single-scan (digital out)	50 Hz	1728	864	262144	262144	13.5	15.625
	60 Hz				263892	13.59	15.734

3. I²C Bus

3.1. I²C Bus Slave Address

When pin ADR/TDI is connected to Vss, VSP 94xxB reacts on first I²C address. The second address is active, when pin ADR/TDI is connected to Vdd.

Table 3–1: I²C slave address

Write Address	
10110000=**B0h**	ADR/TDI=0
10110010=**B2h**	ADR/TDI=1
Read Address	
10110001=**B1h**	ADR/TDI=0
10110011=**B3h**	ADR/TDI=1

3.2. I²C Bus Format

The VSP 94x7B I²C bus interface acts as a slave receiver and a slave transmitter and provides two different access modes (write, read). All modes run with a subaddress auto increment. The interface supports the normal 100 kHz transmission speed as well as the high speed 400 kHz transmission. VSP 94x7B has 16 bit I²C registers only. The two bytes per register are referred as Byte_A and Byte_B. They are either read_only or write_only registers. Byte A is the higher byte and is transmitted first. It is always transmitted if the register is addressed. Byte B is the lower byte. It need not be transmitted if only byte A is of interest. Byte A has always to be transmitted before byte B can be accessed. All read and write registers are auto increment registers. However, the auto increment function can be disabled by the control bit ***AUTOINC_OFF*** in register DAh. If the auto increment function is switched off, the bytes A and B of write registers will be updated (overwritten) cyclically every second data byte. The bytes A and B of read registers will be polled cyclically every second byte.

Table 3–2: 16 bit I²C format

A7, A6, A5, A4, A3, A2, A1, A0	**B7, B6, B5, B4, B3, B2, B1, B0**
Byte_A: MSB	Byte_B: LSB

Table 3–3: Index of I²C abbreviations

S	START
A	ACKNOWLEDGE
SAW	SLAVE ADDRESS WRITE
SAR	SLAVE ADDRESS READ
SBR	SUBADDRESS
D_A	DATA BYTE A
D_B	DATA BYTE B
STP	STOP

Table 3–4: Write sequence examples

S	SAW	A	SBR	A	D_A	A	STP					
S	SAW	A	SBR	A	D_A	A	D_B	A	STP			
S	SAW	A	SBR	A	D_A	A	D_B	A	D_A	...	A	STP

Table 3–5: Read sequence examples

S	SAW	A	SBR	A	S	SAR	A	D_A	NA	STP				
S	SAW	A	SBR	A	S	SAR	A	D_A	A	D_B	NA	STP		
S	SAW	A	SBR	A	S	SAR	A	D_A	A	D_B	A	D_A	...	NA	STP

The transmitted data is internally stored in registers. The registers are located in different clock and functional domains. The clock domains can be found in Table 3–6.

Table 3–6: I²C bus clock domains

Domain	Description	Clock
CP1	CVBS frontend Master	CLKF20
IP1	Input Processing Master	CLKF40
DP1	Display Processing Master	CLKB3, CLKB72
OP1	Output Processing Master	CLKB36
CP2	CVBS frontend Slave	CLKF20
FP	RGB processing	CLKF40
IP2	Input Processing Slave	CLKF40
DP2	Display Processing Slave	CLKB36
OP2	Output Processing Slave	CLKB36
ITU	ITU656 processing	CLKF27, CLKF40
PP	LL-PLL	CLKF36
C800	C800	CLKF40
MEM	Memory Controller	CLKB36
MAUS	Motion adaptive upconversion	CLKB36
ODC	Output Data Controller	CLKB36

3.3. Modification of I²C Write Registers

Modified register data becomes effective

– After being activated by a store command (nearly all registers).

– In some cases immediately after writing, if the register is marked by "NTO" (=no take over mechanism)

There are two types of store commands:

– Immediately after store command specified for this register domains (FEh)

Table 3–7: Store Commands

S	SAW	A	'FEh'	A	***IM***_high	A	***IM***_low	A	STP

– At the next rising edge of the V-sync signal specified for this register domains (FFh)

Both store commands should not be used in the same I²C telegram.

Table 3–8: Store Commands

S	SAW	A	'FFh'	A	***VS***_high	A	***VS***_low	A	STP

The registers are grouped into update-domains. The update of each domain must be enabled by setting the corresponding bit in the store command word.

The update domain, where the data are made valid with the V-sync signal of the 20.25 MHz domain are indicated in the register overview by ***VS1_20*** or ***VS2_20*** respectively.

The others update domains are called ***VSM1_40***, ***VSM2_40***, ***VSS1_40***, ***VSS2_40***, ***VSRGB_40***, ***VSBM1_36***, ***VSBM2_36***, ***VSBS_36***, ***VSDCI_36*** and ***VS656_27***.

For immediate update (no wait for V-sync), ***IM1_20, IM2_20, IMM1_40***, ***IMM2_40***, ***IMS1_40***, ***IMS2_40***, ***IMRGB_40***, ***IMBM1_36***, ***IMBM2_36***, ***IMBS_36***, ***IMDCI_36*** and ***IM656_27*** can be used.

The update status of the registers can be checked by read register F7h.

The I²C parameter ***VS1_20stat***, ***VS2_20stat***, ***VSM1_40stat***, ***VSM2_40stat***, ***VSS1_40stat***, ***VSS2_40stat***, ***VSRGB_40stat***, ***VSBM1_36stat***, ***VSBM2_36stat***, ***VSBS_36stat***, ***VSDCI_36stat*** **and** ***VS656_27stat*** reflect the state of the register values. If these bits are read as 1, then the store command was sent, but the data is not made available yet. If these bits are 0, then the data was made valid and a new write or read cycle can start. These registers may be checked before writing or reading new data, otherwise data can be lost if different data is written too fast to a register.

Table 3–9: I²C bus register types

Register Types	
W	Write register
R	Read register
Rrstyp	Reset register after reading
HS	Hand-shake mechanism

Table 3–10: I²C bus register characterization

Take-over Mechanism		
NTO	No take-over mechanism	
VS1_20	CVBS frontend master	Take-over with V-sync in 20 MHz domain
VS2_20	CVBS frontend slave	
VSSLI_20	Data slicer	
VSRGB_40	RGB frontend	Take-over with V-sync in 40 MHz domain
VSM1_40	Input processing master before V-scaler	
VSM2_40	Input processing master behind V-scaler	
VSS1_40	Input processing slave before V-scaler	
VSS2_40	Input processing slave behind V-scaler	
VSBM1_36	Master behind memory	Take-over with V-sync in backend 36.0 MHz domain
VSBM2_36	Master behind v-scaler	
VSBS_36	Slave behind memory	
VS656_27	ITU656 input / ITU656 output	Take-over with V-sync in 27.0 MHz domain

3.4. Update of I²C Read Registers

The read process does not make use of store commands.

The update of read register data is done

– By the sync signals as described for the write registers, but the direction of the data flow is opposite ("normal" read registers). The update status of the registers can be checked by read register F7h.
– Immediately (NTO read registers)
– With reset after read (RS read registers)

RS type registers behave like a RS flip flops. Whenever the corresponding signal has a high level it sets the register bit to "1". After being read by the I²C bus master, the whole register will be automatically reset (means value 0) .

For example the register ***NMSTATUSM*** belongs to the “rs typ” read registers. ***NMSTATUSM*** signalizes a new value for ***NOISEMEM***. So if ***NMSTATUSM*** is read as 0 the current noise measurement has not been updated. If the ***NMSTATUSM*** is read as 1 a new noise measurement value can be read. All other “rs typ” read registers work in the same way. The “rs typ” read registers will be marked in the overview with the short cut “rstyp” or will have the additional hint “**Note**: reset automatically when read/write” in the detailed I²C bus command description.

Registers which need a hand-shake mechanism between the I²C bus interface and the different blocks are marked with the shortcut HS (Hand shake mechanism). This means that all bits of the registers are used when the last register is written. After ***IICINCR18-3*** is written, ***IICINCR2-0*** must be written to allow these bits to have effect.

The registers for the write parameter ***RMODE*** are directly connected to the read registers of the parameter ***RMMIRROR***. So it is possible to check the I²C bus protocol by writing and reading to the register ***RMODE*** and ***RMMIRROR***, respectively.

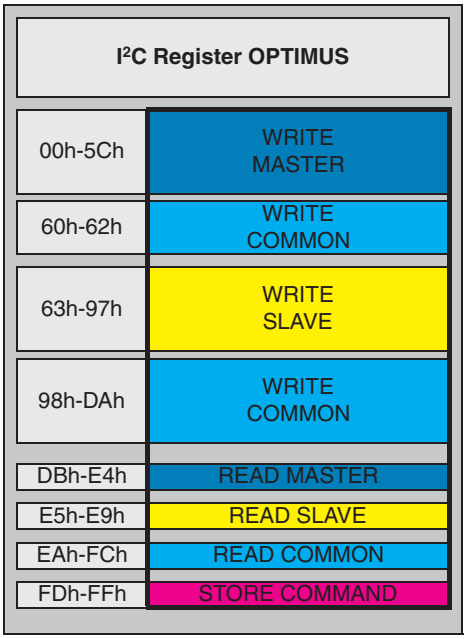


Fig. 3–1: I²C bus address overview

3.5. Miscellaneous

After switching on the IC, all bits of the VSP 94x2A are set to defined states.

POR is set after reset to pin 24. It stays 1, until it is canceled via software ***PORCNCL***. This can be used to detect a reset on pin 24. During TV operation, it can be used to decide whether to program all registers (e.g. after power failure reset) or only altered ones (normal TV operation).

Writing to or reading from a non -existent register is permitted but does not generate a fault by the IC.

Two counters (0...15) are available, which are incremented with every vertical pulse of input processing master (***FCIM***) or output processing master (***FCBM***). They can be used for software synchronization.

3.6. Important Hints

The signal ***FJMODE*** can be found in 57h and 5Eh (same position). Do always write the same values to ***FJMODE*** in 57h and ***FJMODE*** in 5Eh.

The signal ***LPFOPOFF*** can be found in BBh and BFh (different position). Do always write the same values to ***LPFOPOFF*** in BBh and ***LPFOPOFF*** in BFh.

3.7. I²C Bus List in Alphabetical Order

Table 3–11: I²C bus list in alphabetical order

Name	Address
656BLANK	9Ch
AABYP	A7h
AASEL	A4h
AB_FTCM	4Eh
ACCFIXM	01h
ACCFIXS	65h
ACCFRZM	01h
ACCFRZS	65h
ACCLIMM	0Eh
ACCLIMS	72h
ADATA0	F9h
ADATA1	F9h
ADATA2	FAh
ADATA3	FAh
ADATA4	FBh
ADATA5	FBh
ADATA6	FCh
ADATA7	FCh
ADCSEL	A7h
ADINS	9Fh
ADLCKCCM	0Fh
ADLCKCCS	73h
ADLCKM	0Fh
ADLCKS	73h
ADLCKSELM	0Fh
ADLCKSELS	73h
ADLINE	9Fh
ADR_RDY	F7h
AFPROC	C1h
AGCADJ1M	0Bh
AGCADJ1S	6Fh
AGCADJ2M	0Ch
AGCADJ2S	70h
AGCADJB	A8h
AGCADJCV1	DDh
AGCADJCV2	E7h
AGCADJF	A9h
AGCADJG	A9h
AGCADJR	A8h
AGCFRZEM	0Ch
AGCFRZES	70h
AGCMDM	0Bh
AGCMDS	6Fh
AGCPWRESM	5Fh
AGCPWRESS	63h
AGCRESM	0Ch
AGCRESS	70h
AGCTHDM	5Fh
AGCTHDS	63h
ALPFIPI	A2h
ALPFIPM	26h
ALPFIPS	88h
AMMON	2Dh
AMSTD50M	5Fh
AMSTD50S	63h
AMSTD60M	5Fh
AMSTD60S	5Fh63h
APENSELM	22h
APENSELS	84h
APK1BPM	49h
APK1BPS	95h

Table 3–11: I²C bus list in alphabetical order

Table 3–11: I²C bus list in alphabetical order

Name	Address
APK1HPM	4Ah
APK1HPS	96h
APK2BPM	49h
APK2BPS	95h
APK2HPM	4Ah
APK2HPS	96h
APPLIPI	A1h
APPLIPM	23h
APPLIPS	85h
ARSDIS	BFh
ARTSYNC	3Fh
ATH1BPM	49h
ATH1BPS	95h
ATH1HPM	4Ah
ATH1HPS	96h
ATH2BPM	49h
ATH2BPS	95h
ATH2HPM	4Ah
ATH2HPS	96h
AUTOFRRN	45h
AUTOGAP	20h
AUTOINC_OFF	DAh
BELLFIRM	11h
BELLFIRS	75h
BELLIIRM	11h
BELLIIRS	75h
BGPOSM	12h
BGPOSS	76h
BGSHIFTM	60h
BGSHIFTS	63h
BLANDEL	D4h

Table 3–11: I²C bus list in alphabetical order

Name	Address
BLANLEN	D5h
BLANPOL	D4h
BLUESEL	AAh
BLUETWO	AAh
BRTADJ	A4h
C1	C2h/C5h
C2	C2h/C5h
C3	C3h/C5h
C4	C3h/C5h
C5	C4h/C5h
C6	C4h/C5h
C800	D9h
C800	FDh
CDELHPOSM	33h
CDELHPOSS	8Ah
CFORMAT	A3h
CHRFM	04h
CHRFS	68h
CHROMAMP	C9h
CHROMSIGN656	C1h
CHRSFM	C1h
CHRSFR	A4h
CKILLM	05h
CKILLS	69h
CKILLSM	06h
CKILLSS	6Ah
CKSTATM	DCh
CKSTATS	E6h
CLK656OUT	9Eh
CLK656OUTINV	C1h
CLKF2PAD	A5h

Table 3–11: I²C bus list in alphabetical order

Name	Address
CLKOUT72	D4h
CLKOUTINV	D4h
CLKOUTON	D4h
CLKOUTSEL	D4h
CLKOUTSEL72	D5h
CLKT1	ACh
CLMPD1M	01h
CLMPD1S	65h
CLMPD1SM	0Fh
CLMPD1SS	73h
CLMPD2M	02h
CLMPD2S	66h
CLMPD2SM	0Fh
CLMPD2SS	73h
CLMPHIGHM	0Dh
CLMPHIGHS	71h
CLMPLOWM	0Eh
CLMPLOWS	72h
CLMPSIG1	98h
CLMPSIG2	98h
CLMPST1M	03h
CLMPST1S	67h
CLMPST1SM	0Ch
CLMPST1SS	70h
CLMPST2M	04h
CLMPST2S	68h
CLMPST2SM	0Dh
CLMPST2SS	71h
CLMPVG	A7h
CLMPVRB	A8h
CLPSTGYM	01h

Table 3–11: I²C bus list in alphabetical order

Name	Address
CLPSTGYS	65h
CLRANGEM	12h
CLRANGES	76h
COARSEDEL	D8h
COLONM	01h
COLONS	65h
COMBM	05h
COMBS	69h
COMBUSEM	02h
COMBUSES	66h
CONADJ	A4h
CONM	02h
CONS	66h
CONSM	01h
CONSS	65h
COR	9Ah
CORONM	4Ah
CORONS	96h
CPLLOFM	01h
CPLLOFS	65h
CPLLRESM	0Ch
CPLLRESS	70h
CPUDISABLE	DAh
CPUIRQ2V	DAh
CRCBM	03h
CRCBS	67h
CSC_ONM	4Ch
CSTANDM	05h
CSTANDS	69h
CVBOSEL1	99h
CVBOSEL2	99h

Table 3–11: I²C bus list in alphabetical order

Name	Address
CVBOSEL3	99h
CVBSEL1	98h
CVBSEL2	98h
DATA_CCWSS1	EAh
DATA_CCWSS2	EAh
DATA_USWSS1	ECh
DATA_USWSS2	EBh
DATA_USWSS3	EBh
DATAVCCWSS	ECh
DATAVUSWSS	ECh
DBDHPOSM	33h
DBDHPOSS	8Ah
DBDPICIM	4Ah
DBDPICIS	96h
DC	9Ah
DCI_CORM	4Dh
DCIONM	4Ch
DCLMPF	A7h
DCR	9Ah
DDR	9Ah
DDR_CC	60h
DEC2	A5h
DEEMPFIRM	10h
DEEMPFIRS	74h
DEEMPIIRM	10h
DEEMPIIRS	74h
DEEMPSTDM	11h
DEEMPSTDS	75h
DETHPOLM	DCh
DETHPOLS	E6h
DETVPOLM	DCh

Table 3–11: I²C bus list in alphabetical order

Name	Address
DETVPOLS	E6h
DIGOUTEN	C1h
DISALLRESM	07h
DISALLRESS	6Bh
DISCHCHM	01h
DISCHCHS	65h
DISCOMB	9Bh
DISPMODE	BFh
DISRES	ACh
DPBRT	42h
DPCON	42h
DPOUT656	C1h
DPUSAT	83h
DPVSAT	82h
DSFTCM	50h
DT	9Ah
DTFDT	2Eh
DWO	C1h
DYNOPFJGM	58h
DYNOPFJGS	58h
DYNOPFJN0	59h
DYNOPFJN1	59h
DYNOPFJN2	5Ah
DYNOPFJN3	5Ah
DYNOPFJN4	5Bh
DYNOPFJP0	55h
DYNOPFJP1	5Bh
DYNOPFJV	55h
DYNOPITGM	58h
DYNOPITGS	58h
DYNOPITN0	59h

Table 3–11: I²C bus list in alphabetical order

Name	Address
DYNOPITN1	59h
DYNOPITN2	5Ah
DYNOPITN3	5Ah
DYNOPITN4	5Bh
DYNOPITP0	55h
DYNOPITP1	5Bh
DYNOPITV	55h
DYNOPLSGM	56h
DYNOPLSGS	56h
DYNOPLSN	57h
DYNOPLSP0	56h
DYNOPLSP1	56h
DYNOPLSV	56h
DYNOPMSGM	58h
DYNOPMSGS	58h
DYNOPMSN0	59h
DYNOPMSN1	59h
DYNOPMSN2	5Ah
DYNOPMSN3	5Ah
DYNOPMSN4	5Bh
DYNOPMSP0	55h
DYNOPMSP1	5Bh
DYNOPMSV	55h
DYNOPSMGM	58h
DYNOPSMGS	58h
DYNOPSMN0	59h
DYNOPSMN1	59h
DYNOPSMN2	5Ah
DYNOPSMN3	5Ah
DYNOPSMN4	5Bh
DYNOPSMP0	55h

Table 3–11: I²C bus list in alphabetical order

Name	Address
DYNOPSMP1	5Bh
DYNOPSMV	55h
DYTCM	51h
EIA770M	0Fh
EIA770S	73h
ELINEM	4Dh
EN_656	A3h
ENA_DEMOM	4Ch
ENLIMM	11h
ENLIMS	75h
EPIXELM	4Ch
ERRORCMPM	51h
EXTRD	C0h
F_OFFS	9Fh
F2F1F0	9Ah
FBLACTIVE	EDh
FBLCONF	A6h
FBLDEL	A5h
FBLOFFST	AAh
FEMAGM	19h
FEMAGS	7Bh
FETHD	B2h
FHDETM	02h
FHDETS	66h
FHFRRNM	06h
FHFRRNS	6Ah
FIELDBINV	45h
FILE	ACh
FILMMODEM	DFh
FINEDEL	D8h
FIOFFOFF	C1h

Table 3–11: I²C bus list in alphabetical order

Name	Address
FION	AEh
FJMODE	57h/5Eh
FJSELLNV	54h
FKOI	AFh
FKOIHYS	AFh
FLDINVM	01h
FLDINVS	65h
FLINEM	01h
FLINES	65h
FLNSTRDM	11h
FLNSTRDS	75h
FMATH	2Ch
FMDCTH	2Bh
FMDSON	2Bh
FMDTH	2Ch
FMFORCE	57h
FMFORCETRIG	57h
FMMEMHIS	2Ch
FMOD	ADh
FMODE	BDh
FMOTREGM	E0h
FMREGION	2Bh
FMRES	2Bh
FMSCALEL	2Bh
FMSCALEU	2Bh
FMSTATUSM	E2h
FMSYN	14h
FMSYNUNS	14h
FMTHRON	2Bh
FMTHYON	2Bh
FPOL	9Fh

Table 3–11: I²C bus list in alphabetical order

Name	Address
FRAFION	2Fh
FRAMEDIMM	D2h
FRAMEDIMS	D2h
FRCBGNDM	21h
FRCBGNDS	83h
FRCMMODM	22h
FRCMMODS	84h
FREEZE_ANLM	4Dh
FREEZEM	13h
FREEZES	77h
FREQSELL	AFh
FRFIX	5Dh
FRINC	5Dh
FRZLIMLR	5Eh
FSWFTL	C1h
GAINSEG1FRCM	E3h
GAINSEG2FRCM	E4h
GAPM	32h
GCMON	5Ch
GFBON	BDh
GMAMM	29h
GMASM	28h
GMDSTATUSM	E2h
GMFMFBENA	54h
GMOTIONM	E1h
GMOTREGM	E1h
GMSTEN	29h
GMSTSL	29h
GMSTSS	28h
GMSTTH	28h/29h
GMSTTHV	21h

Table 3–11: I²C bus list in alphabetical order

Name	Address
GMTHLM	29h
GMTHUM	28h
GOFST	A5h
GPH50	DAh
GPP0	20h
GPP1	24h
GPP2	24h
GRADELAA	F5h
GRADISSTABLE	F3h
GRADSLAA	F2h
GSFMFBENA	54h
GSTHLM	2Ah
GSTHUM	2Ah
GSTILLENA	54h
GSTILLM	E1h
H50SKEW	5Fh
HAAPRESCM	23h
HAAPRESCS	85h
HDCPRESCM	23h
HDCPRESCS	85h
HDG	99h
HDTOTEST	ACh
HINC0M	34h
HINC0S	8Bh
HINC1M	35h
HINC1S	8Ch
HINC2M	36h
HINC2S	8Dh
HINC3M	37h
HINC3S	8Eh
HINC4M	38h

Table 3–11: I²C bus list in alphabetical order

Name	Address
HINC4S	8Fh
HINCR_EXT	ADh
HINPM	03h
HINPS	67h
HORFRAMEF	CBh
HORFRAMEG	D0h
HOROFFS	91h/92h
HORPOSF	CAh
HORPOSG	CEh
HORPOSM	45h
HORPOSNM	27h
HORPOSP	C6h
HORPOSS	91h
HORWIDTHF	CBh
HORWIDTHG	CFh
HORWIDTHM	47h
HORWIDTHNM	27h
HORWIDTHP	C7h
HORWIDTHS	93h
HOUTDEL	BCh
HOUTFR	BCh
HOUTPOL	D4h
HOUTTR	C1h
HPANONM	33h
HPANONS	8Ah
HPE1OFF	C0h
HPE2OFF	C0h
HPEXOFF	C0h
HPOL	A3h
HPOLM	02h
HPOLS	66h

Table 3–11: I²C bus list in alphabetical order

Name	Address
HPS1OFF	C0h
HPS2OFF	C0h
HRES	AEh
HSCPOSCM	33h
HSCPOSCS	8Ah
HSCPRESCM	22h
HSCPRESCS	84h
HSEG1M	34h/35h
HSEG1S	8Bh/8Ch
HSEG2M	36h/37h
HSEG2S	8Dh/8Eh
HSEG3M	38h/39h
HSEG3S	8Fh/90h
HSEG4M	39h
HSEG4S	90h
HSPPL	61h
HSWIN	ADh
HTESTW	ADh
HUEM	08h
HUES	6Ch
HWID	AEh
IFCOMPM	0Eh
IFCOMPS	72h
IFCOMPSTRM	0Eh
IFCOMPSTRS	72h
IICINCR	ABh/ACh
IM1_20	FEh
IM2_20	FEh
IM656_27	FEh
IMBM1_36	FEh
IMBM2_36	FEh

Table 3–11: I²C bus list in alphabetical order

Name	Address
IMBS_36	FEh
IMDCI_36	FEh
IMM1_40	FEh
IMM2_40	FEh
IMODE	9Fh
IMRGB_40	FEh
IMS1_40	FEh
IMS2_40	FEh
IMSLI_20	FEh
INCOMB	9Ch
INCOMBC	5Fh
INITLINESEL	57h
INTM	DCh
INTPROGM	13h
INTPROGS	77h
INTS	E6h
INVSKEW	3Fh
IRQCON	9Ch
ISHFTM	11h
ISHFTS	75h
ITUPRTSEL	A3h
ITUSYNC	3Fh
JLCRES	BFh
KD2	ADh
KIL	AFh
KINL	B1h
KOIH	ADh
KOIWID	ADh
KPL	B1h
KPNL	B1h
LB43SENS	B4h

Table 3–11: I²C bus list in alphabetical order

Name	Address
LBACTIVITY	BAh
LBASDEL	BAh
LBELAA	F4h
LBFORMAT	F3h
LBFS	B8h
LBGFBDEL	B9h
LBGRADDET	B5h
LBGRADRST	B4h
LBGSDEL	B9h
LBHISTBLA	B7h
LBHIWHITE	B6h
LBHSDEL	B4h
LBHWEND	B6h
LBHWST	B7h
LBMASLA	B8h
LBNGFEN	B4h
LBSLAA	F4h
LBSTABILITY	B4h
LBSTATUS	E2h
LBSUB	B4h
LBSUBTITLE	F3h
LBTHDNBNG	BAh
LBTHDNBNHA	B4h
LBTOPTITLE	F3h
LBVISUON	BAh
LBVWENDLO	B5h
LBVWENDUP	B8h
LBVWSTLO	B8h
LBVWSTUP	B9h
LIMEN	B3h
LIMHI	ACh

Table 3–11: I²C bus list in alphabetical order

Name	Address
LIMII	B2h
LIMIP	B0h
LIMLR	AFh
LINLENH50	9Bh
LINLENH60	9Bh
LMOFSTM	03h
LMOFSTS	67h
LNL	ACh
LNSTDRDM	DCh
LNSTDRDS	E6h
LOCKSPM	0Fh
LOCKSPS	73h
LPBLACK	F3h
LPCDELM	07h
LPCDELS	6Bh
LPFIPI	A0h
LPFIPMD	45h
LPFLDM	DBh
LPFLDS	E5h
LPFOP	BDh/BEh
LPFOPOFF	BBh/BFh
LPPOSTM	01h
LPPOSTS	65h
LPWHITE	F3h
LSWFM	4Fh
LTIM	49h
LTIS	95h
LUMAMP	C8h
M422	C1h
MASLEX	BFh
MASTERON	BDh

Table 3–11: I²C bus list in alphabetical order

Name	Address
MAXALC	F0h/F1h
MAXAUC	F2h
MAXGLC	EFh
MAXGUC	EEh
MAXHLC	F1h
MAXHUC	F0h
MDVFFON	2Bh
MIXGAIN	A5h
MIXOP	A8h
MOTONM	24h
MOTONS	86h
MOTVALON	BFh
MPFBLBM	1Fh
MPFBLBS	81h
MPFBLTM	20h
MPFBLTS	82h
MPFBPLM	21h
MPFBPLS	83h
MPFBPRM	20h
MPFBPRS	82h
MVCHOLD	54h
MVCOFA0	53h
MVCOFA1	53h
MVCOFP0	53h
MVCOFP1	53h
MVDIVA	53h
MVDIVP	53h
MVDIVR	53h
MVFIXENA	54h
MVFIXVAL	54h
MVMODE	54h

Table 3–11: I²C bus list in alphabetical order

Name	Address
MVPGM	60h
MVPGS	63h
MVPM	60h
MVPS	63h
MVREFPOS	54h
MVVISENA	54h
NALPFIPI	A1h
NALPFIPM	25h
NALPFIPS	87h
NAPIPPHI	9Fh
NAPPLIPI	A2h
NAPPLIPM	24h
NAPPLIPS	86h
NAPPLOP	BBh
NEGLINESEL	57h
NMCHAN	20h
NMLINEM	18h
NMLINES	7Ah
NMPOSM	18h
NMPOSS	7Ah
NMSENSEM	18h
NMSENSES	7Ah
NMSTATUSM	E2h
NMSTATUSS	E9h
NOFHSYNC	48h
NOGRADFOUND	F3h
NOISE	DEh
NOISEMEM	DEh
NOISEMES	E8h
NOISESTATUS	E2h
NOSEL	9Ah

Table 3–11: I²C bus list in alphabetical order

Name	Address
NOSIGBM	03h
NOSIGBS	67h
NOSYNC	BCh
NOTCHOFFM	11h
NOTCHOFFS	75h
NRONM	19h
NRONS	7Bh
NRPIXELM	DBh
NRPIXELS	E5h
NSHAP	C1h
NSREDM	07h
NSREDS	6Bh
NTCHSELM	12h
NTCHSELS	76h
NTSCREFM	09h
NTSCREFS	6Dh
OBSOFT	D2h
OBTEMP	D2h
OFFSET	32h
OMODE	9Eh
OPDEL	BCh/BEh
OPPHASEFR	56h
OSCPD	AFh
P3DIS	C0h
P4DIS	C0h
PALDELM	12h
PALDELS	76h
PALDETIDLM	3Fh
PALDETIDLS	46h
PALDETM	DDh
PALDETS	E7h

Table 3–11: I²C bus list in alphabetical order

Name	Address
PALIDL0M	0Ah
PALIDL0S	6Eh
PALIDL1M	09h
PALIDL1S	6Dh
PALIDL2M	12h
PALIDL2S	76h
PALIDM	DCh
PALIDS	E6h
PALINC1M	12h
PALINC1S	76h
PALINC2M	12h
PALINC2S	76h
PALREFM	0Ah
PALREFS	6Eh
PATTMODE	D2h
PB	EDh
PDGSR	BDh
PEAK_SIZEM	52h
PFBL	EDh
PG	EDh
PIXELPLINEM	4Eh
PIXPLINM	13h
PIXPLINS	77h
PK_FTCM	52h
PKCTIBPM	49h
PKCTIBPS	95h
PKCTIHPM	49h
PKCTIHPS	95h
PKLU	D7h
PKLV	D8h
PKLY	D7h

Table 3–11: I²C bus list in alphabetical order

Name	Address
PLLTCM	04h
PLLTCS	68h
POR	ECh
PORCNCL	9Bh
PPLIP	AEh
PPLIPI	9Eh
PPLOFF	BBh
PPLOP	BDh
PR	EDh
PRIOC	D3h
PRIOF	D3h
PRIOG	D3h
PRIOM	D3h
PRIOP	D2h
PRIOS	D3h
PWTHDM	03h
PWTHDS	67h
RBOFST	A9h
RDPNTOFF	16h
RDPOSXM	16h
RDPOSXS	79h
RDPOSYM	17h
RDPOSYS	79h
READM	16h
READM2S	77h
READS	79h
REFRON	BFh
REFRPER	BFh
REFTRIM	9Dh
REFTRIMCV	9Dh
REFTRIMCVRD	62h

Table 3–11: I²C bus list in alphabetical order

Name	Address
REFTRIMEN	9Bh
REFTRIMRD	62h
REFTRIMRGB	9Dh
REFTRIMRGBRD	62h
REMDEL1	60h
REMDEL2	60h
RESETPC1	9Bh
RESETPC2	9Bh
RESMODE	9Bh
REV	F6h
RGBSEL	A6h
RMMIRROR	F6h
RMODE	BCh
RSHIFTM	17h
RSHIFTS	17h
SATNRM	07h
SATNRS	6Bh
SCADJM	0Bh
SCADJS	6Fh
SCAN_IDM	4Ch
SCDEVM	DCh
SCDEVS	E6h
SCMIDLM	0Dh
SCMIDLS	71h
SCMRELM	10h
SCMRELS	74h
SCOUTENM	DCh
SCOUTENS	E6h
SDBM	19h
SDBS	7Bh
SDRM	19h

Table 3–11: I²C bus list in alphabetical order

Name	Address
SDRS	7Bh
SECACCLM	0Eh
SECACCLS	72h
SECACCM	10h
SECACCS	74h
SECDELM	3Fh
SECDELS	46h
SECDIVM	10h
SECDIVS	74h
SECINC1M	10h
SECINC1S	74h
SECINC2M	10h
SECINC2S	74h
SECNTCHM	02h
SECNTCHS	66h
SELCOMB	9Bh
SELMASTER	AAh
SELSLAVE	AAh
SELSM	AAh
SENSBSM	50h
SENSITIVM	32h
SENSWSM	4Fh
SERVICE	9Ch
SETSTABLL	ADh
SHAPERDIS	AFh
SHIFTACT	F8h
SHIFTUV	C1h
SKEWSEL	A9h
SLAVEON	BDh
SLFLDCCWSS	ECh
SLFLDUSWSS	ECh

Table 3–11: I²C bus list in alphabetical order

Name	Address
SLINEM	4Dh
SLLTHDM	0Bh
SLLTHDS	6Fh
SLLTHDVM	11h
SLLTHDVPM	0Fh
SLLTHDVPS	73h
SLLTHDVS	75h
SLLWIN	B2h
SLNCW	60h
SLNRUW	60h
SLOWVAR	20h
SLS	F6h
SLSRC	9Ch
SMMODE	54h
SMOP	AAh
SPIXELM	4Ch
STABLL	F6h
STABM	DDh
STABS	E7h
STANDBYCV	A5h
STANDBYDAC	15h
STANDBYRGB	A5h
STATOPMSC	57h
STATOPMSCENA	57h
STATSIZE	DFh
STDETM	DCh
STDETS	E6h
STOPMOS	C0h
SUBTITLE	F3h
SVALFI	2Dh
SVALFR	2Dh

Table 3–11: I²C bus list in alphabetical order

Name	Address
SVALLI	2Fh
SWGM	2Dh
SWITCHTO43	F3h
SYNCFTHDM	00h
SYNCFTHDS	64h
SYNCGAINM	5Fh
SYNCGAINS	63h
SYNCOMB	9Ah
TBLEND	D2h
TFDPPM	E3h/E4h
TFDT	2Dh
TFLDDON	2Dh
TFON	2Eh
THEM	49h
THES	95h
THFI0	2Eh
THFI1	2Fh
THFI2	30h
THFI3	31h
THFR0	2Eh
THFR1	2Fh
THFR2	30h
THFR3	31h
THLI0	2Fh
THLI1	30h
THLI2	31h
THRGM	2Dh
THRMOV	2Eh
THRSELM	07h
THRSELS	6Bh
TINT	15h

Table 3–11: I²C bus list in alphabetical order

Name	Address
TNOTCHOFFM	12h
TNOTCHOFFS	76h
TNRABSM	19h
TNRABSS	7Bh
TNRCLCM	1Eh
TNRCLCS	80h
TNRCLYM	1Eh
TNRCLYS	80h
TNRCS0M	1Ch
TNRCS0S	7Eh
TNRCS1M	1Ch
TNRCS1S	7Eh
TNRCS2M	1Ch
TNRCS2S	7Eh
TNRCS3M	1Ch
TNRCS3S	7Eh
TNRCS4M	1Dh
TNRCS4S	7Fh
TNRCS5M	1Dh
TNRCS5S	7Fh
TNRCS6M	1Dh
TNRCS6S	7Fh
TNRCS7M	1Dh
TNRCS7S	7Fh
TNRCSSM	1Eh
TNRCSSS	80h
TNRMD4YM	19h
TNRNR4CM	19h
TNRNR4YM	19h
TNRNR4YS	7Bh
TNRSELM	19h

Table 3–11: I²C bus list in alphabetical order

Name	Address
TNRSELS	7Bh
TNRYS0M	1Ah
TNRYS0S	7Ch
TNRYS1M	1Ah
TNRYS1S	7Ch
TNRYS2M	1Ah
TNRYS2S	7Ch
TNRYS3M	1Ah
TNRYS3S	7Ch
TNRYS4M	1Bh
TNRYS4S	7Dh
TNRYS5M	1Bh
TNRYS5S	7Dh
TNRYS6M	1Bh
TNRYS6S	7Dh
TNRYS7M	1Bh
TNRYS7S	7Dh
TNRYSSM	1Eh
TNRYSSS	80h
TO1RGB	C5h
TOPTITLE	F3h
TRAPBLUM	12h
TRAPBLUS	76h
TRAPREDM	12h
TRAPREDS	76h
TSTSHABRI	AFh
TVMODE	ECh
UBAGR	CEh
UBORDERM	1Fh
UBORDERS	81h
UCUR	C9h

Table 3–11: I²C bus list in alphabetical order

Name	Address
UENINV	C5h
UFRAMEM	4Bh
UFRAMES	97h
UPBLACK	F3h
UPDATERATEM	20h
UPDATESS	14h
UPWHITE	F3h
USATADJ	A7h
UVCODE	C1h
UVCORM	02h
UVCORS	66h
UVDEL	A6h
V100IN	C1h
V50BLANK	9Bh
V656DEL	C1h
VAAPRESCM	25h
VAAPRESCS	87h
VBAGR	CFh
VBLANDEL	D5h/D6h
VBLANLEN	D6h
VBLANPOL	D4h
VBORDERM	1Fh
VBORDERS	81h
VCRDETHD	98h
VCRPRESCM	25h
VCRPRESCS	87h
VCUR	CAh
VDCPRESCM	26h
VDCPRESCS	88h
VDELAY_BE	DAh
VDETIFSM	0Fh

Table 3–11: I²C bus list in alphabetical order

Name	Address
VDETIFSS	73h
VDETITCM	10h
VDETITCS	74h
VDG	99h
VDOUBLEM	3Ah
VERFRAMEF	CCh
VERFRAMEG	D1h
VEROFFS	94h
VERPOSF	CCh
VERPOSG	D0h
VERPOSM	46h
VERPOSP	C8h
VERPOSS	92h
VERRESM	13h
VERRESS	77h
VERSION	F6h
VERWIDTHF	CDh
VERWIDTHG	D1h
VERWIDTHM	48h
VERWIDTHP	C9h
VERWIDTHS	94h
VFLYMDM	DDh
VFLYMDS	E7h
VFLYWHLM	0Ch
VFLYWHLMDM	04h
VFLYWHLMDS	68h
VFLYWHLS	70h
VFRAMEM	4Bh
VFRAMES	97h
VINC0M	3Bh
VINC1M	3Ch

Table 3–11: I²C bus list in alphabetical order

Name	Address
VINC2M	3Dh
VINC3M	3Eh
VINC4M	3Fh
VINMTHD	45h
VINPM	03h
VINPS	67h
VLENGTHM	DDh
VLENGTHS	E7h
VLEROFF	C0h
VLEXOFF	C0h
VLPM	11h
VLPS	75h
VLS1OFF	C0h
VOFPOSC	40h/41h
VOUTFR	BCh
VOUTPOL	D4h
VPANONM	3Ah
VPK	9Ah
VPKPRESCM	25h
VPKPRESCS	87h
VPOL	A3h
VPOLM	07h
VPOLS	6Bh
VPREBYPM	26h
VPREBYPS	88h
VS1_20	FFh
VS1_20STAT	F7h
VS2_20	FFh
VS2_20STAT	F7h
VS656_27	FFh
VS656_27STAT	F7h

Table 3–11: I²C bus list in alphabetical order

Name	Address
VSATADJ	A7h
VSBM1_36	FFh
VSBM1_36STAT	F7h
VSBM2_36	FFh
VSBM2_36STAT	F7h
VSBS_36	FFh
VSBS_36STAT	F7h
VSCPOSCM	3Ah
VSCPRESCM	27h
VSCPRESCS	89h
VSDCI_36	FFh
VSDCI_36STAT	F7h
VSEG1M	3Bh/3Ch
VSEG2M	3Dh/3Eh
VSEG3M	40h
VSEG4M	41h
VSEL_BE	DAh
VSHIFTM	08h
VSHIFTS	6Ch
VSIGNAL	A3h
VSLPF	61h
VSM1_40	FFh
VSM1_40STAT	F7h
VSM2_40	FFh
VSM2_40STAT	F7h
VSREF	9Fh
VSRGB_40	FFh
VSRGB_40STAT	F7h
VSS1_40	FFh
VSS1_40STAT	F7h
VSS2_40	FFh

Table 3–11: I²C bus list in alphabetical order

Name	Address
VSS2_40STAT	F7h
VSSLI_20	FFh
VSSLI_20STAT	F7h
VTHRH50M	0Ah
VTHRH50S	6Eh
VTHRH60M	00h
VTHRH60S	64h
VTHRL50M	09h
VTHRL50S	6Dh
VTHRL60M	00h
VTHRL60S	64h
WINDHDR	C7h
WINDHON	C7h
WINDHSP	C7h
WINDHST	C7h
WINDVDR	C6h
WINDVON	C6h
WINDVSP	C6h
WINDVST	C6h
WRITEM	13h
WRITES	77h
WRITES2M	13h
WRPOSXM	13h
WRPOSXS	77h
WRPOSYM	14h
WRPOSYS	78h
XDSCLS	9Ch
XDSTPE	9Ch
Y2RGB	AAh
YBAGR	CDh
YBORDERM	1Fh

Table 3–11: I²C bus list in alphabetical order

Name	Address
YBORDERS	81h
YCBYB	98h
YCBYR	98h
YCDELM	07h
YCDELS	6Bh
YCSELM	03h
YCSELS	67h
YCTOCOMB	98h
YCUR	C8h
YFDEL	A6h
YFRAMEM	4Bh
YFRAMES	97h
YUVMAT	15h
YUVSEL	AAh

3.8. I²C Command Table

Table 3–12: I²C Command Table

Subadd (Hex)	Data Byte A								Data Byte B							
	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0
00h	SYNCFTHDM		VTHRH60M							VTHRL60M						
01h	CONSM			COLONM	CPLLOFM	LPPOSTM	ACCFIXM	ACCFRZM	FLINEM	FLDINVM	CLPSTGYM	DISCHCHM	CLMPD1M			
02h	CONM			UVCORM		SECNTCHM		HPOLM		FHDETM	COMBUSEM		CLMPD2M			
03h	PWTHDM		CRCBM		LMOFSTM		VINPM	YCSELM	NOSIGBM	HINPM	CLMPST1M					
04h	VFLYWHLMDM		CHRFM						PLLTCM		CLMPST2M					
05h	COMBM	CSTANDM							CKILLM							
06h	CKILLSM								FHFRRNM							
07h	VPOLM		THRSELM	YCDELM					DISALLRESM	SATNRM	NSREDM			LPCDELM		
08h	HUEM								VSHIFTM							
09h	NTSCREFM								PALIDL1M	VTHRL50M						
0Ah	PALREFM								PALIDL0M	VTHRH50M						
0Bh	SLLTHDM		SCADJM						AGCMDM		AGCADJ1M					
0Ch	AGCRESM	AGCFRZEM	AGCADJ2M						VFLYWHLM	CPLLRESM	CLMPST1SM					
0Dh	CLMPHIGHM								SCMIDLM		CLMPST2SM					
0Eh	IFCOMPSTRM	SECACCLM			CLMPLOWM				ACCLIMM					IFCOMPM		
0Fh	SLLTHDVPM	EIA770M	VDETIFSM	LOCKSPM		ADLCKM	ADLCKSELM	ADLCKCCM	CLMPD2SM				CLMPD1SM			
10h	DEEMPFIRM			DEEMPIIRM		VDETITCM			SECACCM	SECDIVM	SECINC1M		SECINC2M		SCMRELM	
11h	DEEMPSTDM	BELLFIRM		BELLIIRM		SLLTHDVM			FLNSTRDM		ENLIMM	ISHFTM		NOTCHOFFM	VLPM	
12h	PALDELM		TNOTCHOFFM	BGPOSM			PALINC1M	PALINC2M	PALIDL2M	CLRANGEM		NTCHSELM			TRAPBLUM	TRAPREDM
13h	INTPROGM	FREEZEM	VERRESM	WRITEM		WRITES2M	PIXPLINM		WRPOSXM							
14h	WRPOSYM								UPDATESS	FMSYN			FMSYNUNS			
15h							STANDBYDAC	YUVMAT		TINT						
16h	RDPNTOFF					RDPOSXM									READM	
17h	RDPOSYM														RSHIFTM	RSHIFTS
18h	NMLINEM									NMSENSEM		NMPOSM				
19h	FEMAGM					SDRM		SDBM		TNRABSM	NRONM	TNRSELM	TNRNR4YM	TNRMD4YM	TNRNR4CM	

Table 3–12: I²C Command Table, continued

Subadd (Hex)	Data Byte A								Data Byte B							
	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0
1Ah	TNRYS0M				TNRYS1M				TNRYS2M				TNRYS3M			
1Bh	TNRYS4M				TNRYS5M				TNRYS6M				TNRYS7M			
1Ch	TNRCS0M				TNRCS1M				TNRCS2M				TNRCS3M			
1Dh	TNRCS4M				TNRCS5M				TNRCS6M				TNRCS7M			
1Eh	TNRYSSM				TNRCSSM				TNRCLYM				TNRCLCM			
1Fh	YBORDERM				UBORDERM				VBORDERM				MPFBLBM			
20h	MPFBPRM		MPFBLTM				GPPO			NMCHAN	SLOWVAR	AUTOGAP	UPDATERATEM			
21h	FRCBGNDM	MPFBPLM							GMSTTHV							
22h	FRCMMODM	APENSELM			HSCPRESCM											
23h	HAAPRESCM			HDCPRESCM				APPLIPM								
24h	MOTONM	GPP2		GPP1			NAPPLIPM									
25h	VAAPRESCM	VPKPRESCM					VCRPRESCM	NALPFIPM								
26h	VERBYPM		VDCPRESCM				ALPFIPM									
27h	HORPOSNM		HORWIDTHNM		VSCPRESCM											
28h	GMSTTH[1]	GMTHUM							GMSTSS			GMASM				
29h	GMSTTH[0]	GMTHLM							GMSTEN	GMSTSL		GMAMM				
2Ah	GSTHUM								GSTHLM							
2Bh		MDVFFON	FMDSON	FMDCTH				FMRES	FMTHYON	FMTHRON	FMSCALEL		FMSCALEU		FMREGION	
2Ch	FMMEMHIS				FMATH						FMDTH					
2Dh	TFLDDON	THRGM					SVALFI		SVALFR		AMMON		SWGM		TFDT	
2Eh	DTFDT[1]	THRMOV					DTFDT[0]	THFR0				TFON	THFI0			
2Fh	SVALLI		THLI0				FRAFION	THFR1				THFI1				
30h		THLI1					THFR2					THFI2				
31h	THLI2						THFR3					THFI3				
32h	GAPM						SENSITIVM		OFFSET							
33h	HPANONM	DBDHPOSM	CDELHPOSM		HSCPOSCM											
34h	HSEG1M[10:5]							HINC0M								
35h	HSEG1M[4:0]							HINC1M								

Table 3–12: I²C Command Table, continued

Subadd (Hex)	Data Byte A								Data Byte B							
	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0
36h	HSEG2M[10:5]							HINC2M								
37h	HSEG2M[4:0]							HINC3M								
38h	HSEG3M[10:5]							HINC4M								
39h	HSEG3M[4:0]					HSEG4M										
3Ah	VPANONM	VDOUBLEM	VSCPOSCM													
3Bh	VSEG1M[9:5]						VINC0M									
3Ch	VSEG1M[4:0]						VINC1M									
3Dh	VSEG2M[9:5]						VINC2M									
3Eh	VSEG2M[4:0]						VINC3M									
3Fh	INVSKEW	ARTSYNC	ITUSYNC	SECDELM	PALDETIDL			VINC4M								
40h	VOFPOSC[7:3]						VSEG3M									
41h	VOFPOSC[2:0]						VSEG4M									
42h	DPBRT						DPCON						DPCNS			
43h				PWADJCNTM					MINVM							
44h				PWADJCNTS					MINVS							
45h	AUTOFRRN		LPFIPMD	VINMTHD	FIELDBINV	HORPOSM										
46h				SECDELS	PALDETIDLS		VERPOSM									
47h						HORWIDTHM										
48h	NOFHSYNC					VERWIDTHM										
49h	PKCTIBPM		PKCTIHPM		LTIM	APK1BPM		APK2BPM			ATH1BPM		ATH2BPM		THEM	
4Ah	APK1HPM[1:0]		APK2HPM			ATH1HPM		ATH2HPM		DBDPICIM	APK1BPM[3:2]		APK1HPM[3:2]		CORONM	
4Bh					YFRAMEM			UFRAMEM					VFRAMEM			
4Ch	SPIXELM					EPIXELM							ENA_DEMOM	SCAN_IDM	CSC_ONM	DCIONM
4Dh	SLINEM				ELINEM						DCI_CORM					FREEZE_ANLM
4Eh	PIXELPLINEM									AB_FTCM						
4Fh	SENSWSM												LSWFM			
50h	SENSBSM										DSFTCM					
51h	ERRORCMPM										DYTCM					
52h				PK_FTCM									PEAK_SIZEM			

Table 3–12: I²C Command Table, continued

Subadd (Hex)	Data Byte A								Data Byte B							
	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0
53h	MVCOFA0		MVCOFA1			MVCOFP0		MVCOFP1			MVDIVA		MVDIVP		MVDIVR	
54h	MVMODE	MVREFPOS	SMMODE	MVFIXENA	MVFIXVAL						GMFMFBENA	GSFMFBENA	GSTILLENA	MVVISENA	FJSELLNV	MVCHOLD
55h	DYNOPMSV			DYNOPITV			DYNOPSMV	DYNOPFJV	DYNOPMSP0			DYNOPITP0			DYNOPSMP0	DYNOPFJP0
56h	DYNOPLSGM			DYNOPLSGS			OPPHASEFR	DYNOPLSV			DYNOPLSP0			DYNOPLSP1		
57h	DYNOPLSN			FMFORCETRIG	FJMODE		NEGLINESEL	FMFORCE				INITLINESEL	STATOPMSC			STATOPMSCENA
58h	DYNOPMSGM			DYNOPITGM			DYNOPSMGM	DYNOPFJGM	DYNOPMSGS			DYNOPITGS			DYNOPSMGS	DYNOPFJGS
59h	DYNOPMSN0			DYNOPITN0			DYNOPSMN0	DYNOPFJN0	DYNOPMSN1			DYNOPITN1			DYNOPSMN1	DYNOPFJN1
5Ah	DYNOPMSN2			DYNOPITN2			DYNOPSMN2	DYNOPFJN2	DYNOPMSN3			DYNOPITN3			DYNOPSMN3	DYNOPFJN3
5Bh	DYNOPMSN4			DYNOPITN4			DYNOPSMN4	DYNOPFJN4	DYNOPMSP1			DYNOPITP1			DYNOPSMP1	DYNOPFJP1
5Ch																GCMON
5Dh	FRINC[18:3]															
5Eh					FJMODE							FRZLIMLR	FRFIX	FRINC[2:0]		
5Fh	INCOMBC		BELLIIRM[2]	BELLFIRM[2]	DEEMPIIRM[2]	DEEMPFIRM[2]		AMSTD50M		AMSTD60M		SYNCGAINM	AGCPWRESM	H50SKEW	AGCTHDM	
60h	MVPM	MVPGM	SLNCW					SLNRUW					DDR_CC	BGSHIFTM	REMDEL2	REMDEL1
61h	HSPPL									VSLPF						
62h	REFTRIMRD								REFTRIMCVRD				REFTRIMRGBRD			
63h	MVPS	MVPGS	BELLIIRS[2]	BELLFIRS[2]	DEEMPIIRS[2]	DEEMPFIRS[2]		AMSTD50S		AMSTD60S		SYNCGAINS	AGCPWRESS	BGSHIFTS	AGCTHDS	
64h	SYNCFTHDS		VTHRH60S							VTHRL60S						
65h	CONSS			COLONS	CPLLOFS	LPPOSTS	ACCFIXS	ACCFRZS	FLINES	FLDINVS	CLPSTGYS	DISCHCHS	CLMPD1S			
66h	CONS			UVCORS		SECNTCHS		HPOLS		FHDETS	COMBUSES		CLMPD2S			
67h	PWTHDS		CRCBS		LMOFSTS		VINPS	YCSELS	NOSIGBS	HINPS	CLMPST1S					
68h	VFLYWHLMDS		CHRFS						PLLTCS		CLMPST2S					
69h	COMBS	CSTANDS							CKILLS							
6Ah	CKILLSS								FHFRRNS							
6Bh	VPOLS		THRSELS	YCDELS					DISALLRESS	SATNRS	NSREDS			LPCDELS		
6Ch	HUES								VSHIFTS							
6Dh	NTSCREFS								PALIDL1S	VTHRL50S						
6Eh	PALREFS								PALIDL0S	VTHRH50S						

Table 3–12: I²C Command Table, continued

Subadd (Hex)	Data Byte A								Data Byte B							
	A7	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
6Fh	SLLTHDS		SCADJS						AGCMDS		AGCADJ1S					
70h	AGCRESS	AGCFRZES	AGCADJ2S						VFLYWHLS	CPLLRESS	CLMPST1SS					
71h	CLMPHIGHS								SCMIDLS		CLMPST2SS					
72h	IFCOMPSTRS	SECACCLS			CLMPLOWS				ACCLIMS					IFCOMPS		
73h	SLLTHDVPS	EIA770S	VDETIFSS	LOCKSPS		ADLCKS	ADLCKSELS	ADLCKCCS	CLMPD2SS				CLMPD1SS			
74h	DEEMPFIRS			DEEMPIIRS		VDETITCS			SECACCS	SECDIVS	SECINC1S		SECINC2S		SCMRELS	
75h	DEEMPSTDS	BELLFIRS		BELLIIRS		SLLTHDVS			FLNSTRDS		ENLIMS	ISHFTS		NOTCHOFFS	VLPS	
76h	PALDELS		**TNOTCHOFFS**	BGPOSS			PALINC1S	PALINC2S	PALIDL2S	CLRANGES		NTCHSELS			TRAPBLUS	TRAPREDS
77h	INTPROGS	FREEZES	VERRESS	WRITES		READM2S	PIXPLINS		WRPOSXS							
78h	WRPOSYS															
79h	RDPOSYS									RDPOSXS					READS	
7Ah	NMLINES									NMSENSES		NMPOSS				
7Bh	FEMAGS					SDRS	SDBS			TNRABSS	NRONS	TNRSELS	TNRNR4YS			
7Ch	TNRYS0S				TNRYS1S				TNRYS2S				TNRYS3S			
7Dh	TNRYS4S				TNRYS5S				TNRYS6S				TNRYS7S			
7Eh	TNRCS0S				TNRCS1S				TNRCS2S				TNRCS3S			
7Fh	TNRCS4S				TNRCS5S				TNRCS6S				TNRCS7S			
80h	TNRYSSS				TNRCSSS				TNRCLYS				TNRCLCS			
81h	YBORDERS				UBORDERS				VBORDERS				MPFBLBS			
82h	MPFBPRS		MPFBLTS								DPVSAT					
83h	FRCBGNDS	MPFBPLS									DPUSAT					
84h	FRCMMODS	APENSELS		HSCPRESCS												
85h	HAAPRESCS			HDCPRESCS			APPLIPS									
86h	MOTONS					NAPPLIPS										
87h	VAAPRESCS	VPKPRESCS				VCRPRESCS	NALPFIPS									
88h	VPREBYPS		VDCPRESCS			ALPFIPS										
89h				VSCPRESCS												
8Ah	HPANONS	DBDHPOSS	CDELHPOSS		HSCPOSCS											
8Bh	HSEG1S[10:5]							HINC0S								

Table 3–12: I²C Command Table, continued

Subadd (Hex)	Data Byte A								Data Byte B							
	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0
8Ch	HSEG1S[4:0]							HINC1S								
8Dh	HSEG2S[10:5]							HINC2S								
8Eh	HSEG2S[4:0]							HINC3S								
8Fh	HSEG3S[10:5]							HINC4S								
90h	HSEG3S[4:0]					HSEG4S										
91h	HOROFFS[10:6}					HORPOSS										
92h	HOROFFS[5:0]						VERPOSS									
93h						HORWIDTHS										
94h	VEROFFS					VERWIDTHS										
95h	PKCTIBPS		PKCTIHPS		LTIS	APK1BPS		APK2BPS			ATH1BPS		ATH2BPS		THES	
96h	APK1HPS[1:0]		APK2HPS			ATH1HPS		ATH2HPS		DBDPICIS	APK1BPS[3:2]		APK1BPS[3:2]		CORONS	
97h					YFRAMES				UFRAMES				VFRAMES			
98h	CVBSEL1				CVBSEL2				CLMPSIG1		CLMPSIG2		VCRDETHD	YCBYR	YCBYB	YCTOCOMB
99h	CVBOSEL1				CVBOSEL2				CVBOSEL3				VDG		HDG	
9Ah	DDR		F2F1F0			DT	DC	COR	NOSEL		DCR	SYNCOMB	VPK			
9Bh	LINLENH50				LINLENH60				REFTRIMEN	V50BLANK	PORCNCL	RESETPC1	RESETPC2	SELCOMB	DISCOMB	RESMODE
9Ch	XDSCLS					656BLANK	XDSTPE			IRQCON			SERVICE	INCOMB		SLSRC
9Dh	REFTRIM								REFTRIMCV				REFTRIMRGB			
9Eh	OMODE		CLK656out					PPLIPI								
9Fh	NAPIPPHI		F_OFFS		ADLINE					FPOL	IMODE		ADINS	VSREF		
A0h							LPFIPI									
A1h	APPLIPI									NALPFIPI						
A2h	NAPPLIPI								ALPFIPI							
A3h	VSIGNAL	CFORMAT	HPOL	VPOL	EN_656		ITUPRTSEL									
A4h	BRTADJ								CONADJ						CHRSFR	AASEL
A5h	CLKF2PAD	FBLDEL			GOFST		MIXGAIN							STANDBYRGB	STANDBYCV	DEC2
A6h	YFDEL							UVDEL							RGBSEL	FBLCONF
A7h	USATADJ						VSATADJ						ADCSEL	AABYP	CLMPVG	DCLMPF
A8h	AGCADJR						AGCADJB						MIXOP		CLMPVRB	

Table 3–12: I²C Command Table, continued

Subadd (Hex)	Data Byte A								Data Byte B							
	A7	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
A9h	AGCADJG						AGCADJF						RBOFST			SKEWSEL
AAh	FBLOFFST						SELMASTER		SELSLAVE		SELSM	YUVSEL	SMOP	Y2RGB	BLUESEL	BLUETWO
ABh	IICINCR[18:3]															
ACh	CLKT1		HDTOTEST	FILE							LNL	DISRES	LIMHI	IICINCR[2:0]		
ADh	KOIWID		KOIH		HTESTW				HSWIN[2:0]			SETSTABLL	KD2	HINCR_EXT	LMOD	FMOD
AEh	HRES	HWID	FION				PPLIP									
AFh	FREQSELL		OSCPD	SHAPERDIS	TSTSHABRI	LIMLR[2:0]			FKOI	FKOIHYS	KIL[3:0]					
B0h									LIMIP							
B1h	KPNL[3:0]				KPL[3:0]				KINL[3:0]				KPNL[4]	KPL[4]	KINL[4]	KIL[4]
B2h					SLLWIN		FETHD		LIMII							
B3h													HSWIN[3]	LIMLR[3]	LIMEN	
B4h	LBSUB		LBGRADRST	LBSTABILITY	LB43SENS	LBNGFEN	LBTHDNBNHA					LBHSDEL				
B5h	LBGRADDET								LBVWENDLO							
B6h	LBHIWHITE								LBHWEND							
B7h	LBHISTBLA									LBHWST						
B8h	LBMASLA	LBVWSTLO							LBFS	LBVWENDUP						
B9h	LBGSDEL					LBGFBDEL					LBVWSTUP					
BAh	LBASDEL					LBVISUON	LBACTIVITY					LBTHDNBNG				
BBh	PPLOFF			LPFOPOFF				NAPPLOP								
BCh	VOUTFR	HOUTFR	NOSYNC	RMODE		OPDEL(MSB)	HOUTDEL									
BDh	GFBON	FMODE	PDGSR	MASTERON	SLAVEON	LPFOP(8)	PPLOP									
BEh	OPDEL								LPFOP[7:0]							
BFh	DISPMODE				MOTVALON		REFRON	REFRPER	LPFOPOFF					ARSDIS	JLCRES	MASLEX
C0h	STOPMOS				EXTRD	P3DIS	P4DIS		HPE1OFF	VLEROFF	HPS1OFF	HPE2OFF	HPEXOFF	VLEXOFF	HPS2OFF	VLS1OFF
C1h	CHROMSIGN656	FIOFFOFF	DPOUT656	SHIFTUV	FSWFTL	AFPROC	V656DEL	CLK656OUTINV	HOUTTR	UVCODE	V100IN	DIGOUTEN	M422	CHRSFM	NSHAP	DWO
C2h	C1								C2							
C3h	C3								C4							
C4h	C5								C6							
C5h	TO1RGB			UENINV	C6		C5		C4		C3		C2		C1	

Table 3–12: I²C Command Table, continued

Subadd (Hex)	Data Byte A								Data Byte B							
	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0
C6h	WINDVSP		WINDVST	WINDVDR	WINDVON	HORPOSP										
C7h	WINDHSP		WINDHST	WINDHDR	WINDHON	HORWIDTHP										
C8h	YCUR				LUMAMP		VERPOSP									
C9h	UCUR				CHROMAMP		VERWIDTHP									
CAh	VCUR					HORPOSF										
CBh	HORFRAMEF					HORWIDTHF										
CCh	VERFRAMEF						VERPOSF									
CDh	YBAGR						VERWIDTHF									
CEh	UBAGR					HORPOSG										
CFh	VBAGR					HORWIDTHG										
D0h	HORFRAMEG					VERPOSG										
D1h	VERFRAMEG					VERWIDTHG										
D2h				PRIOP			OBTEMP	OBSOFT	PATTMODE			TBLEND		FRAMEDIMM	FRAMEDIMS	
D3h	PRIOC			PRIOS			PRIOF			PRIOM			PRIOG			
D4h	BLANDEL								VBLANPOL	CLKOUT72	CLKOUTINV	HOUTPOL	VOUTPOL	BLANPOL	CLKOUTSEL	CLKOUTON
D5h	CLKOUTSEL72		VBLANDEL[9:5]					BLANLEN								
D6h	VBLANDEL[4:0]						VBLANLEN									
D7h	PKLY								PKLU							
D8h					COARSEDEL			FINEDEL	PKLV							
D9h	C800															
DAh	VDELAY_BE		VSEL_BE								GPH50		CPUIRQ2V		CPUDISABLE	AUTOINC_OFF
DBh	LPFLDM								NRPIXELM							
DCh	DETHPOLM	DETVPOLM	STDETM			SCOUTENM	PALIDM	CKSTATM	LNSTDRDM	INTM	SCDEVM					
DDh	VFLYMDM	VLENGTHM							AGCADJCV1						PALDETM	STABM
DEh	NOISEMEM								NOISE							
DFh	FCIM									STATSIZE			FILMMODEM			
E0h			FMOTREGM													
E1h	GMOTREGM														GSTILLM	GMOTIONM

Table 3–12: I²C Command Table, continued

Subadd (Hex)	Data Byte A								Data Byte B							
	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0
E2h	AM50_OM	AM60_OM										LBSTATUS	NOISESTATUS	GMDSTATUSM	FMSTATUSM	NMSTATUSM
E3h	TFDPPM[8:4]						GAINSEG1FRCM									
E4h		TFDPPM[3:0]					GAINSEG2FRCM									
E5h	LPFLDS								NRPIXELS							
E6h	DETHPOLS	DETVPOLS	STDETS			SCOUTENS	PALIDS	CKSTATS	LNSTDRDS	INTS	SCDEVS					
E7h	VFLYMDS	VLENGTHS							AGCADJCV2						PALDETS	STABS
E8h	NOISEMES															
E9h	AM50_OS	AM60_OS														NMSTATUSS
EAh	DATA_CCWSS2								DATA_CCWSS1							
EBh	DATA_USWSS3								DATA_USWSS2							
ECh	DATA_USWSS1								POR			TVMODE	SLFLDUSWSS	DATAVUSWSS	SLFLDCCWSS	DATAVCCWSS
EDh									FBSTAT	FBFALL	FBRISE	PFBL	PG	PB	PR	FBLACTIVE
EEh							MAXGUC									
EFh							MAXGLC									
F0h	MAXALC[8:5]						MAXHUC									
F1h	MAXALC[4:0]						MAXHLC									
F2h	GRADSLAA							MAXAUC								
F3h	LBFORMAT	LBSUBTITLE	LBTOPTITLE	GRADISSTABLE	TOPTITLE	SUBTITLE		NOGRADFOUND	SWITCHTO43	UPWHITE	LPWHITE	UPBLACK	LPBLACK			
F4h	LBSLAA							LBELAA								
F5h						GRADELAA										
F6h	VERSION			SLS	REV				RMMIRROR		CHIPID					STABLL
F7h	ADR_RDY	FIELDCD1	FIELDCD2	VSRGB_40STAT	VSBM2_36STAT	VSBM1_36STAT	VSDCI_36STAT	VSBS_36STAT	VSSLI_20STAT	VSS2_40STAT	VSS1_40STAT	VSM2_40STAT	VSM1_40STAT	VS656_27STAT	VS2_20STAT	VS1_20STAT
F8h	FCBM															SHIFTACT
F9h	ADATA0								ADATA1							
FAh	ADATA2								ADATA3							
FBh	ADATA4								ADATA5							
FCh	ADATA6								ADATA7							
FDh	C800 commands															

Table 3–12: I²C Command Table, continued

Subadd (Hex)	Data Byte A								Data Byte B							
	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0
FEh				IMRGB_40	IMBM2_36	IMBM1_36	IMDCI_36	IMBS_36	IMSLI_20	IMS2_40	IMS1_40	IMM2_40	IMM1_40	IM656_27	IM2_20	IM1_20
FFh				VSRGB_40	VSBM2_36	VSBM1_36	VSDCI_36	VSBS_36	VSSLI_20	VSS2_40	VSS1_40	VSM2_40	VSM1_40	VS656_27	VS2_20	VS1_20

Note: Bits written with grey background are intended not to be user adjustable and should be set to the default value written in this data sheet or according to an updated list available from Micronas.

3.9. I²C Command Description

3.9.1. Master Channel

Table 3–13: Master channel

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
Color Decoder Master																				
00h	W	VS1_20	SYNCFTHDM	x	x															**SYNCF threshold** 00: 4 lines 01: 3 lines 10: 2lines 11:1 line
			VTHRH60M			x	x	x	x	x	x	x								**Vertical Sync gating: Closing 60 Hz** Closing=262+4*__VTHRH60M__ 0000000: Closing in line 262 1111111: Closing in line 770
			VTHRL60M										x	x	x	x	x	x	x	**Vertical Sync gating: Opening 60 Hz** Opening=4*__VTHRL60M__ 0000000: Opening in first line 1111111: Opening in line 508
01h	W	VS1_20	CONSM	x	x	x														**Color switched on at level above CKILLS (SECAM)** at level=CKILLS+CONS 000: Min value 010: Default 111: Max value
			COLONM				x													**Forces color on** 0: Color depends on color decoder status 1: Color always on
			CPLLOFM					x												**Opens the closed loop** 0: Normal operation 1: Chroma PLL opened
			LPPOSTM						x											**Additional filtering of luminance** 0: No filtering 1: Filtering
			ACCFIXM							x										**Fix ACC to nominal value** 0: ACC is working 1: ACC is set to fixed value according to **PALREFM**/**NTSCREFM**
			ACCFRZM								x									**Freeze ACC** 0: ACC is working 1: ACC is frozen at current value
			FLINEM									x								**Mode selection** 0: Interlace input 1: Progressive input

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			FLDINVM										x							**Field inversion** 0: No inversion 1: Inversion
			CLPSTGYM											x						**Clamping strategy** 0: Back-porch clamping 1: Sync-tip-clamping
			DISCHCHM												x					**Disable channel change signal** 0: Color decoder not reset after channel-change 1: Color decoder reset after channel change
			CLMPD1M													x	x	x	x	**Measurement duratation CD1, signals 1** Granularity: 200 ns 0000: 0 µs 0111: 1.4 µs 1111: 3 µs
02h	W	VS1_20	CONM	x	x	x														**Color switched on at level above CKILL (PAL/NTSC)** At level=CKILL+CON 000: Min value 010: Default 111: Max value
			UVCORM				x	x												**Chrominance coring** 00: Disabled 01: ± 1LSB 10: ± 2LSB 11: ± 3LSB
			SECNTCHM						x	x										**Selection of notch filter behavior in SECAM mode** 00: 4.406 MHz 01: 4.250 MHz 10: 4.33 MHz 11: 4.406/4.205 dependent on transmitted color
			HPOLM								x	x								**H Polarity at HINP** 00: Use Hsync 01: Use inverted Hsync 10: Autodetect polarity 11: (Reserved)
			FHDETM										x							**Automatic multisync capability** 0: Disabled 1: Enabled
			COMBUSEM											x	x					**Comb filter usage CD1** 00: Use first CVBS input 01: Use second CVBS input 10: Use comb-filter 11: ADCG / ADCF **(dependent on *ADCSEL*)**

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			CLMPD2M													x	x	x	x	**Measurement duration CD1, signals** Granularity: 200 ns 0000: 0 µs 0111: 1.4 µs 1111: 3 µs
03h	W	VS1_20	PWTHDM	x	x															**Selection of "Peak-White" threshold** 00: 448 01: 470 10: 500 11: 511
			CRCBM			x	x													**Choice of UV or CrCb output** 00: UV color space 01: CrCb color space 10: Modified CrCb color space (SECAM only)
			LMOFSTM					x	x											**Luminance offset in color decoder during visible picture** 00: No offset (NTSC) 01: - 7.5 IRE 10: + 7.5 IRE (PAL, SECAM) 11: -3.7 IRE A 7.5 IRE offset is added during blanking in display processing. When chosing 10, the luminance offset is equal to the offset of the CVBS input as in both picture and blanking the same 7.5 IRE offset is used.
			VINPM							x										**Vertical pulse detection** 0: From sync signal (CVBS, Y, or G)) 1: From separate V-input pin When set to 0, no V polarity detection possible
			YCSELM								x									**Y/C selec**t 0: CVBS input 1: Y/C input
			NOSIGBM									x								**No signal behavior** 0: Noisy screen when out of sync 1: Colored background insertion instead
			HINPM										x							**Synchronization input** 0: Synchronization from CVBS front-end (CVBS or Y/C) 1: Synchronization via RGB front-end (green or fbl ADC) When set to 0, no H polarity detection possible
			CLMPST1M											x	x	x	x	x	x	**Measurement start: CD1, Signals1** 000000: 0 µs 011100: 5.6 µs 111111: 12.8 µs

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
04h	W	VS1_20	VFLYWHLMDM	x	x															**Vertical flywheel mode** 00: Check for correct standard 01: 3 lines deviation allowed 10: 4 lines deviation allowed, no check for interlace 11: 5 lines deviation allowed, no check for interlace
			CHRFM			x	x	x	x	x	x									**Chroma bandwidth** Selects chroma bandwidth 011100: Nominal bandwidth
			PLLTCM									x	x							**Time constant HPLL (VCR...TV)** 00: Very fast 01: Fast 10: Slow 11: Very slow
			CLMPST2M											x	x	x	x	x	x	**Measurement start CD1, Signals 2** 000000: 0 µs 011100: 5.6 µs 111111: 12.8 µs
05h	W	VS1_20	COMBM	x																**Delay line** 0: Use delay line 1: Do not use delay line (only suited for NTSC)
			CSTANDM		x	x	x	x	x	x	x									**Color standard assignment** 0000000: No color standard chosen 0000001: PAL N 0000010: PAL B 0000100: SECAM 0001000: PAL 60 0010000: PAL M 0100000: NTSC M 1000000: NTSC 44 For allowed combinations please refer to chapter “chroma decoder” 1100110: PALB/SECAM/NTSCM/NTSC44/PAL60
			CKILLM									x	x	x	x	x	x	x	x	**Chroma level for color off (PAL/NTSC)** 00000000: High burst amplitude 01000000: Default 11111111: Low burst amplitude
06h	W	VS1_20	CKILLSM	x	x	x	x	x	x	x	x									**Chroma level for color off (SECAM)** 00000000: Low burst amplitude 01000000: Default 11111111: High burst amplitude Behavior is opposite to **CKILL** (PAL/NTSC case)
			FHFRRNM									x	x	x	x	x	x	x	x	**Free running frequency of horizontal PLL** 00000000: 384 clocks (52.7 kHz) 11100100: 1296 clocks (15.625 kHz) 11111111: 1404 clocks (14.423 kHz)

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
07h	W	VS1_20	VPOLM	x	x															**V-Polarity at VINP** 00: Use Vsync 01: Use inverted Vsync 10: Autodetect polarity 11: (Reserved)
			THRSELM			x														**H-Slicing level threshold** 0: 50 % 1: 37 %
			YCDELM				x	x	x	x	x									**Luminance delay** 10000: 800 ns 0000: no delay 01111: -700 ns
			DISALLRESM									x								**Disable all chroma resets** 0: Resets allowed 1: Resets disabled May only be used if ONE color standard is selected
			SATNRM										x							**Noise reduction for satellite signal** 0: Disabled 1: Enabled
			NSREDM											x	x	x				**Noise reduction for horizontal PLL** 000: 1/8 001: 1/4 010: 1/2 011: 1 100: 2 101: 4 110: 8 111: 16
			LPCDELM														x	x	x	**Window shift for fine error calculation** 100: -4 clock cycles 000: No offset 011: +3 clock cycles
08h	W	VS1_20	HUEM	x	x	x	x	x	x	x	x									**Hue control (tint)** 10000000: -89° 00000000: 0° 01111111: +88°
			VSHIFTM									x	x	x	x	x	x	x	x	**Field detection window shift** 00000000: No shift 11111111: Shifted by 2048
09h	W	VS1_20	NTSCREFM	x	x	x	x	x	x	x	x									**ACC reference adjustment (NTSC)** 00000000: Low reference value 10010001: Nominal value 11111111: High reference value

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			PALIDL1M									x								**PAL/NTSC identification level 1** 0: Less sensitive (192) 1: More sensitive (64)
			VTHRL50M										x	x	x	x	x	x	x	**Vertical sync gating: Opening 5 Hz** Opening=4*__VTHRL50M__ 0000000: Opening in first line 1111111: Opening in line 508
0Ah	W	VS1_20	PALREFM	x	x	x	x	x	x	x	x									**ACC reference adjustment (PAL)** 00000000: Low reference value 11110000: Nominal value 11111111: High reference value
			PALIDL0M									x								**PAL/NTSC identification level 0** 0: Less sensitive 1: More sensitive
			VTHRH50M										x	x	x	x	x	x	x	**Vertical sync gating: Closing 50 Hz** Closing=312+4*__VTHRH50M__ 0000000: Closing in line 312 1111111: Closing in line 820 When VINPM (03h) is set, 50 Hz values are taken for opening and closing values.
0Bh	W	VS1_20	SLLTHDM	x	x															**Slicing level threshold H** 00: No offset 01: Small negative 10: Small positive 11: Large positive (adaptive)
			SCADJM			x	x	x	x	x	x									**Subcarrier adjustment** 000000: -262 ppm 001111: 0 ppm 111111: 840 ppm
			AGCMDM									x	x							**AGC method** 00: Sync amplitude and peak white 01: Sync amplitude only 10: Peak white only 11: Fixed to value __AGCADJ1M__
			AGCADJ1M											x	x	x	x	x	x	**Gain adjustment ADC1** 000000: 0.6 V input signal 100000: 1.2 V input signal: 111111: 1.8 V input signal
0Ch	W	VS1_20	AGCRESM	x																**AGC reset** 0: No reset 1: Reset
			AGCFRZEM		x															**Freeze AGC (ADC_CVBS)** 0: Normal operation 1: Freeze AGC at current value

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			AGCADJ2M			x	x	x	x	x	x									**Gain adjustment ADC2** 000000: 0.6 V input signal 100000: 1.2 V input signal 111111: 1.8 V input signal
			VFLYWHLM									x								**Vertical flywheel** 0: Disabled 1: Enabled
			CPLLRESM										x							**Force chroma PLL reset** 0: No reset 1: Reset chroma PLL After use, **CPLLRESM** must be set to 0 again
			CLMPST1SM											x	x	x	x	x	x	**Clamping start CD1, Signals 1** 000000: 0 µs 011100: 5.6 µs 111111: 12.8 µs
0Dh	W	VS1_20	CLMPHIGHM	x	x	x	x	x	x	x	x									**Vertical end of clamping pulse** 00000000: Line 256 00111100: Line 376 11111111: Line 766
			SCMIDLM									x	x							**SECAM identification level** 00: 128 01: 64 10: 96 11: 80
			CLMPST2SM											x	x	x	x	x	x	**Clamping start CD1, Signals 2** 000000: 0 µs 011100: 5.6 µs 111111: 12.8 µs
0Eh	W	VS1_20	IFCOMPSTRM	x																**2nd IF compensation filter** 0: Disabled 1: Enabled
			SECACCLM		x	x	x													**Secam acceptance level** 000: 100 001: 84 010: 64 011: 32 100: 70 101: 76 110: 90 *Note: Has only effect if SECACCM (0Eh) is enabled*
			CLMPLOWM					x	x	x	x									**Vertical start of clamping pulse** 0000: Line 0 0011: Line 6 1111: Line30

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			ACCLIMM									x	x	x	x	x				**ACC limitation** 00000: Limit at high color-carrier 01000: Limit at -24 dB 11111: Limit at low color-carrier
			IFCOMPM														x	x	x	**IF compensation filter** 000: Pal prefiltering 001: Pal prefiltering + IF 010: Prefiltering 011: IF 6dB 100: Flat
0Fh	W	VS1_20	SLLTHDVPM	x																**Vertical slicing level threshold polarity** 0: Positive 1: Negative
			EIA770M		x															**EIA 770 support** 0: Standard TV signals expected 1: Progressive signals expected *Note: Timing according to EIA 770.1 or 770.2 when 1*
			VDETIFSM			x														**Vertical sync-detection slope** 0: Normal 1: Slow
			LOCKSPM				x	x												**Duration of chroma-PLL search** 00: 25 fields 01: 20 fields 10: 17 fields 11: 15 fields
			ADLCKM						x											**Additional lock-detection** 0: No used 1: Used
			ADLCKSELM							x										**Additional lock-detection selection** 0: PALID 1: PALDET
			ADLCKCCM								x									**Additional lock-detection color-killer** 0: Do not use lock signal 1: Use lock-signal
			CLMPD2SM									x	x	x	x					**Clamping duration CD1, signals 2 (for RGBF)** Granularity: 200 ns 0000: 0 µs 0111: 1.4 µs 1111: 3 µs

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			CLMPD1SM													x	x	x	x	**Clamping duration CD1, signals 1** Granularity: 200 ns 0000: 0 µs 0111: 1.4 µs 1111: 3 µs
10h	W	VS1_20	DEEMPFIRM[2:0]	x	x	x														**Deemphase filter FIR component** 0000:16 0101: 21 1111: 31 DEEMPFIRM[3] is in 5Fh
			DEEMPIIRM[1:0]				x	x												**Deemphase filter IIR component** 000: 5 001: 6 010: 7 011: 8 100: 9 101: 10 110: (reserved) 111: (reserved) DEEMPIIRM[2] is in 5Fh
			VDETITCM						x	x	x									**Vertical detection integration time constant** 000: 400 clock cycles 001: 375 clock cycles 010: 350 clock cycles 011: 300 clock cycles 100: 250 clock cycles 101: 225 clock cycles 110: 200 clock cycles 111: Automatic
			SECACCM									x								**Secam acceptance** 0: Disabled 1: Enabled
			SECDIVM										x							**Secam divider** 0: Divide by 4 1: Divide by 2
			SECINC1M											x	x					**Secam increment 1** 00: 2 01: 3 10: 4 11: 5
			SECINC2M													x	x			**Secam increment 2** 00: 1 01: 2 10: 3 11: 4

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			SCMRELM															x	x	**Secam rejection level** 00: 320 01: 384 10: 352 11: 1024
11h	W	VS1_20	DEEMPSTDM	x																**Deemphase filtering for standard detection** 0: Weak 1: Strong
			BELLFIRM[1:0]		x	x														**Bell filter FIR component** 000: -116 001: -113 010: -110 011: -108 100: -106 101: -104 110: -102 111: -100 BELLPFIRM[2] is in 5Fh
			BELLIIRM[1:0]				x	x												**Bell filter IIR component** 000: 8 001: 9 010: 10 011: 11 100: 12 101: 13 110: 14 111: 16 BELLIIRM[2] is in 5Fh
			SLLTHDVM						x	x	x									**Slicing level threshold V** 000: No offset 001: 4 010: 8 011: 12 101: Adaptive (limited to +-4) 110: Adaptive (limited to +-8) 111: Adaptive (limited to +-12)
			FLNSTRDM									x	x							**Force line standard at CVBS/RGB front-end** 00: Automatic 01: Force 50 Hz 10: Force 60 Hz 11: (Reserved)
			ENLIMM											x						**Enable limiter** 0: Disabled 1: Enabled

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			ISHFTM												x	x				**I-adjustment for horizontal PLL** 00: *1 01: *16 10: *4 11: *8
			NOTCHOFFM														x			**Luminance notch-filter** 0: Notch-filter enabled 1: Filter bypassed for PAL/NTSC/filter enabled for SECAM To switch-off filter for SECAM, use **TNOTCHOFF**
			VLPM															x	x	**Lowpass for vertical sync-separation** 00: None 01: Weak 10: Medium 11: Strong
12h	W	VS1_20	PALDELM	x	x															**PAL/NTSC delay vs. SECAM (chrominance)** 00: PAL/NTSC most left 11: PAL/NTSC most right
			TNOTCHOFFM			x														**Luminance notch-filter** 0: Notch-filter according to **NOTCHOFFM** 1: Notch-filter disabled
			BGPOSM				x	x	x											**Burstgate delay (SECAM only)** Granularity: 200 ns 000: Most left (-400 ns) 010: No delay 111: Most right (+1 us)
			PALINC1M							x										**Pal detection: Increment 1** 0: +3 1: +2
			PALINC2M								x									**Pal detection: Increment 2** 0: -1 1: -2 Do not use PALINC2M=1 in combination with PALINC1M=1
			PALIDL2M									x								**PAL/NTSC identification level 2** 0: Less sensitive 1: More sensitive
			CLRANGEM										x	x						**Chroma lock-range** 00: ± 425 Hz 01: ± 463 Hz 10: ± 505 Hz 11: ± 550 Hz

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			NTCHSELM												x	x	x			**Luminance notch selection** 000: Sharp notch 001: Medium 1 010: Medium 2 011: Broad notch 100: Broad steep notch (PAL, SECAM only)
			TRAPBLUM															x		**Notch frequency for 4,250 MHz** 0: 4.25 MHz 1: 4.2 MHz Has only effect in SECAM mode
			TRAPREDM																x	**Notch frequency for 4,406 MHz** 0: 4.406 MHz 1: 4.356 MHz Has only effect in SECAM mode
Memory Controller Master Channel																				
13h	W	VSM2_40	INTPROGM	x																**Interlaced or progressive input signal for master channel** 0: Interlaced input source 1: Progressive input source (e.g. VGA)
			FREEZEM		x															**Freeze master picture** 0: Live 1: Frozen (no writing of master data)
			VERRESM			x														**Vertical resolution master channel for frame based MUP-Mode** 0: Field resolution 1: Frame resolution
			WRITEM				x	x												**Write mode master channel** 00: All incoming fields are stored 01: Only A fields are stored 10: Only B fields are stored 11: (Reserved) For DISPMODE=0001 (Snap Shot): 0X, 1X: Writing all fields only to live channel
			WRITES2M						x											**Write slave data to master memory** 0: Slave data is written to slave memory 1: Slave data is written to master memory
			PIXPLINM							x	x									**Pixels per line master channel** 00: Defined by DISPMODE 01: 448 pixels/line 10: 768 (***MOTVALON***=0) or 704 (***MOTVALON***=1) pixels/line 11: 896 pixels/line

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			WRPOSXM									x	x	x	x	x	x			**Horizontal writing position of master picture in the memory** Position=(***WRPOSXM***/32) *128 pixel (FSM mode, ***MOTVALON***=1) Position=(***WRPOSXM***/2) *32 pixel (FSM mode, ***MOTVALON***=0) Position=(***WRPOSXM***/2) *32 pixel (SPS, PCF, PCP) Position=***WRPOSXM*** *16 pixel (others) Note: Stepsize depends on selected mode
14h	W	VSM2_40	WRPOSYM	x	x	x	x	x	x	x	x									**Vertical position of master picture in the memory** 00000000: Upper border position Resolution: 1 line
			UPDATESS									x								**Update snap shot picture** 0: Live picture is updated 1: Still picture (snap shot) is updated
			FMSYN										x	x	x					**Synchronisation of film mode signal** 000: Synchronisation disabled 001: No delay 010: 1 field delay 101: 4 fields delay 110: (Reserved) 111: (Reserved)
			FMSYNUNS													x				**Synchronisation of film mode signal when unsecure** 0: Synchronisation disabled when unsecure 1: Synchronisation always active
15h	W	VSM2_40	STANDBYDAC							x										**Standby mode DAC** 0: DACs active 1: DACs in standby mode
			YUVMAT								x	x								**YUV-matrix** 00: YCbCr 01: YPbPr (CCIR) 10: YPbPr (BTA) 11: (Reserved)
			TINT										x	x	x	x	x	x	x	**Tint control** 1000000: Max negative tint 0000000: No tint 0111111: Max positive tint

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
16h	W	VSBM1_36	RDPNTOFF	x	x															**Offset of read pointers for port P6 (neighboured lines)** 00: 1 line 01: 2 lines 10: 3 lines 11: 4 lines
			RDPOSXM						x	x	x	x	x	x	x	x	x			**Horizontal read position master** Pixel number indicating the start position of reading for the master channel 000000000: First left pixel Effective value: RDPOSXM*2
			READM															x	x	**Read mode master channel** 00: Reading A and B fields 01: Reading only A fields 10: Reading only B fields 11: (Reserved) For DISPMODE=0001 (Snap Shot): 00: Reading live channel ≠ 00: Reading still picture
17h	W	VSBM1_36	RDPOSYM	x	x	x	x	x	x	x	x									**Vertical read position master** Line number indicating the start line of reading for the master channel Granularity: 1 line 00000000: First line
			RSHIFTM															x		**Raster shift master** Enable raster shift for master channel for joint line free SSC mode 0: Disable raster shift 1: Enable raster shift
			RSHIFTS																x	**Raster shift slave** Enable raster shift for slave channel for joint line free SSC mode 0: Disable raster shift 1: Enable raster shift
Noise Measurement Master Channel																				
18h	W	VSM1_40	NMLINEM	x	x	x	x	x	x	x	x	x								**Line for noise measurement** 0_d: Line 2 1_d: Line 3 311_d: Line 1 (PAL) 261_d: Line 1 (NTSC) Lines 3-260 are not standard dependent
			NMSENSEM										x	x						**Noise measurement sensitivity** 00: *1 01: *2 10: *4 11: *8

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			NMPOSM												x	x				**Noise measurement analyze window position** 00: 6.3 µs 01: 12.6 µs 10: 18.9 µs 11: 23.7 µs
Temporal Noise Reduction Master Channel																				
19h	W	VSM2_40	FEMAGM	x	x	x	x	x												**Fine error characteristic** 00000: Smallest gain 10000: Default (equal to B11 version) 11111: Largest gain
			SDRM						x	x										**Secam Dr adjustment** 00: 191 01: 194 10: 197 11: 200
			SDBM								x	x								**Secam Db adjustment** 00: -55 01: -58 10: -61 11: -64
			TNRABSM										x							**Motion detector works on absolute values:** 0: Absolute values not calculated 1: Absolute values calculated
			NRONM											x						**Temporal noise reduction** 0: Disabled 1: Enabled
			TNRSELM												x					**Chrominance motion values from:** 0: luminance motion detector 1: separate chrominance motion detector
			TNRNR4YM													x				**Temporal noise reduction of luminance:** 0: Frame based 1: Field based
			TNRMD4YM														x			**Motion detection of temporal noise reduction of luminance:** 0: Frame based 1: Field based
			TNRNR4CM															x		**Temporal noise reduction and motion detection of chrominance:** 0: Frame based 1: Field based
1Ah	W	VSM2_40	TNRYS0M	x	x	x	x													**TNR curve characteristic of luma segment 0** 0001: Default
			TNRYS1M					x	x	x	x									**TNR curve characteristic of luma segment 1** 1111: Default

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			TNRYS2M									x	x	x	x					**TNR curve characteristic of luma segment 2** 1111: Default
			TNRYS3M													x	x	x	x	**TNR curve characteristic of luma segment 3** 0100: Default
1Bh	W	VSM2_40	TNRYS4M	x	x	x	x													**TNR curve characteristic of luma segment 4** 0100: Default
			TNRYS5M					x	x	x	x									**TNR curve characteristic of luma segment 5** 0100: Default
			TNRYS6M									x	x	x	x					**TNR curve characteristic of luma segment 6** 0000: Default
			TNRYS7M													x	x	x	x	**TNR curve characteristic of luma segment 7** 0000: Default
1Ch	W	VSM2_40	TNRCS0M	x	x	x	x													**TNR curve characteristic of chroma segment 0** 0001: Default
			TNRCS1M					x	x	x	x									**TNR curve characteristic of chroma segment 1** 1111: Default
			TNRCS2M									x	x	x	x					**TNR curve characteristic of chroma segment 2** 1111: Default
			TNRCS3M													x	x	x	x	**TNR curve characteristic of chroma segment 3** 0100: Default
1Dh	W	VSM2_40	TNRCS4M	x	x	x	x													**TNR curve characteristic of chroma segment 4** 0100: Default
			TNRCS5M					x	x	x	x									**TNR curve characteristic of chroma segment 5** 0100: Default
			TNRCS6M									x	x	x	x					**TNR curve characteristic of chroma segment 6** 0000: Default
			TNRCS7M													x	x	x	x	**TNR curve characteristic of chroma segment 7** 0000: Default
1Eh	W	VSM2_40	TNRYSSM	x	x	x	x													**TNR start value of luma LUT** 1111: Default
			TNRCSSM					x	x	x	x									**TNR start value of chroma LUT** 1111: Default
			TNRCLYM									x	x	x	x					**TNR luminance classification:** 0000: Strong noise reduction 1111: Slight noise reduction
			TNRCLCM													x	x	x	x	**TNR chrominance classification:** 0000: Strong noise reduction 1111: Slight noise reduction

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
Preframe Generator Master Channel																				
1Fh	W	VSM2_40	YBORDERM	x	x	x	x													**Y border value of display** Granularity: 16 0000: 0 0001: 16 1111: 240
			UBORDERM					x	x	x	x									**U border value of display** Granularity: 16 0000: 0 0001: 16 0111: 112 1000: -128 1111: -16
			VBORDERM									x	x	x	x					**V border value of display** Granularity: 16 0000: 0 0001: 16 0111: 112 1000: -128 1111: -16
			MPFBLBM													x	x	x	x	**Multi picture force background lines bottom** Number of lines of background color to be appended 0000: 0 lines 1111: 15 lines
20h	W	VSM2_40	MPFBPRM	x	x															**Multi picture force background pixels right** Number of pixels of background color to be appended 00: 0 pixels 01: 16 pixels 10: 32 pixels 11: 48 pixels
			MPFBLTM			x	x	x	x											**Multi picture force background lines top** Number of lines to be overwritten with background color from top 0000: 0 lines 1111: 15 lines
			GP0							x	x									**General purpose GP0 (pin 83)** 00: Tristate 01: Tristate 10: Low level 11: High level Note: QFP144 only
			NMCHAN										x							**Channel for noise measurement (picture)** 0: Master 1: Slave

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			SLOWVAR											x						**Modification of NOISE** 0: ***NOISE***~NOISE_SUM_REG 1: ***NOISE***=incremental steps
			AUTOGAP												x					**Modifies GAP for increasing homogenous regions** AUTOGAP==1&&STAT_SIZE==0: GAP+=8; AUTOGAP==1&&STAT_SIZE==1: GAP+=4; AUTOGAP==1&&STAT_SIZE==2: GAP+=2; AUTOGAP==0 || STAT_SIZE==3: GAP+=0;
			UPDATERATEM													x	x	x	x	**Update rate** ***UPDATERATEM****32+31 fields are necessary for the next update 0000: 31 1111: 511
21h	W	VSM2_40	FRCBGNDM	x																**Background generator in pre-frame generator** 0: Disabled 1: Enabled
			MPFBPLM		x	x	x	x	x											**Multi picture force background pixels left** Number of pixels to be overwritten with background color from left Granularity: 2 pixel 00000: 0 pixels 11111: 62 pixels
			GMSTTHV									x	x	x	x	x	x	x	x	**Global motion detection stock ticker threshold value** 00111100: Default
Horizontal Prescaler Master Channel																				
22h	W	VSM1_40	FRCMMODM	x																**Mosaic mode generator** 0: Disabled 1: Enabled
			APENSELM		x															**Active pixel enable select** 0: Count clock cycles (recommended for CVBS/RGB input) 1: Count active pixels (recommended for ITU656 input)
			HSCPRESCM					x	x	x	x	x	x	x	x	x	x	x	x	**Control signal for HSCALE in horizontal pre-scaler** Subsampling factor by prescaler is (int) 0: 1 (int) 2048: 1.5 (720 pixels) (int) 2371: 1.578 (->684 pixels) (int) 4095: 2 (540 pixels)
23h	W	VSM1_40	HAAPRESCM	x	x															**Horizontal antialiasing filter** 00: Filter bypassed 01: Force characteristic weak 10: Force characteristic strong 11: Automatic characteristic (weak or strong) *Note: For normal CVBS/RGB full-screen, filter should be set to weak or automatic characteristic. For ITU656 full-screen input, filter should be bypassed. Strong characteristic is for split-screen and PiP only.*

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			HDCPRESCM				x	x	x	x										**Horizontal pre-scaler decimates by** 0000: 1 0001: 2 0010: 3 0011: 4 0100: 6 0101: 8 0110: 12 0111: 16 1000: 24 1001: 32
			APPLIPM								x	x	x	x	x	x	x	x	x	**Active pixel per line (pre scaler)** Describes, how many decimated active pixels are generated. Granularity: 2 pixels (int) 0: 0 pixels (int) 342: 684 pixels (int) 511: 1022 pixels
24h	W	VSM1_40	MOTONM	x																**Line memories availability** 0: Available for vertical prescaler 1: Available for motion-detector
			GP2		x	x														**General purpose GP2 (pin 85)** 00: Tristate 01: Tristate 10: Low level 11: High level Note: QFP144 only
			GP1				x	x												**General purpose GP1 (pin 84)** 00: Tristate 01: Tristate 10: Low level 11: High level Note: QFP144 only
			NAPPLIPM							x	x	x	x	x	x	x	x	x	x	**Not active pixel per line (pre scaler)** Granularity: 2 clock cycles (int) 0: 0 pixels (int) 100: 200 pixels (int) 1023: 2046 pixels
Vertical Prescaler Master Channel																				
25h	W	VSM1_40	VAAPRESCM	x																**Vertical lowpass filter (pre-scaler)** 0: Disabled 1: Enabled
			VPKPRESCM		x	x	x	x	x											**Vertical peaking** 00000: Maximum vertical peaking (enhancement) 10000: Vertical peaking has no effect (flat) 11111: Maximum attenuation (damping)

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			VCRPRESCM							x										**Shift of chrominance signal** 0: No shift 1: One line upward (e.g. for VCR)
			NALPFIPM								x	x	x	x	x	x	x	x	x	**Not active lines per field input** (int) 0: Shift is 0 (int) 22: Shift is 22 lines (int) 511: Shift is 511 lines (max. shift is 1 field)
26h	W	VSM2_40	VPREBYPM	x																**Vertical prescaler by-pass** 0: Vertical pre scaler enabled 1: Vertical pre scaler by-passed
	W		VDCPRESCM			x	x	x	x											**Vertical pre-scaler decimates by** 0000: 1 0001: 2 0010: 3 0011: 4 0100: 6 0101: 8 0110: 12 0111: 16 1000: 24 1001: 32
			ALPFIPM							x	x	x	x	x	x	x	x	x	x	**Active lines per field (input processing)** (int) 0: No active line (int) 288: 288 active lines (int) 1023: 1023 lines
27h	W	VSM2_40	HORPOSNM	x	x															**Horizontal start position of active measurement area** 00: 0 01: 128 10: 256 11: 384
			HORWIDTHNM			x	x													**Duration of active measurement area** 00: 400 01: 600 10: 800 11: 1200
			VSCPRESCM					x	x	x	x	x	x	x	x	x	x	x	x	**Control signal for VSCALE in vertical pre-scaler** (int) 0: Scaling factor is 1 (int) 4095: Scaling factor is 2
Global Motion Detection Master Channel																				
28h	W	VSM2_40	GMSTTH[1]	x																**GMD stock ticker segment threshold** (int) 0: Default
			GMTHUM		x	x	x	x	x	x	x									**GMD spatial hysteresis: upper threshold** (int) 68: Default

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			GMSTSS									x	x	x						**GMD stock ticker segment start** (int)5: Default]
			GMASM												x	x	x	x	x	**GMD Amount of still pictures** (int) 29: Default
29h	W	VSM2_40	GMSTTH[0]	x																(see 28h)
			GMTHLM		x	x	x	x	x	x	x									**GMD spatial hysteresis: lower threshold** (int) 67: Default
			GMSTEN									x								**GMD stock ticker enable** 0: disabled 1: enabled
			GMSTSL										x	x						**GMD stock ticker segment length** (int)1: Default]
			GMAMM												x	x	x	x	x	**GMD amount of motion pictures** (int) 16: Default
2Ah	W	VSM2_40	GSTHUM	x	x	x	x	x	x	x	x									**GMD spatial hysteresis: upper threshold** (int) 11: Default
			GSTHLM									x	x	x	x	x	x	x	x	**GMD spatial hysteresis: lower threshold** (int) 10: Default
Film Mode Detection Master Channel																				
2Bh	W	VSM2_40	MDVFFON		x															**Motion detection vertical filter for frame difference** 0: Disabled 1: Enabled
			FMDSON			x														**FMD still detection on/off** Forces camera mode, if still sequence is d 0: Disabled 1: Enabled
			FMDCTH				x	x	x	x										**FMD threshold for dc level** (int) 7: Default]
			FMRES								x									**FMD reset** 0: Not forced 1: Forced to camera mode
			FMTHYON									x								**FMD temporal hysteresis on/off** 0: History length = 2 * (***FMMEMHIS***+1) 1: History length = 2 * (***FMMEMHIS***+1), camera-> film mode History length = 1* (***FMMEMHIS***+1), film -> camera mode
			FMTHRON										x							**FMD trash counter on/off** If trash counter > 120, the film mode detector switches automatically to camera mode. 0: Disabled 1: Enabled

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			FMSCALEL											x	x					**Limitation of lower boundary:** 00: 16 01: 32 10: 64 11: 64
			FMSCALEU													x	x			**Limitation of upper boundary:** 00: 256 01: 128 10: 64 11: 64
			FMREGION															x	x	**Region to be investigated by the film mode detector:** 00: Upper half (line 0 to line 127) 01: Lower half (line 128 to last line) 10: Complete picture 11: Complete picture
2Ch	W	VSM2_40	FMMEMHIS	x	x	x	x													**History length of film mode detection** (int) 3: Default
			FMATH					x	x	x	x	x	x							**FMD threshold for absolute value** (int) 10: Default
			FMDTH											x	x	x	x	x	x	**FMD threshold for difference value** (int) 15: Default
Motion Detection Master Channel																				
2Dh	W	VSM2_40	TFLDDON	x																**Temporal field delay on** 0: Two bit of field delayed motion values 1: One bit current motion value and one bit field delayed
			THRGM		x	x	x	x	x											**Threshold of frame difference in MD for global motion detection:** (int) 8: Default
			SVALFI							x	x									**Sensitivity factor of field difference** 00 : Factor 1(maximum) 01 : Factor 2 10 : Factor 4 11 : Factor 8 (minimum)
			SVALFR									x	x							**Sensitivity of frame difference** 00 : Factor 1(maximum) 01 : Factor 2 10 : Factor 4 11 : Factor 8 (minimum)
			AMMON											x	x					**Automatic movie mode detection** In case of movie mode, the motion detection will be automatically switched to 00 : Disabled 01 : Disabled 10 : Only frame difference 11 : No motion

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			SWGM													x	x			**Switch input value for global motion detection** 00: Frame difference, influenced by motion detection 01: Frame difference, not influenced by motion detection 10: Field difference, influenced by motion detection 11: Field difference, not influenced by motion detection
			TFDT															x	x	**Temporal filter delay time** 00: Factor 0 01: Factor 1 10: Factor 2 11: Factor 3
2Eh	W	VSM2_40	DTFDT[1]	x																**Switch double temporal filter delay time** 00: Single delay time 01: 4 times delayed 10: 8 times delayed 11: 16 times delayed
			THRMOV		x	x	x	x	x											**Threshold of field difference in MD for movie mode detection:** (int) 8: Default
			DTFDT[0]							x										**(See MSB)**
			THFR0								x	x	x	x						**Threshold for frame difference look up table:** (int) 3: Default
			TFON												x					**Temporal filter** 0: Disabled 1: Enabled
			THFI0													x	x	x	x	**Threshold for field difference look up table:** (int) 8: Default
2Fh	W	VSM2_40	SVALLI	x	x															**Sensitivity of line differences** 00 : Factor 4 (maximum) 01 : Factor 8 10 : Factor 16 11 : Factor 32 (minimum)
			THLI0			x	x	x	x											**Thresholds of line difference look up table:** (int) 4: Default
			FRAFION							x										**Frame or frame and field difference for motion detection** 0 : Based on frame difference only 1 : Based on frame and field difference *Note: In case of **AMMON** >1 and no movie mode, the motiondetection is still defined by **FRAFION*****
			THFR1								x	x	x	x						**Threshold for frame difference look up table:** (int) 4: Default
			THFI1												x	x	x	x	x	**Threshold for field difference look up table:** (int) 6: Default

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
30h	W	VSM2_40	THLI1		x	x	x	x	x											**Threshold for line difference look up table:** (int) 8: Default
			THFR2							x	x	x	x	x						**Threshold for frame difference look up table:** (int) 6: Default
			THFI2												x	x	x	x	x	**Threshold for field difference look up table:** (int) 18: Default
31h	W	VSM2_40	THLI2	x	x	x	x	x	x											**Threshold for line difference look up table:** (int) 12: Default
			THFR3							x	x	x	x	x						**Threshold for frame difference look up table:** (int) 10: Default
			THFI3												x	x	x	x	x	**Threshold for field difference look up table:** (int) 28: Default
Noise Measurement in Picture Content																				
32h	W	VSM1_40	GAPM	x	x	x	x	x	x											**Threshold for homogenous areas** 000000: 0 111111: 63
			SENSITIVM							x	x									**Fixes sensitivity of measurement** 00: NOISE_SUM_REG=NOISE_SUM*0.5 01: NOISE_SUM_REG=NOISE_SUM 10: NOISE_SUM_REG=NOISE_SUM*2 11: NOISE_SUM_REG=NOISE_SUM*4
			OFFSET									x	x	x	x	x	x	x	x	**Offset for eliminating standard noise** 00000000: 0 11111111: 255
Horizontal Post Scaler Master Channel																				
33h	W	VSBM2_36	HPANONM	x																**Horizontal panorama mode** 0: Panorama disabled 1: Panorama enabled
			DBDHPOSM		x															**Disable border detection (postscaler)** 0: Border detection active 1: Border detection not active
			CDELHPOSM			x														**Chrominance delay** 0: No delay 1: Half-pixel delay
			HSCPOSCM					x	x	x	x	x	x	x	x	x	x	x	x	**Horizontal scaling factor for post scaler** (int) 1024: Upsampling factor is 4 (int) 2910: Upsampling factor is 1.407 (int) 4095: Upsampling factor is 1

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
34h	W	VSBM2_36	HSEG1M[10:5]	x	x	x	x	x	x											**Beginning of segment 1 for horizontal panorama mode** Granularity: 2 pixels (int) 0: 0 pixel behind picture start (int) 2047: 4094 pixel behind picture start
			HINC0M								x	x	x	x	x	x	x	x	x	**Horizontal post-scaler increment 0** 100000000: -32 pixels 000000000: 0 pixels 011111111: 31.875 pixels
35h	W	VSBM2_36	HSEG1M[4:0]	x	x	x	x	x												(See 33h)
			HINC1M								x	x	x	x	x	x	x	x	x	**Horizontal post-scaler increment 1** 100000000: -32 pixels 000000000: 0 pixels 011111111: 31.875 pixels
36h	W	VSBM2_36	HSEG2M[10:5]	x	x	x	x	x	x											**Beginning of segment 2 for panorama mode** Granularity: 2 pixels (int) 0: 0 pixel behind picture start (int) 2047: 4094 pixel behind picture start
			HINC2M								x	x	x	x	x	x	x	x	x	**Horizontal post-scaler increment 2** 100000000: -32 pixels 000000000: 0 pixels 011111111: 31.875 pixels
37h	W	VSBM2_36	HSEG2M[4:0]	x	x	x	x	x												(see 36h)
			HINC3M								x	x	x	x	x	x	x	x	x	**Horizontal post-scaler increment 3** 100000000: -32 pixels 000000000: 0 pixels 011111111: 31.875 pixels
38h	W	VSBM2_36	HSEG3M[10:5]	x	x	x	x	x	x											**Beginning of segment 3 for panorama mode** Granularity: 2 pixels (int) 0: 0 pixel behind picture start (int) 2047: 4094 pixel behind picture start
			HINC4M								x	x	x	x	x	x	x	x	x	**Horizontal post-scaler increment 4** 100000000: -32 pixels 000000000: 0 pixels 011111111: 31.875 pixels
39h	W	VSBM2_36	HSEG3M[4:0]	x	x	x	x	x												(see 38h)
			HSEG4M						x	x	x	x	x	x	x	x	x	x	x	**Beginning of segment 4 for panorama mode** Granularity: 2 pixels (int) 0: 0 pixel behind picture start (int) 2047: 4094 pixel behind picture start

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
Vertical Post Scaler Master Channel																				
3Ah	W	VSBM2_36	VPANONM	x																**Vertical panorama mode** 0: Panorama disabled 1: Panorama enabled
			VDOUBLEM		x															**Vertical upsampling unit** 0: No doubling 1: Number of output lines is doubled by interpolation
			VSCPOSCM			x	x	x	x	x	x	x	x	x	x	x	x	x	x	**Vertical scaling factor for post scaler** (int) 256: Upsampling factor is 16 (int) 4096: Up/ downsampling factor is 1 (int) 8192: Downsampling factor is 2 (int) 16383: Downsampling factor is 4
3Bh	W	VSBM2_36	VSEG1M[9:5]	x	x	x	x	x												**Beginning of segment 1 for vertical panorama mode** (int) 0: 0 lines behind picture start (int) 1023: 1023 lines behind picture start (***VDOUBLE***=0) (int) 1023: 1023*2 lines behind picture start (***VDOUBLE***=1)
			VINC0M								x	x	x	x	x	x	x	x	x	**Vertical post-scaler increment 0** 100000000: Picture becomes bigger 000000000: No action 011111111: Picture becomes smaller
3Ch	W	VSBM2_36	VSEG1M[4:0]	x	x	x	x	x												(See 3Bh)
			VINC1M								x	x	x	x	x	x	x	x	x	**Vertical post-scaler increment 1** 100000000: Picture becomes bigger 000000000: No action 011111111: Picture becomes smaller
3Dh	W	VSBM2_36	VSEG2M[9:5]	x	x	x	x	x												**Beginning of segment 2 for vertical panorama mode** (int) 0: 0 lines behind picture start (int) 1023: 1023 lines behind picture start (***VDOUBLE***=0) (int) 1023: 1023*2 lines behind picture start (***VDOUBLE***=1)
			VINC2M								x	x	x	x	x	x	x	x	x	**Vertical post-scaler increment 2** 100000000: Picture becomes bigger 000000000: No action 011111111: Picture becomes smaller
3Eh	W	VSBM2_36	VSEG2M[4:0]	x	x	x	x	x												(See 3Bh)
			VINC3M								x	x	x	x	x	x	x	x	x	**Vertical post-scaler increment 3** 100000000: Picture becomes bigger 000000000: No action 011111111: Picture becomes smaller
3Fh	W	VSBM2_36	INVSKEW	x																**Invert skew signal from input PLL** 0: No inversion 1: Inversion

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			ARTSYNC		x															**LL-PLL input** 0: From CVBS input directly (PLL parallel mode) 1: From synthesizer
			ITUSYNC			x														**Input sync synthesizer source** 0: Use sync from front-end PLL (PLL serial mode) 1: Use itu656 sync
			SECDELM				x													**Secam v-delay** 0: Zero delay 1: Delay v-channel by 1 pixel
			PALDETIDLM					x	x											**PALDET identification level** 00: 240 01: 192 10: 128 11: 64
			VINC4								x	x	x	x	x	x	x	x	x	**Vertical Post-scaler increment 4** 100000000: Picture becomes bigger 000000000: No action 011111111: Picture becomes smaller
40h	W	VSBM2_36	VOFPOSC[7:3]	x	x	x	x	x												**Vertical post-scaler phase offset** Granularity: 16 (int) 0: Vertical offset for dto is 0 (int) 255: Vertical offset for dto is 4080
			VSEG3M							x	x	x	x	x	x	x	x	x	x	**Beginning of segment 3 for vertical panorama mode** (int) 0: 0 lines behind picture start (int) 1023: 1023 lines behind picture start (***VDOUBLE***=0) (int) 1023: 1023*2 lines behind picture start (***VDOUBLE***=1)
41h	W	VSBM2_36	VOFPOSC[2:0]	x	x	x														(See 40h)
			VSEG4M							x	x	x	x	x	x	x	x	x	x	**Beginning of segment 4 for vertical panorama mode** (int) 0: 0 lines behind picture start (int) 1023: 1023 lines behind picture start (***VDOUBLE***=0) (int) 1023: 1023*2 lines behind picture start (***VDOUBLE***=1)
Output Data Controller Master Channel																				
42h	W	VSBM2_36	DPBRT	x	x	x	x	x	x											Brightness 000000: + 48 LSB 110000: no offset 111111: - 15 LSB
			DPCON							x	x	x	x	x	x					Contrast 000000: 0 100000: 1 111111: 63/32

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			DPCNS													x				**Contrast noise shaper** 0: Disabled 1: Enabled
43h	R	VS1_20	PWADJCNTM				x	x	x	x	x									**Peak-white reduction** 00000: No reduction 11111: Max. reduction
			MINVM									x	x	x	x	x	x	x	x	**Measured sync amplitude** 00000000: Smallest sync 11111111: Largest sync
44h	R	VS2_20	PWADJCNTS				x	x	x	x	x									**Peak-white reduction** 00000: No reduction 11111: Max. reduction
			MINVS									x	x	x	x	x	x	x	x	**Measured sync amplitude** 00000000: Smallest sync 11111111: Largest sync
45h	W	VSBM2_36	AUTOFRRN	x	x															**Automatic freerun when sync-separartion not stable** 00: Disabled (keep H/V locked, if selected) 01: Vertical freerun when not stable 10: Horizontal freerun when not stable 11: Horizontal and vertical freerun when not stable Depends on color decoder which is selected to be master with **SELMASTER** and **SELSM**
			LPFIPMD			x														**Lines per field method** 0: Back-end 1: Front-end
			VINMTHD				x													**Vertical ODC line counting** 0: Field delay 1: Frame delay
			FIELDBINV					x												**Back-end field inversion** 0: No inversion 1: Inversion
			HORPOSM						x	x	x	x	x	x	x	x	x	x	x	**Horizontal position inside active picture area** (int) 32: Most left display position (int) 4095: Most right display position Values smaller than 32 are not usable
46h	W	VSBM2_36	SECDELS				x													**Secam v-delay** 0: Zero delay 1: Delay v-channel by 1 pixel

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			PALDETIDLS					x	x											**PALDET identification level** 00: 240 01: 192 10: 128 11: 64
			VERPOSM							x	x	x	x	x	x	x	x	x	x	**Vertical position inside active picture area** Granularity: 1 line (***FMODE***=0) or 2 lines (***FMODE***=1) (int) 0: Most top display position (int) (2047): Most bottom display position
47h	W	VSBM2_36	HORWIDTHM						x	x	x	x	x	x	x	x	x	x	x	**Horizontal picture width** Granularity: 2 pixels (int) 0: No display (int) 960: Default (int) 2047: 4094 pixels
48h	W	VSBM2_36	NOFHSYNC	x																**No fine horizontal synchronization** 0: Horizontal synchronization 1: Horizontal synchronization without finer steps
			VERWIDTHM						x	x	x	x	x	x	x	x	x	x	x	**Vertical picture width** (int) 0: 0 lines (int) 288: Default (int) 2047: 2047 lines
Picture Improvement Master Channel																				
49h	W	VSBM2_36	PKCTIBPM	x	x															**Peaking factor for CTI (bandpass part)** 00: 2 (CTI bp off) 01: 16 10: 24 11: 32
			PKCTIHPM			x	x													**Peaking factor for CTI (highpass part)** 00: 2 (CTI hp off) 01: 16 10: 24 11: 32
			LTIM					x												**Luminance transition improvement** 0: Disabled 1: Enabled
			APK1BPM[1:0]						x	x										**1st adaptive peaking factor (bandpass part)** 0000: 0.5 0100: 2.5 1111: 8

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			APK2BPM								x	x	x							**2nd adaptive peaking factor (bandpass part)** 000: 1 001: 2(peaking bp off) 011: 4 111: 8
			ATH1BPM											x	x					**Peaking denoising threshold (bandpass part)** 00: 0 (denoising off) 01: 2 10: 4 11: 8
			ATH2BPM													x	x			**2nd peaking threshold (bandpass part)** 00: 0 01: 4 10: 8 11: 16
			THEM															x	x	**Turningpoint threshold for CTI** 00: 1 01: 2 10: 3 11: 4
4Ah	W	VSBM2_36	APK1HPM[1:0]	x	x															**1st adaptive peaking factor (highpass part)** 0000: 0.5 0100: 2.5 1111: 8
			APK2HPM			x	x	x												**2nd adaptive peaking factor (highpass part)** 000: 1 001: 2 (peaking hp off) 011: 4 111: 8
			ATH1HPM						x	x										**Peaking denoising threshold (highpass part)** 00: 0 (denoising off) 01: 2 10: 4 11: 8
			ATH2HPM								x	x								**2nd peaking threshold (highpass part)** 00: 0 01: 4 10: 8 11: 16
			DBDPICIM										x							**Disable border detection (picture improvement)** 0: Border detection active 1: Border detection not active
			APK1BPM[3:2]											x	x					(See 49h)

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			APK1HPM[3:2]													x	x			(See 49h)
			CORONM															x		**Coring or denoising for low amplitudes** 0: Coring off, denoising on 1: Coring on, denoising off
Pixel Mixer Master Channel																				
4Bh	W	VSBM2_36	YFRAMEM					x	x	x	x									**Luminance value for the master frame (4MSB)** 0001: Default value (yields value 0001 00000=32)
			UFRAMEM									x	x	x	x					**Chrominance value for the master frame (4MSB)** 0000: Default value (yields value 0000 00000=0)
			VFRAMEM													x	x	x	x	**Chrominance value for the master frame (4MSB)** 0000: Default value (yields value 0000 00000=0)
Dynamic Contrast Improvement Master Channel																				
4Ch	W	VSDCI_36	SPIXELM	x	x	x	x	x												**Start pixel number for analysis window** START= ***SPIXEL*** x 8 (int) 2: 16 pixels
			EPIXELM						x	x	x	x	x	x	x					**End pixel number for analysis window** END = ***EPIXEL*** x 8 + 512 (int) 54: 944 pixels
			ENA_DEMOM													x				**Enable split-screen demo mode** 0: Disabled 1: Enabled
			SCAN_IDM														x			**Scanning mode for DCI** 0: Interlaced 1: Progressive
			CSC_ONM															x		**Color saturation compensation** 0: Disabled 1: Enabled
			DCIONM																x	**Digital contrast improvement (DCI)** 0: Disabled 1: Enabled The analysis continues also if **DCI_ONM** = 0, but it has no effect to the output.
4Dh	W	VSDCI_36	SLINEM	x	x	x	x													**Start line number for analysis window** START = ***SLINE*** x 8 (int) 1: 8 lines
			ELINEM					x	x	x	x	x	x							**End line number for analysis window** END = ***ELINE*** x 8 + 128 (int) 55: 568 lines

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			DCI_CORM											x	x	x	x	x		**DCI coring level for adaptive signal split** (int) 0: No coring (int) 5: Default (int) 31: Max. coring
			FREEZE_ANLM																x	**DCI analysis on/off (only for test purpose)** 0: Disabled 1: Enabled
4Eh	W	VSDCI_36	PIXELPLINEM	x	x	x	x	x	x	x	x	x	x	x						**Total number of active pixel per line** (int) 960: 960 pixel
			AB_FTCM												x	x	x	x	x	**Filter time constant for average brightness** (int) 16: 16 frames of settling tine of DCI analysis
4Fh	W	VSDCI_36	SENSWSM	x	x	x	x	x	x	x	x									**Sensitivity of average brightness analysis (ABA)** (int) 40: Default
			LSWFM													x	x	x	x	**Light sample weighting factor** (int) 2: Default
50h	W	VSDCI_36	SENSBSM	x	x	x	x	x	x	x	x									**Sensitivity of dark sample distribution analysis (DSDA)** (int) 40: Default
			DSFTCM												x	x	x	x	x	**Filter time constant for dark sample distribution** (int) 16: Default
51h	W	VSDCI_36	ERRORCMPM	x	x	x	x	x	x	x	x	x	x							**Correction factor SENSBS x 32/DYTC** (int) 75: Default
			DYTCM											x	x	x	x	x	x	**Dark area size for DSDA** (int) 17: Default
52h	W	VSDCI_36	PK_FTCM				x	x	x	x	x									**Filter time constant for frame peak value** (int) 16: Default
			PEAK_SIZEM													x	x	x	x	**Peak area size. Range [0...9] (internally limited to max.9]** (int) 4: Default
MAU																				
53h	W	VSBM1_36	MVCOFA0	x	x															**Motion value factor 0 for actual field for calculating motion result without accumulator** 00: *0 01: *1 10: *2 11: *3

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			MVCOFA1			x	x	x												**Motion value factor 1 for actual field for calculating motion result without accumulator** 000: *1 001: *2 010: *3 011: *4 100: *5 101: *6 110: *7 111: *8
			MVCOFP0						x	x										**Motion value factor 0 for previous field for calculating motion result without accumulator** 00: *0 01: *1 10: *2 11: *3
			MVCOFP1								x	x	x							**Motion value factor 1 for previous field for calculating motion result without accumulator** 000: *1 001: *2 010: *3 011: *4 100: *5 101: *6 110: *7 111: *8
			MVDIVA											x	x					**Motion value divider for actual field for calculating motion result without accumulator** 00: /1 01: /2 10: /4 11: /8
			MVDIVP													x	x			**Motion value divider for previous field for calculating motion result without accumulator** 00: /1 01: /2 10: /4 11: /8
			MVDIVR															x	x	**Motion value divider for calculating motion result without accumulator** 00: /1 01: /2 10: /4 11: /8
54h	W	VSBM1_36	MVMODE	x																**Method selection for creation the motion value result** 0: Accumulator method 1: New method w/o accumulator

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			MVREFPOS		x															**Indicating the reference position for MvMode = 0** 0: Delayed value 1: Actual value
			SMMODE			x														**Soft mix method selection** 0: 2 field access 1: 3 field access (Only valid in field jam mode)
			MVFIXENA				x													**Enabling the fixed motion value** 0: Use incoming motion values 1: Use value adjusted by MvFixVal
			MVFIXVAL					x	x	x										**Fixed motion value used if MvFixEna is enabled**
			GMFMFBENA											x						**Global motion film mode fallback enable** 0: Global motion fallback is disabled for film mode phases 1: Global motion fallback is enabled for film mode phases
			GSFMFBENA												x					**Global still film mode fallback enable** 0: Global still fallback is disabled for film mode phases 1: Global still fallback is enabled for film mode phases
			GSTILLENA													x				**Global still enable** 0: Off 1: On
			MVVISENA														x			**Motion value visibility enable** 0: Off 1: On
			FJSELLNV															x		**Field jam selection inversion** Inverts the field jam selection output bit 0: No inversion 1: Inversion
			MVCHOLD																x	**Motion value chrominance UV hold switch** 0: Use new motion value on each incoming motion value 1: Use motion value for u channel for v channel also (hold)
55h	W	VSBM1_36	DYNOPMSV	x	x	x														**Dynamic operation table entry:** Motion sequence when **video mode** active 000: MotSeqAAAA 001: MotSeqBBBB 010: MotSeqAABB 011: MotSeqABBA 100: MotSeqBBAA 101: MotSeqBAAB 110: MotSeqABAB 111: MotSeqBABA

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			DYNOPITV				x	x	x											**Dynamic operation table entry:** Interpolation type when **video mode** active 000: IpolTypeAB 001: IpolTypeLineDb 010: IpolTypeLin2 011: (reserved) 100: IpolTypeLin4
			DYNOPSMV							x										**Dynamic operation table entry:** Soft mix enable switch position when **video mode** active 0: Soft mix disabled 1: Soft mix enabled
			DYNOPFJV								x									**Dynamic operation table entry:** Field jam switch position when **video mode** active 0: Get old stored field data 1: Get new incoming field data
			DYNOPMSP0									x	x	x						**Dynamic operation table entry:** Motion sequence when 2-2-pull-down **(PAL) film mode phase 0** active 000: MotSeqAAAA 001: MotSeqBBBB 010: MotSeqAABB 011: MotSeqABBA 100: MotSeqBBAA 101: MotSeqBAAB 110: MotSeqABAB 111: MotSeqBABA
			DYNOPITP0												x	x	x			**Dynamic operation table entry:** Interpolation type when 2-2-pull-down **(PAL) film mode phase 0** active 000: IpolTypeAB 001: IpolTypeLineDb 010: IpolTypeLin2 011: (reserved) 100: IpolTypeLin4
			DYNOPSMP0															x		**Dynamic operation table entry:** Soft mix enable switch position when 2-2-pull-down **(PAL) film mode phase 0** active 0: Soft mix disabled 1: Soft mix enabled
			DYNOPFJP0																x	**Dynamic operation table entry:** Field jam switch position when 2-2-pull-down **(PAL) film mode phase 0** active 0: Get old stored field data 1: Get new incoming field data

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
56h	W	VSBM1_36	DYNOPLSGM	x	x	x														**Dynamic operation table entry:** Line scan pattern sequence when **global motion** active 000: LspSeqAAAA 001: LspSeqBBBB 010: LspSeqAABB 011: LspSeqABBA 100: LspSeqBBAA 101: LspSeqBAAB 110: LspSeqABAB 111: LspSeqBABA
			DYNOPLSGS				x	x	x											**Dynamic operation table entry:** Line scan pattern sequence when **global still** active 000: LspSeqAAAA 001: LspSeqBBBB 010: LspSeqAABB 011: LspSeqABBA 100: LspSeqBBAA 101: LspSeqBAAB 110: LspSeqABAB 111: LspSeqBABA
			OPPHASEFR							x										**Linescan pattern freerun** 0: lsp freerun disabled 1: lsp freerun enabled
			DYNOPLSV								x	x	x							**Dynamic operation table entry:** Line scan pattern sequence when **video mode** active 000: LspSeqAAAA 001: LspSeqBBBB 010: LspSeqAABB 011: LspSeqABBA 100: LspSeqBBAA 101: LspSeqBAAB 110: LspSeqABAB 111: LspSeqBABA
			DYNOPLSP0											x	x	x				**Dynamic operation table entry:** Line scan pattern sequence when 2-2-pull-down **(PAL) film mode phase 0** active 000: LspSeqAAAA 001: LspSeqBBBB 010: LspSeqAABB 011: LspSeqABBA 100: LspSeqBBAA 101: LspSeqBAAB 110: LspSeqABAB 111: LspSeqBABA

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			DYNOPLSP1														x	x	x	**Dynamic operation table entry:** Line scan pattern sequence when 2-2-pull-down **(PAL) film mode phase 1** active 000: LspSeqAAAA 001: LspSeqBBBB 010: LspSeqAABB 011: LspSeqABBA 100: LspSeqBBAA 101: LspSeqBAAB 110: LspSeqABAB 111: LspSeqBABA
57h	W	VSBM1_36	DYNOPLSN	x	x	x														**Dynamic operation table entry:** Line scan pattern sequence when 2-3-pull-down **(NTSC) film mode phase 0** active 000: LspSeqAAAA 001: LspSeqBBBB 010: LspSeqAABB 011: LspSeqABBA 100: LspSeqBBAA 101: LspSeqBAAB 110: LspSeqABAB 111: LspSeqBABA
			FMFORCETRIG				x													**Force the actual adjusted FM phase (FmForce) if strictly force of FM PAL or FM NTSC is selected (FmForce = 1/2/3/4/5/6/7)** As long as the trigger is set the phase is forced to the selected value On I2C_FmForce = 0/8/9/10/11-15 this parameter has no effect 0: Phase forcing is disabled 1: Phase forcing is enabled
			FJMODE					x	x											**Field jam mode selector** 00: Field jam disabled 01: Field jam enabled but always soft mix mode is activated 10: Field jam enabled and forced 11: Field jam enabled with adaptive behavior to film mode generator
			NEGLINESEL							X										**Control signal for the line select generator output** (int) 0: LineSel is NOT altered (int) 1: LineSel is inverted

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			FMFORCE								x	x	x	x						**Indicates film mode force/hold method** 0000: Strictly force VIDEO 0001: Strictly force FM PAL (initial phase 0) 0010: Strictly force FM PAL (initial phase 1) 0011: Strictly force FM NTSC (initial phase 0) 0100: Strictly force FM NTSC (initial phase 1) 0101: Strictly force FM NTSC (initial phase 2) 0110: Strictly force FM NTSC (initial phase 3) 0111: Strictly force FM NTSC (initial phase 4) 1000: Auto detect & hold VIDEO 1001: Auto detect and hold FM PAL 1010: Auto detect & hold FM NTSC 1011: Auto detect and hold VIDEO or FM PAL 1100: Auto detect and hold VIDEO or FM NTSC 1101: Auto detect and hold FM PAL or FM NTSC 1110: Force/hold disabled, use FM detector result 1111: Force/hold disabled, use FM detector result
			INITLINESEL												x					**Control signal for the line select generator initialisation** (int) 0: Init value for LineSel is 0 (int) 1: Init value for LineSel is 1
			STATOPMSC													x	x	x		**Chrominance static operation motion sequence** If enabled use always this motion sequence for chrominance signals 000: MotSeqAAAA 001: MotSeqBBBB 010: MotSeqAABB 011: MotSeqABBA 100: MotSeqBBAA 101: MotSeqBAAB 110: MotSeqABAB 111: MotSeqBABA
			STATOPMSCENA																x	**Chrominance static operation motion sequence enable switch** Enable signal for separate static chrominance motion sequence 0: Use motion sequence from dynamic operation table 1: Use StatOpMsC motion sequence for chroma channel only
58h	W	VSBM1_36	DYNOPMSGM	x	x	x														**Dynamic operation table entry:** Motion sequence when **global motion active** 000: MotSeqAAAA 001: MotSeqBBBB 010: MotSeqAABB 011: MotSeqABBA 100: MotSeqBBAA 101: MotSeqBAAB 110: MotSeqABAB 111: MotSeqBABA

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			DYNOPITGM				x	x	x											**Dynamic operation table entry:** Interpolation type when **global motion active** 000: IpolTypeAB 001: IpolTypeLineDb 010: IpolTypeLin2 011: (reserved) 100: IpolTypeLin4
			DYNOPSMGM							x										**Dynamic operation table entry:** Soft mix enable switch position when **global motion active** 0: Soft mix disabled 1: Soft mix enabled
			DYNOPFJGM								x									**Dynamic operation table entry:** Field jam switch position when **global motion active** 0: Get old stored field data 1: Get new incoming field data
			DYNOPMSGS									x	x	x						**Dynamic operation table entry:** Motion sequence when **global still** active 000: MotSeqAAAA 001: MotSeqBBBB 010: MotSeqAABB 011: MotSeqABBA 100: MotSeqBBAA 101: MotSeqBAAB 110: MotSeqABAB 111: MotSeqBABA
			DYNOPITGS												x	x	x			**Dynamic operation table entry:** Interpolation type when **global still** active 000: IpolTypeAB 001: IpolTypeLineDb 010: IpolTypeLin2 011: (reserved) 100: IpolTypeLin4
			DYNOPSMGS															x		**Dynamic operation table entry:** Soft mix enable switch position when **global still**active 0: Soft mix disabled 1: Soft mix enabled
			DYNOPFJGS																x	**Dynamic operation table entry:** Field jam switch position when **global still** active 0: Get old stored field data 1: Get new incoming field data

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
59h	W	VSBM1_36	DYNOPMSN0	x	x	x														**Dynamic operation table entry:** Motion sequence when 2-3-pull-down **(NTSC) film mode phase 0** active 000: MotSeqAAAA 001: MotSeqBBBB 010: MotSeqAABB 011: MotSeqABBA 100: MotSeqBBAA 101: MotSeqBAAB 110: MotSeqABAB 111: MotSeqBABA
			DYNOPITN0				x	x	x											**Dynamic operation table entry:** interpolation type when 2-3-pull-down **(NTSC) film mode phase 0** active 000: IpolTypeAB 001: IpolTypeLineDb 010: IpolTypeLin2 011: (reserved) 100: IpolTypeLin4
			DYNOPSMN0							x										**Dynamic operation table entry:** Soft mix enable switch position when 2-3-pull-down **(NTSC) film mode phase 0** active 0: Soft mix disabled 1: Soft mix enabled
			DYNOPFJN0								x									**Dynamic operation table entry:** Field jam switch position when 2-3-pull-down **(NTSC) film mode phase 0** active 0: Get old stored field data 1: Get new incoming field data
			DYNOPMSN1									x	x	x						**Dynamic operation table entry:** Motion sequence when 2-3-pull-down **(NTSC) film mode phase 1** active 000: MotSeqAAAA 001: MotSeqBBBB 010: MotSeqAABB 011: MotSeqABBA 100: MotSeqBBAA 101: MotSeqBAAB 110: MotSeqABAB 111: MotSeqBABA
			DYNOPITN1												x	x	x			**Dynamic operation table entry**: Interpolation type when 2-3-pull-down **(NTSC) film mode phase 1** active 000: IpolTypeAB 001: IpolTypeLineDb 010: IpolTypeLin2 011: (reserved) 100: IpolTypeLin4

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			DYNOPSMN1															x		**Dynamic operation table entry:** Soft mix enable switch position when 2-3-pull-down **(NTSC) film mode phase 1** active 0: Soft mix disabled 1: Soft mix enabled
			DYNOPFJN1																x	**Dynamic operation table entry:** Field jam switch position when 2-3-pull-down **(NTSC) film mode phase 1** active 0: Get old stored field data 1: Get new incoming field data
5Ah	W	VSBM1_36	DYNOPMSN2	x	x	x														**Dynamic operation table entry:** Motion sequence when 2-3-pull-down **(NTSC) film mode phase 2** active 000: MotSeqAAAA 001: MotSeqBBBB 010: MotSeqAABB 011: MotSeqABBA 100: MotSeqBBAA 101: MotSeqBAAB 110: MotSeqABAB 111: MotSeqBABA
			DYNOPITN2				x	x	x											**Dynamic operation table entry:** interpolation type when 2-3-pull-down **(NTSC) film mode phase 2** active 000: IpolTypeAB 001: IpolTypeLineDb 010: IpolTypeLin2 011: (reserved) 100: IpolTypeLin4
			DYNOPSMN2							x										**Dynamic operation table entry:** Soft mix enable switch position when 2-3-pull-down **(NTSC) film mode phase 2** active 0: Soft mix disabled 1: Soft mix enabled
			DYNOPFJN2								x									**Dynamic operation table entry** Field jam switch position when 2-3-pull-down **(NTSC) film mode phase 2** active 0: Get old stored field data 1: Get new incoming field data
			DYNOPMSN3									x	x	x						**Dynamic operation table entry:** Motion sequence when 2-3-pull-down **(NTSC) film mode phase 3** active 000: MotSeqAAAA 001: MotSeqBBBB 010: MotSeqAABB 011: MotSeqABBA 100: MotSeqBBAA 101: MotSeqBAAB 110: MotSeqABAB 111: MotSeqBABA

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			DYNOPITN3												x	x	x			**Dynamic operation table entry:** Interpolation type when 2-3-pull-down **(NTSC) film mode phase 3** active 000: IpolTypeAB 001: IpolTypeLineDb 010: IpolTypeLin2 011: (reserved) 100: IpolTypeLin4
			DYNOPSMN3															x		**Dynamic operation table entry:** Soft mix enable switch position when 2-3-pull-down **(NTSC) film mode phase 3** active 0: Soft mix disabled 1: Soft mix enabled
			DYNOPFJN3																x	**Dynamic operation table entry:** Field jam switch position when 2-3-pull-down **(NTSC) film mode phase 3** active 0: Get old stored field data 1: Get new incoming field data
5Bh	W	VSBM1_36	DYNOPMSN4	x	x	x														**Dynamic operation table entry:** Motion sequence when 2-3-pull-down **(NTSC) film mode phase 4** active 000: MotSeqAAAA 001: MotSeqBBBB 010: MotSeqAABB 011: MotSeqABBA 100: MotSeqBBAA 101: MotSeqBAAB 110: MotSeqABAB 111: MotSeqBABA
			DYNOPITN4				x	x	x											**Dynamic operation table entry:** Interpolation type when 2-3-pull-down **(NTSC) film mode phase 4** active 000: IpolTypeAB 001: IpolTypeLineDb 010: IpolTypeLin2 011: (reserved) 100: IpolTypeLin4
			DYNOPSMN4							x										**Dynamic operation table entry:** Soft mix enable switch position when 2-3-pull-down **(NTSC) film mode phase 4** active 0: Soft mix disabled 1: Soft mix enabled
			DYNOPFJN4								x									**Dynamic operation table entry:** Field jam switch position when 2-3-pull-down **(NTSC) film mode phase 4** active 0: Get old stored field data 1: Get new incoming field data

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			DYNOPMSP1									x	x	x						**Dynamic operation table entry:** Motion sequence when 2-2-pull-down **(PAL) film mode phase 1** active 000: MotSeqAAAA 001: MotSeqBBBB 010: MotSeqAABB 011: MotSeqABBA 100: MotSeqBBAA 101: MotSeqBAAB 110: MotSeqABAB 111: MotSeqBABA
			DYNOPITP1												x	x	x			**Dynamic operation table entry:** interpolation type when 2-2-pull-down **(PAL) film mode phase 1** active 000: IpolTypeAB 001: IpolTypeLineDb 010: IpolTypeLin2 011: (reserved) 100: IpolTypeLin4
			DYNOPSMP1															x		**Dynamic operation table entry:** Soft mix enable switch position when 2-2-pull-down **(PAL) film mode phase 1** active 0: Soft mix disabled 1: Soft mix enabled
			DYNOPFJP1																x	**Dynamic operation table entry:** Field jam switch position when 2-2-pull-down **(PAL) film mode phase 1** active 0: Get old stored field data 1: Get new incoming field data
5Ch			GCMON																x	**ProgressivePicture Improvement** 0: off 1: on
5Dh	W	NTO	FRINC[18:3]	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	**HDTO freerunning frequency** Granularity=103 Hz (int) 33981 (minimum: nominal pixel clock= 3.5 MHz) (int) 349525 (nominal pixel clock= 36 MHz) (int) 388362 (maximum: nominal pixel clock= 40 MHz)
5Eh	W	NTO	FJMODE					x	x											(see 57h)
			FRZLIMLR												x					**Reduce hold-range of LLPLL in unlocked HPLL state** 0: Disabled 1: Enabled
			FRFIX													x				**Freerunning clocks** 0: From fixed clock divider 1: From freerunning DTO (adjustable clocks)
			FRINC[2:0]														x	x	x	(See 5Dh)

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
5Fh	W	VS1_20	INCOMBC	x	x															**Chroma Input for comb filter** 00: ADC 2 01: Blue ADC 10: Red ADC 11: (Reserved)
			BELLIIRM[2]			x														(See 11h)
			BELLFIRM[2]				x													(See 11h)
			DEEMPIIRM[2]					x												(See 10h)
			DEEMPFIRM[3]						x											(See 10h)
			AMSTD50M								x	x								**Automatic standard detection priority 50 Hz** 00: PAL B 01: SECAM 10: (Reserved) 11: Automatic
			AMSTD60M										x	x						**Automatic standard detection priority 60 Hz** 00: NTSC M 01: NTSC44/PAL60 10: (Reserved) 11: Automatic
			SYNCGAINM												x					**Reference for sync-AGC** 0: Normal reference 1: Referenc reduced by 2%
			AGCPWRESM													x				**AGC peak-white counter reset** 0: No reset 1: Reset
			H50SKEW														x			**De-skewing of H50 pulse** 0: Disabled 1: Enabled
			AGCTHDM															x	x	**AGC hysterisys** 00: Broad 01: Medium 1 10: Medium 2 11: Small
60h	W	VS1_20	MVPM	x																**Vertical length measurement with vertical pulse detection** 0: Disabled 1: Enabled
			MVPGM		x															**Vertical pulse gating** 0: Disabled 1: Enabled
			SLNCW			x	x	x	x	x										**Slicer line number CC or WSS**

Table 3–13: Master channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			SLNRUW								x	x	x	x	x					**Slicer line number US-WSS**
			DDR_CC													x				**Double data rate CC (test only)** 0: Normal data-rate 1: Double data-rate
			BGSHIFTM														x			**Clamp signal adapation** 0: Disabled 1: Enabled *Note: MUST be enabled when internal 4H comb-filter is used for master. MUST be disabled, if no or external comb-filter is used for master.*
			REMDEL2															x		**Combfilter compensation delay (ADC2)** 0: Enabled 1: Disabled
			REMDEL1																x	**Combfilter compensation delay (ADC1)** 0: Enabled 1: Disabled
61h	W	VS656_27	HSPPL	x	x	x	x	x	x	x	x									**Hsync shift** Shift=HSPPL * 4 00000000: Default
			VSLPF										x	x	x	x	x	x	x	**Vsync shift** Shift=VSLPF * 4 0000000: Default
62h	R	NTO	REFTRIMRD	x	x	x	x	x	x	x	x									**Reference value bandgap** 01000000: Low reference 00000000: Medium reference 00111111: High reference 1XXXXXXX: Reference disabled, resistor used contains fused value only when **REFTRIMEN**=0.
			REFTRIMCVRD									x	x	x	x					**Reference value CVBS ADC** 0000: Narrow 1111: Wide *Note: Contains fused value only when REFTRIMEN=0.*
			REFTRIMRGBRD													x	x	x	x	**Reference value RGB ADC** 0000: Narrow 1111: Wide *Note: Contains fused value only when REFTRIMEN=0.*

3.9.2. Slave Channel

Table 3–14: Slave channel

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
Color Decoder Slave																				
63h	W	VS2_20	MVPS	x																**Vertical length measurement with vertical pulse detection** 0: Disabled 1: Enabled
			MVPGS		x															**Vertical pulse gating** 0: Disabled 1: Enabled
			BELLIIRS[2]			x														(See 75h)
			BELLFIRS[2]				x													(See 75h)
			DEEMPIIRS[2]					x												(See 74h)
			DEEMPFIRS[3]						x											(See 74h)
			AMSTD50S								x	x								**Automatic standard detection priority 50 Hz** 00: PAL B 01: SECAM 10: (Reserved) 11: Automatic
			AMSTD60S										x	x						**Automatic standard detection priority 60 Hz** 00: NTSC M 01: NTSC44/PAL60 10: (Reserved) 11: Automatic
			SYNCGAINS												x					**Reference for sync-AGC** 0: Normal reference 1: Referenc reduced by 2%
			AGCPWRESS													x				**AGC peak-white counter reset** 0: No reset 1: Reset
			BGSHIFTS														x			**Clamp signal adapation** 0: Disabled 1: Enabled *Note: MUST be enabled when internal 4H comb-filter is used for slave. MUST be disabled, if no or external comb-filter is used for slave.*
			AGCTHDS															x	x	**AGC hysterisys** 00: Broad 01: Medium 1 10: Medium 2 11: Small

Table 3–14: Slave channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
64h	W	VS2_20	SYNCFTHDS	x	x															**SYNCF threshold** 00: 4 lines 01: 3 lines 10: 2 lines 11: 1 line
			VTHRH60S			x	x	x	x	x	x	x								**Vertical Sync Gating: Closing 60 Hz** Closing=262+4*__VTHRH60M__ 0000000: Closing in line 262 1111111: Closing in line 770
			VTHRL60S										x	x	x	x	x	x	x	**Vertical Sync Gating: Opening 60 Hz** Opening=4*__VTHRL60M__ 0000000: Opening in first line 1111111: Opening in line 508
65h	W	VS2_20	CONSS	x	x	x														**Color switched on at level above CKILLS (SECAM)** At level=CKILLS+CONS 000: Min value 010: Default 111: Max value
			COLONS				x													**Forces color on** 0: Color depends on color decoder status 1: Color always on
			CPLLOFS					x												**Opens the closed loop** 0: Normal operation 1: Chroma PLL opened
			LPPOSTS						x											**Enabling of additional lowpass filtering of luminance channel** 0: No filtering 1: Filtering
			ACCFIXS							x										**Fix ACC to nominal value** 0: ACC is working 1: ACC is set to fixed value according to **PALREFS**/**NTSCREFS**
			ACCFRZS								x									**Freeze ACC** 0: ACC is working 1: ACC is frozen at current value
			FLINES									x								**Mode selection** 0: Interlace input 1: Progressive input
			FLDINVS										x							**Field inversion** 0: No inversion 1: Inversion
			CLPSTGYS											x						**Clamping strategy** 0: Back-porch clamping 1: Sync-tip-clamping

Table 3–14: Slave channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			DISCHCHS												x					**Disable channel change signal** 0: Color decoder not reset after channel-change 1: Color decoder reset after channel change
			CLMPD1S													x	x	x	x	**Clamping duration CD2, signals 1** Granularity: 200 ns 0000: 0 µs 0111: 1.4 µs 1111: 3 µs
66h	W	VS2_20	CONS	x	x	x														**Color switched on at level above CKILL (PAL/NTSC)** Level=CKILL+CON 000: Min value 010: Default 111: Max value
			UVCORS				x	x												**Chrominance coring** 00: Off 01: ± 1LSB 10: ± 2LSB 11: ± 3LSB
			SECNTCHS						x	x										**Selection of notch filter behaviour in SECAM mode** 00: 4.406 MHz 01: 4.250 MHz 10: 4.33 MHz 11: 4.406 / 4.205 dependent on line switch
			HPOLS								x	x								**H polarity at HINP** 00: Use Hsync 01: Use inverted Hsync 10: Autodetect polarity 11: (Reserved)
			FHDETS										x							**Automatic multisync capability** 0: Disabled 1: Enabled
			COMBUSES											x	x					**Comb filter usage CD2** 00: Use first CVBS input 01: Use second CVBS input 10: Use comb-filter 11: ADCG / ADCF (dependent on ***ADCSEL***)
			CLMPD2S													x	x	x	x	**Clamping duration CD2, signals 1** Granularity: 0000: 0 µs 0111: 1.4 µs 1111: 3 µs

Table 3–14: Slave channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
67h	W	VS2_20	PWTHDS	x	x															**Selection of "Peak-White" Threshold** 00: 448 01: 470 10: 500 11: 511
			CRCBS			x	x													**Choice of UV or CrCb output** 00: UV color space 01: CrCb color space 10: Modified CrCb color space (SECAM only)
			LMOFSTS					x	x											**Luminance offset** 00: No offset (NTSC) 01: - 7.5 IRE 10: + 7.5 IRE (PAL, SECAM) 11: -3.7 IRE *Note: A 7.5 IRE offset is added during blanking in display processing. When chosing 10, the luminance offset is equal to the offset of the CVBS input as in both picture and blanking the same 7.5 IRE offset is used.*
			VINPS							x										**Vertical pulse detection** 0: From sync signal (CVBS, Y, or G)) 1: From separate V-input pin *Note: When set to 0, no V polarity detection possible*
			YCSELS								x									**Y/C select** 0: CVBS input 1: Y/C input
			NOSIGBS									x								**No signal behavior** 0: Noisy screen when out of sync 1: Colored background insertion instead
			HINPS										x							**Synchronization input** 0: Synchronization from CVBS front-end (CVBS or Y/C) 1: Synchronization via RGB front-end (green or fbl ADC) When set to 0, no H polarity detection possible
			CLMPST1S											x	x	x	x	x	x	**Measurement start CD2, Signals 1** 000000:0 µs 011100:5.6 µs 111111: 12.8 µs
68h	W	VS2_20	VFLYWHLMDS	x	x															**Vertical flywheel mode** 00: Check for correct standard 01: 3 lines deviation allowed 10: 4 lines deviation allowed, no check for interlace 11: 5 lines deviation allowed, no check for interlace
			CHRFS			x	x	x	x	x	x									**Chroma bandwidth** Selects chroma bandwidth 011100: Nominal bandwidth

Table 3–14: Slave channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			PLLTCS									x	x							**Time constant HPLL (VCR...TV)** 00: Very fast 01: Fast 10: Slow 11: Very slow
			CLMPST2S											x	x	x	x	x	x	**Clamping start CD2, Signals 2** 000000: 0 µs 011100: 5.6 µs 111111: 12.8 µs
69h	W	VS2_20	COMBS	x																**Delay line** 0: Use delay line 1: Do not use delay line (only suited for NTSC)
			CSTANDS		x	x	x	x	x	x	x									**Color standard assignment** 0000000: No color standard chosen 0000001: PAL N 0000010: PAL B 0000100: SECAM 0001000: PAL 60 0010000: PAL M 0100000: NTSC M 1000000: NTSC 44 For allowed combinations please refer to chapter “chroma decoder” 1100110: PALB/SECAM/NTSCM/NTSC44/PAL60
			CKILLS									x	x	x	x	x	x	x	x	**Chroma level for color off (PAL/NTSC)** 00000000: High burst amplitude 01000000: Default 11111111: Low burst amplitude
6Ah	W	VS2_20	CKILLSS	x	x	x	x	x	x	x	x									**Chroma level for color off (SECAM)** 00000000: Low burst amplitude 01000000: Default 11111111: High burst amplitude Behavior is opposite to **CKILL** (PAL/NTSC case)
			FHFRRNS									x	x	x	x	x	x	x	x	**Free running frequency of horizontal PLL** 00000000: 384 clocks (52.7 kHz) 11100100: 1296 clocks (15.625 kHz) 11111111: 1404 clocks (14.423 kHz)
6Bh	W	VS2_20	VPOLS	x	x															**V Polarity at VINP** 00: Use Vsync 01: Use inverted Vsync 10: Autodetect polarity 11: (Reserved)
			THRSELS			x														**H slicing level threshold** 0: 50 % 1: 37 %

Table 3–14: Slave channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			YCDELS				x	x	x	x	x									**Luminance delay** 10000: 800 ns 0000: No delay 01111: -700 ns
			DISALLRESS									x								**Disable all chroma resets** 0: Resets allowed 1: Resets disabled May only be used if ONE color standard is selected
			SATNRS										x							**Noise reduction for satellite signal** 0: Disabled 1: Enabled
			NSREDS											x	x	x				**Noise reduction for horizontal PLL** 000: 1/8 001: 1/4 010: 1/2 011: 1 100: 2 101: 4 110: 8 111: 16
			LPCDELS														x	x	x	**Window shift for fine error calculation** 100: -4 clock cycles 000: No offset 011: +3 clock cycles
6Ch	W	VS2_20	HUES	x	x	x	x	x	x	x	x									**Hue control (tint)** 10000000: -89° 00000000: 0° 01111111: +88°
			VSHIFTS									x	x	x	x	x	x	x	x	**Field detection window shift** 00000000: No shift 11111111: Shifted by 2048
6Dh	W	VS2_20	NTSCREFS	x	x	x	x	x	x	x	x									**ACC reference adjustment (NTSC)** 00000000: Low reference value 10010001: Nominal value 11111111: High reference value
			PALIDL1S									x								**PAL/NTSC identification level 1** 0: Less sensitive (192) 1: More sensitive (64)
			VTHRL50S										x	x	x	x	x	x	x	**Vertical Sync Gating: Opening 50 Hz** Opening=4****VTHRL50M*** 0000000: Opening in first line 1111111: Opening in line 508

Table 3–14: Slave channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
6Eh	W	VS2_20	PALREFS	x	x	x	x	x	x	x	x									**ACC reference adjustment (PAL)** 00000000: Low reference value 11110000: Nominal value 11111111: High reference value
			PALIDL0S									x								**PAL/NTSC identification level 0** 0: Less sensitive 1: More sensitive
			VTHRH50S										x	x	x	x	x	x	x	**Vertical sync gating: Closing 50 Hz** Closing=312+4*__VTHRH50M__ 0000000: Closing in line 312 1111111: Closing in line 820 When VINPS (67h) is set, 50 Hz values are taken for opening and closing values.
6Fh	W	VS2_20	SLLTHDS	x	x															**Slicing level threshold H** 00: No offset 01: Small negative 10: Small positive 11: Large positive (adaptive)
			SCADJS			x	x	x	x	x	x									**Subcarrier adjustment** 000000: -262 ppm 001111: 0 ppm 111111: 840 ppm
			AGCMDS									x	x							**AGC method** 00: Sync amplitude and peak white 01: Sync amplitude only 10: peak white only 11: Fixed to value __AGCADJ1S__
			AGCADJ1S											x	x	x	x	x	x	**Gain adjustment ADC1** 000000: 0.6 V input sign 100000: 1.0 V input signal 111111: 1.8 V input signal
70h	W	VS2_20	AGCRESS	x																**AGC reset** 0: No reset 1: Reset
			AGCFRZES		x															**Freeze AGC (ADC_CVBS)** 0: Normal operation 1: Freeze AGC at current value
			AGCADJ2S			x	x	x	x	x	x									**Gain adjustment ADC2** 000000: 0.6 V input signal 100000: 1.0 V input signal 111111: 1.8 V input signal
			VFLYWHLS									x								**Vertical flywheel** 0: Disabled 1: Enabled

Table 3–14: Slave channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			CPLLRESS										x							**Force chroma PLL reset** 0: No reset 1: Reset chroma PLL *Note: After use,* ***CPLLRESS*** *must be set to 0 again*
			CLMPST1SS											x	x	x	x	x	x	**Clamping start CD2, Signals 1** 000000: 0 µs 011100: 5.6 µs 111111: 12.8 µs
71h	W	VS2_20	CLMPHIGHS	x	x	x	x	x	x	x	x									**Vertical end of clamping pulse** 00000000: Line 256 00111100: Line 376 11111111: Line 766
			SCMIDLS									x	x							**SECAM identification level** 00: 128 01: 64 10: 96 11: 80
			CLMPST2SS											x	x	x	x	x	x	**Measurement start CD2, Signals 2** 000000: 0 µs 011100: 5.6 µs 111111: 12.8 µs
72h	W	VS2_20	IFCOMPSTRS	x																**2nd IF compensation filter** 0: Disabled 1: Enabled
			SECACCLS		x	x	x													**Secam acceptance level** 000: 100 001: 84 010: 64 011: 32 100: 70 101: 76 110: 90 has only effect if **SECACCS** (74h) is enabled
			CLMPLOWS					x	x	x	x									**Vertical start of clamping pulse** 0000: Line 0 0011: Line 6 1111: Line30
			ACCLIMS									x	x	x	x	x				**ACC limitation** 00000: Limit at high color-carrier 01000: Limit at -24 dB 11111: Limit at low color-carrier

Table 3–14: Slave channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			IFCOMPS														x	x	x	**IF compensation filter** 000: Pal prefiltering 001: Pal prefiltering + IF 010: Prefiltering 011: IF 6 dB 100: Flat
73h	W	VS2_20	SLLTHDVPS	x																**Vertical slicing level threshold polarity** 0: Positive 1: Negative
			EIA770S		x															**EIA 770 support** 0: Standard TV signals expected 1: Progressive signals expected *Note: Timing according to EIA 770.1 or 770.2 when 1*
			VDETIFSS			x														**Vertical sync-detection slope** 0: Normal 1: Slow
			LOCKSPS				x	x												**Duration of chroma-PLL search** 00: 25 fields 01: 20 fields 10: 17 fields 11: 15 fields
			ADLCKS						x											**Additional lock-detection** 0: No used 1: Used
			ADLCKSELS							x										**Additional lock-detection selection** 0: PALID 1: PALDET
			ADLCKCCS								x									**Additional lock-detection color-killer** 0: Do not use lock signal 1: Use lock-signal
			CLMPD2SS									x	x	x	x					**Clamping duration for CD2, signals 2 (for RGBF)** Granularity: 200 ns 0000: 0 µs 0111: 1.4 µs 1111: 3.2 µs
			CLMPD1SS													x	x	x	x	**Clamping duration for CD2, signals 1** Granularity: 200 ns 0000: 0 µs 0111: 1.4 µs 1111: 3.2 µs

Table 3–14: Slave channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
74h	W	VS2_20	DEEMPFIRS[2:0]	x	x	x														**Deemphase filter FIR component** 0000:16 0101: 21 1111: 31 DEEMPFIRS[3] is in 63h
			DEEMPIIRS[1:0]				x	x												**Deemphase filter IIR component** 000: 5 001: 6 010: 7 011: 8 100: 9 101: 10 110: (reserved) 111: (reserved) DEEMPIIRS[2] is in 63h
			VDETITCS						x	x	x									**Vertical detection integration time constant** 000: 400 clock cycles 001: 375 clock cycles 010: 350 clock cycles 011: 300 clock cycles 100: 250 clock cycles 101: 225 clock cycles 110: 200 clock cycles 111: Automatic
			SECACCS									x								**Secam acceptance** 0: Disabled 1: Enabled
			SECDIVS										x							**Secam divider** 0: Divide by 4 1: Divide by 2
			SECINC1S											x	x					**Secam increment 1** 00: 2 01: 3 10: 4 11: 5
			SECINC2S													x	x			**Secam increment 2** 00: 1 01: 2 10: 3 11: 4
			SCMRELS															x	x	**Secam rejection level** 00: 320 01: 384 10: 352 11: 1024

Table 3–14: Slave channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
75h	W	VS2_20	DEEMPSTDS	x																**Deemphase filtering for standard detection** 0: Weak 1: Strong
			BELLFIRS[1:0]		x	x														**Bell filter FIR component** 000: -116 001: -113 010: -110 011: -108 100: -106 101: -104 110: -102 111: -100 BELLFIRS[2] is in 63h
			BELLIIRS[1:0]				x	x												**Bell filter IIR component** 000: 8 001: 9 010: 10 011: 11 100: 12 101: 13 110: 14 111: 16 BELLIIRI[2] is in 63h
			SLLTHDVS						x	x	x									**Slicing level threshold V** 000: No offset 001: 4 010: 8 011: 12 101: Adaptive (limited to +-4) 110: Adaptive (limited to +-8) 111: Adaptive (limited to +-12)
			FLNSTRDS									x	x							**Force line standard at CVBS/RGB front-end** 00: Automatic 01: Force 50 Hz 10: Force 60 Hz 11: (Reserved)
			ENLIMS											x						**Enable limiter** 0: Disabled 1: Enabled
			ISHFTS												x	x				**I -adjustment for horizontal PLL** 00: *1 01: *16 10: *4 11: *8

Table 3–14: Slave channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			NOTCHOFFS														x			**Luminance notch-filter** 0: Notch-filter enabled 1: Filter bypassed for PAL/NTSC / filter enabled for SECAM *Note: To switch-off filter for SECAM, use **TNOTCHOFF***
			VLPS															x	x	**Lowpass for vertical sync-separation** 00: None 01: Weak 10: Medium 11: Strong
76h	W	VS2_20	PALDELS	x	x															**PAL/NTSC delay vs. SECAM (chrominance)** 00: PAL/NTSC most left 11: PAL/NTSC most right
			TNOTCHOFFS			x														**Luminance notch-filter** 0: Notch-filter according to **NOTCHOFFS** 1: Notch-filter disabled
			BGPOSS				x	x	x											**Burstgate delay (SECAM only)** Granularity: 200 ns 000: Most left (-400 ns) 010: No delay 111: Most right (+1 µs)
			PALINC1S							x										**Pal detection: Increment 1** 0: +3 1: +2
			PALINC2S								x									**Pal detection: Increment 2** 0: -1 1: -2 Do not use PALINC2S=1 in combination with PALINC1S=1
			PALIDL2S									x								**PAL / NTSC identification level 2** 0: less sensitive 1: more sensitive
			CLRANGES										x	x						**Chroma lock-range** 00: ±425 Hz 01: ± 463 Hz 10: ± 505 Hz 11: ±550 Hz
			NTCHSELS												x	x	x			**Luminance notch selection** 000: Sharp notch 001: Medium 1 010: Medium 2 011: Broad notch 100: Broad steep notch (PAL, SECAM only)

Table 3–14: Slave channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			TRAPBLUS															x		**Notch frequency for 4.250 MHz** 0: 4.25 MHz 1: 4.2 MHz Has only effect in SECAM mode
			TRAPREDS																x	**Notch frequency for 4.406 MHz** 0: 4.406 MHz 1: 4.356 MHz *Note: Has only effect in SECAM mode*
Memory Controller Slave Channel																				
77h	W	VSS2_40	INTPROGS	x																**Interlaced or progressive input signal for master channel** 0: Interlaced input source 1: Progressive input source (e.g. VGA)
			FREEZES		x															**Freeze master picture** 0: Live 1: Frozen (no writing of master data)
			VERRESS			x														**Vertical resolution master channel for frame based MUP-mode** 0: Field resolution 1: Frame resolution
			WRITES				x	x												**Write mode master channel** 00: All incoming fields are stored 01: Only A fields are stored 10: Only B fields are stored 11: Not defined
			READM2S						x											**Read master memory data to slave** 0: Slave data is read from slave memory 1: Slave data is read from master memory
			PIXPLINS							x	x									**Pixels per line slave channel** 00: Defined by DISPMODE 01: 448 pixels/line 10: 768 pixels/line 11: 896 pixels/line
			WRPOSXS									x	x	x	x	x	x			**Horizontal Position of master picture in the memory** 000000: Left border position Effective values: WRPOSXS/2 * 32 pixel, WRPOSXS* 16 pixel (MUP-modes), WRPOSXS/8 * 128 pixel (DISPMODE=0000, MOTVALON=1)
78h	W	VSS2_40	WRPOSYS	x	x	x	x	x	x	x	x									**Vertical position of master picture in the memory** 00000000: Upper border position Resolution: 1 line

Table 3–14: Slave channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
79h	W	VSBS_36	RDPOSYS	x	x	x	x	x	x	x	x									**Vertical read position slave** Line number indicating the start line of reading for the master channel Granularity: 1 line 00000000: First line
			RDPOSXS										x	x	x	x	x			**Horizontal read position slave** Pixel number indicating the start position of reading for the master channel 00000: First left pixel position=***RDPOSXS****32
			READS															x	x	**Read mode master channel** 00: Reading A and B fields 01: Reading only A fields 10: Reading only B fields 11: (Reserved) For DISPMODE=0001 (Snap Shot): 00: Reading live channel ≠ 00: Reading still picture
Noise Measurement Slave Channel																				
7Ah	W	VSS1_40	NMLINES	x	x	x	x	x	x	x	x	x								**Line for noise measurement** 0_d: Line 2 1_d: Line 3 311_d: Line 1 (PAL) 261_d: Line 1 (NTSC) *Note: Lines 3-260 are not standard dependent*
			NMSENSES									x	x	x						**Noise measurement sensitivity** 00: *1 01: *2 10: *4 11: *8
			NMPOSS												x	x				**Noise measurement analyze window position** 00: 6.3 µs 01: 12.6 µs 10: 18.9 µs 11: 23.7 µs
Temporal Noise Reduction Slave Channel																				
7Bh	W	VSS2_40	FEMAGS	x	x	x	x	x												**Fine error characteristic** 00000: Smallest gain 10000: Default (equal to B11version) 11111: Largest gain
			SDRS						x	x	x									**Secam Dr adjustment** 00: 191 01: 194 10: 197 11: 200

Table 3–14: Slave channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			SDBS									x								**Secam Db adjustment** 00: -55 01: -58 10: -61 11: -64
			TNRABSS										x							**Motion detector works on absolute values:** 0: Absolute values not calculated 1: Absolute values calculated
			NRONS											x						**Temporal noise reduction** 0: Disabled 1: Enabled
			TNRSELS												x					**Chrominance motion values from:** 0: Luminance motion detector 1: Separate chrominance motion detector
			TNRNR4YS													x				**Temporal noise reduction of luminance and chrominance** 0: Frame based 1: Field based
7Ch	W	VSS2_40	TNRYS0S	x	x	x	x													**TNR curve characteristic of luma segment 0** 0001: Default
			TNRYS1S					x	x	x	x									**TNR curve characteristic of luma segment 1** 1111: Default
			TNRYS2S									x	x	x	x					**TNR curve characteristic of luma segment 2** 1111: Default
			TNRYS3S													x	x	x	x	**TNR curve characteristic of luma segment 3** 0100: Default
7Dh	W	VSS2_40	TNRYS4S	x	x	x	x													**TNR curve characteristic of luma segment 4** 0100: Default
			TNRYS5S					x	x	x	x									**TNR curve characteristic of luma segment 5** 0100: Default
			TNRYS6S									x	x	x	x					**TNR curve characteristic of luma segment 6** 0000: Default
			TNRYS7S													x	x	x	x	**TNR curve characteristic of luma segment 7** 0000: Default
7Eh	W	VSS2_40	TNRCS0S	x	x	x	x													**TNR curve characteristic of chroma segment 0** 0001: Default
			TNRCS1S					x	x	x	x									**TNR curve characteristic of chroma segment 1** 1111: Default
			TNRCS2S									x	x	x	x					**TNR curve characteristic of chroma segment 2** 1111: Default

Table 3–14: Slave channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			TNRCS3S													x	x	x	x	**TNR curve characteristic of chroma segment 3** 0100: Default
7Fh	W	VSS2_40	TNRCS4S	x	x	x	x													**TNR curve characteristic of chroma segment 4** 0100: Default
			TNRCS5S					x	x	x	x									**TNR curve characteristic of chroma segment 5** 0100: Default
			TNRCS6S									x	x	x	x					**TNR curve characteristic of chroma segment 6** 0000: Default
			TNRCS7S													x	x	x	x	**TNR curve characteristic of chroma segment 7** 0000: Default
80h	W	VSS2_40	TNRYSSS	x	x	x	x													**TNR start value of luma LUT** 1111: Default
			TNRCSSS					x	x	x	x									**TNR start value of chroma LUT** 1111: Default
			TNRCLYS									x	x	x	x					**TNR luminance classification:** 0000: Strong noise reduction 1111: Slight noise reduction
			TNRCLCS													x	x	x	x	**TNR chrominance classification:** 0000: Strong noise reduction 1111: Slight noise reduction
Preframe Generator Slave Channel																				
81h	W	VSS2_40	YBORDERS	x	x	x	x													**Y border value of display** Granularity: 16 0000: 0 0001: 16 1111: 240
			UBORDERS					x	x	x	x									**U border value of display** Granularity: 16 0000: 0 0001: 16 0111: 112 1000: -128 1111: -16
			VBORDERS									x	x	x	x					**V border value of display** Granularity: 16 0000: 0 0001: 16 0111: 112 1000: -128 1111: -16

Table 3–14: Slave channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			MPFBLBS													x	x	x	x	**Multi picture force background lines bottom** Number of lines of background color to be appended 0000: 0 lines 1111: 15 lines
82h	W	VSS2_40	MPFBPRS	x	x															**Multi picture force background pixels right** Number of pixels of background color to be appended 00: 0 pixels 01: 16 pixels 10: 32 pixels 11: 48 pixels
			MPFBLTS			x	x	x	x											**Multi picture force background lines top** Number of lines to be overwritten with background color from top 0000: 0 lines 1111: 15 lines
			DPVSAT											x	x	x	x	x	x	**V saturation** 000000: 0 100000: 1 111111: 63/32
83h	W	VSS2_40	FRCBGNDS	x																**Background generator in pre-frame generator** 0: Disabled 1: Enabled
			MPFBPLS		x	x	x	x	x											**Multi picture force background pixels left** Number of pixels to be overwritten with background color from left Granularity: 2 pixel 00000: 0 pixels 11111: 62 pixels
			DPUSAT											x	x	x	x	x	x	**U saturation** 000000: 0 100000: 1 111111: 63/32
Horizontal Prescaler Slave Channel																				
84h	W	VSS1_40	FRCMMODS	x																**Mosaic mode generator** 0: Disabled 1: Enabled
			APENSELS		x															**Active pixel enable select** 0: Count clock cycles (recommended for CVBS/RGB input) 1: Count active pixels (recommended for ITU656 input)
			HSCPRESCS					x	x	x	x	x	x	x	x	x	x	x	x	**Control signal for HSCALE in horizontal pre-scaler** Subsampling factor by prescaler is (int) 0: 1 (int) 2048: 1.5 (720 pixels) (int) 2371: 1.578 (→684 pixels) (int) 4095: 2 (540 pixels)

Table 3–14: Slave channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
85h	W	VSS1_40	HAAPRESCS	x	x															**Horizontal antialiasing filter** 00: Filter bypassed 01: Force characteristic weak 10: Force characteristic strong 11: Automatic characteristic (weak or strong) *Note: For normal CVBS/RGB full-screen, filter should be set to weak or automatic characteristic. For ITU656 full-screen input, filter should be bypassed. Strong characteristic is for split-screen and PiP only.*
			HDCPRESCS				x	x	x	x										**Horizontal pre-scaler decimates by** 0000: 1 0001: 2 0010: 3 0011: 4 0100: 6 0101: 8 0110: 12 0111: 16 1000: 24 1001: 32
			APPLIPS								x	x	x	x	x	x	x	x	x	**Active pixel per line (pre scaler)** Describes, how many decimated active pixels are generated. Granularity: 2 pixels (int) 0: 0 pixels (int) 342: 684 pixels (int) 511: 1022 pixels
86h	W	VSS1_40	MOTONS	x																**Line memories** 0: Available for vertical prescaler 1: Disabled
			NAPPLIPS							x	x	x	x	x	x	x	x	x	x	**Not active pixel per line (pre scaler)** Granularity: 2 clock cycles (int) 0: 0 pixels (int) 100: 200 pixels (int) 1023: 2046 pixels
Vertical Prescaler Slave Channel																				
87h	W	VSS1_40	VAAPRESCS	x																**Vertical lowpass filter (pre-scaler)** 0: Disabled 1: Enabled
			VPKPRESCS		x	x	x	x	x											**Vertical peaking** 00000: Maximum vertical peaking (enhancement) 10000: Vertical peaking has no effect (flat) 11111: Maximum attenuation (damping)
			VCRPRESCS							x										**Shift of chrominance signal** 0: No shift 1: One line upward (e.g. for VCR)

Table 3–14: Slave channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			NALPFIPS								x	x	x	x	x	x	x	x	x	**Not active lines per field input** (int) 0: Shift is 0 (int) 22: Shift is 22 lines (int) 511: Shift is 511 lines (max. shift is 1 field)
88h	W	VSS2_40	VPREBYPS	x																**Vertical Pre scaler Bypass** 0: Vertical pre scaler enabled 1: Vertical pre scaler bypassed
			VDCPRESCS			x	x	x	x											**Vertical pre-scaler decimates by** 0000: 1 0001: 2 0010: 3 0011: 4 0100: 6 0101: 8 0110: 12 0111: 16 1000: 24 1001: 32
			ALPFIPS							x	x	x	x	x	x	x	x	x	x	**Active lines per field (input processing)** (int) 0: No active line (int) 288: 288 active lines (int) 1023: 1023 lines
89h	W	VSS2_40	VSCPRESCS					x	x	x	x	x	x	x	x	x	x	x	x	**Control signal for VSCALE in vertical pre-scaler** (int) 0: Scaling factor is 1 (int) 4095: Scaling factor is 2
Horizontal Postscaler Slave Channel																				
8Ah	W	VSBS_36	HPANONS	x																**Horizontal panorama mode** 0: Panorama disabled 1: Panorama enabled
			DBDHPOSS		x															**Disable border detection (postscaler)** 0: Border detection active 1: Border detection not active
			CDELHPOSS			x														**Chrominance delay** 0: No delay 1: Half-pixel delay
			HSCPOSCS					x	x	x	x	x	x	x	x	x	x	x	x	**Horizontal scaling factor for post scaler** (int) 1024: Upsampling factor is 4 (int) 2910: Upsampling factor is 1.40 (int) 4095: Upsampling factor is 1
8Bh	W	VSBS_36	HSEG1S[10:5]	x	x	x	x	x	x											**Beginning of segment 1 for horizontal panorama mode** Granularity: 2 pixels (int) 0: 0 pixel behind picture start (int) 2047: 4094 pixel behind picture start

Table 3–14: Slave channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			HINC0S								x	x	x	x	x	x	x	x	x	**Horizontal post-scaler increment 0** 100000000: -32 pixels 000000000: 0 pixels 011111111: 31.875 pixels
8Ch	W	VSBS_36	HSEG1S[4:0]	x	x	x	x	x												(See 8Dh)
			HINC1S								x	x	x	x	x	x	x	x	x	**Horizontal post-scaler increment 1** 100000000: -32 pixels 000000000: 0 pixels 011111111: 31.875 pixels
8Dh	W	VSBS_36	HSEG2S[10:5]	x	x	x	x	x	x											**Beginning of segment 2 for panorama mode** Granularity: 2 pixels (int) 0: 0 pixel behind picture start (int) 2047: 4094 pixel behind picture start
			HINC2S								x	x	x	x	x	x	x	x	x	**Horizontal post-scaler increment 2** 100000000: -32 pixels 000000000: 0 pixels 011111111: 31.875 pixels
8Eh	W	VSBS_36	HSEG2S[4:0]	x	x	x	x	x												(See 8Fh)
			HINC3S								x	x	x	x	x	x	x	x	x	**Horizontal post-scaler increment 3** 100000000: -32 pixels 000000000: 0 pixels 011111111: 31.875 pixels
8Fh	W	VSBS_36	HSEG3S[10:5]	x	x	x	x	x	x											**Beginning of segment 3 for panorama mode** Granularity: 2 pixels (int) 0: 0 pixel behind picture start (int) 2047: 4094 pixel behind picture start
			HINC4S								x	x	x	x	x	x	x	x	x	**Horizontal post-scaler increment 4** 100000000: -32 pixels 000000000: 0 pixelsi 011111111: 31.875 pixels
90h	W	VSBS_36	HSEG3S[4:0]	x	x	x	x	x												(See 91h)
			HSEG4S						x	x	x	x	x	x	x	x	x	x	x	**Beginning of segment 4 for panorama mode** Granularity: 2 pixels (int) 0: 0 pixel behind picture start (int) 2047: 4094 pixel behind picture start
Output Data Controller Slave Channel																				
91h	W	VSBS_36	HOROFFS [10:6]	x	x	x	x	x												**Horizontal offset to compensate slave processing delay** (int) 64: Default
			HORPOSS						x	x	x	x	x	x	x	x	x	x	x	**Horizontal position inside active picture area** (int) 0: Most left display position (int) 4095: Most right display position

Table 3–14: Slave channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
92h	W	VSBS_36	HOROFFS[5:0]	x	x	x	x	x	x											(See 91h)
			VERPOSS							x	x	x	x	x	x	x	x	x	x	**Vertical position inside active picture area** Granularity: 1 line (***FMODE***=0) or 2 lines (***FMODE***=1) (int) 0: Most top display position (int) (2047): Most bottom display position
93h	W	VSBS_36	HORWIDTHS						x	x	x	x	x	x	x	x	x	x	x	**Horizontal picture width** Granularity: 2 pixels (int) 0: No display (int) 960: Default (int) 2047:4094 pixels
94h	W	VSBS_36	VEROFFS	x	x	x	x	x												**Vertical offset to compensate slave processing delay** (int) 17: Default
			VERWIDTHS						x	x	x	x	x	x	x	x	x	x	x	**Vertical picture width** (int) 0: 0 lines (int) 288: Default (int) 2047: 2047 lines
Picture Improvement Slave Channel																				
95h	W	VSBS_36	PKCTIBPS	x	x															**Peaking factor for CTI (bandpass part)** 00: 2 (CTI bp off) 01: 16 10: 24 11: 32
			PKCTIHPS			x	x													**Peaking factor for CTI (highpass part)** 00: 2 (CTI hp off) 01: 16 10: 24 11: 32
			LTIS					x												**Luminance transition improvement** 0: disabled 1: enabled
			APK1BPS[1:0]						x	x										**1st adaptive peaking factor (bandpass part)** 0000: 0.5 0100: 2.5 1111: 8
			APK2BPS								x	x	x							**2nd adaptive peaking factor (bandpass part)** 000: 1 001: 2 (peaking bp off) 011: 4 111: 8

Table 3–14: Slave channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			ATH1BPS											x	x					**Peaking denoising threshold (bandpass part)** 00: 0 (denoising off) 01: 2 10: 4 11: 8
			ATH2BPS													x	x			**2nd peaking threshold (bandpass part)** 00: 0 01: 4 10: 8 11: 16
			THES															x	x	**Turning point threshold for CTI** 00: 1 01: 2 10: 3 11: 4
96h	W	VSBS_36	APK1HPS[1:0]	x	x															**1st adaptive peaking factor (highpass part)** 0000: 0.5 0100: 2.5 1111: 8
			APK2HPS			x	x	x												**2nd adaptive peaking factor (highpass part)** 000: 1 001: 2 (peaking hp off) 011: 4 111: 8
			ATH1HPS						x	x										**Peaking denoising threshold (highpass part)** 00: 0 (denoising off) 01: 2 10: 4 11: 8
			ATH2HPS								x	x								**2nd peaking threshold (highpass part)** 00: 0 01: 4 10: 8 11: 16
			DBDPICIS										x							**Disable border detection (picture improvement)** 0: Border detection active 1: Border detection not active
			APK1BPS[3:2]											x	x					(See 49h)
			APK1HPS[3:2]													x	x			(See 49h)
			CORONS															x		**Coring or denoising for low amplitudes** 0: Coring off, denoising on 1: Coring on, denoising off

Table 3–14: Slave channel, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
Pixel mixer slave channel																				
97h	W	VSBS_36	YFRAMES					x	x	x	x									**Luminance value for the slave frame (4MSB)** 0001: Default value (yields value 0001 00000=32)
			UFRAMES									x	x	x	x					**Chrominance value for the slave frame (4MSB)** 0000: Default value (yields value 0000 00000=0)
			VFRAMES													x	x	x	x	**Chrominance value for the slave frame (4MSB)** 0000: Default value (yields value 0000 00000=0)

3.9.3. Common

Table 3–15: Common

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
Comb filter																				
98h	W	VS1_20	CVBSEL1	x	x	x	x													**Input select for ADC1** 0000: CVBS1 0001: CVBS2 0010: CVBS3 0011: CVBS4 or Y1 0100: CVBS5 or C1 0101: CVBS6 or Y2 0110: CVBS7 or C2 0111: Y1 + C1 1000: Y2 + C2 1001: CVBS8 (QFP144 versions only) 1010: CVBS9 (QFP144 versions only) 1111: Disabled
			CVBSEL2					x	x	x	x									**Input select for ADC2** 0000: CVBS1 0001: CVBS2 0010: CVBS3 0011: CVBS4 or Y1 0100: CVBS5 or C1 0101: CVBS6 or Y2 0110: CVBS7 or C2 0111: Y1 + C1 1000: Y2 + C2 1001: CVBS8 (QFP144 versions only) 1010: CVBS9 (QFP144 versions only) 1111: Disabled

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			CLMPSIG1									x	x							**Clamping signals ADC1** 00: 1st color decoder: signals 1 01: 1st color decoder: signals 2 10: 2nd color decoder: signals 1 11: 2nd color decoder: signals 2
			CLMPSIG2											x	x					**Clamping signals ADC2** 00: 1st color decoder: signals 1 01: 1st color decoder: signals 2 10: 2nd color decoder: signals 1 11: 2nd color decoder: signals 2
			VCRDETHD													x				**VCR detection threshold** 0: High threshold 1: Low threshold
			YCBYR														x			**YC by Red** 0: Normal operation 1: C input from red ADC
			YCBYB															x		**YC by Blue** 0: Normal operation 1: C input from blue ADC
			YCTOCOMB																x	YC to Comb filter 0: Normal comb operation 1: yc signal fed through comb delays Use INCOMB instead of YCBYR or YCBYB for this mode
99h	W	VS1_20	CVBOSEL1	x	x	x	x													**Output select 1 for pin cvbso1** 0000: CVBS1 0001: CVBS2 0010: CVBS3 0011: CVBS4 or Y1 0100: CVBS5 or C1 0101: CVBS6 or Y2 0110: CVBS7 or C2 0111: Y1 + C1 1000: Y2 + C2 1001: CVBS8 (QFP144 versions only) 1010 : CVBS9 (QFP144 versions only) 1111: Disabled

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			CVBOSEL2					x	x	x	x									**Output select for pin cvbso2** 0000: CVBS1 0001: CVBS2 0010: CVBS3 0011: CVBS4 or Y1 0100: CVBS5 or C1 0101: CVBS6 or Y2 0110: CVBS7 or C2 0111: Y1 + C1 1000: Y2 + C2 1001: CVBS8 (QFP144 versions only) 1010 : CVBS9 (QFP144 versions only) 1111: Disabled
			CVBOSEL3									x	x	x	x					**Output select for pin cvbso3** 0000: CVBS1 0001: CVBS2 0010: CVBS3 0011: CVBS4 or Y1 0100: CVBS5 or C1 0101: CVBS6 or Y2 0110: CVBS7 or C2 0111: Y1 + C1 1000: Y2 + C2 1001: CVBS8 (QFP144 versions only) 1010 : CVBS9 (QFP144 versions only) 1111: Disabled
			VDG													x	x			**Vertical difference gain** 00: Max. gain 01: Medium 2 10: Medium 1 11: Min. gain
			HDG															x	x	**Horizontal difference gain** 00: Min. gain 01: Medium 1 10: Medium 2 11: Max. gain
9Ah	W	VS1_20	DDR	x	x															**Diagonal dot reduction** 00: Min. reduction 01: Medium 1 10: Medium 2 11: Max. reduction
			F2F1F0			x	x	x												**Test only** 000: Normal operation
			DT						x											**Test only** 0: Normal operation

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			DC							x										**Test only** 0: Normal operation
			COR								x									**Vertical peaking coring** 0: Disabled 1: Enabled
			NOSEL									x	x							**Notch filter select** 00: Flat frequency characteristic 01: Min. peaked 10: Med. peaked 11: Max. peaked
			DCR											x						**Vertical peaking DC rejection filter** 0: Disabled 1: Enabled
			SYNCOMB												x					**Timing of Rising edge of H50 sync** 0: late 1: early
			VPK													x	x	x	x	**Vertical peaking gain (comb-filter peaking)** 0000: No vertical peaking 1111: Max. vertical peaking
9Bh	W	VS1_20	LINLENH50	x	x	x	x													**Nr. of pixel for 50 Hz signals** Length=1284+***LINLENH50*** LINLENH50=12 (=1296 pixel per line)
			LINLENH60					x	x	x	x									**Nr. of pixel for 60 Hz signals** Length=1284+***LINLENH60*** LINLENH60=3 (= 1287 pixel per line)
			REFTRIMEN									x								**Reference value enable** 0: Use on-chip fused values 1: Use I²C values
			V50BLANK										x							**Signal select for PIN Vout50** 0: Single scan vertical output 1: Blank signal output
			PORCNCL											x						**Reset control bit cancel** 0: No operation 1: Reset ***POR*** bit (EBh) After use, ***PORCNCL*** must be set to 0 again
			RESETPC1												x					**Reset PC1 signal (test only)** 0: Normal operation 1: Reset PC1
			RESETPC2													x				**Reset PC2 signal (test only)** 0: Normal operation 1: Reset PC2

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			SELCOMB														x			**COMB filter used for first or second color-decoder** 0: CD 1 1: CD 2
			DISCOMB															x		**Disable comb-filter** 0: Comb-filter enabled 1: Comb-filter disabled (notch CVBS or Y/C input)
			RESMODE																x	**Resampling mode (test only)** 0: Fractionally subcarrier locked 1: Fractionally line-locked mode
SLICER/ANALOG																				
9Ch	W	VS1_20	XDSCLS	x	x	x	x	x												**XDS-Primary-filter (class)** 00000: Transparent (all sliced data, both fields) 1xxxx: “Current” selected (only second field) x1xxx: “Future” selected (only second field) xx1xx: “Channel” selected (only second field) xxx1x: “Miscellenious” selected (only second field) xxxx1: “Public Services” selected (only second field)
			656BLANK						x											**Signal select for PIN 656VIO** 0: 656vin or 656vout (dependent on operation mode) 1: Blank signal output
			XDSTPE							x	x	x								**XDS-secondary-filter (class→type) / [WSS field]** 000: ALL (no filtering) [field 1 only] 001: 05h (program rating) [field 2 only] 010: 01h, 04h (time information only)[both fields] 011: 40h (out of band only) 100: 01h,02h,03h,04h,0Dh,40h (VCR information) 101: 01h, 04h,05h (time information only and PR)[both fields] 110: 05h,40h (out of band only and PR) 111: 01h,02h,03h,04h,05h,0Dh,40h (VCR information and PR)
			IRQCON										x	x	x					**IRQpin selection** 000: Horizontal sync (2 µs) 001: Interrupt, when new data arrived (pos. polarity)(2 µs) 010: Interrupt, when new data arrived (neg. polarity)(2 µs) 011: Equivalent to DATAV for both registers (pos. pol.) 100: Equivalent to DATAV for both registers (neg. pol.) 101: Vertical sync (2 µs) 110: Selected line for slicing 111: Cvbs field at output
			SERVICE													x				**Closed caption or WSS** 0: Closed caption 1: WSS
			INCOMB														x	x		**Input for comb filter** 00: ADC 1 01: ADC 2 10: ADCG / ADCF (dependent on ***ADCSEL***)

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			SLSRC																x	**Select Slicer source** 0: Master front-end 1: Slave front-end
9Dh	W	NTO	REFTRIM	x	x	x	x	x	x	x	x									**Reference value bandgap** 01000000: Low reference 00000000: Medium reference 00111111: High reference 1XXXXXXX: Reference disabled, resistor used
			REFTRIMCV									x	x	x	x					**Reference value ADC CVBS (antialiasing filter)** 0000: Narrow 1111: Wide
			REFTRIMRGB													x	x	x	x	**Reference value ADC RGBF (antialiasing filter)** 0000: Narrow 1111: Wide
ITU Input/Output Interface																				
9Eh	W	VS656_27	OMODE	x	x															**Output format:** 00: Full ITU656 01: ITU656 only data, H- and V-blank as outputs, according to ITU656 10: ITU656 only data, H- and V-blank as inputs, according to ITU656 11: (Reserved)
			CLK656OUT			x														**Clock for ITUO** 0: 656clk is clock input 1: 656clk is output equal to pin clkout
			PPLIPI								x	x	x	x	x	x	x	x	x	**Pixels per line ITU** Granularity: 2 pixel (int) 432: Default
9Fh	W	VS656_27	NAPIPPHI	x	x															**CbYCrY-phase shift** 00: No phase shift 01: 1 clk 10: 2 clk 11: 3 clk
			F_OFFS			x	x													**Offset of active field at interlaced mode (line offset):** 00: NALPFIPI+1 (A), NALPFIPI (B) 01: NALPFIPI (A), NALPFIPI+1 (B) 01: 1 H delay in field A 11: 1 H delay in field B
			ADLINE					x	x	x	x	x								**Ancillary data line number** if ***ADINS***=0: Tansmitter address is: 111(+5 bits of ***ADLINE***), if ***ADINS***=1: ***ADLINE*** defines the line, which should contain the ancillary data.
			FPOL										x							**Field polarity** 0: Field A=0, Field B=1 1: Field A=1, Field B=0

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			IMODE											x	x					**Input format** 00: Full ITU mode (automatic) 01: Full ITU mode (manual) 10: ITU656 only data, H/V-sync according PAL/NTSC 11: ITU656 only data, H/V-sync according ITU656
			ADINS													x				**Ancillary data insertion** 0: Transmitter preamble is detected in the data stream. If identical as ***ADLINE*** data are stored in I2C-Registers. 1: Ancillary data detection in video line ***ADLINE*** only, transmitter address ignored. If preamble detected, data are stored in I2C-Registers.
			VSREF														x			**Generate V-sync related to F- or V-flag** 0: Use F-flag 1: Use V-flag
A0h	W	VS656_27	LPFIPI							x	x	x	x	x	x	x	x	x	x	**Lines per field for ITU** (int)625: 625 lines per field
A1h	W	VS656_27	APPLIPI	x	x	x	x	x	x	x	x	x								**Active pixels per line for ITU** Active pixels = ***APPLIPI*** * 2 (int) 360=720 lines]
			NALPFIPI										x	x	x	x	x	x	x	**Not active lines per field for ITU** (int) 20= 20 lines
A2h	W	VS656_27	NAPPLIPI	x	x	x	x	x	x	x	x									**Not active pixels from HSYNC to input data for ITU** Delay = ***NAPPLIPI*** * 2 + ***NAPIPPHI***
			ALPFIPI									x	x	x	x	x	x	x	x	**Active lines per field for ITU** Active lines = ALPFIPI * 2 (int) 144: 288 active lines
A3h	W	VS656_27	VSIGNAL	x																**Input signal** 0: Interlaced 1: Non interlaced
			CFORMAT		x															**Chrom. data format** 0: Unsigned 1: 2s complement
			HPOL			x														**H656 polarity** 0: H656 active low 1: H656 active high
			VPOL				x													**V656 polarity** 0: V656 active low 1: V656 active high
			EN_656					x	x											**ITU656-interface:** 00: input mode 01: memory read output 1x: output display data

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			ITUPRTSEL							x										**ITU port selection** 0: First input (656io) 1: Second input (i656i)
RGB Interface																				
A4h	W	VSRGB_40	BRTADJ	x	x	x	x	x	x	x	x									**Brightness adjustment** 10000000: -128 (darkest picture) 00000000: 0 01111111: 127 (brightest picture)
			CONADJ									x	x	x	x	x	x			**Contrast adjustment** 0000000: 0 000001: 1/32 100000: 1 111111: 63/32
			CHRSFR															x		**Chroma subsampling filter** 0: Disabled 1: Enabled
			AASEL																x	**(Digital) antialiasing selection** 0: -3dB @ 10.6MHz 1: -3dB @ 11.8MHz
A5h	W	VSRGB_40	CLKF2PAD	x																**Front-end clock is given to pin 74 (mqfp80)** 0: Pin 74 is used as h-input for ITU656 1: CLKF20 (20.25 MHz) is given to pin 74
			FBLDEL		x	x	x													**Fast blank delay vs. RGB/YUV input** Granularity: 25 ns 000: -50 ns delay 010: No delay 110: +100 ns delay 111: (Reserved)
			GOFST					x	x											**Clamping correction for G ADC** 00: 0 (G/Y, pedestal offset visible) 01: 16 (G/Y, no pedestal offset visible) 10: 64 (G/Y with sync, pedestal offset visible) 11: 80 (G/Y with sync, no pedestal offset visible)
			MIXGAIN							x	x	x	x	x	x	x				**Gain of fast blank signal** 1000000: -64 0000000: 0 0111111: +63 *Note: For proper operation in dynamic soft-mix mode, absolute value of **MIXGAIN** must be bigger than 2 (e.g. 3)*
			STANDBYRGB														x			**Standby mode RGB ADC** 0: RGBF ADCs active 1: RGBF ADCs in standby mode

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			STANDBYCV															x		**Standby mode CVBS ADC** 0: CVBS ADCs active 1: CVBS ADCCs in standby mode
			DEC2																x	**Decimation by 2** Decimation of RGB/YUV signal before soft-mix 0: No decimation 1: Decimation by 2
A6h	W	VSRGB_40	YFDEL	x	x	x	x	x	x	x										**Y delay adjustment** Granularity: 50 ns 0000000: No delay 1111111: 6.3 µs
			UVDEL								x	x	x	x	x	x	x			**UV delay adjustment** Granularity: 50 ns 0000000: No delay 1111111: 6.3 µs
			RGBSEL															x		**RGB input selection** 0 : Use RGB/YUV input1 1 : Use RGB/YUV input2
			FBLCONF																x	**Configuration of FBLACTIVE signal** 0: React for one clock active FBL input 1: React for 5 clock active FBL input
A7h	W	VSRGB_40	USATADJ	x	x	x	x	x	x											**U saturation adjustment** 000000: 0 000001: 1/32 100000: 1 111111: 63/32
			VSATADJ							x	x	x	x	x	x					**V saturation adjustment** 000000: 0 000001: 1/32 100000: 1 111111: 63/32
			ADCSEL													x				**Select ADC for sync signal conversion** 0: Use ADC_G 1: Use ADC_FBL
			AABYP														x			**Bypass RGB/YUV antialiasing filter** 0: Use filter 1: Bypass
			CLMPVG															x		**Clamping value G ADC** 0 : 16 1 : 80
			DCLMPF																x	**Clamping value fast blank input** 0 : Enable clamping 1 : Disable clamping (DC coupling)

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
A8h	W	VSRGB_40	AGCADJR	x	x	x	x	x	x											**Gain adjustment Red** 000000: 0.5 V input signal 111111: 1.5 V input signal
			AGCADJB							x	x	x	x	x	x					**Gain adjustment Blue** 000000: 0.5 V input signal 111111: 1.5 V input signal
			MIXOP													x	x			**Mixing configuration** 00: Enable Soft-Mix 01: Only RGB path visible 10: Only CVBS path visible 11: (Reserved)
			CLMPVRB															x	x	**Clamping value Red and Blue ADC** 00 : 16 (B/R signal without sync) 01 : 80 (B/R signal without sync) 10 : 128 (U/V signal) 11: (Reserved)
A9h	W	VSRGB_40	AGCADJG	x	x	x	x	x	x											**Gain adjustment Green** 000000: 0.5 V input signal 111111: 1.5 V input signal
			AGCADJF							x	x	x	x	x	x					**Gain adjustment fast Blank** 000000: 0.5 V input signal 111111: 1.5 V input signal
			RBOFST													x	x	x		**Clamping correction for R/B ADC** 000: 0 (R/B, pedestal offset visible) 001: 16 (R/B, no pedestal offset visible) 010: 64 (R/B with sync, pedestal offset visible) 011: 80 (R/B with sync, no pedestal offset visible) 100: 127 (UV negative pedestal offset) 101: 128 (UV) 110: 129 (UV positive pedestal offset) 111: (Reserved)
			SKEWSEL																x	**SKEW correction for RGB/YUV channel** 0: SKEW correction enabled 1: SKEW correction disabled
AAh	W	VSRGB_40	FBLOFFST	x	x	x	x	x	x											**Fast blank offset correction** 000000 : 0 offset 111111: 63 offset
			SELMASTER							x	x									**Select master channel input** 00: CD1 01: CD2 10: Soft-mix output 11: 656 input

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			SELSLAVE									x	x							**Select slave channel input** 00: CD1 01: CD2 10: Soft-mix output 11: 656 input
			SELSM											x						**Select soft-mix input (and clamp, deskew)** 0: CD1 1: CD2
			YUVSEL												x					**YUV or RGB input selection** 0: YUV expected 1: RGB expected
			SMOP													x				**Soft-mix operation mode** 0: Dynamic 1: Static
			Y2RGB														x			**Y to RGB (for YUV mode)** 0: Use Y from green ADC 1: Use Y from CVBS ADC
			BLUESEL															x		**Blue ADC selection** 0: Blue ADC gets B1 or B2 (dependent on ***RGBSEL***) 1: Blue ADC gets R2 (independent on ***RGBSEL***)
			BLUETWO																x	**Blue ADC clamping selection** 0: CD 1 (signals 2) 1: CD 2 (signals 2)'
LL-PLL Processing																				
ABh	W	NTO/HS	IICINCR[18:3]	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	**Set HDTO frequency** Granularity=103 Hz 33981_d (minimum: nominal pixel clock= 3.5 MHz) 349525_d (nominal pixel clock= 36 MHz) 388362_d (maximum: nominal pixel clock= 40 MHz)
ACh	W	NTO/HS	CLKT1	x	x															**Switch clkf20 and clkf40 to pads *cvbs1* or *bin2*** 00: No clock 01: Cvbs1 is output of clkf40 10: *Bin2* is output of clkf20 11: *Cvbs1* is output of clkf40 and *bin2* is output of clkf20
			HDTOTEST			x														**Test-bit for HPLL** 0: Normal mode 1: Test mode
			FILE				x	x	x	x										**Increment freeze duration** 0: No freeze 15: Increment is frozen for 15 lines
			LNL											x						**Dynamic time constant control** 0: Linear mode 1: Non linear mode

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			DISRES												x					**Disable reset of LL-PLL watchdog** 0: Reset disabled 1: Reset enabled
			LIMHI													x				**Limit value for DTO increment** 0: No limit '1' : Increment value for DTO is limited to 393216 (Max. frequency of back-end clocks: clkb72: 81 MHz / clkb36: 40.5 MHz)
			IICINCR[2:0]														x	x	x	(see ABh)
ADh	W	NTO	KOIWID	x	x															**Window-width of coincidence detector** 00: ± 32 pixel (= ± 0.9 µs for TV application) 01: ± 64 pixel (= ± 1.8 µs for TV application) 10: ± 128 pixel (= ± 3.6 µs for TV application) 11: ± 256 pixel (= ± 7.2 µs for TV application)
			KOIH			x	x													**Hysteresis of coincidence detector** 00: 0 lines 01: 8 lines 10: 16 lines 11: 32 lines
			HTESTW					x	x	x	x									**Test bits for HPLL** 00: default
			HSWIN[2:0]									x	x	x						**Width of noise suppression window of LL-HPLL** 0000: ±28 µs 0001: ±24 µs 0010: ±20 µs 0011: ±16 µs 0100: ±12 µs 0101: ±8 µs 0110: ±4 µs 0111: Dynamic windowing. 1000: ±30 µs 1001: ±27 µs 1010: ±26 µs 1011: ±22 µs 1100: ±18 µs 1101: ±14 µs 1110: ±10 µs 1111: ±6 µs HSWIN[3] is in B3h
			SETSTABLL												x					**Stability signal of LL_HPLL** 0: STABLL is generated by the HPLL 1: STABLL is forced to 1
			KD2													x				**Phase detector steepness** 0: Steepness for normal TV operation mode 1: Steepness for operations where PPLIP is less than 288_d

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			HINCR_EXT														x			**HDTO testmode** 0: Normal mode 1: Increment is taken from pins
			LMOD															x		**Selects line locked mode** 0: Line locked-clocks derived from HPLL 1: Line-locked-clocks derived from front-end line-length
			FMOD																x	**Selects freerun mode** 0: Freerun-clocks derived from crystal 1: Freerun-clocks derived from HDTO *Note: Adjustable frequency is only possible when set to 1. When set to 00, Back-end clock is always 36 MHz (single-scan versions: 18 MHz)*
AEh	W	NTO	HRES	x																**Reset of LL-HPLL** 0: No reset 1: Reset Reset automatically when written
			HWID		x															**Minimum width of H-sync** 0: $60*T_{clkllf36}$ 1: $15*T_{clkllf36}$
			FION			x	x	x	x											**Increment freeze before V-sync** 0: No freeze 15: Freeze starts 15 lines before V-sync
			PPLIP							x	x	x	x	x	x	x	x	x	x	**Pixel per line LL_PLL** Granularity=4 pixel (int) 175: 700 (minimum) (int) 576: 2304 (int) 963: 3852 (maximum)
AFh	W	NTO	FREQSELL	x	x															**Amplifier current setting of oscillator pad** 00: 100 µA 01: 590 µA 10: 235 µA 11: 1730 µA
			OSCPD			x														**Power down of crystal oscillator amplifier** 0: Normal mode 1: Power down mode
			SHAPERDIS				x													**Power down of crystal oscillator shaper** 0: Normal operation 1: Power down active
			TSTSHABRI					x												**Testmode control of crystal oscillator** 0: Normal operation (shaper active) 1: External clock input (shaper replaced)

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			LIMLR[2:0]						x	x	x									**Limit LL-PLL lock-in range** 0000: Full lock-in range of +/- 5.85 % 0001: Lock in range limited to +/- 3.8 % 0010: Lock in range limited to +/- 2.55 % 0011: Lock in range limited to +/- 1.27 % 0100: Lock in range limited to +/- 0.63 % 0101: Lock in range limited to +/- 0.32 % 0110: Lock in range limited to +/- 0.19 % 0111: Lock in range limited to +/- 0.13 % 1000: Lock in range limited to +/- 5 % 1001: Lock in range limited to +/- 4.5 % 1010: Lock in range limited to +/- 3.1 % 1011: Lock in range limited to +/- 2.1 % 1100: Lock in range limited to +/- 1.5 % 1101: lock in range limited to +/- 1 % 1110: (Reserved) 1111: (Reserved) LIMLR[3] is in B3h
			FKOI									x								**Force coincidence bit** 0: Coincidence bit dynamically changed 1: Coincidence bit forced to 1
			FKOIHYS										x							**Force coincidence hysteresis bit** 0: Coincidence hysteresis bit dynamically changed 1: Coincidence hysteresis bit forced to 1

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			KIL[3:0]											x	x	x	x			**Integrational factor for loop filter if HPLL is locked** 00000: 0 00001: 1 00010: 2 00011: 4 00100: 8 00101: 16 00110: 32 00111: 64 01000: 128 01001: 256 01010: 512 01011: 1024 01100: 2048 01101: 4096 01110: 8192 01111: 16384 10000: 0.5 10001: 1.5 10010: 2.5 10011: 3 10100: 3.5 10101: 4.5 10110: 5 10111: 6 11000: 7 KIL[4] is in B1h
B0h	W	NTO	LIMIP									x	x	x	x	x	x	x	x	**Limiter Control for P-part for increased dynamic range** LIMIT_P= ±16****LIMIP*** 00000000: ±0 11111110: ±4064 11111111: No limitation
B1h	W	NTO	KPNL[3:0]	x	x	x	x													**Proportional factor for loop filter if HPLL is not locked** Same values as in locked condition (***KPL***)

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			KPL[3:0]					x	x	x	x									**Proportional factor for loop filter if HPLL is locked**) 00000: 0 00001: 1 00010: 2 00011: 4 00100: 8 00101: 16 00110: 32 00111: 64 01000: 128 01001: 256 01010: 512 01011: 1024 01100: 2048 01101: 4096 01110: 8192 01111: 16384 10000: 0.5 10001: 1.5 10010: 2.5 10011: 3 10100: 3.5 10101: 4.5 10110: 5 10111: 6 11000: 7 KPL[4] is in B1h
			KINL[3:0]									x	x	x	x					**Proportional factor for loop filter if HPLL is not locked** Same vales as in locked condition (***KPI***)
			KPNL[4]													x				(See B1h)
			KPL[4]														x			(See B1h)
			KINL[4]															x		(See B1h)
			KIL[4]																x	(See AFh)
B2h	W	NTO	SLLWIN					x	x											**STABLL detection window** 00: 64 01: 72 10: 48 11: 32
			FETHD							x	x									**Fine/coarse error selection threshold** 00: 16 01: 12 10: 8 11: 0 (never use fine-error)

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			LIMII									x	x	x	x	x	x	x	x	**Limiter control for I-part for increased dynamic range** LIMIT_I= ±16****LIMII*** 00000000: ± 0 11111110: ±4064 11111111: No limitation
B3h	W	NTO	HSWIN[3]													x				(See ADh)
			LIMLR[3]														x			(See AFh)
			LIMEN															x		**Limiter enable** 0: B11 behavior for ***LIMIP*** and ***LIMII*** 1: Normal ***LIMII*** and ***LIMIP*** characteristic
Letterbox Detection																				
B4h	W	VSM1_40	LBSUB	x	x															**Subsampling mode** 0x: Others (factor 1) 10: 20.25 MHz source (factor 1.5) 11: 40.5 MHz source (factor 3)
			LBGRADRST			x														**Reset of gradient method** 0: No reset 1: Reset
			LBSTABILITY				x													**Stability flag** 0: Continuous format update 1: Format update only once
			LB43SENS					x												**Sensitivity to 4:3 switch** 0: Off 1: On
			LBNGFEN						x											**No gradient found** 0: Disabled 1: Enabled
			LBTHDNBNHA							x	x	x	x	x						**Threshold for darkness-brightness, histogram, activity** (int)30: Default
			LBHSDEL												x	x	x	x	x	**Histogram stability delay** (int)10: Default
B5h	W	VSM1_40	LBGRADDET	x	x	x	x	x	x	x	x									**Threshold for gradient detected** (int) 50: Default
			LBVWENDLO									x	x	x	x	x	x	x	x	**Vertical measure window lower end** (int) 150: Default, [in lines (*2) related to VSYNC]
B6h	W	VSM1_40	LBHIWHITE	x	x	x	x	x	x	x	x									**Histogram white** (int) 50: Default
			LBHWEND									x	x	x	x	x	x	x	x	**Horizontal measure window end** (int) 180: Default, [in active pixels (*4) related to HSYNC]

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
B7h	W	VSM1_40	LBHISTBLA	x	x	x	x	x	x	x	x									**Histogram black** (int) 25: Default
			LBHWST										x	x	x	x	x	x	x	**Horizontal measure window start** (int) 36: Default, [in active pixels (*4) related to HSYNC]
B8h	W	VSM1_40	LBMASLA	x																**Master-slave switch for detection** 0: Slave 1: Master
			LBVWSTLO		x	x	x	x	x	x	x									**Vertical measure window lower start** (int) 96: Default], [in lines (*2) related to VSYNC]
			LBFS									x								**Field subsampling mode** 0: A+B fields 1: Only A field
			LBVWENDUP										x	x	x	x	x	x	x	**Vertical measure window upper end** (int) 73: Default], [in lines (*2) related to VSYNC]
B9h	W	VSM1_40	LBGSDEL	x	x	x	x	x												**Gradient stability delay value** (int) 10: Default]
			LBGFBDEL						x	x	x	x	x							**Gradient fall back delay value** (int) 11: Default]
			LBVWSTUP											x	x	x	x	x	x	**Vertical measure window upper start** (int) 20: Default], [in lines (*2) related to VSYNC]
BAh	W	VSM1_40	LBASDEL	x	x	x	x	x												**Activity stability delay** (int) 10: Default]
			LBVISUON						x											**Visualisation of letter box results** 0: Disabled 1: Enabled
			LBACTIVITY							x	x	x	x	x						**Activity** (int) 5: Default]
			LBTHDNBNG												x	x	x	x	x	**Threshold for darkness-brightness, gradient only** (int) 15: Default]
Output Data Controller																				
BBh	W	VSBM2_36	PPLOFF	x	x	x														**Synchronization offset** (For switching from hor. freerun mode to locked mode) Granularity: 4 pixel 000: 0 010: 8 111: 28

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			LPFOPOFF				x	x	x	x										**Lines per field offset:** (For switching from vertical freerun mode to locked mode) Granularity: 2 lines 0000: 0 0110: 12 1111: 31 (Set equal to LPFOPOFF in BFh)
			NAPPLOP								x	x	x	x	x	x	x	x	x	**Not active pixel per line output:** Granularity: 4pixel 000000000: No not active pixel 000000001: 4 not active pixel 111111111: 2044not active pixel
BCh	W	VSBM2_36	VOUTFR	x																**VSYNC freerun:** 0: Locked mode 1: Freerun mode
			HOUTFR		x															**HSYNC freerun:** 0: Locked mode 1: Freerun mode
			NOSYNC			x														**No horizontal synchronization will be performed:** 0: Horizontal synchronization 1: No horizontal synchronization
			RMODE				x	x												**Raster mode: (50p / 100 i)** 00 = αβαβ / αβ 01 = ααββ / αβ 10 = αααα / αα 11 = ββββ / αα
			OPDEL						x											(see BEh)
			HOUTDEL							x	x	x	x	x	x	x	x	x	x	**H Sync output Delay:** Granularity: 4 pixel 0000000000: No delay 0000000001: 4 pixel delay 1111111111: 4092 pixel delay
BDh	W	VSBM2_36	GFBON	x																**Global fallback** 0: Disabled 1: Enabled
			FMODE		x															**Frame mode** 0: $2f_V$, 1: $1f_V$
			PDGSR			x														**Switch for Vsync transfer algorithm:** 0: Vsync transfer algorithm is enabled 1: Vsync transfer algorithm is disabled

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			MASTERON				x													**Master channel** 0: Disabled (no master picture visible) 1: Enabled
			SLAVEON					x												**Slave channel** 0: Disabled (no slave picture visible) 1: Enabled
			LPFOP[8]						x											(See BEh)
			PPLOP							x	x	x	x	x	x	x	x	x	x	**Pixel per line output:** Granularity: 4 0000000000: 0 pixel 0100100000: 1152 pixel 1111111111: 4092 pixel
BEh	W	VSBM2_36	OPDEL	x	x	x	x	x	x	x	x									**V delay for output operation:** 000000000: No delay 010101010: 170 lines 111111111: 511 lines
			LPFOP[7:0]									x	x	x	x	x	x	x	x	**Lines per field output:** Only used for freerun mode Granularity: 2 lines 000000000: No lines 010011100: 312 lines 111111111: 1022 lines
Memory Controller																				
BFh	W	VSBM1_36	DISPMODE	x	x	x	x													**Display mode** 0000: FSM-mode 0001: SPS-mode 0010: SSC1-mode 0011: MUP1-mode 0100: MUP2-mode 0101: PCE-mode 0110: PCF-mode 0111: PCP-mode 1000: SSC2-mode
			MOTVALON					x												**Motion values on** (Only active for DISPMODE=0000) 0: Motion values are not stored 1: Motion values are stored
			REFRON							x										**Refresh on** 0: No memory refresh 1: Memory refresh active

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			REFRPER								x	x								**Refresh period** 00: 3.2 ms 01: 6.5 ms 10: 13 ms 11: 26 ms
			LPFOPOFF										x	x	x	x				**Lines per field offset:** (For switching from vertical freerun mode to locked mode) Granularity: 2 lines 0000: 0 0110: 12 1111: 30 (Set equal to LPFOPOFF in BBh)
			ARSDIS														x			**Automatic raster-shift enable** 0: Allow raster shift if stable signals detected 1: Allow raster shift always
			JLCRES															x		**Reset joint line controller** Reset of joint line controller for SSC mode 0: Enable 1: Reset
			MASLEX																x	**Master slave exchange** Synchronize the display raster to the slave channel for master slave exchange 0: Display raster phase is synchronized to master channel 1: Display raster phase is synchronized to slave channel
C0h	W	VSBS_36	STOPMOS	x	x	x														**Static operation mode slave** Defines the algorithm of upconversion for slave channel 000: (reserved) 001: ABAB (αβαβ) or A+B, A+B (α+β, α+β) 010: AABB (ααββ) or A+A, B+B (α+β, α+β) 011: AAAA (αβαβ) or A+A, A+A (α+β, α+β) 100: AAAA (αααα) or A+A*, A+A* (α+β, α+β) 101: BBBB (αβαβ) or B+B, B+B (α+β, α+β) 110: BBBB (ββββ) or B+B*, B+B* (α+β, α+β) 111: AA*B*B (αβαβ) or A+A*, B*+B (α+β, α+β)
			EXTRD					x												**External read** Reading data via ITU R656 to an external controller 0: External read disabled 1: External read enabled
			P3DIS						x											**Port P3 disable** 0: Enabled 1: Disabled
			P4DIS							x										**Port P4 disable** 0: Enabled 1: Disabled

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			HPE1OFF									x								**Horizontal pixel erosion 1** 0: On 1: Off
			VLEROFF										x							**Vertical line erosion** 0: On 1: Off
			HPS1OFF											x						**Horizontal pixel smearing 1** 0: On 1: Off
			HPE2OFF												x					**Horizontal pixel erosion 2** 0: On 1: Off
			HPEXOFF													x				**Horizontal pixel extension** 0: On 1: Off
			VLEXOFF														x			**Vertical line extension** 0: On 1: Off
			HPS2OFF															x		**Horizontal pixel smearing 2** 0: On 1: Off
			VLS1OFF																x	**Vertical line smearing** 0: On 1: Off
Formatter																				
C1h	W	VSBM2_36	CHROMSIGN656	x																**Chrominance format for 656 output** 0: (R-Y), (B-Y) output 1: -(R-Y), -(B-Y) output
			FIOFFOFF		x															**Fieldoffset for ITU656 NTSC signals** 0: Disabled 1: Enabled
			DPOUT656			x														**Enable (single or double-scan) digital DP656 output** 0: Disable output 1: Enable output
			SHIFTUV				x													**Shift UV subsampling at digital output** 0: Take first UV couple 1: Take second UV couple
			FSWFTL					x												**Stability signal of LL_HPLL** 0: STABLL is generated accoding to ***SETSTABLL*** 1: STABLL is forced to 1 (hout synchronization enabled)

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			AFPROC						x											**Active field processing for 656V generation** 0: Inverted active field used as v-sync output 1: V-sync modifies end of active video
			V656DEL							x										**V656 delay** 0: Identical delay for modification 1: Field 0 is one line shorter Note: Has only effect when **AFPROC** =1
			CLK656OUTINV								x									**656CLK output inversion** 0: Normal cloct 1: Inverted clock
			HOUTTR									X								**Horizontal output tristate** 0: Normal operation 1: Tristate
			UVCODE										X							**Chroma output data format** 0: Signed 2's complement 1: Binary
			V100IN											X						**VOUT pin used as input** 0: Output 1: Input
			DIGOUTEN												X					**Digital output (drout, dbout, dgout)** 0: Disabled 1: Enabled
			M422													x				**Output mode** 0: 4:4:4 1: 4:2:2
			CHRSFM														x			**Chroma subsampling filter** 0: Disabled 1: Enabled
			NSHAP															x		**Noise shaper** 0: Dabled 1: Enabled
			DWO																x	**Data width at output** 0: 8-bit 1: 9-bit
YUV_RGB																				
C2h	W	VSBM2_36	C1[10:2]	x	x	x	x	x	x	x	x									**Matrix coefficient C1** (2c) 0: Default
			C2[10:2]									x	x	x	x	x	x	x	x	**Matrix coefficient C2** (2c) 179: Default
C3h	W	VSBM2_36	C3[10:2]	x	x	x	x	x	x	x	x									**Matrix coefficient C3** (2c) -44: Default

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			C4[10:2]									x	x	x	x	x	x	x	x	**Matrix coefficient C4** (2c) -91: Default
C4h	W	VSBM2_36	C5[10:2]	x	x	x	x	x	x	x	x									**Matrix coefficient C5** (2c) 227: Default
			C6[10:2]									x	x	x	x	x	x	x	x	**Matrix coefficient C6** (2c) 0: Default
C5h	W	VSBM2_36	TO1RGB	x	x	x														**RGB or YUV output selection** 000: YUV output 001: RGB outpu (others): Reserved
			UENINV				x													**Digital 601 output** 0: Starting with U sample at beginning of line 1: Starting with V sample at beginning of line
			C6[1:0]					x	x											(See C4h)
			C5[1:0]							x	x									(See C4h)
			C4[1:0]									x	x							(See C3h)
			C3[1:0]											x	x					(See C3h)
			C2[1:0]													x	x			(See C2h)
			C1[1:0]															x	x	(See C2h)
Pixel Mixer																				
C6h	W	VSBM2_36	WINDVSP	x	x															**Vertical window speed** 00: Slow 01: medium 10: Fast 11: Very fast
			WINDVST			x														**Vertical windowing: Start** 0: Window is closed 1: Window is open
			WINDVDR				x													**Vertical windowing: Direction** 0: Open the vertical window 1: Close the vertical window
			WINDVON					x												**Vertical windowing: Enable** 0: Off 1: On
			HORPOSP						x	x	x	x	x	x	x	x	x	x	x	**Horizontal position inside active picture area** (int) 0: 0 pixel (int) 2047: 2047 pixel

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
C7h	W	VSBM2_36	WINDHSP	x	x															**Horizontal windowing: Speed** 00: Slow 01: Medium 10: Fast 11: Very fast
			WINDHST			x														**Horizontal windowing: Start** 0: Window is closed 1: Window is open
			WINDHDR				x													**Horizontal windowing: Direction** 0: Open the horizontal window 1: Close the horizontal window
			WINDHON					x												**Horizontal windowing: Enable** 0: Off 1: On
			HORWIDTHP						x	x	x	x	x	x	x	x	x	x	x	**Horizontal position inside active picture area** (int) 0: 0 pixel (int) 2047: 2047 pixel
C8h	W	VSBM2_36	YCUR	x	x	x	x													**Luminance value for curtain (4MSB)** 0001: Default value (yields value **0 001**0 0000=32)
			LUMAMP					x	x											**Luminance amplification** 00: 1 01: 5/4 10: 6/4 11: 8/4
			VERPOSP							x	x	x	x	x	x	x	x	x	x	**Vertical start position of background (or test-pattern)** (int) 0: 0 lines (int) 1023: lines
C9h	W	VSBM2_36	UCUR	x	x	x	x													**Chrominance value for curtain (4MSB)** 0000: Default value (yields value **0 000**0 0000=0)
			CHROMAMP					x	x											**Chrominance Amplification** 00: -2 01: -1 10: +1 11: +2
			VERWIDTHP							x	x	x	x	x	x	x	x	x	x	**Vertical width of background or pattern (or test-pattern)** (int) 0: 0 lines (int) 1023: 1023 lines
CAh	W	VSBS_36	VCUR	x	x	x	x													**Chrominance value for curtain (4MSB)** 0000: Default value (yields value **0 000**0 0000=0)
			HORPOSF						x	x	x	x	x	x	x	x	x	x	x	**Horizontal position of slave frame** (int) 0: most left (int) 2047: most right

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
CBh	W	VSBS_36	HORFRAMEF	x	x	x	x	x												**Horizontal slave frame size** (int) 0: 0 pixel (int) 31: 31 pixel
			HORWIDTHF						x	x	x	x	x	x	x	x	x	x	x	**Horizontal width of slave frame hole** (int) 0: 0 pixel (int) 2047: 2047 pixel
CCh	W	VSBS_36	VERFRAMEF	x	x	x	x	x												**Vertical slave frame size** (int) 0: 0 lines (int) 31: 31 lines
			VERPOSF							x	x	x	x	x	x	x	x	x	x	**Vertical position of slave frame** (int) 0: top (int) 1023: bottom
CDh	W	VSBS_36	YBAGR	x	x	x	x													**Luminance Value for background (4MSB)** 0001: Default value (yields value **0 001**0 0000=32)
			VERWIDTHF							x	x	x	x	x	x	x	x	x	x	**Vertical width of slave frame hole** (int) 0: 0 lines (int) 1023: lines
CEh	W	VSBM2_362	UBAGR	x	x	x	x													**Chrominance value for background (4MSB)** 0000: Default value (yields value **0 000**0 0000=0)
			HORPOSG						x	x	x	x	x	x	x	x	x	x	x	**Horizontal position of master frame** (int) 0: most left (int) 2047: most right
CFh	W	VSBM2_36	VBAGR	x	x	x	x													**Chrominance value for background (4MSB)** 0000: default value (yields value **0 000**0 0000=0)
			HORWIDTHG						x	x	x	x	x	x	x	x	x	x	x	**Horizontal width of master frame hole** (int) 0: 0 pixel (int) 2047: 2047 pixel
D0h	W	VSBM2_36	HORFRAMEG	x	x	x	x	x												**Horizontal master frame size** (int) 0: 0 lines (int) 31: 31 lines
			VERPOSG							x	x	x	x	x	x	x	x	x	x	**Vertical position of master frame** (int) 0: top (int) 1023: bottom
D1h	W	VSBM2_36	VERFRAMEG	x	x	x	x	x												**Vertical master frame size** (int) 0: 0 lines (int) 31: 31 lines
			VERWIDTHG							x	x	x	x	x	x	x	x	x	x	**Vertical width of master frame hole** (int) 0: 0 lines (int) 1023: lines

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
D2h	W	VSBM2_36	PRIOP				x	x	x											**Priority background (or test-pattern)** 000: 0 010: 4 111: 14
			OBTEMP							x										**Temporary overlapping flag** 0: Static overblending 1: Temporal overblending
			OBSOFT								x									**Overblending flag** 0: No overblending 1: Soft overblending
			PATTMODE									x	x	x						**Test-pattern mode** 000: Trivial background mode 001: Trivial background mode 010: trivial background mode 011: Y-ramp (strong) 100: Y-ramp (soft) 101: YUV-ramp 110: Color bar 111: Crosshatch
			TBLEND												x	x				**Time for smooth temporal overblending** 00: 64 01: 128 10: 256 11: 512
			FRAMEDIMM														x			**Frame dimension master** 0: 2-dim. 1: 3-dim.
			FRAMEDIMS															x		**Frame dimension slave** 0: 2-dim. 1: 3-dim.
D3h	W	VSBM2_36	PRIOC	x	x	x														**Priority curtain** 000: 0 001: 2 111: 14
			PRIOS				x	x	x											**Priority slave** 000: 0 110: 12 111: 14
			PRIOF							x	x	x								**Priority slave frame** 000: 0 101: 10 111: 14

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			PRIOM										x	x	x					**Priority master** 000: 0 100: 8 111: 14
			PRIOG													x	x	x		**Priority master frame** 000: 0 011: 6 111: 14
Output sync controller																				
D4h	W	VSBM2_36	BLANDEL	x	x	x	x	x	x	x	x									**Delay in pixels from hsync to active edge of blank signal:** Blank_start=4****BLANDEL*** 00000000: No delay 00000001: 4 pixel delay 11111111: 1020 pixel delay
			VBLANPOL									x								**Vertical blank signal polarity** 0: Positive 1: Negative
			CLKOUT72										x							**Output clock select** 0: Clkout_o depends on ***CLKOUTSEL*** 1: Ckout_o is identical to clkb72
			CLKOUTINV											x						**CLKOUT inversion** 0: No inverted CLKOUT 1: Inverted CLKOUT
			HOUTPOL												x					**HOUT polarity:** 0: High active 1: Low active
			VOUTPOL													x				**VOUT polarity:** 0: High active 1: Low active
			BLANPOL														x			**Blank polarity:** 0: Blank is high active 1: Blank is low active
			CLKOUTSEL															x		**Output clock select** 0: Clkout_o is identical to clkb27 1: Clkout_o is identical to clkb36 *Note: HSYNC, VSYNC, BLANK are transferred to selected clock*
			CLKOUTON																x	**Output clock (pin clkout)** 0: Disabled 1: Enabled
D5h	W	VSBM2_36	CLKOUTSEL72	x																**Output clock select** 0: CLKOUT depends on **CLKOUTSEL** 1: CLKOUT is identical to clkb72

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			VBLANDEL[9:5]			x	x	x	x	x										(see D6h)
			BLANLEN								x	x	x	x	x	x	x	x	x	**Length in pixels from start of active blank signal:** Blank_length=4*__BLANLEN__ 00000000: No pixel 11110000: 960 pixel 11111111: 1020 pixel length
Delay block																				
D6h	W	VSBM2_36	VBLANDEL[4:0]	x	x	x	x	x												**Vertical delay in lines from vsync to active edge of blank signal:** Blank_start=4*V__BLANDEL__ 00000000: No delay 11111111: 1020 lines delay
			VBLANLEN							x	x	x	x	x	x	x	x	x	x	**Vertical length in lines from start of active blank signal:** Blank_length=4*__VBLANLEN__ 00000000: No line 11111111: 1020 lines
D7h	W	VSBM2_36	PKLY	x	x	x	x	x	x	x	x									**Voltage level for Y DAC output** 00000000: 0.4 V 10000000: 1.0 V 11111111: 1.9 V *Note: Including peaking overshoots. 0.9V for white max.*
			PKLU									x	x	x	x	x	x	x	x	**Voltage level for U DAC output** 00000000: 0.4 V 10000000: 1.0 V 11111111: 1.9 V
D8h	W	VSBM2_36	COARSEDEL					x	x	x										**Luminance coarse delay output** Granularity: 1 CLKB36 (27.8 ns for TV signal) 000: -4 CLKB36 100: No delay 111: +3 CLKB36
			FINEDEL								x									**Luminance fine delay output** 0: No delay 1: +1 CLKB72 (13.9 ns for TV signal)
			PKLV									x	x	x	x	x	x	x	x	**Voltage level for U DAC output** 00000000: 0.4 V 10000000: 1.0 V 11111111: 1.9 V
C800																				
D9h	W	NTO	C800	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	C800 (reserved)
DAh	W	NTO	VDELAY_BE	x	x															00: vertical synchronized takeover, no sychronisation of FE and BE 01: Update of BE register with the next BE v after update of the FE registers 10: Update of BE register like VDELAY_BE=1 plus one additional BE field delay 11: Update of BE register like VDELAY_BE=1 plus two additional BE fields delay

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			VSEL_BE			x														0: master channel synchonizes BE 1: slave channel synchonizes BE
			GPH50											x	x					**H50/IRQ-pin switching** 00: Normal function 01: Normal function 10: H50/IRQ static 0 11: H50/IRQ static 1
			CPUIRQ2V													x	x			**VIN/INTR-pin switching** 00: V-pin used as v-input for front-end 01: V-pin is output of C800 interrupt 10: V static 0 11: V static 1
			CPUDISABLE															x		**C800 processor** 0: Processor enabled 1: Processor disabled
			AUTOINC_OFF																x	**I²C Autoincrement** 0: Autoincrement after 2 byte access 1: No autoincrement
Read Registers Master Channel																				
DBh	R	VS1_20	LPFLDM	x	x	x	x	x	x	x	x									**Nr. of lines per field (input signal)** 00000000: 256 lines or less 11111111: 766 lines or more LINES=2*_**LPFLD**_+256
			NRPIXELM									x	x	x	x	x	x	x	x	**Pixel number of input signal** Granularity: 4 00000000: 384 or less 11111111: 1404 or more PIXEL=4*_**NRPIXEL**_+384
DCh	R	VS1_20	DETHPOLM	x																**Detected polarity of HSync** 0: Negative 1: Positive
			DETVPOLM		x															**Detected polarity of V sync** 0: Negative 1: Positive
			STDETM			x	x	x												**Detected color standard** 000: Non standard or standard not detected 001: NTSC M 010: PAL M 011: NTSC44 100: PAL60 101: PAL N 110: SECAM 111: PAL B/G

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			SCOUTENM						x											**SCDEV valid indication** 0: SCDEV not valid 1: SCDEV valid
			PALIDM							x										**PAL identification** 0: Not PAL 1: PAL
			CKSTATM								x									**Colorkill status** 0: Color off 1: Color on
			LNSTDRDM									x								**Line standard detection** 0: 60 Hz 1: 50 Hz
			INTM										x							**Interlace detection** 0: Progressive input 1: Interlace input
			SCDEVM											x	x	x	x	x	x	**Deviation of clock system or color carrier** 100000: Minimum deviation 000000: No deviation 011111: Maximum deviation
DDh	R		VFLYMDM	x																**Vertical flywheel mode locked** 0: Unlocked 1: Locked
			VLENGTHM		x	x	x	x	x	x	x									**Length of vertical pulse** 0000000: Short v 1111111: Long v
			AGCADJCV1									x	x	x	x	x	x			**AGC value for ADC1** 000000: Smallest input range 111111: Biggest input range
			PALDETM															x		**PAL identification (algorithm 2)** 0: Not PAL 1: PAL
			STABM																x	**Status of synchronization** 0: Sync separation not locked 1: Sync separation locked and stable
DEh	R	VSM1_40	NOISEMEM	x	x	x	x	x	x	x										**Noise level of the input signal (blanking algorithm):** 0000000: No noise 1111110: Strong noise 1111111: Strong noise or measurement failed
			NOISE									x	x	x	x	x	x	x	x	**Noise level of the input signal (picture algorithm):** 00000000: No noise 11111111: Strong noise
DFh	R	VSM2_40	FCIM	x	x	x	x													Cyclic field counter Input processing master

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			STATSIZE										x	x						**Statistic of homogenous areas** 00: Not enough homogenous areas 11: Many homogenous areas found
			FILMMODEM													x	x	x	x	**Film mode detection value:** 0000: Camera mode (secure detection) 0001: Film mode PAL phase 0 (secure detection) 0010: Film mode PAL phase 1 (secure detection) 0011: Film mode NTSC phase 0 (secure detection) 0100: Film mode NTSC phase 1 (secure detection) 0101: Film mode NTSC phase 2 (secure detection) 0110: Film mode NTSC phase 3 (secure detection) 0111: Film mode NTSC phase 4 secure detection) 1000: Camera mode (unsecure detection) 1001: Film mode PAL phase 0 (unsecure detection) 1010: Film mode PAL phase 1 (unsecure detection) 1011: Film mode NTSC phase 0 (unsecure detection) 1100: Film mode NTSC phase 1 (unsecure detection) 1101: Film mode NTSC phase 2 (unsecure detection) 1110: Film mode NTSC phase 3 (unsecure detection) 1111: Film mode NTSC phase 4 (unsecure detection)
E0h	R	VSM2_40	FMOTREGM			x	x	x	x	x	x	x	x	x	x	x	x	x	x	**Film mode detection register value**
E1h	R	VSM2_40	GMOTREGM	x	x	x	x	x	x	x	x	x	x	x	x	x	x			**Global motion detection register value**
			GSTILLM															x		**Global still detection value:** 0: Picture status: not still 1: Picture status: still
			GMOTIONM																x	**Global motion detection value:** 0: Picture status: no motion 1: Picture status: in motion
E2h	R	NTO/RSTYP	AM50_OM	x																**Last detected Standard 50 Hz** 0: PAL or none 1: SECAM
			AM60_OM		x															**Last detected Standard 60 Hz** 0: NTSC M or none 1: NTSC44 or PAL60
			LBSTATUS												x					**Status bit for letter box detection:** 0: No new value available 1: New value from Letter Box Detection available
			NOISESTATUS													x				**Indicates new value of the global motion detector available** 0: ***NOISESTATUS*** has not been updated 1: New value of ***NOISESTATUS*** available reset automatically when read

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			GMDSTATUSM														x			**Indicates new value of the gobal motion detector available** 0: ***GMDSTATUS*** has not been updated 1: New value of ***GMDSTATUS*** available reset automatically when read
			FMSTATUSM															x		**Indicates new value of the film mode detector available** 0: ***FMSTATUS*** has not been updated 1: New value of ***FMSTATUS*** available reset automatically when read
			NMSTATUSM																x	**Indicates new value of the noise measurement** 0: NOISEME has not been updated 1: New value of NOISEME available reset automatically when read
E3h	R	VSDCI_36	TFDPPM[8:4]	x	x	x	x	x												**Calculated pivot point** Pivot point=12.5 IRE+(***TFDPPM***+192)*0.192 IRE ***TFDDPM*** is limited to -192....-44 Pivot point is in the range of 12.5 IRE ...41 IRE
			GAINSEG1FRCM							x	x	x	x	x	x	x	x	x	x	**Calculated gain segment 1** Gain_Segment_1=1+***GAINSEG1FRCM***/1024 **GAINSEG1FRCM** is limited to 0...510 Gain_Segment_1 is in the range of 1 ... 1.5
E4h	R	VSDCI_36	TFDPPM[3:0]		x	x	x	x												(See E3h)
			GAINSEG2FRCM							x	x	x	x	x	x	x	x	x	x	**Calculated gain segment 2** Gain_Segment_2=1+***GAINSEG2FRCM***/1024 **GAINSEG2FRCM** is limited to 0...716 Gain_Segment_2 is in the range of 1 ... 1.7
Read registers slave channel																				
E5h	R	VS1_20	LPFLDS	x	x	x	x	x	x	x	x									**Nr. of lines per field (input signal)** 00000000: 256 lines or less 11111111: 766 lines or more LINES=2*__LPFLD__+256
			NRPIXELS									x	x	x	x	x	x	x	x	**Pixel number of input signal** Granularity: 4 00000000: 384 or less 11111111: 1404 or more PIXEL=4*__NRPIXEL__+384
E6h	R	VS1_20	DETHPOLS	x																**Detected polarity of H Sync** 0: Negative 1: Positive
			DETVPOLS		x															**Detected polarity of V Sync** 0: Negative 1: Positive

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			STDETS			x	x	x												**Detected color standard** 000: Non standard or standard not detected 001: NTSC M 010: PAL M 011: NTSC44 100: PAL60 101: PAL N 110: SECAM 111: PAL B/G
			SCOUTENS						x											**SCDEV valid indication** 0: SCDEV not valid 1: SCDEV valid
			PALIDS							x										**PAL identification** 0: Not PAL 1:PAL
			CKSTATS								x									**Colorkill status** 0: Color off 1: Color on
			LNSTDRDS									x								**Line standard detection** 0: 60 Hz 1: 50 Hz
			INTS										x							**Interlace detection** 0: Progressive input 1: Interlace input
			SCDEVS											x	x	x	x	x	x	**Deviation of clock system or color carrier** 100000: Minimum deviation 000000: No deviation 011111: Maximum deviation
E7h	R	VS1_20	VFLYMDS	x																**Vertical flywheel mode locked** 0: Unlocked 1: Locked
			VLENGTHS		x	x	x	x	x	x	x									**Length of vertical pulse** 0000000: Short v 1111111: Long v
			AGCADJCV2									x	x	x	x	x	x			**AGC value for ADC2** 000000: Smallest input range 111111: Biggest input range
			PALDETS															x		**PAL identification (algorithm 2)** 0: Not PAL 1: PAL
			STABS																x	**Status of synchronization** 0: Sync separation not locked 1: Sync separation locked and stable

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
E8h	R	VSS1_40	NOISEMES	x	x	x	x	x	x	x										**Noise level of the input signal (blanking algorithm):** 0000000: No noise 1111110: Strong noise 1111111: Strong noise or measurement failed
E9h	R	NTO/RSTYP	AM50_OS	x																**Last detected standard 50 Hz** 0: PAL or none 1: SECAM
			AM60_OS		x															**Last detected standard 60 Hz** 0: NTSC M or none 1: NTSC44 or PAL60
			NMSTATUSS																x	**Indicates new value of the noise measurement** 0: NOISEME has not been updated 1: New value of NOISEME available reset automatically when read
Read Registers Common Channel																				
EAh	R	VSSLI_20	DATA_CCWSS2	x	x	x	x	x	x	x	x									**Second CC or WSS DATA Byte (A7=MSB, A0=LSB)**
			DATA_CCWSS1									x	x	x	x	x	x	x	x	**First CC or WSS DATA Byte(B7=MSB, B0=LSB)**
EBh	R	VSSLI_20	DATA_USWSS3	x	x	x	x	x	x	x	x									**Third US-WSS DATA Byte (A7=MSB, A0=LSB)**
			DATA_USWSS2									x	x	x	x	x	x	x	x	**Second US-WSS DATA Byte(B7=MSB, B0=LSB)**
ECh	R	VSSLI_20	DATA_USWSS1	x	x	x	x	x	x	x	x									**First US-WSS DATA Byte (A7=MSB, A0=LSB)**
			POR									x								**Reset indication** A reset at pin 24 (reset) sets ***POR***. ***POR*** is reset with ***PORCNCL*** (9Bh) 0: No reset appeared 1: Reset appeared
			TVMODE												x					**TV mode detection** 0: Comb filter input is nonstandard signal (VCR) 1: Comb filter input is standard signal (TV)
			SLFLDUSWSS													x				**Field number of sliced data (US-WSS)** 0: First field 1: Second field
			DATAVUSWSS														x			**New data indication (US WSS)** 0: Data read via I²C or no new data available 1: New data received and available in DATAA and DATAB
			SLFLDCCWSS															x		**Field number of sliced data (CC or WSS)** 0: First field 1: Second field
			DATAVCCWSS																x	**New data indication (CC or WSS** 0: Data read via I²C or no new data available 1: New data received and available in DATAA and DATAB

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
EDh	R	NTO/RSTYP	FBSTAT									x								**Indicates overflow at FBL input** 0: No overflow 1: Overflow
			FBFALL										x							**Indicates falling edge at FBL input** 0: No falling edge 1: Flling edge detected Reset automatically when read
			FBRISE											x						**Indicates rising edge at FBL input** 0: No rising edge 1: Rising edge detected Reset automatically when read
			PFBL												x					**Indicates overflow at FBL input** 0: No overflow 1: Overflow
			PG													x				**Indicates overflow at GREEN input** 0: No overflow 1: Overflow
			PB														x			**Indicates overflow at BLUE input** 0: No overflow 1: Overflow
			PR															x		**Indicates overflow at RED input** 0: No overflow 1: Overflow
			FBLACTIVE																x	**Activity at FBL input** 0: No activity 1: Activity Reset automatically when read
EEh	R	VSM1_40	MAXGUC							x	x	x	x	x	x	x	x	x	x	**Letter box detection: Maximum gradient upper part** Internal value, only for test purposes
EFh	R	VSM1_40	MAXGLC							x	x	x	x	x	x	x	x	x	x	**Letter box detection: Maximum gradient lower part** Internal value, only for test purposes
F0h	R	VSM1_40	MAXALC	x	x	x	x													(see F1h)
			MAXHUC							x	x	x	x	x	x	x	x	x	x	**Letter box detection: Maximum histogram upper part** Internal value, only for test purposes
F1h	R	VSM1_40	MAXALC	x	x	x	x	x												**Letter box detection: Maximum activity lower part** Internal value, only for test purposes
			MAXHLC							x	x	x	x	x	x	x	x	x	x	**Letter box detection: Maximum histogram lower part** Internal value, only for test purposes
F2h	R	VSM1_40	GRADSLAA	x	x	x	x	x	x	x	x									**Letter box detection: Gradient start line of active area** Internal value, only for test purposes

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			MAXAUC									x	x	x	x	x	x	x	x	**Letter box detection: Maximum activity upper part** Internal value, only for test purposes
F3h	R	VSM1_40	LBFORMAT	x																**Letter box detection: Format** 0: 4:3 format 1: Other format (letter box)
			LBSUBTITLE		x															**Letter box detection: Subtitle flag** 0: No subtitle 1: Subtitle available
			LBTOPTITLE			x														**Letter box detection: Toptitle flag** 0: No toptitle 1: Toptitle available
			GRADISSTABLE				x													**Letter box detection: Gradient is stable** Internal value, only for test purposes
			TOPTITLE					x												**Letter box detection: Upper area contains high activity** Internal value, only for test purposes
			SUBTITLE						x											**Letter box detection: Lower area contains high activity** Internal value, only for test purposes
			NOGRADFOUND								x									**Letter box detection: No gradient found** Internal value, only for test purposes
			SWITCHTO43									x								**Letter box detection: Switch to 4:3 format** Internal value, only for test purposes
			UPWHITE										x							**Letter box detection: Upper area contains high brightness level** Internal value, only for test purposes
			LPWHITE											x						**Letter box detection: Lower area contains high brightness level** Internal value, only for test purposes
			UPBLACK												x					**Letter box detection: Upper area contains medium brightness level** Internal value, only for test purposes
			LPBLACK													x				**Letter box detection: Lower area contains medium brightness level** Internal value, only for test purposes
F4h	R	VSM1_40	LBSLAA	x	x	x	x	x	x	x										**Letter box detection: Start line of active area** LBSLAA is measured in relation to VSYNC
			LBELAA								x	x	x	x	x	x	x	x	x	**Letter box detection: End line of active area** LBELAA is measured in relation to VSYNC
F5h	R	VSM1_40	GRADELAA								x	x	x	x	x	x	x	x	x	**Letter box detection: Gradient end line of active area** Internal value, only for test purposes

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
F6h	R	NTO	VERSION	x	x	x														**Version of VSP 94xx family:** 010: VSP 94x2A 001: VSP 94x5B 011:VSP 94x7B 101: VSP 94x9C
			SLS				x													**Line standard at device output** 0: 100 Hz 1: 50 Hz
			REV					x	x	x	x									**Revision of VSP 94xxB family:** 0000: A11 0001: B11 0100: C1
			RMMIRROR									x	x							**= Readable value of RMODE**
			CHIPID											x	x	x	x			**Chip ID** 0000: VSP9405B / VSP 9425B (double scan mode) 0001: VSP9407B / VSP 9427B (double scan mode) 0010: VSP9435B / VSP 9425B (single scan mode) 0011: VSP9437B / VSP 9427B (single scan mode) 0100: VSP9415B 0101: VSP9417B 0110: VSP9445B 0111: VSP9447B
			STABLL																x	**Shows LL-HPLL lock status** 0: LL_HPLL is not locked 1: LL_HPLL is locked
F7h	R	NTO	ADR_RDY	x																**Ancillary data (656 input)** 0: not detected 1: detected
			FIELDCD1		x															**Field output CD1** 0: First field 1: Second field
			FIELDCD2			x														**Field output CD2** 0: First field 1: Second field
			VSRGB_40STAT				x													**V status bit of 40.5 MHz domain (RGB)** 0: New write or read cycle can start 1: No new write or read cycle can start
			VSBM2_36STAT					x												**V status bit of 36 MHz domain (back-end master 2)** 0: New write or read cycle can start 1: No new write or read cycle can start
			VSBM1_36STAT						x											**V status bit of 36 MHz domain (Back-end master 2)** 0: New write or read cycle can start 1: No new write or read cycle can start

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			VSDCI_36STAT							x										**V status bit of 36 MHz domain (DCI)** 0: New write or read cycle can start 1: No new write or read cycle can start
			VSBS_36STAT								x									**V status bit of 36 MHz domain (back-end slave)** 0: New write or read cycle can start 1: No new write or read cycle can start
			VSSLI_20STAT									x								**V status bit of 20.25 MHz domain (data slicer)** 0: New write or read cycle can start 1: No new write or read cycle can start
			VSS2_40STAT										x							**V status bit of 40.5 MHz domain (input slave 2)** 0: New write or read cycle can start 1: No new write or read cycle can start
			VSS1_40STAT											x						**V status bit of 40.5 MHz domain (input slave 1)** 0: New write or read cycle can start 1: No new write or read cycle can start
			VSM2_40STAT												x					**V status bit of 40.5 MHz domain (input master 2)** 0: New write or read cycle can start 1: No new write or read cycle can start
			VSM1_40STAT													x				**V status bit of 40.5 MHz domain (input master 1)** 0: New write or read cycle can start 1: No new write or read cycle can start
			VS656_27STAT														x			**V status bit of 27 MHz domain (ITU)** 0: New write or read cycle can start 1: No new write or read cycle can start
			VS2_20STAT															x		**V status bit of 20.25 MHz domain (CD 2)** 0: New write or read cycle can start 1: No new write or read cycle can start
			VS1_20STAT																x	**V status bit of 20.25 MHz domain (CD 1)** 0: New write or read cycle can start 1: No new write or read cycle can start
F8h	R	VSBM2_36	FCBM	x	x	x	x													Cyclic field counter output processing master
			SHIFTACT																x	**Raster phase shifting active** Indication of performing display raster phase shifting for joint line free SSC1 mode 0: Phase shift not active 1: Phase shift in progress
F9h	R	VS656_27	ADATA0	x	x	x	x	x	x	x	x									ITU656 input data **byte 1**
			ADATA1									x	x	x	x	x	x	x	x	ITU656 input data **byte 0**
FAh	R	VS656_27	ADATA2	x	x	x	x	x	x	x	x									ITU656 input data **byte 3**
			ADATA3									x	x	x	x	x	x	x	x	ITU656 input data **byte 2**

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
FBh	R	VS656_27	ADATA4	x	x	x	x	x	x	x	x									ITU656 input data **byte 5**
			ADATA5									x	x	x	x	x	x	x	x	ITU656 input data **byte 4**
FCh	R	VS656_27	ADATA6	x	x	x	x	x	x	x	x									ITU656 input data **byte 7**
			ADATA7									x	x	x	x	x	x	x	x	ITU656 input data **byte 6**
Command Registers																				
FDh	W		C800																	**C800 (reserved)**
FEh	W		IMRGB_40				x													**Immediate take-over 40.5 MHz domain (RGB)** 0: No immediate take-over 1: Immediate take-over
			IMBM2_36					x												**Immediate take-over 36 MHz dom. (back-end master 2)** 0: No immediate take-over 1: Immediate take-over
			IMBM1_36						x											**Immediate take-over 36 MHz dom. (back-end master 1)** 0: No immediate take-over 1: Immediate take-over
			IMDCI_36							x										**Immediate take-over 36 MHz domain (back-end master)** 0: No immediate take-over 1: Immediate take-over
			IMBS_36								x									**Immediate take-over 36 MHz domain (back-end slave)** 0: No immediate take-over 1: Immediate take-over
			IMSLI_20									x								**Immediate take-over 20.25 MHz domain (data slicer)** 0: No immediate take-over 1: Immediate take-over
			IMS2_40										x							**Immediate take-over 40.5 MHz domain (input slave 2)** 0: No immediate take-over 1: Immediate take-over
			IMS1_40											x						**Immediate take-over 40.5 MHz domain (input slave 1)** 0: No immediate take-over 1: Immediate take-over
			IMM2_40												x					**Immediate take-over 40.5 MHz domain (input master 2)** 0: No immediate take-over 1: Immediate take-over
			IMM1_40													x				**Immediate take-over 40.5 MHz domain (input master 1)** 0: No immediate take-over 1: Immediate take-over
			IM656_27														x			**Immediate take-over 27 MHz domain (ITU)** 0: No immediate take-over 1: Immediate take-over

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			IM2_20															x		**Immediate take-over 20.25 MHz domain (CD 2)** 0: No immediate take-over 1: Immediate take-over
			IM1_20																x	**Immediate take-over 20.25 MHz domain (CD 1)** 0: No immediate take-over 1: Immediate take-over
FFh	W		VSRGB_40				x													**V take-over 40.5 MHz domain (RGB)** 0: No V take-over 1: V take-over
			VSBM2_36					x												**V take-over 36 MHz dom. (back-end master 2)** 0: No V take-over 1: V take-over
			VSBM1_36						x											**V take-over 36 MHz dom. (back-end master 1)** 0: No V take-over 1: V take-over
			VSDCI_36							x										**V take-over 36 MHz domain (back-end master)** 0: No V take-over 1: V take-over
			VSBS_36								x									**V take-over 36 MHz domain (back-end slave)** 0: No V take-over 1: V take-over
			VSSLI_20									x								**V take-over 20.25 MHz domain (data slicer)** 0: No V take-over 1: V take-over
			VSS2_40										x							**V take-over 40.5 MHz domain (iInput slave 2)** 0: No V take-over 1: V take-over
			VSS1_40											x						**V take-over 40.5 MHz domain (input slave 1)** 0: No V take-over 1: V take-over
			VSM2_40												x					**V take-over 40.5 MHz domain (input master 2)** 0: No V take-over 1: V take-over
			VSM1_40													x				**V take-over 40.5 MHz domain (input master 1)** 0: No V take-over 1: V take-over
			VS656_27														x			**V take-over 27 MHz domain (ITU)** 0: No V take-over 1: V take-over
			VS2_20															x		**V take-over 20.25 MHz domain (CD 2)** 0: No V take-over 1: V take-over

Table 3–15: Common, continued

Subadd	R/W	Take Over	Name	A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	Description
			VS1_20																x	**V take-over 20.25 MHz domain (CD 1)** 0: No V take-over 1: V take-over

4. Specifications

4.1. Outline Dimensions

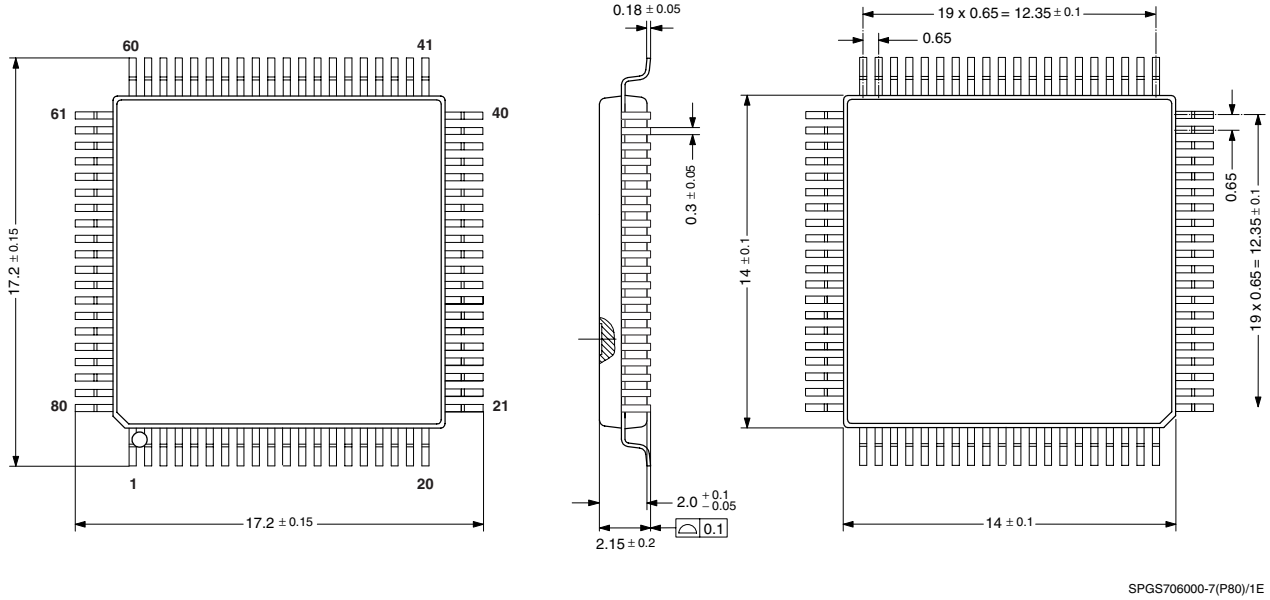


Fig. 4–1:
80-Pin Plastic Metric Quad Flat Pack
(MQFP80)
Weight approximately 0.96 g
Dimensions in mm

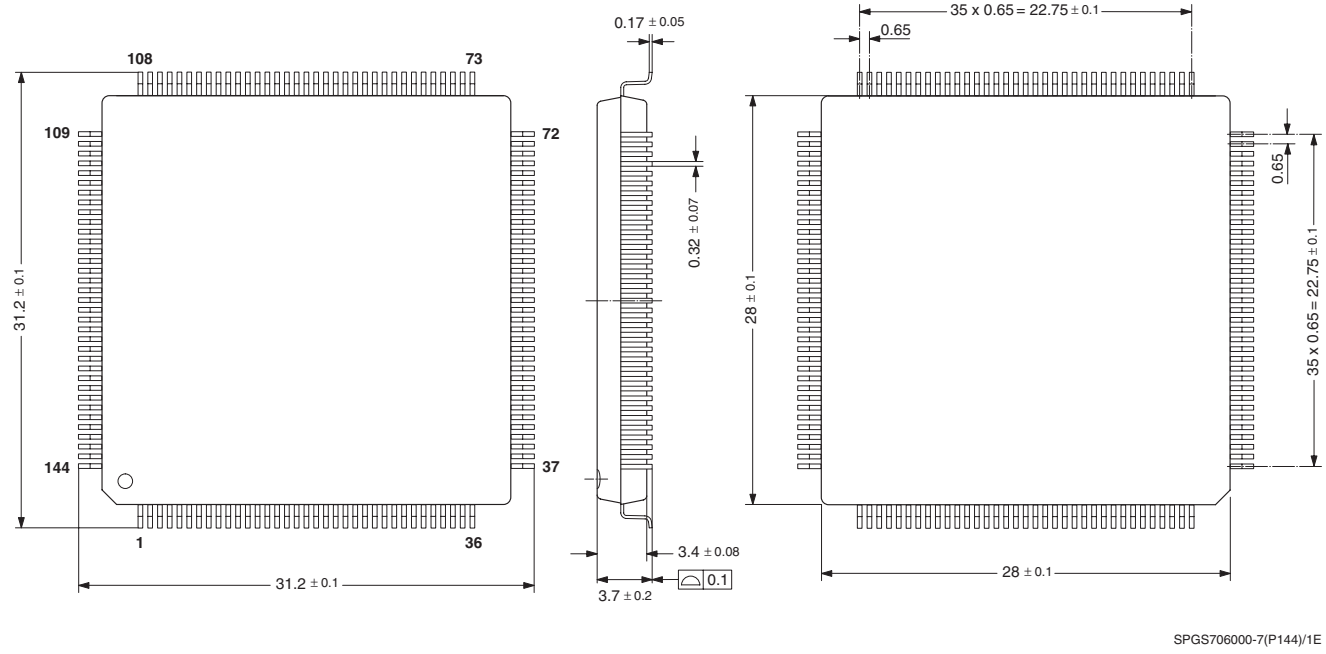


Fig. 4–2:
144-Pin Plastic Metric Quad Flat Pack
(MQFP144)
Weight approximately 5.5 g
Dimensions in mm

4.2. Pin Connections and Short Descriptions for VSP 94xxB

For VSP 941x/4x, the pin connections differ for pins: 1, 2, 3, 75, 76, 77, 78, 79 ,80 (see Section 4.2.2. on page 215).

4.2.1. Common Pin Connection and Short Descriptions

Pin No.		Pin Name	Type	Connection (If not used)	Short Description
MQFP 80-pin	MQFP 144-pin				
1	1	VDDDACY	S		DAC (Y)
2		AYOUT	O	Leave open or connect to vss and disable DAC	Y output
3	3	VSSDACY	S		DAC (Y)
4	4	VSSD2	S		Supply voltage for digital (0 V digital)
5	5	VDDD2	S		Supply voltage for digital (1.8 V digital)
6	10	SDA	I/O		I^2C-Bus data
7	13	TMS	I		Testmode select (Connected to vdd33)
8	14	656VIN/BLANK[1)]	I/O	Connect to vss and disable blank	Separate V input for 656 / BLANK output
9	15	656CLK	I/O	Leave open	Digital input / output clock
10	16	656IO7	I/O	Leave open	Digital input / output (MSB)
11	19	VSSP2	S		Supply voltage for digital (0 V pad)
12	20	VDDP2	S		Supply voltage for digital (3.3 V pad)
13	28	SCL	I		I^2C-Bus clk
14	29	V[2)]	I	Connect to vss	Vertical pulse for RGB input
15	30	656IO6	I/O	Leave open	Digital input / output
16	31	656IO5	I/O	Leave open	Digital input / output
17	32	HOUT	O	Leave open	Horizontal output (Single or double scan, dependent on version)
18	33	H50[3)]	O	Leave open	Hout 50 Hz (with skew)
19	34	ADR / TDI	I		I^2C address / test data in
20	35	V50[4)]	O	Leave open	Vout 50 Hz
21	37	656IO4	I/O	Leave open	Digital input / output
22	38	656IO3	I/O	Leave open	Digital input / output
23	39	VOUT	O	Leave open	Vertical output (Single or double scan, dependent on version)

Pin No.		Pin Name	Type	Connection (If not used)	Short Description
MQFP 80-pin	MQFP 144-pin				
24	40	RESET	I		$\overline{\text{Reset}}$ input (Reset active low)
25	41	VDDP3	S		Supply voltage for digital (0 V pad)
26	42	VSSP3	S		Supply voltage for digital (3.3 V pad)
27	51	CLKOUT	O	Leave open	Output clock (27 MHz nom.)
28	58	VDDD3	S		Supply voltage for DRAM (1.8 V digital)
29	59	VSSD3	S		Supply voltage for digital (0 V digital)
30	60	656IO2	I/O	Leave open	Digital input / output
31	61	656IO1	I/O	Leave open	Digital input / output
32	62	656IO0	I/O	Leave open	Digital input / output (LSB)
33	63	VSSD4	S		Supply voltage for digital (0 V digital)
34	64	VDDD4	S		Supply voltage for digital 1.8 V digital
35	65	VDDAFBL	S		Supply voltage for FBL (1.8 V)
36	66	VSSAFBL	S		Supply voltage for FBL (0 V)
37	67	FBL1	I	Connect to vss	Fast Blank input 1 (H1) (Analog input)
38	68	FBL2	I	Connect to vss	Fast Blank input 2 (H2) (Analog input)
39	70	RIN1	I	Connect to vss	R or V in1 (Analog input)
40	72	GIN1	I	Connect to vss	G or Y in1 (Analog input)
41	73	BIN1	I	Connect to vss	B of U in1 (Analog input)
42	74	VDDARGB	S		Supply voltage for RGB (1.8 V)
43	75	VSSARGB	S		Supply voltage for RGB (0 V)
44	76	VDD33RGB	S		Supply voltage RGB (3.3 V)
45	77	VSS33RGB	S		Supply voltage RGB (0 V)
46	78	RIN2	I	Connect to vss	R or V in2 (Analog input)
47	80	GIN2	I	Connect to vss	G or Y in2 (Analog input)
48	82	BIN2	I	Connect to vss	B of U in2 (Analog inpu)
49	89	VSSD5[5)]	S	Connect to vss	Supply voltage for digital (0 V)
50	92	VDDAC1	S		Supply voltage CVBS1 (1.8 V) and digital core supply
51	93	VSSAC1	S		Supply voltage CVBS1 (0 V)
52	96	CVBS1	I	Connect to vss	CVBS input (Analog input)
53	97	CVBS2	I	Connect to vss	CVBS input (Analog input)

Pin No.		Pin Name	Type	Connection (If not used)	Short Description
MQFP 80-pin	MQFP 144-pin				
54	98	CVBS3	I	Connect to vss	CVBS input (Analog input)
55	100	CVBS4	I	Connect to vss	CVBS input or Y1 (Analog input)
56	102	CVBS5	I	Connect to vss	CVBS input or C1 (Analog input)
57	104	CVBS6	I	Connect to vss	CVBS input or Y2 (Analog input)
58	106	CVBS7	I	Connect to vss	CVBS input or C2 (Analog input)
	94	CVBS8	I	Connect to vss	CVBS input (Analog input)
	95	CVBS9	I	Connect to vss	CVBS input (Analog input)
59	107	VDD33C	S		Supply voltage CVBS (3.3 V)
60	108	VSS33C	S		Supply voltage CVBS (0 V)
61	111	CVBSO3	O	Leave open	CVBS output 3 (Analog output)
62	110	CVBSO2	O	Leave open	CVBS output 2 (Analog output)
63	109	CVBSO1	O	Leave open	CVBS output 1 (Analog output
64	112	VDDAC2	S		Supply voltage CVBS2 (1.8 V)
65	113	VSSAC2	S		Supply voltage CVBS2 (0 V)
66	117	VDDD1	S		Supply voltage for digital (1.8 V digital)
67	118	VSSD1	S		Supply voltage for digital (0 V digital)
68	119	VDDAPLL	S		Supply voltage for PLL (1.8 V)
69	122	XOUT	O		Crystal connection 2
70	123	XIN	I		Crystal connection 1
71	129	TCLK	I		Testclock
72	130	VDDP1	S		Supply voltage for digital (3.3 V pad)
73	131	VSSP1	S		Supply voltage for digital (0 V pad)
74	138	656HIN/CLKF20	I/O	Connect to vss and disable clock	Separate H input for 656 / 20.25 clock output
75	139	VDDDACV	S		DAC (V)
76	140	AVOUT	O	Leave open or connect to vss and disable DAC	V output
77	141	VSSDACV	S		DAC (V)
78	142	VDDDACU	S		DAC (U)

Pin No.		Pin Name	Type	Connection (If not used)	Short Description
MQFP 80-pin	MQFP 144-pin				
79	143	AUOUT	O	Leave open or connect to vss and disable DAC	U output
80	144	VSSDACU	S		DAC (U)
	11	VDDP4			Supply voltage for digital (3.3 V)
	12	VSSP4			Supply voltage for digital (0 V)
	36	VSSPDB1			Bulk supply voltage (0 V)
	50	VSSP3			Supply voltage for digital (0 V)
	55	VDDP5			Supply voltage for digital (3.3 V)
	56	VSSP5			Supply voltage for digital (0 V)
	86	VDDPOR			Supply voltage for digital (1.8 V)
	87	VDDP6			Supply voltage for digital (3.3 V)
	88	VSSP6			Supply voltage for digital (0 V)
	120	VSSP7			Supply voltage for digital (0 V)
	121	VDDP7			Supply voltage for digital (3.3 V)
	134	VSSP8			Supply voltage for digital (0 V)
	135	VDDP8			Supply voltage for digital (3.3 V)
	17	(reserved)		Leave open	(Reserved)
	57	(reserved)		Leave open	(Reserved)
	85	GP2		Leave open	General purpose pin 2
	84	GP1		Leave open	General purpose pin 1
	83	GP0		Leave open	General purpose pin 0
	133	(reserved)		Leave open	(Reserved)
	136	(reserved)		Leave open	(Reserved)
	137	(reserved)		Leave open	(Reserved)
	69	(NC)			(Not connected)
	71	(NC)			(Not connected)
	79	(NC)			(Not connected)
	81	(NC)			(Not connected)
	99	(NC)			(Not connected)
	101	(NC)			(Not connected)

Pin No.		Pin Name	Type	Connection (If not used)	Short Description
MQFP 80-pin	MQFP 144-pin				
	103	(NC)			(Not connected)
	105	(NC)			(Not connected)
	54	DROUT0	O	Leave open	Digital out red
	53	DROUT1	O	Leave open	Digital out red
	52	DROUT2	O	Leave open	Digital out red
	48	DROUT3	O	Leave open	Digital out red
	47	DROUT4	O	Leave open	Digital out red
	46	DROUT5	O	Leave open	Digital out red
	45	DROUT6	O	Leave open	Digital out red
	44	DROUT7	O	Leave open	Digital out red
	43	DROUT8	O	Leave open	Digital out red
	25	DGOUT0	O	Leave open	Digital out green/656out0
	24	DGOUT1	O	Leave open	Digital out green/656out1
	23	DGOUT2	O	Leave open	Digital out green/656out2
	22	DGOUT3	O	Leave open	Digital out green/656out3
	21	DGOUT4	O	Leave open	Digital out green/656out4
	9	DGOUT5	O	Leave open	Digital out green/656out5
	8	DGOUT6	O	Leave open	Digital out green/656out6
	7	DGOUT7	O	Leave open	Digital out green/656out7
	6	DGOUT8	O	Leave open	Digital out green
	132	DBOUT0	O	Leave open	Digital out blue
	128	DBOUT1	O	Leave open	Digital out blue
	127	DBOUT2	O	Leave open	Digital out blue
	126	DBOUT3	O	Leave open	Digital out blue
	125	DBOUT4	O	Leave open	Digital out blue
	124	DBOUT5	O	Leave open	Digital out blue
	116	DBOUT6	O	Leave open	Digital out blue
	115	DBOUT7	O	Leave open	Digital out blue
	114	DBOUT8	O	Leave open	Digital out blue
	91	SISCEN	I		Single-scan enable

Pin No.		Pin Name	Type	Connection (If not used)	Short Description
MQFP 80-pin	MQFP 144-pin				
	18	TDO	O	Leave open	Test data out

[1)] This pin is not used and not bonded in VSP 94x2A.
All VDDPx, VSSx and VDDDx must be connected within their group with low resistance.
Analog supplies are internally connected to digital supplies via antiparallel diodes.

4.2.2. Differing Pin Connections and Short Descriptions for VSP 941xB and VSP 944xB

Pin No. MQFP 80-pin	Pin Name	Type	Connection (If not used)	Short Description
1	I656I5	I	Connect to Vdd (3.3V)	656 input
2	I656I6	I	Connect to Vss	656 input
3	I656I7	I		656 input (MSB)
75	I656ICLK	I	Connect to Vdd (3.3V) (or leave open)	656 input clock (27 MHz nom.)
76	I656I0	I	Connect to Vss	656 input (LBS)
77	I656I1	I		656 input
78	I656I2	I	Connect to Vdd (3.3V)	656 input
79	I656I3	I	Connect to Vss	656 input
80	I656I4	I		656 input

4.3. Pin Configurations

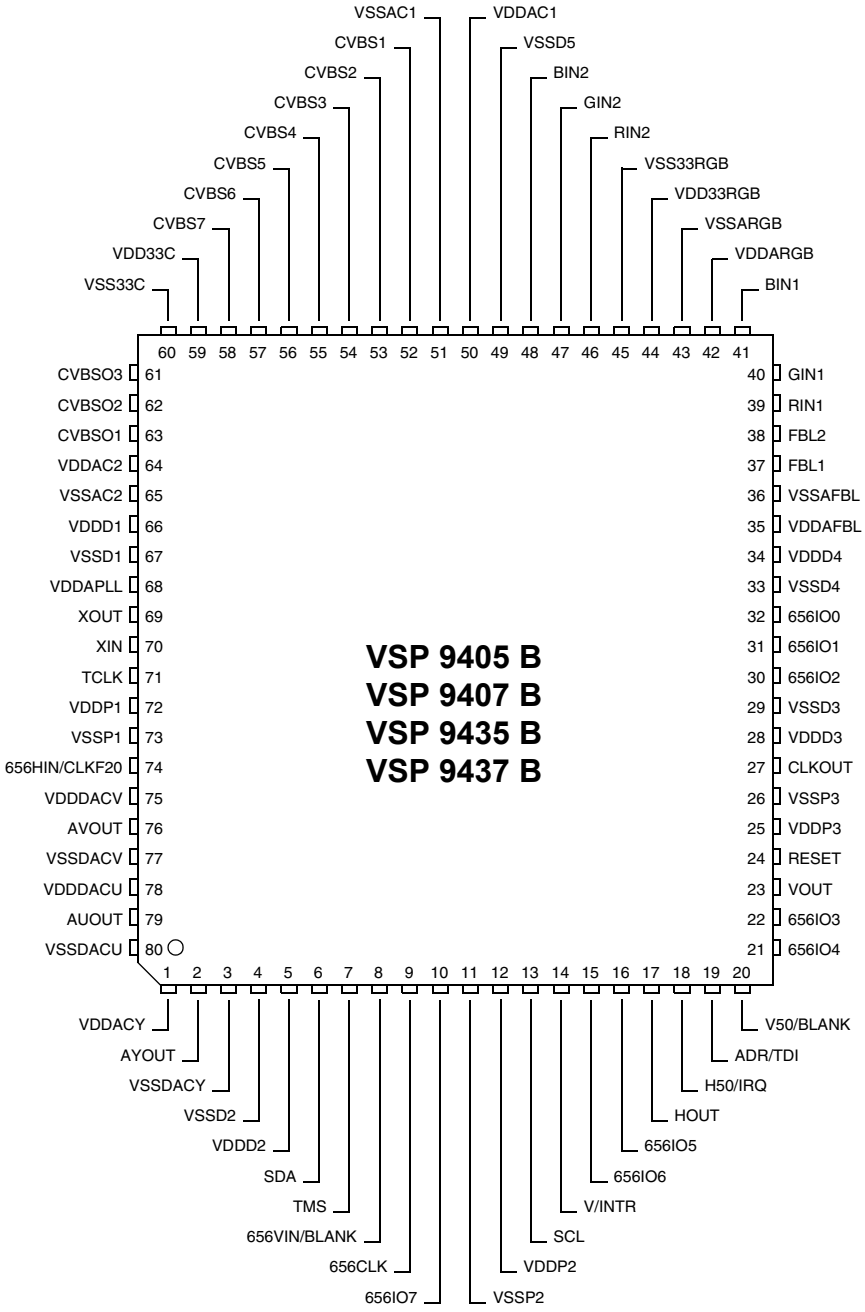


Fig. 4–3: MQFP80 package: 9405/07/35/37 versions

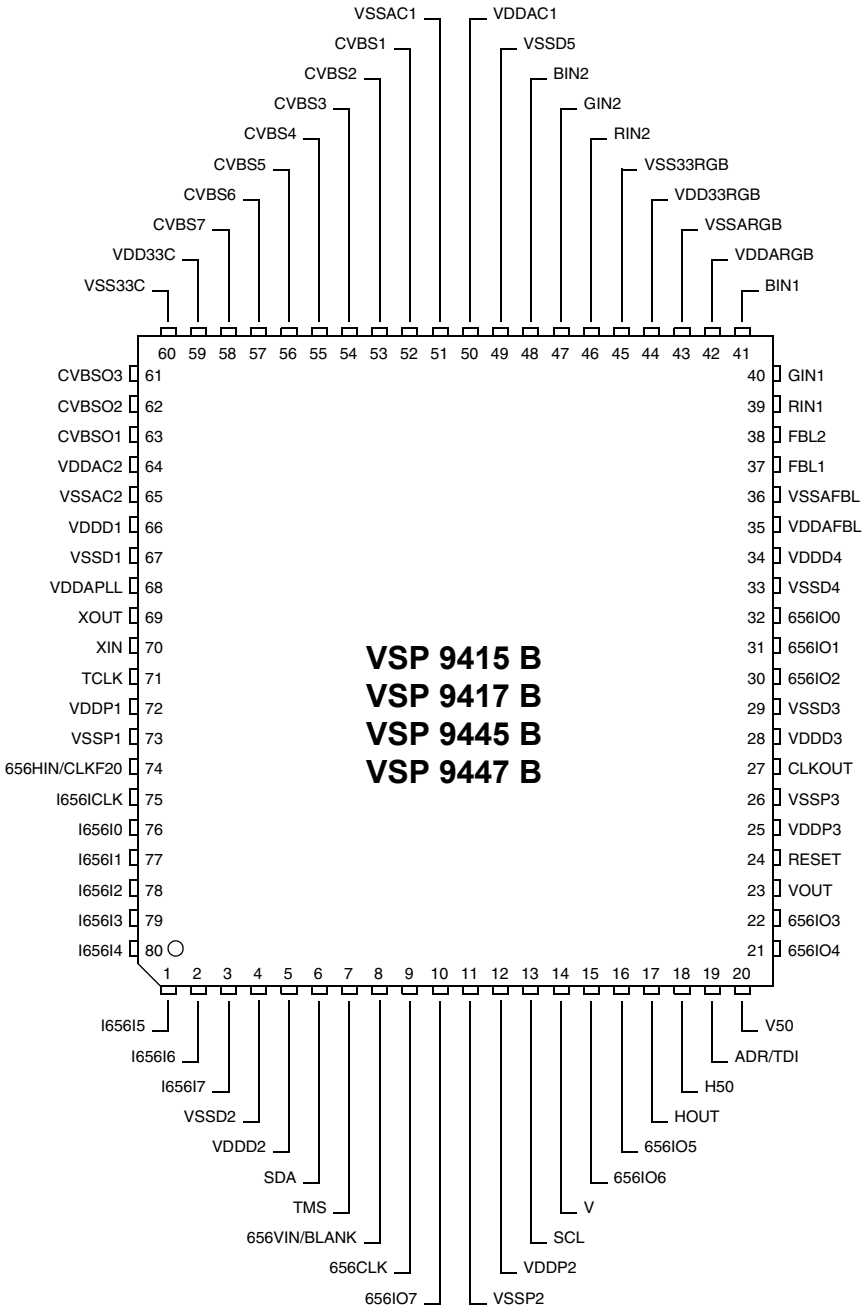


Fig. 4–4: MQFP80 package: 9415/17/45/47 versions

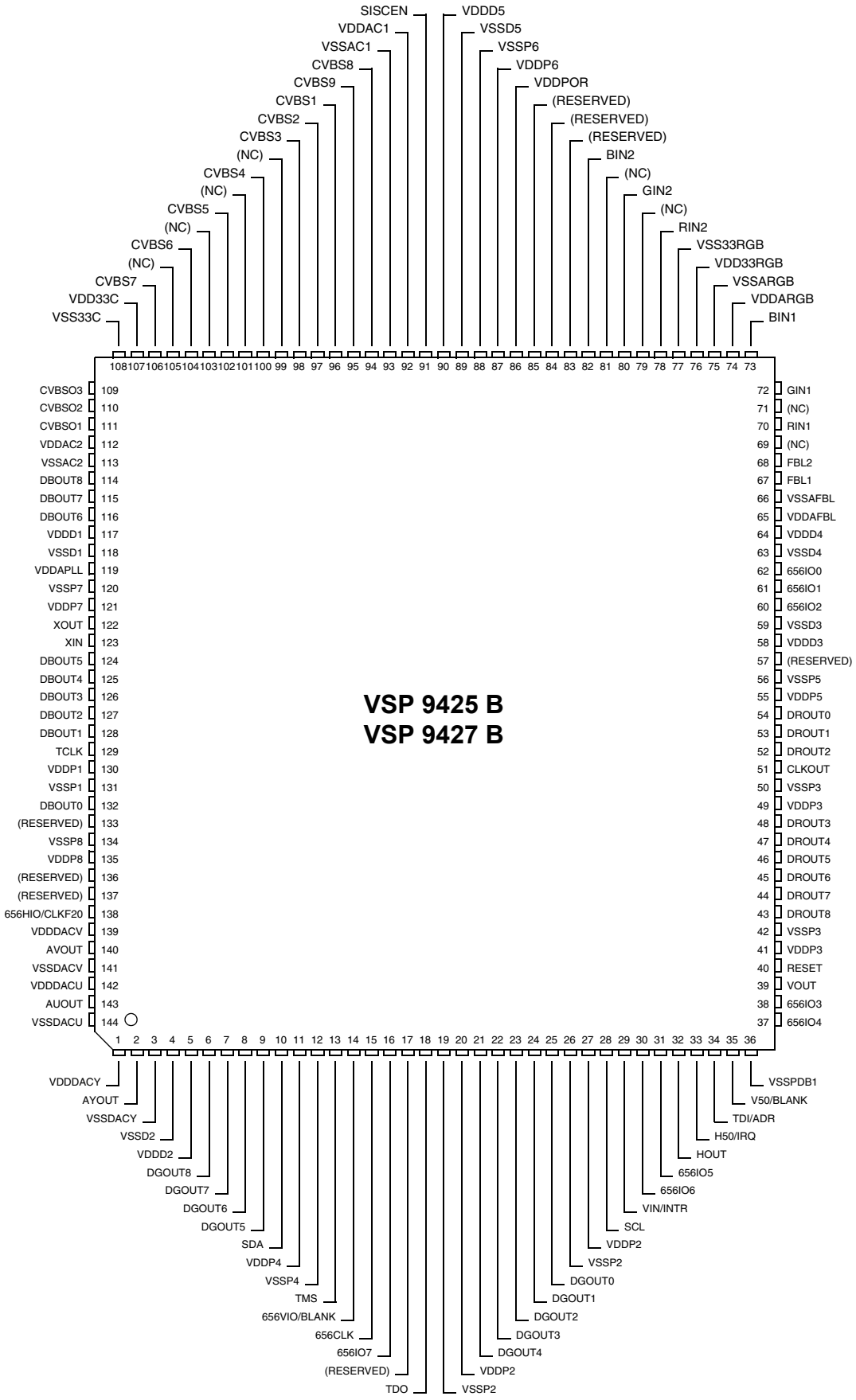


Fig. 4–5: MQFP144 package: 9425 and 9427 versions

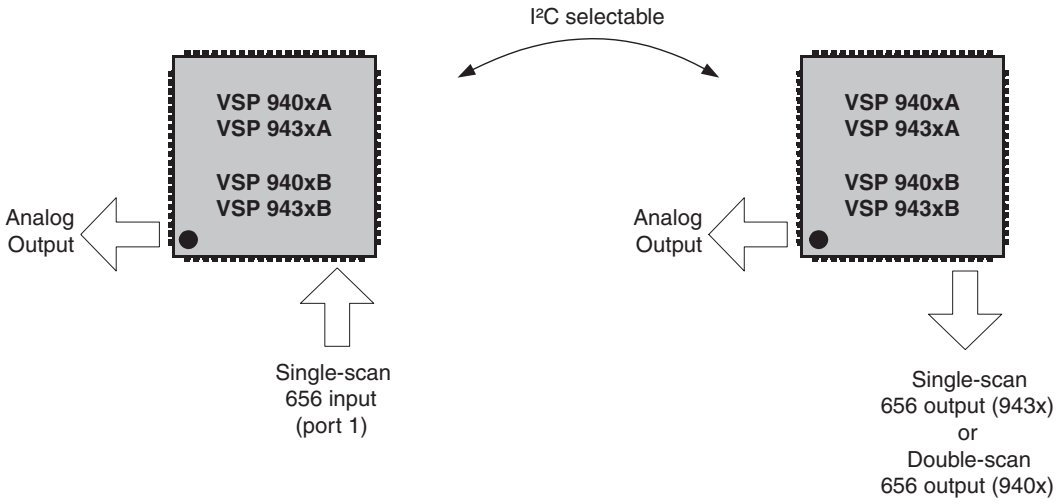


Fig. 4–6: Signal flow 940x, 943x

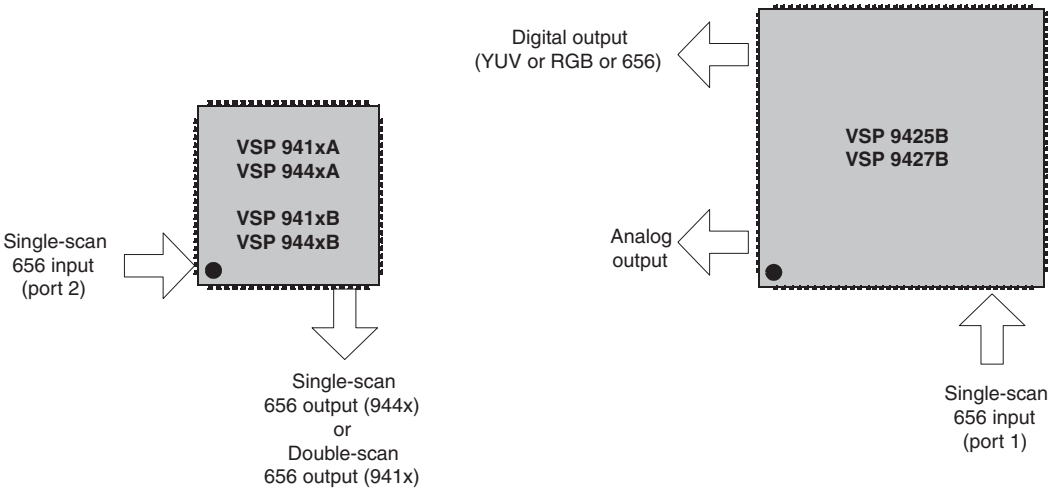


Fig. 4–7: Signal flow 941x, 944x, 942x

4.4. Pin Circuits

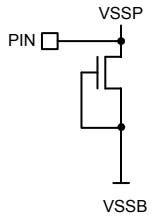


Fig. 4–8: Supply Pins (Ground): **VSSDACY, VSSDACU, VSSDACV, VSS33C, VSS33RGB, VSSP1 ... VSSP8, VSSPDB1**

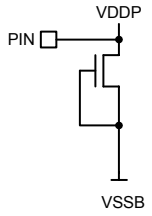


Fig. 4–9: Supply Pins (Power 3.3 V): **VDDDACY, VDDDACU, VDDACV, VDD33C, VDD33RGB, VDDP1 ... VDDP8, VDDPOR**

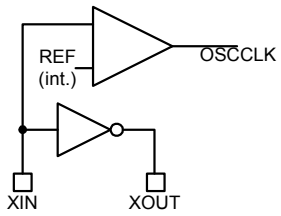


Fig. 4–10: Input/Output Pins (Crystal connection): **XIN, XOUT**

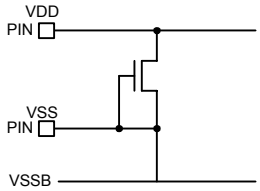


Fig. 4–11: Supply Pins (Power 1.8 V and Ground): **VDDAC1, VSSAC1, VDDAC2, VSSAC2, VDDARGB,VSSARGB, VDDAFBL, VSSAFBL, VDDAPLL, VDDD1, VSSS1, VDDD2, VSSS2, VDDD3, VSSS3, VDDD4, VSSS4, VDDD5, VSSS5**

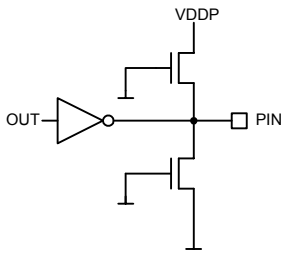


Fig. 4–12: Digital Output Pins: **H50, V50, CLKOUT, HOUT, VOUT, DGOUT0 ... DGOUT8, DROUT0 ... DROUT8, DBOUT0 ... DBOUT8**

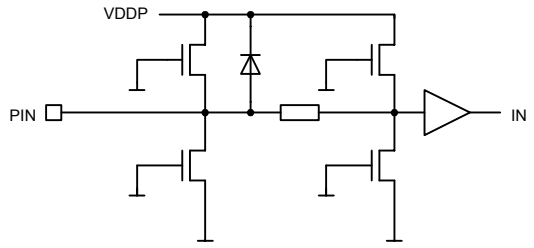


Fig. 4–13: Digital Input Pins: **V, TMS, ADR/TDI, RESET, TCLK**

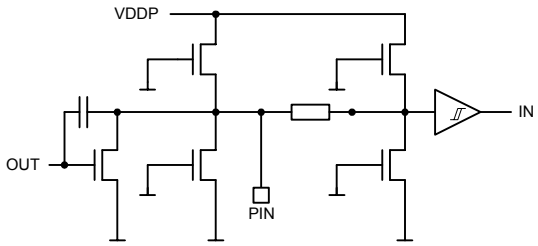


Fig. 4–14: I^2C bus Pins: **SDA, SCL**

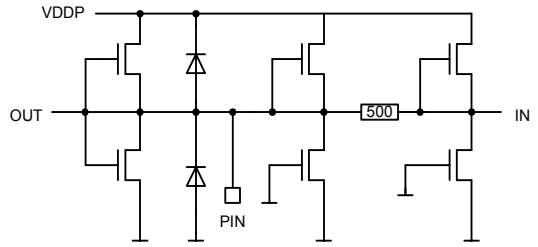


Fig. 4–15: Digital Input/Output Pins: **656IOX,656CLK, 656HIN/CLKF20, 656VIN/BLANK**

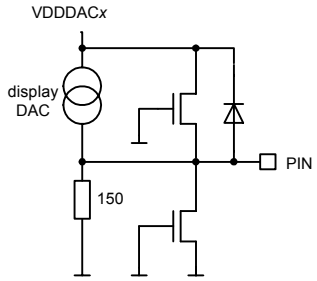


Fig. 4–16: Analog Output Pins: **AYOUT, AUOUT, AVOUT**

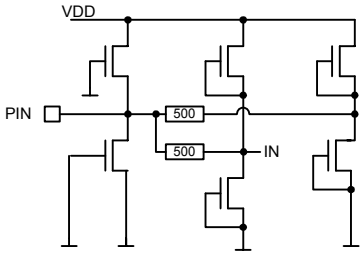


Fig. 4–17: Analog Input Pins: **RIN1, RIN2, GIN1, GIN2, BIN1, BIN2, FBL1, FBL2, CVBS1...CVBS9** (if cvbsx is connected to any ADC)

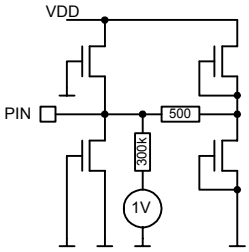


Fig. 4–18: Analog Input Pins: **CVBS1...CVBS9** (if cvbsx is not connected to any ADC)

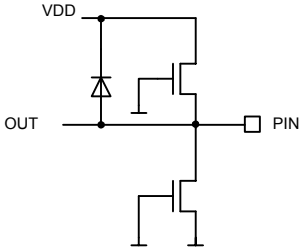


Fig. 4–19: Analog Output Pins: **CVBSO1...CVBSO3**

4.5. Electrical Characteristics

4.5.1. Absolute Maximum Ratings

All voltages listed are referenced to ground (0 V, V_{SS}) except where noted.

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	+70	°C
T_S	Storage Temperature	–	-45	+125	°C
T_C	Case Operating Temperature	–	–	+115	°C
V_I	Input Voltage [1)]	–	-0.3	V_{DD2}+0.3	V
V_O	Output Voltage [2)]	–	-0.3	V_{DD2}+0.3	V
V_{DD1}	Supply Voltages1	–	-0.3	2[4) 5)]	V
V_{DD2}	Supply Voltages2	–	-0.3	3.6[4) 5)]	V
P_{tot80}	Total Power Dissipation QFP80[3)]	–		1.2	W
P_{tot144}	Total Power Dissipation QFP144[3)]	–		1.2	W

[1)] Not valid for V_{DD1} supply pins
[2)] Not valid for V_{DD1} supply pins
[3)] Package limit
[4)] V_{DD2} (3.3V nom.) must always be higher than V_{DD1} (1.8V nom.) - 0.3 (even during power-up)
[5)] The deviation among all V_{DD1} or V_{DD2} supplies may never exceed 0.3 V.

Stresses beyong those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

4.5.2. Recommended Operating Conditions

In the operating conditions, the functions given in the circuit description are fulfilled.

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
T_A	Ambient Operating temperature[1)]	–	0	+25	+70	°C
3.3 V Power Supply						
V_{DDxx}	Supply voltages[2)]	VDDP1, VDDP2, VDDP3, VDDACY, VDDACU, VDDACV, VDD33C, VDD33RGB	3.14	3.3	3.47	V
1.8 V Power Supply						
V_{DDxx}	Supply voltages[2)]	VDDAC1, VDDAC2, VDDARGB, VDDAFBL, VDDAPLL; VDDD1; VDDD2;VDDD3; VDDD4	1.71	1.8	1.89	V
CVBS/RGB Frontend						
$V_{i,CVBS}$	Analog CVBS input voltage	CVBS1, CVBS2, CVBS3, CVBS4, CVBS5, CVBS6, CVBS7, CVBS8, CVBS9, RIN1, RIN2, GIN1, GIN2, BIN1, BIN2, FBL1, FBL2	0.6	1.2	1.8	V
$V_{i,RGB}$	Analog RGB input voltage		0.5	1.2	1.5	V
$V_{i,FBL}$	Analog FBL input voltage		0.5	1.2	1.5	V
	Analog chroma input voltage (burst)		–	0.3	–	V
	Input coupling capacitors CVBS		–	100	–	nF
	Input coupling capacitors RGB/FBL		–	47	–	nF
	Source resistance		–	0.1	–	kΩ
Reset Input						
	Rise time	RESET	0		tbd	µs
t_{RES}	Active time reset (after power-on)		1.3	–	–	µs
t_{RES}	Active time reset (during normal operation, if required)		100	–	–	ns
Digital To Analog Converters						
R_L	Load resistance	AYOUT, AUOUT, AVOUT	10	–	–	kΩ
C_L	Load capacitance		–	–	15	pF

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Crystal Specification						
f_{xtal}	Frequency (fundamental)[3]	XIN, XOUT	20.248	20.25	20.252	MHz
$\Delta f_{max}/f_{xtal}$	Maximum permissible frequency deviation[4]		-100	–	100	ppm
$\Delta f/f_{xtal}$	Recommended permissible frequency deviation[4]		-40	0	40	ppm
C_L	Load capacitance		–	13	–	pF
R_S	Series resistance		–	tbd	25	Ω
C_1	Motional capacitance		20	–	30	fF
C_0	Parallel capacitance		–	7	–	pF
$C_{L,EXT}$	External load capacitance to ground		–	13	–	pF
All Digital Inputs						
$V_{in,L}$	Input voltage low	TMS, ADR/TDI, V, TCLK, RESET, 656VIN/BLANK, 656HIN, 656IO[0...7], 656CLK I656I[0...7], I656ICLK	–	–	0.8	V
$V_{in,H}$	Input voltage high		2.0	–	–	V

1) Favourable PCB design required. Two layer boards recommended.
2) ±5%
3) Values outside this range may cause color decoding failures.
4) after (subcarrier) adjustment // including temperature and aging deviations

4.5.3. Characteristics

Min./Max. values at T_A= 0 to 70 °C, f_{CLOCK} = 20.25 MHz, $V_{SUP3,3\ V}$ = 3.14 to 3.47 V, $V_{SUP1.8\ V}$ = 1.71 to 1.89 V
Typical values at T_A= 25 °C, f_{CLOCK} = 20.25 MHz, $V_{SUP3.3\ V}$ = 3.3 V, $V_{SUP1.8\ V}$ = 1.1.8 V

4.5.3.1. General Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
$I_{DDtot\ 1.8\ V}$	Average total supply current	-	-	-	470	mA	
$I_{DDtot\ 3.3\ V}$	Average total supply current	-	-	65	90	mA	
P_{tot}	Total power dissipation	-	-	0.85	1.2	W	
P_{totPD}	Total power dissipation in power-save-mode	-	-	0.45	tbd	W	STANDBYxx='1'
Digital Inputs							
C_I	Input capacitance	TMS, ADR/ TDI, V, TCLK, RESET, 656VIN/ BLANK, 656HIN/, 656IO[0...7], 656CLK, 656I[0...7], I656ICLK	-	7	-	pF	
	Input leakage current		-1	-	1	µA	Incl. leakage current of SDA output stage Except for current of below specified pullup or pulldown pins.
t_{SI}	set-up-time	656IO[0...7], I656I[0...7]	2.5			ns	wrt. 656clk (rising)
t_{HI}	hold-time		2.5			ns	wrt. 656clk (rising)
f_{clkin}	input clock frequency	656CLK, I656ICLK		27	30	MHz	
t_{WL}	Low time		10			ns	
t_{WH}	High time		10			ns	
t_{LH}	Rise time				1.6	ns	
t_{HL}	Fall time				1.6	ns	
Digital Outputs							
V_{OH}	Output voltage high	CLKOUT, HOUT, VOUT, 656CLK, H50, DBOUT[0..8], DROUT[0..8], DGOUT[0..8], VIN/INT, V50	2.4	-	V_{dd2}	V	@-12mA
V_{OL}	Output voltage low		-	-	0.4	V	@8mA

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
t_{LH}	Rise time	CLKOUT, 656CLK	-	-	1.6	ns	@20pF
		DBOUT[0..8], DROUT[0..8], DGOUT[0..8], HOUT, VOUT,	-	-	2.5	ns	@20pF
		H50, V50, VIN/INT	-	-	6	ns	@20pF
t_{HL}	Fall time	CLKOUT, 656CLK	-	-	1.6	ns	@20pF
		DBOUT[0..8], DROUT[0..8], DGOUT[0..8] HOUT, VOUT,	-	-	2.5	ns	@20pF
		H50, V50, VIN/INT	-	-	4	ns	@20pF
f_{clkout}	Output frequency	CLKOUT	10.125	-	81	MHz	
		656CLK	27	-	60	MHz	
	Duty cycle	CLKOUT 656CLK	40	50	60	%	
t_{HO}	Hold-time	656IO[0...7], 656VIO, 656HIO	3			ns	Referred to 656CLK, CLK656INV=1
			3+ $T_{clk}/2$			ns	Referred to 656CLK, CLK656INV=0
		DBOUT[0..8], DROUT[0..8], DGOUT[0..8], HOUT, VOUT	3			ns	Referred to CLKOUT, CLKOUTINV=1
			3+ $T_{clk}/2$			ns	Referred to CLKOUT, CLKOUTINV=0
t_{DO}	Delay-Time	656IO[0...7], 656VIO, 656HIO	0		3+ $T_{clk}/2$	ns	Referred to 656CLK, CLK656INV=1
					3	ns	Referred to 656CLK, CLK656INV=0
		DBOUT[0..8], DROUT[0..8], DGOUT[0..8] HOUT, VOUT	0		3+ $T_{clk}/2$	ns	Referred to CLKOUT, CLKOUTINV=1
					3	ns	Referred to CLKOUT, CLKOUTINV=0
I_{PD}	Pulldown-current (@Vdd)	I656ICLK, 656CLK	-59.5	-122	-235	µA	Pulldown always active
		656VIO/ BLANK, VIN/ INT, ADR/ TDI, TCLK, 656HIO	-11.7	-25.8	-55.5	µA	Pulldown always active

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
I_{PU}	Pullup-current (@Vss)	TMS, SIS-CEN	12.4	21.4	36.4	µA	Pullup always active
Analog CVBS Front-end (2 x 9 bit ADC)							
	Input leakage current	CVBS1, CVBS2, CVBS3, CVBS4, CVBS5, CVBS6, CVBS7, CVBS8, CVBS9	-100	-	100	nA	Clamping inactive
C_I	Input capacitance		-	7	-	pF	
	Input clamping error		-1	-	1	LSB	Settled state
CT	Crosstalk between CVBS inputs		-50	-	-	dB	f_{sig}<5 MHz
BW	Bandwidth		7	-	-	MHz	-3 dB
A_{cvbso}	CVBS output amplification	CVBSO1, CVBSO2, CVBSO3	0.9	-	1.1		
Analog RGBF Front-end (4 x 8 bit ADC)							
	Input leakage current	RIN1, RIN2, BIN1, BIN2, GIN1, GIN2, FBL1, FBL2	-100	-	100	nA	Clamping inactive
C_I	CVBS input capacitance		-	7	-	pF	
	Input clamping error		-1	-	1	LSB	Settled state
CT	Crosstalk between RGB inputs		-50	-	-	dB	
BW	Bandwidth		10	-	-	MHz	-3 dB
Digital To Analog Converters (3 x 9 bit DAC)							
U_{OL}	Full range output voltage		-	0.4	-	V	Nominal conditions PKLY/U/V=min
U_{OH}	Full range output voltage		-	1.9	-	V	Nominal conditions PKLY/U/V=max
	Output matching		-3	-	3	%	
Color Decoder/Synchronization and Luminance Processing							
Δf_{Hf}	Horizontal PLL pull-in-range	–	-	±4.9	-	%	Based on 15625 kHz
	ACC range	–	-30	-	+6	dB	
	AGC range	–	-7.5	-	+2	dB	
Δf_{SC}	Chroma PLL pull-in-range	–	-	±500	-	Hz	Nominal crystal frequency

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

4.5.3.2. I²C Bus Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Fast I^2C Bus (All Values are Referred to Min(V_{IH}) and Max(V_{IL}))							
C_b	Capacitive load/bus line	SDA/SCL			400	pF	
t_R, t_F	SDA/SCL rise/fall times		20+$		300	ns	$=0.1 C_b/pF
t_{BUF}	Inactive time before start of transmission		1300			ns	
f_{SCL}	I^2C clock frequency	SCL	0		400	kHz	
t_{LOW}	SCL low time		1300			ns	
t_{HIGH}	SCL high time		600			ns	
$t_{SU;STA}$	Set-up time start condition	SDA	600			ns	
$t_{HD;STA}$	Hold time start condition		600			ns	
$t_{SU;DAT}$	Set-up time DATA		100			ns	
$t_{HD;DAT}$	Hold time DATA		0		900	ns	
$t_{SU;STO}$	Set-up time stop condition		600			ns	
I^2C Bus pins							
V_{IHr}	Threshold rise	SDA, SCL		2.08		V	
V_{IL}	Threshold fall			1.8		V	

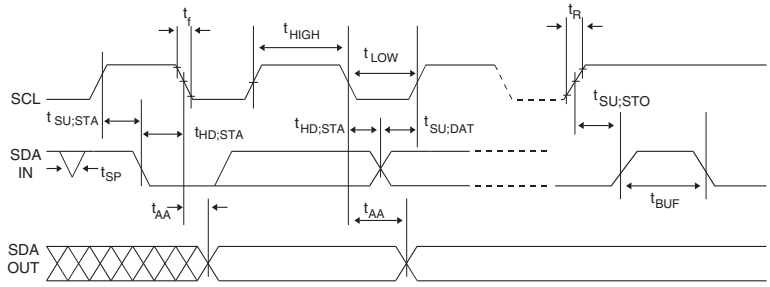


Fig. 4–20: I²C bus timing data

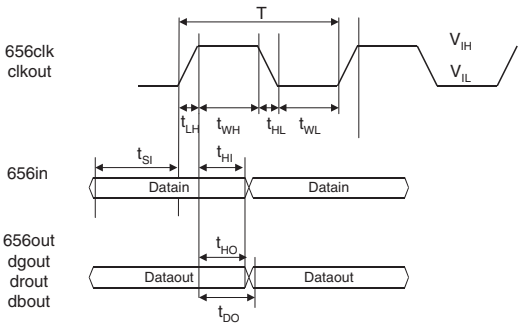


Fig. 4–21: Timing diagram clock

5. Application Circuit

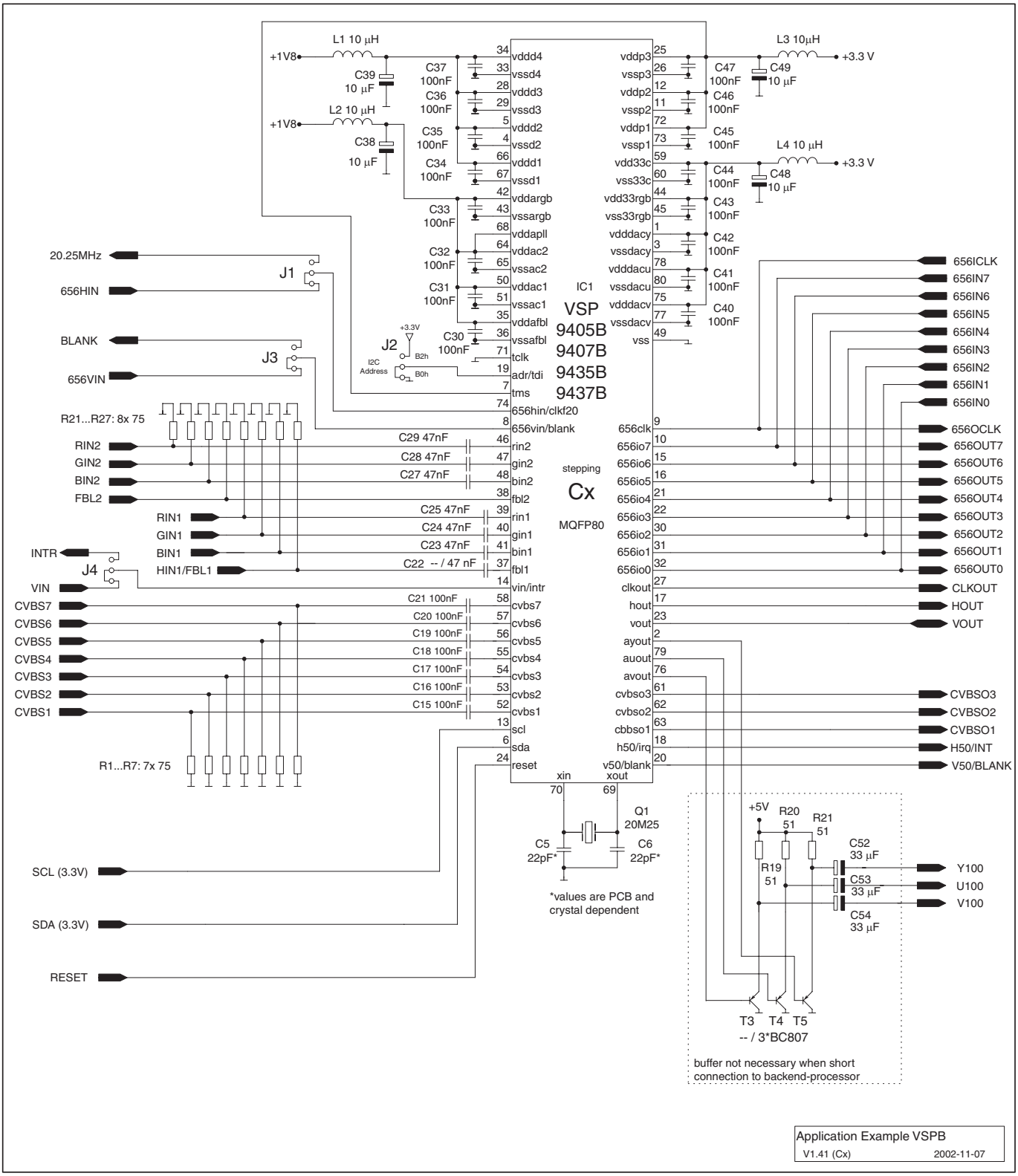


Fig. 5–1: Application Example for 940xB and 943xB

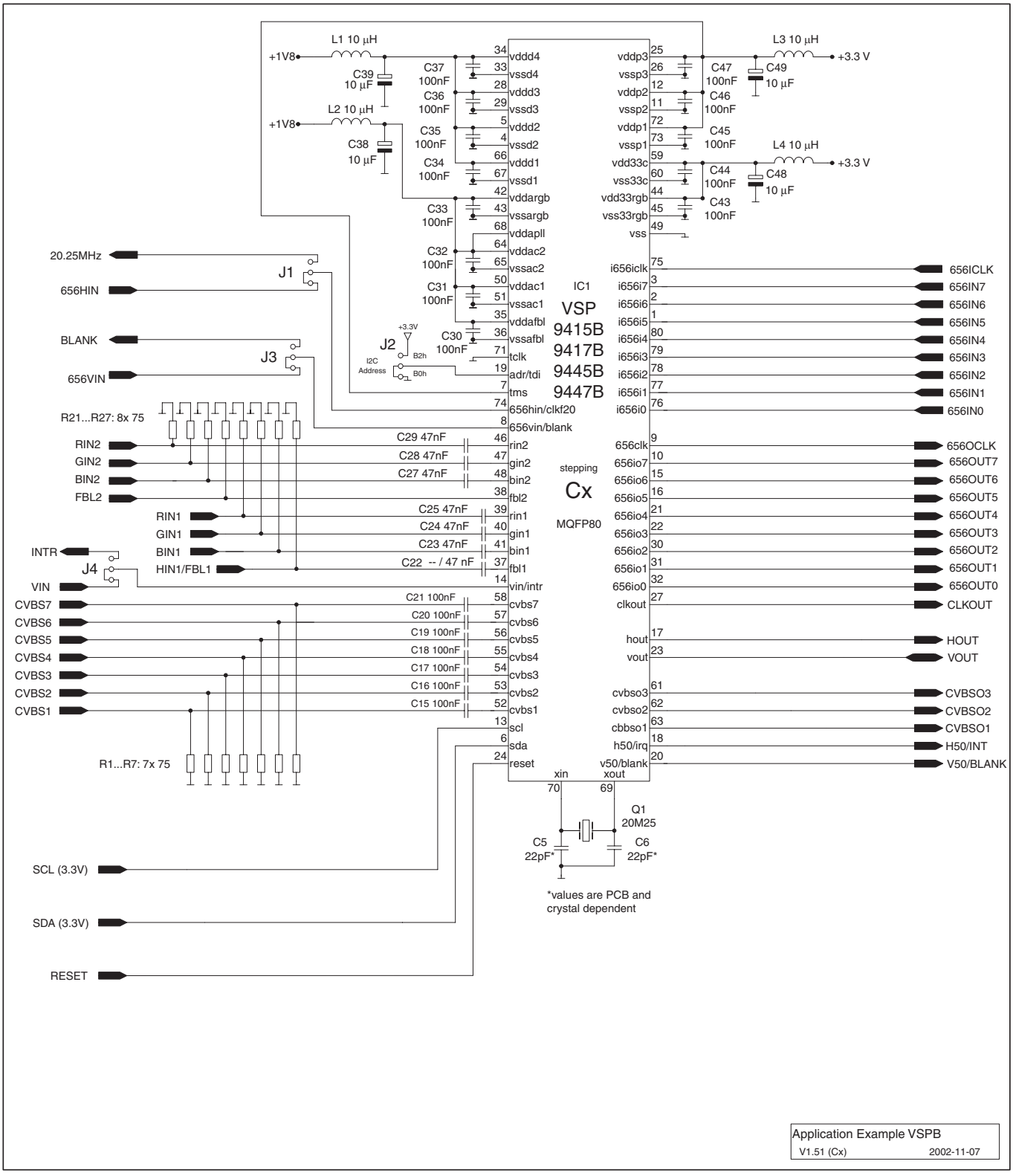


Fig. 5–2: Application Example for 941xB and 944xB

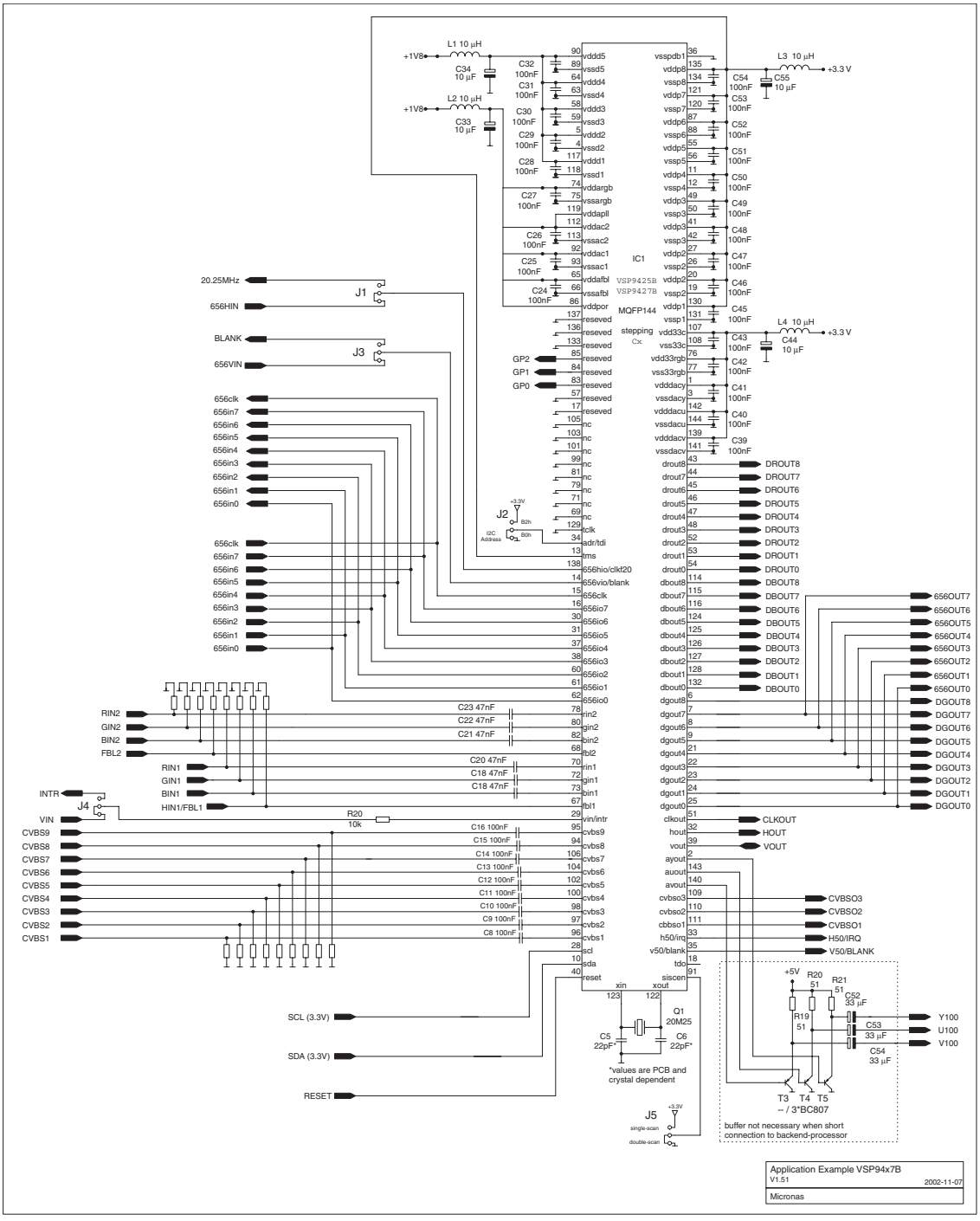


Fig. 5–3: Application Example for 9425B and 9427B

5.1. Application Overview

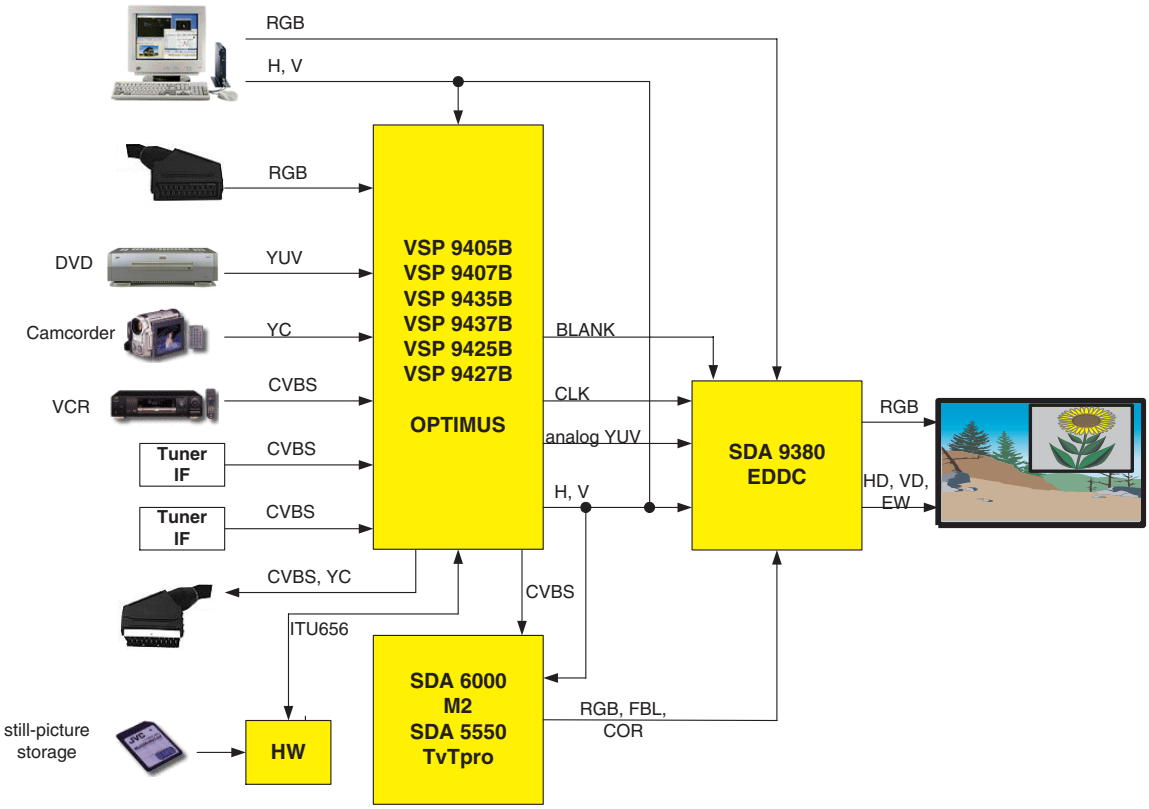


Fig. 5–4: Application overview with analog outputs of VSP 940xB

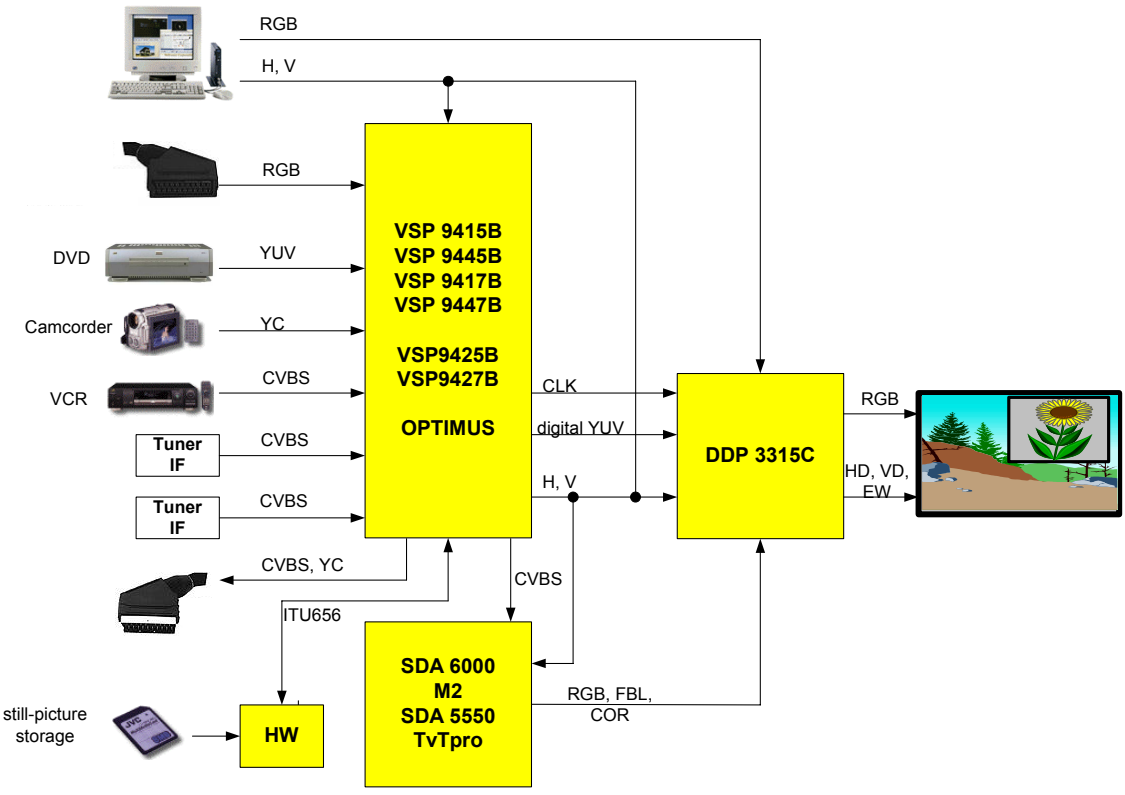


Fig. 5–5: Application overview with digital outputs of VSP 941xB, (VSP 942xB)

6. Data Sheet History

1. Preliminary Data Sheet: “VSP 94x5B, VSP 94x7B OPTIMUS ”, Jan. 18, 2002, 6251-576-1PD . First release of the preliminary data sheet.

2. Preliminary Data Sheet: “VSP 94x5B, VSP 94x7B OPTIMUS”, Oct. 21, 2002, 6251-576-2PD. Second release of the preliminary data sheet.
   Major changes: New revision, complete updated.

3. Preliminary Data Sheet: “VSP 94x5B, VSP 94x7B OPTIMUS”, Nov. 28, 2002, 6251-576-3PD. Third release of the preliminary data sheet.
   Major changes:

– Following sections were revised and updated:
  2.3.15. Digital Prefiltering
  2.3.19. Fast Blank Activity and Overflow Detection
  2.7. Clock Concept
  3.7. I²C Bus Registers
  3.12. I²C Bus Command Table

Micronas GmbH
Hans-Bunte-Strasse 19
D-79108 Freiburg (Germany)
P.O. Box 840
D-79008 Freiburg (Germany)
Tel. +49-761-517-0
Fax +49-761-517-2174
E-mail: docservice@micronas.com
Internet: www.micronas.com

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