VOLTERRA

REVISION - December 30, 2004

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

Smart Slave™	Input Voltage	Output Voltage	Current Rating	VID
VT1105S	7V to 13.2V	0.600V to 1.600V	25A per Phase	VRs 10.X, 11 & Opteron™
VT1125S				

GENERAL DESCRIPTION

Volterra's fourth-generation chipset is a complete, integrated, scalable architecture for the highest density multiphase synchronous buck regulators. This ultra high density solution minimizes external components and offers enhanced regulator performance, comprehensive control and reporting features, ease of design and the smallest footprint available for demanding multiphase synchronous buck converters. The chipset is targeted for applications such as servers and networking systems.

The VT1115M master is part of the Volterra Generation 4 architecture as shown in Figure 1. Each VT1115M drives and controls multiple Generation 4 Smart Slave™ integrated output devices, such as the VT1105S and VT1125S. The number of Generation 4 Smart Slaves™ can be set by design, according to the application requirements. The desired slave and load operating conditions are controlled by a desired current command issued from the VT1115M to the slave devices. Configuration and monitoring of the VR conditions are controlled via an interconnecting bus between the master and the slaves as shown in Figure 1.

The VT1115M supports the following voltage regulator specifications: Intel® VR 10 and extended VR 10, AMD Opteron™ and Intel® VR 11.

The architecture incorporates a SMBus interface for monitoring and control of the voltage regulator. Regulator parameters can be set and monitored via the two-way SMBus for control, protection and shutdown of the regulator. The SMBus can provide a reading of faults such as VX short-circuit or slave over-temperature, so that the regulator can be controlled and protected during all operating conditions. The SMBus can also provide temperature readings of individual slaves.

A key benefit of the architecture is that it provides excellent scalability by increasing the number of slaves per system. This flexibility allows the designer to trade-off cost and performance for a given application using one VT1115M controller and different slave configurations with no redesign or re-layout. The number of phases and output current requirement can be determined by the designer and easily populated or depopulated to meet different load and performance targets.

Output voltage, switching frequency, current per slave, setpoint, droop, over- and undervoltage protection levels and many other voltage regulator parameters are all programmed easily on the VT1115M controller and communicated to the slaves via a bus between master and slaves.

KEY FEATURES

- **Smallest Footprint: Typical Solution Occupies Less than 1600mm^2 in a 150A VRM Application**
- **Lowest Profile: 5mm Maximum Height**
- **Highest Accuracy Current Sharing**
- **Up to 25A/Phase Output – Programmable**
- **Differential Voltage Sense at Point of Load**
- **Scalable Output Current: Up to 8 Slaves**
- **SMBus Interface**
- **Output Status Reporting and Shutdown**
- **Slave Temperature Reporting**
- **Factory Set Presets for High Performance Design**
- **Switching Frequency: 500kHz-1.5MHz**
- **8-Bit VID Input, with 6.25mV Steps and Setpoint Trim for Programmable V_{OUT}**
  - **Intel® VR 10.X: 0.83125V-1.60V**
  - **Intel® Extended (7-Bit) VR 10.X**
  - **Intel® VR 11: 0.6V-1.60V**
  - **AMD Opteron™: 0.80V-1.55V**
- **Dynamic VID**
- **Programmable Setpoint and Droop**
- **Programmable VR_HOT and VR_FAN Functions**
- **Programmable OVP, OVLO and UVLO**
- **Cycle-by-Cycle Current Limiting**
- **Power Good, OVP, Fault Flags and Output Enable**
- **Redundant Inputs for Power Good and OVP**

SYSTEMS

- **Servers and Workstations**
- **Enterprise Storage**
- **Broadband Communication**
- **Networking**
- **Small Form Factor Desktops**

APPLICATIONS

Voltage Regulator Modules (VRMs) and On-Board Regulators (VR Down)

- **Microprocessors (µP): 32 and 64 Bit I/A and RISC Architectures**
- **Memory**
- **Graphics Processors**
- **Network, Chipset ICs**

TYPICAL APPLICATION CIRCUIT

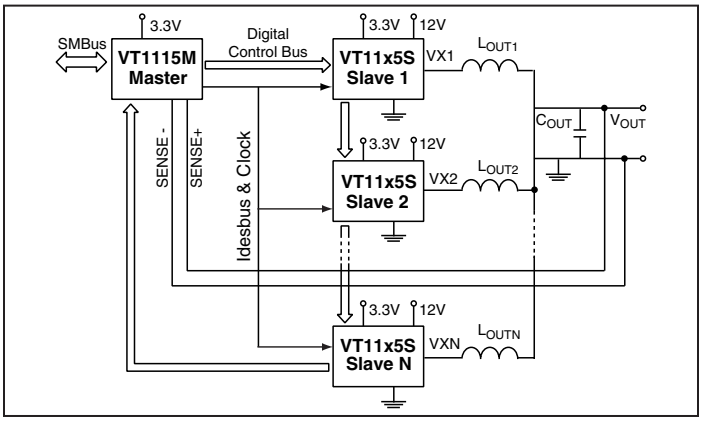


Figure 1. VT1115M System Architecture

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

ORDERING INFORMATION

Part Number	IC	Package Style	Drawing Number	Shipment Method	Package Marking
VT1115MP	Master	TSSOP-48	ES AP-0691	Tubes	VT1115M
VT1115MPX				2.5ku Tape & Reel	
VT1105SCR	24A Smart Slave™	CSP-52	ES AP-0588	250u Tape & Reel	VT1105S
VT1105SCX				2.5ku Tape & Reel	
VT1125SCR	25A Smart Slave™	CSP-69	ES AP-0760	250u Tape & Reel	VT1125S
VT1125SCX				2.5ku Tape & Reel	
Lead-Free Options (RoHS Compliant)					
VT1115MFP	Master	TSSOP-48	ES AP-0691	Tubes	VT1115MF
VT1115MFPX				2.5ku Tape & Reel	
VT1105SFCR	24A Smart Slave™	CSP-52	ES AP-0588	250u Tape & Reel	VT1105SF
VT1105SFCX				2.5ku Tape & Reel	
VT1125SFCR	25A Smart Slave™	CSP-69	ES AP-0760	250u Tape & Reel	VT1125SF
VT1125SFCX				2.5ku Tape & Reel	

ABSOLUTE MAXIMUM RATINGS (SEE NOTE 1)

Supply Voltage (12V) ..... -0.3V to 16V
Supply & Input Pin Voltages (3.3V) ..... -0.3V to 4V
Junction Temperature (T_J) ..... 150°C
Storage Temperature Range ..... -65° to 150°C
Peak Reflow Temperature (30 - 90 sec) ..... 240°C

OPERATING RATINGS

Input 3.3V Voltages (Master &Slave) ..... 2.97V to 3.63V
Slave 12V Supply ..... 7.0V to 13.2V
Junction Temperature (T_J) Master & Slave ..... 0° to 125°C
Frequency (Fsw) ..... 500kHz to 1.5MHz
Slave DC Output Current (VT1105S) 25A
Slave DC Output Current (VT1125S) 25A
Peak Instantaneous Slave Current (VT1105S) 48A
Peak Instantaneous Slave Current (VT1125S) 48A

THERMAL RATINGS

Θ_{JC} Max (TSSOP-48) ..... 30°C/W
Θ_{JC} Max (CSP-52) ..... 0.5°C/W
Θ_{JA} Typ (CSP-52) ..... 30°C/W
Θ_{JC} Max (CSP-69) ..... 0.3°C/W
Θ_{JA} Typ (CSP-69) ..... 28°C/W

NOTE 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

ELECTRICAL CHARACTERISTICS

V_{DD-M} = $V_{DD-S3.3v}$ = 3.3V ±10%, $V_{DD-S12v}$ = 10.8V to 13.2V unless otherwise specified. The ∗ symbol denotes specifications which apply over the full operating junction temperature range ($T_{J-SLAVE}$ = 0 to 125°C and $T_{J-MASTER}$ = 0 to 125°C), otherwise specifications are for T_J = 25°C. The # denotes parameters that are programmable.

Symbol	Parameter	Conditions			Min	Typ	Max	Units
Supply Voltages, V_{DD}								
V_{DD-M}	Supply Voltage Range			∗	2.97	3.3	3.63	V
$V_{DD-S3.3V}$	Supply Voltage Range (Slave 3.3V)			∗	2.97	3.3	3.63	V
$V_{DD-S12V}$	Supply Voltage Range (Slave 12V)			∗	7.0	12.0	13.2	V
I_{DD-M}	Supply Current (Master)	PWM				15		mA
		Shutdown, OE = 0				13		mA
$I_{DD-S3.3V}$	Supply Current (Slave 3.3V)	VT1105S	PWM			45		mA
			Shutdown			20		mA
		VT1125S	PWM			55		mA
			Shutdown			20		mA
$I_{DD-S12V}$	Quiescent Supply Current (Slave 12V)	VT1105S				1		mA
		VT1125S				1		mA
Output Voltage and DC Accuracy								
V_{OUT}	Output Voltage Range	VR 10.X VID Code		∗	0.838		1.60	V
		VR 11 VID Code		∗	0.600		1.60	V
		Opteron™ VID Code		∗	0.8		1.55	V
	DC Setpoint Accuracy	VID = 1.0V to 1.6V			-0.5	0	0.5	%
		0.8V < VID < 1.0V			-5	0	+5	mV
		VID < 0.8V			-8	0	+8	mV
Regulation and System Specifications (Specified by design, tested using circuit in Figure 20)								
ΔV_{OUT}	Line Regulation						4	mV
	Output Ripple					15		mV
SR_{OUT}	Output Slew Rate					1000		A/µs
$T_{SETTLE(LOAD)}$	Load Transient Settling Time					40		µs
$T_{TURN-ON}$	Turn-On Response Time. Time to V_{OUT} > 95% of Final Value	From V_{IN} > UVLO (With OE = High)			0.05		8.6	ms
		From OE Positive Edge (V_{IN} = 12V, V_{CC} = 3.3V)			0.05		1.6	ms
$V_{OVERSHOOT}$	Turn-On Overshoot	Built in Soft Start				0		%
$CMRR_{SENSE}$	Common-Mode Rejection Ratio of Differential Sense					45		dB
Eff	Efficiency (Measured at Inductor), 8 Phases	VT1105S	VID = 1.4V, V_{OUT} = 1.197V, I_{OUT} = 160A			84		%
			VID = 1.4V, V_{OUT} = 1.233V, I_{OUT} = 130A			86		%
	Efficiency (Measured at Inductor), 8 Phases	VT1125S	VID = 1.4V, V_{OUT} = 1.197V, I_{OUT} = 160A			86		%
			VID = 1.4V, V_{OUT} = 1.233V, I_{OUT} = 130A			88		%

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

ELECTRICAL CHARACTERISTICS (CONTINUED)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Slave Scalability and Peak Current Limit							
N_{SLAVE}	Maximum total number of slaves	See Note 2. (Fan-out limitation/ buffering.)				8	
I_{LIM-SL}	Peak Current Limit Per Slave	VT1105S		-47		48	A
		VT1125S				48	A
$I_{MAX-SL(DC)}$	DC Maximum Output Current Per Slave	VT1105S	#			25	A
		VT1125S	#			25	A
-	Slave DC Current Accuracy	VT1105S, VT1125S	*		5	7	%
Data (SD) and Clock (SC) Pins (SMBus High Power Specification Version 2.0)							
V_{IL}	Input Low Voltage					0.8	V
V_{IH}	Input High Voltage			2.1			V
V_{OL}	Output Low Voltage (SD)	@ I_{SINK}				0.4	V
I_{SINK}	Current Sinking (SD)	V_{OL} = 0.4V		2.5			mA
MASTER DIGITAL CONTROL AND STATUS PINS							
Output Enable (OE) Logic Levels							
V_{IH}	OE Turn-On Threshold	VID_SEL = VR 10				0.8	V
V_{IL}	OE Turn-Off Threshold	VID_SEL = VR 10		0.4			V
V_{IH}	OE Turn-On Threshold	VID_SEL = VR 11		0.8	0.85	0.9	V
V_{IL}	OE Turn-Off Threshold Below Turn-On	VID_SEL = VR 11		75	100	125	mV
V_{IH}	OE Turn-On Threshold	VID_SEL = Opteron™				2.0	V
V_{IL}	OE Turn-Off Threshold	VID_SEL = Opteron™		0.7			V
-	OE Timing Hysteresis			0.8	1	1.2	µs
VID Logic Levels							
V_{IH}	VID Turn-On Threshold	VID_SEL = VR 10, VR 11				0.8	V
V_{IL}	VID Turn-Off Threshold	VID_SEL = VR 10		0.4			V
V_{IL}	VID Turn-Off Threshold	VID_SEL = VR11		0.3			V
V_{IH}	VID Turn-On Threshold	VID_SEL = Opteron™				2.0	V
V_{IL}	VID Turn-Off Threshold	VID_SEL = Opteron™		0.8			V
Master FAULTB							
V_{OL}	Output Low Voltage	With 10kΩ external pull-up				0.4	V
I_{SINK}	Current Sink Capability	V_{OL} = 0.4V		4			mA
PWRGD							
-	Lower Threshold Error			-10		+10	mV
-	Upper Threshold Error			-26		+26	mV
-	Delay from V_{OUT} to PWRGD			8		20	µs
-	PWRGD Lockout after DAC Enabled (OE High, UVLO & OVLO Low)			1.6	2.0	2.4	ms
-	External Pull Up Voltage					5.5	V
I_{SINK}	Current Sink Capability	V_{OL} = 0.4V		4			mA

NOTE 2: The number of slaves is only limited by the drive capability of the buffer on the master. If applications require more slaves, additional buffers can be added to the IDES_P, IDES_N and SPHASE signals.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

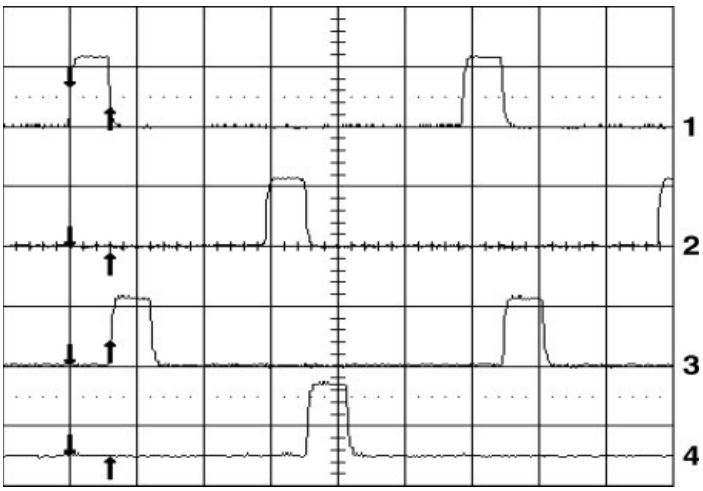
ELECTRICAL CHARACTERISTICS (CONTINUED)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Undervoltage and Overvoltage Lockout 12V Supply							
IN_UVLO_{RE}	12V UVLO Reference Voltage Rising Edge			1.80		1.90	V
IN_UVLO_{FE}	12V UVLO Reference Voltage Falling Edge			1.21		1.31	V
IN_OVLO_{RE}	12V OVLO Reference Voltage Rising Edge			1.80		1.90	V
IN_OVLO_{FE}	12V OVLO Reference Voltage Falling Edge			1.21		1.31	V
$t_{UVLO-RE}$, $t_{OVLO-RE}$,	12V UVLO and OVLO Rising-Edge Response Time	Includes time to shut down the slave			7.25		µs
$t_{UVLO-FE}$, $t_{OVLO-FE}$,	12V UVLO and OVLO Falling-Edge Response Time	Not including soft-start delay			7.25		µs
Undervoltage Lockout 3.3V Supply (Master-Internal)							
3_3V_UVLO	3.3V Internal UVLO	Rising threshold		2.78		2.85	V
		Falling threshold		2.69		2.75	V
$3\_3V\_UVLO_{HYSTERESIS}$	Hysteresis			91	97	103	mV
VR 11 Start-Up Timing (See Figure 18)							
TD1	OE and UVLO to V_{CORE} Starting to Ramp Delay	After V_{CC}/V_{DDH} valid, OE goes high and VR configuration done		1		5	ms
TD2	V_{CORE} Slew Rate to V_{BOOT} = 1.1V	Minimum must be set to comply with VR specifications		0.05		5	ms
TD3	Time to Wait to Read VID Code			50		3000	µs
TD4	Time to Regulate VID Code	Minimum must be set to comply with VR specifications		0	250	2500	µs
TD5	Time Until VR Ready (Power Good)			50		3000	µs
Second Level Redundancy (EXT_REF Pin)							
V_{EXT_REF}	EXT_REF Threshold			-3		+3	% V_{NOM}
t_{EXT_REF}	Fault Response Time					10	µs
OVP							
-	DC Threshold Error			-40		+40	mV
-	Delay with V_{OUT} 100mV Above Threshold				0.5	1.0	µs
-	OVP Lockout after DAC Enabled (OE High, UVLO & OVLO Low)			1.6	2.0	2.4	ms
OCP							
-	Threshold Error at I_{MAX}			-10		+10	% of I_{MAX}
-	Time-Out, PPM & CCM			4	5	6	ms
-	PPM Duty Cycle				10		%
Slave FAULTB Ball (VT1125S)							
$V_{OL-FAULTB}$	FAULTB Output Low Voltage	With 4.7kΩ external pull-up			0.1	0.4	V
$R_{PULLDOWN-FAULTB}$	FAULTB Pull-Down Resistance				50	200	Ω

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

TYPICAL OPERATING CHARACTERISTICS

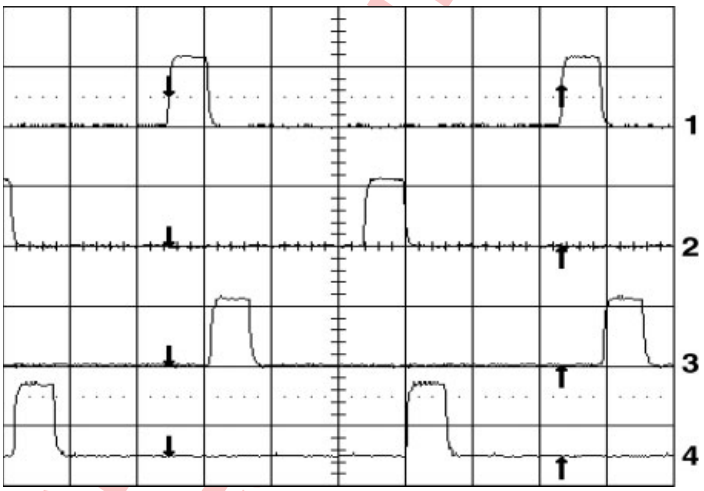
Figure 2. Output Switching Nodes - Eight Slaves Switching Out-of-Phase (Slaves 1-4)



Time/Div: 200ns

Conditions: V_{OUT} = 1.2V, No Load
1: Vx Switching Node for Slave #1 (10V/div)
2: Vx Switching Node for Slave #2 (10V/div)
3: Vx Switching Node for Slave #3 (10V/div)
4: Vx Switching Node for Slave #4 (10V/div)

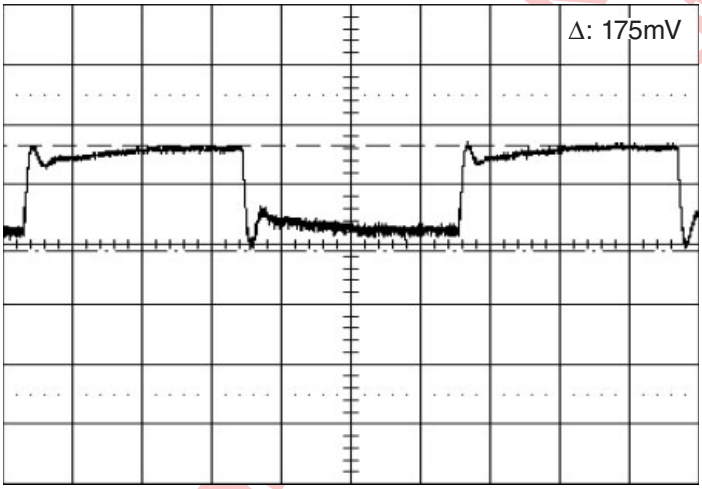
Figure 3. Output Switching Nodes - Eight Slaves Switching Out-of-Phase (Slaves 5-8)



Time/Div: 200ns

Conditions: V_{OUT} = 1.2V, No Load
1: Vx Switching Node for Slave #5 (10V/div)
2: Vx Switching Node for Slave #6 (10V/div)
3: Vx Switching Node for Slave #7 (10V/div)
4: Vx Switching Node for Slave #8 (10V/div)
(Triggered From Slave #1)

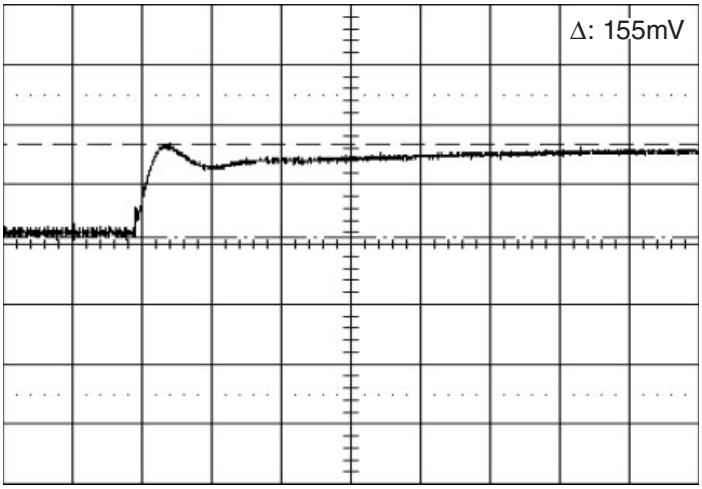
Figure 4. Load Transient Response - 6 Slave VT1105S System



Time/Div: 20µs

Conditions: V_{OUT} = 1.2V
I_{OUT} = 100A-0A Load Step
Slew Rate > 1000A/µs
C_{OUT} = 58 x 22µF
1: Output Voltage (100mV/div)

Figure 5. Output Voltage Overshoot - 6 Slave VT1105S System



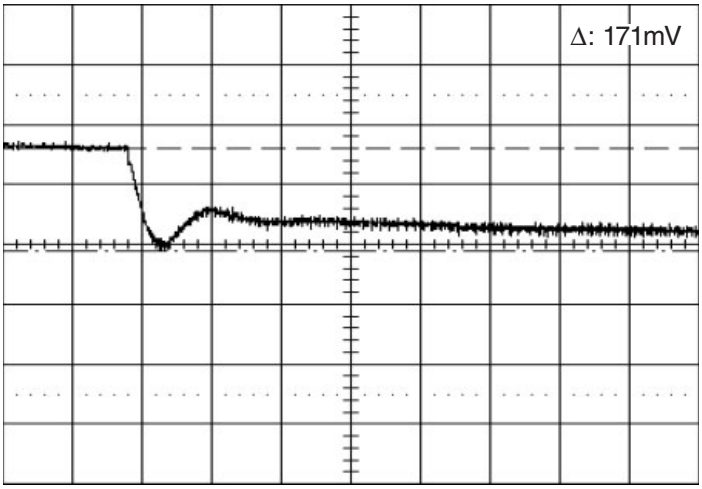
Time/Div: 5µs

Conditions: V_{OUT} = 1.2V
I_{OUT} = 100A-0A Load Step
Loadline = 1.25mΩ
C_{OUT} = 58 x 22µF
1: Output Voltage (100mV/div)

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

TYPICAL OPERATING CHARACTERISTICS (CONTINUED)

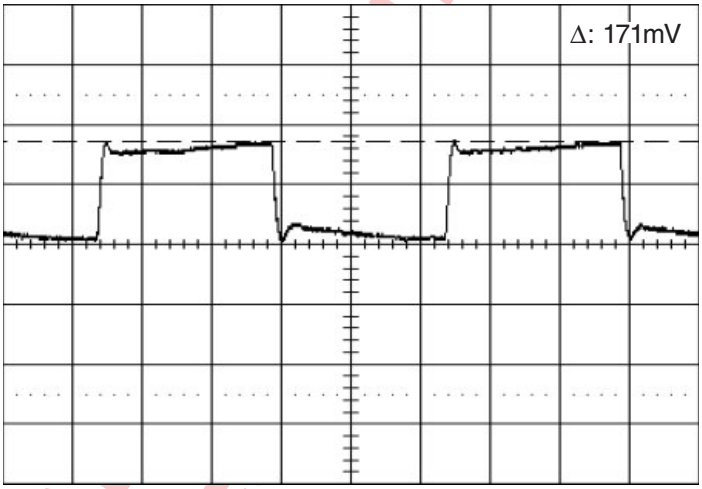
Figure 6. Output Voltage Undershoot - 6 Slave VT1105S System



Time/Div: 5µs

Conditions: V_{OUT} = 1.2V
I_{OUT} = 100A-0A Load Step
Loadline = 1.25mΩ
C_{OUT} = 58 x 22µF
1: Output Voltage (100mV/div)

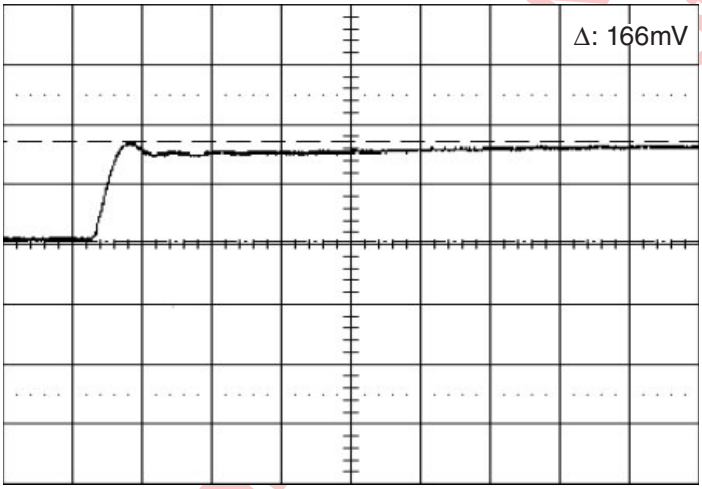
Figure 7. Load Transient Response - 6 Slave VT1125S System



Time/Div:20µs

Conditions: V_{OUT} = 1.2V
I_{OUT} = 120A-0A Load Step
Slew Rate > 1000A/µs
C_{OUT} = 58 x 22µF
1: Output Voltage (100mV/div)

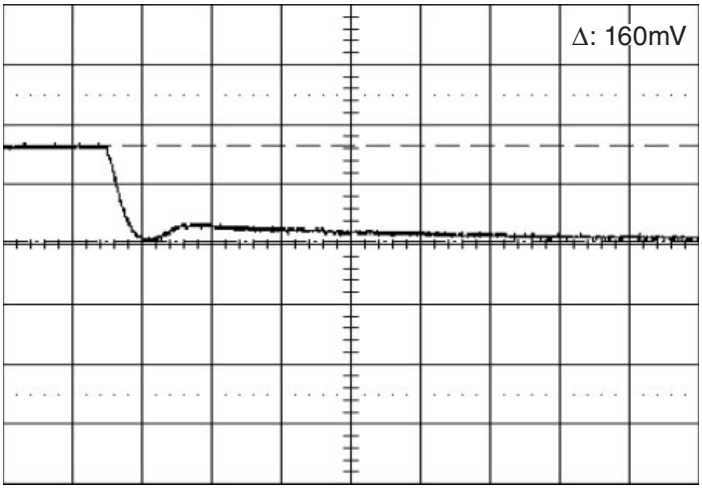
Figure 8. Output Voltage Overshoot - 6 Slave VT1125S System



Time/Div: 5µs

Conditions: V_{OUT} = 1.2V
I_{OUT} = 120A-0A Load Step
Loadline = 1.25mΩ
C_{OUT} = 58 x 22µF
1: Output Voltage (100mV/div)

Figure 9. Output Voltage Undershoot - 6 Slave VT1125S System



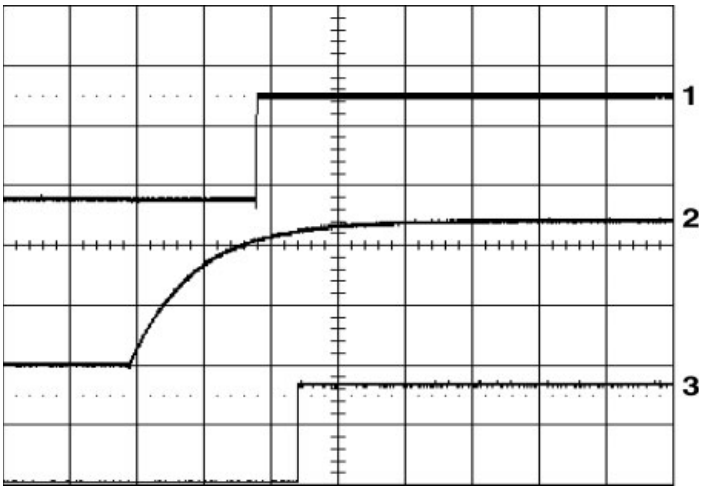
Time/Div: 5µs

Conditions: V_{OUT} = 1.2V
I_{OUT} = 120A-0A Load Step
Loadline = 1.25mΩ
C_{OUT} = 58 x 22µF
1: Output Voltage (100mV/div)

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

TYPICAL OPERATING CHARACTERISTICS (CONTINUED)

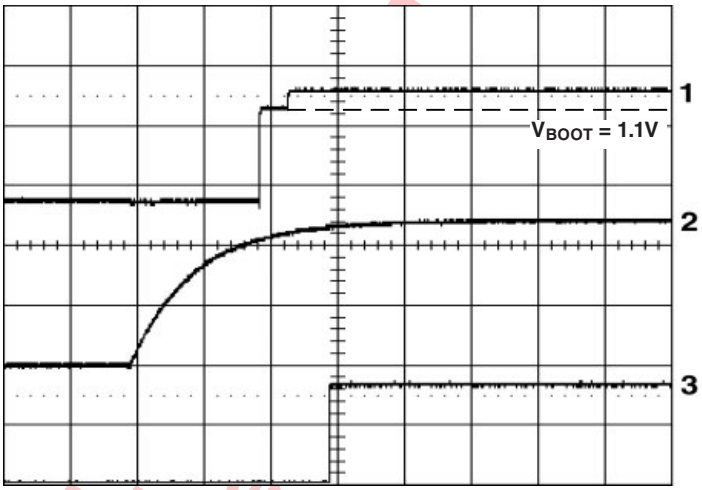
Figure 10. Startup Response References 12V Supply



Time/Div: 5ms

Conditions: V_{OUT} = 1.2V, VR 10, No Load
1: Output Voltage (0.5V/div)
2: 12V Input Voltage (5.0V/div)
3: PWRGD Signal (2.0V/div)

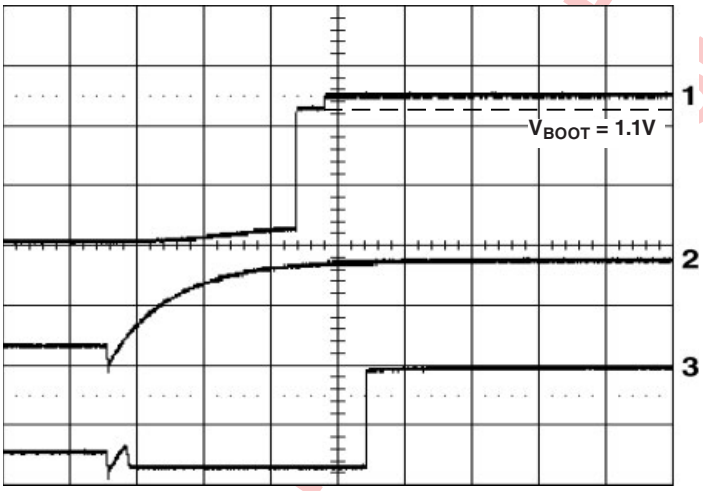
Figure 11. Startup Response References 12V Supply



Time/Div: 5ms

Conditions: V_{OUT} = 1.2V, VR 11, No Load
1: Output Voltage (0.5V/div)
2: 12V Input Voltage (5.0V/div)
3: PWRGD Signal (2.0V/div)

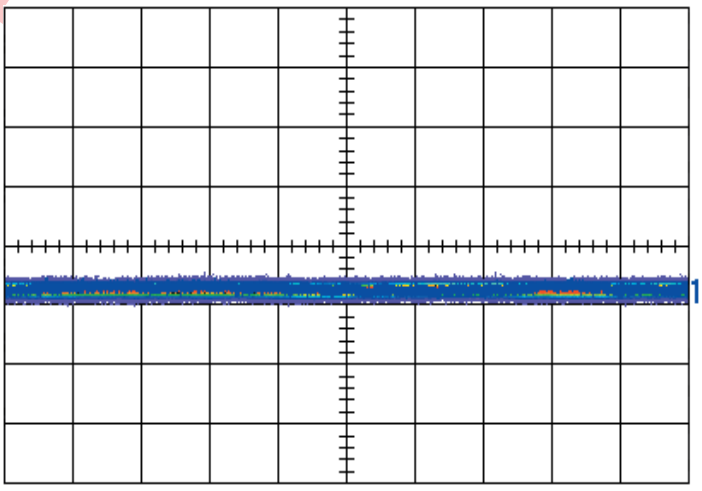
Figure 12. Startup Response References 3.3V Supply



Time/Div: 5ms

Conditions: V_{OUT} = 1.2V, VR 11, No Load
1: Output Voltage (0.5V/div)
2: 12V Input Voltage (2.0V/div)
3: PWRGD Signal (2.0V/div)

Figure 13. Output Ripple - 8 Slave VT1105S System



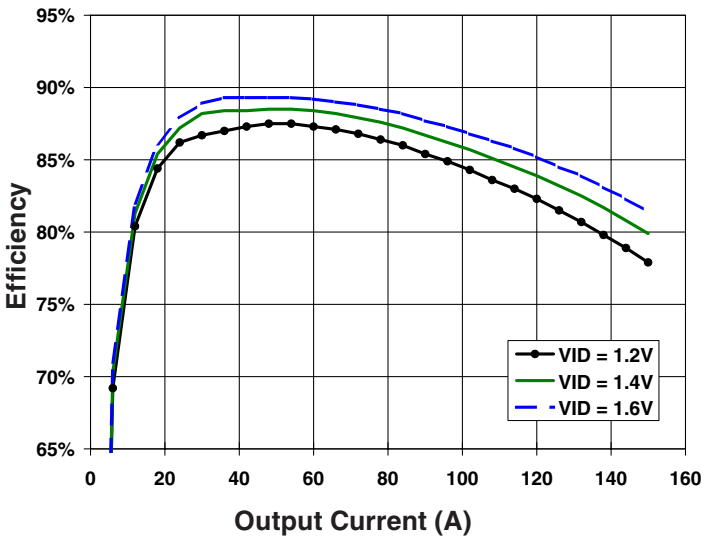
Time/Div: 10µs

Conditions: V_{OUT} = 1.2V
I_{OUT} = 100A
C_{OUT} = 58 x 22µF
1: Output Voltage (20mV/div)
25MHz BWL
Infinite Persistence
Measured @ Scope Jack on Sense Lines

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

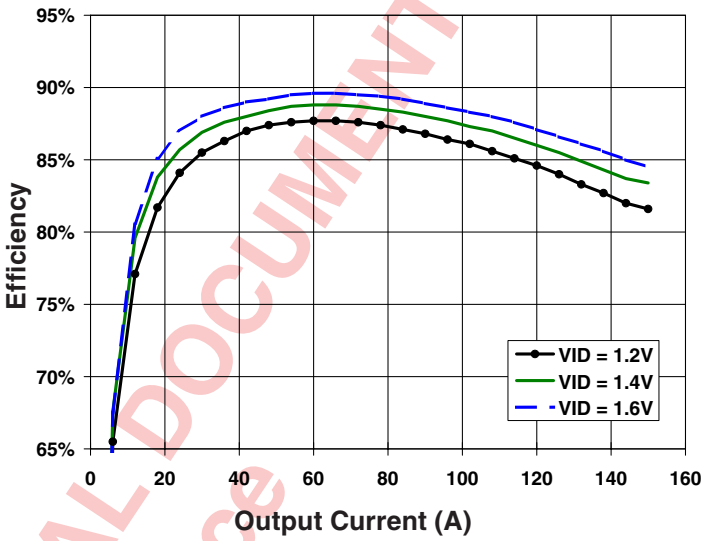
TYPICAL OPERATING CHARACTERISTICS (CONTINUED)

Figure 14. Typical System Efficiency - 6 VT1105S Slaves



Conditions: V_{IN} = 12V
L_{OUT} = 120nH
Fsw= 800kHz
T_A = 25°C
Loadline (@ V_{SENSE}) = 1.25mΩ
V_{OUT} Measured @ Inductor

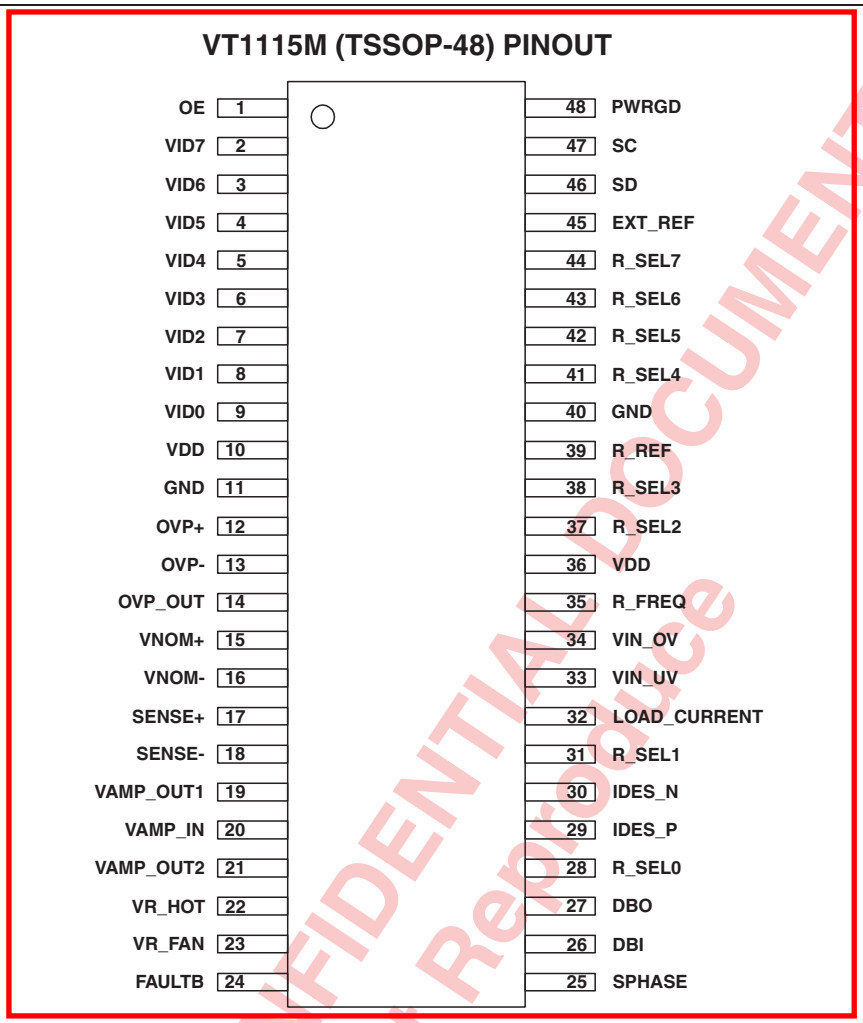
Figure 15. Typical System Efficiency - 6 VT1125S Slaves



Conditions: V_{IN} = 12V
L_{OUT} = 120nH
Fsw = 800kHz
T_A = 25°C
Loadline (@ V_{SENSE}) = 1.2mΩ
V_{OUT} Measured @ Inductor

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

VT1115M (TSSOP-48) PINOUT



PIN INFORMATION FOR MASTER CONTROLLER

OE (Pin 1): Output enable input pin. When this pin is HIGH, the output voltage is enabled. When this pin is LOW, the output voltage is disabled.

VID[7:0] (Pins 2-9): Output voltage identification code.

VDD (Pins 10, 36): Power.

GND (Pins 11, 40): Ground.

OVP+ (Pin 12): Output sensing for over-voltage and power good.

OVP- (Pin 13): Output sensing for over-voltage and power good.

OVP_OUT (Pin 14): OVP event indicator.

VNOM+ (Pin 15): DAC output.

VNOM- (Pin 16): DAC output.

SENSE+ (Pin 17): Positive remote sense.

SENSE- (Pin 18): Negative remote sense.

VAMP_OUT1 (Pin 19): Sense amplifier output.

VAMP_IN (Pin 20): Error amplifier inverting input.

VAMP_OUT2 (Pin 21): Error amplifier output.

VR_HOT (Pin 22): Indicator that one of the slaves has exceeded the programmable VR_HOT threshold.

VR_FAN (Pin 23): Indicator that one of the slaves has exceeded the programmable VR_FAN threshold.

FAULTB (Pin 24): Active low fault condition flag. This open drain output should be externally pulled high with a resistor.

SPHASE (Pin 25): Slave phase clock output. This pin provides a switching frequency reference clock signal to each slave in the system. It should be connected to each slave's SPHASE input.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

DBI (Pin 26): Digital control bus input.

DBO (Pin 27): Digital control bus output.

R_SEL[7:0] (Pin 28, 31, 37, 38, 41-44): System configuration resistors. (Programmable features detailed in Table 6.)

IDES_P (Pin 29): Idesired command (+).

IDES_N (Pin 30): Idesired command (-).

LOAD_CURRENT (Pin 32): Analog voltage representing load current.

VIN_UV (Pin 33): Scaled version of slave VDDH voltage for under voltage shutdown. This pin is used to program the input undervoltage lockout threshold for the slave VDDH supply. See the Undervoltage and Overvoltage Programming and Protection section for additional design information.

VIN_OV (Pin 34): Scaled version of slave VDDH voltage used for over voltage shutdown. This pin is used to program the input overvoltage lockout threshold for the slave VDDH supply. See the Undervoltage and Overvoltage Programming and Protection section for additional design information.

R_FREQ (Pin 35): Resistor used to program switching frequency.

R_REF (Pin 39): Reference resistor used to calibrate R_SEL.

EXT_REF (Pin 45): Precision external reference input. High reliability feature designed to guard against master controller failures. If the VT1115M determines that the voltage on this pin is out of range, it will shut down the system.

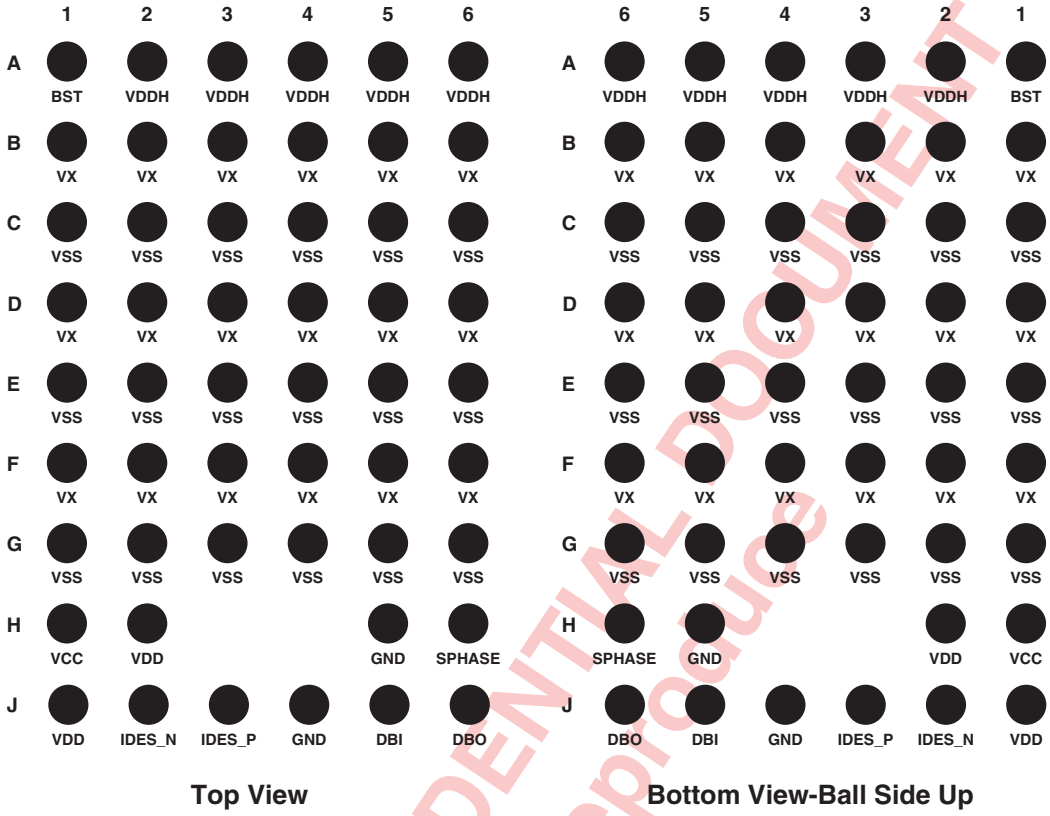
SD (Pin 46): Serial data pin for SMBus interface. See the SMBus Communication with the VT1115M section for additional design information. When not in use, this pin should be connected to VDD.

SC (Pin 47): Serial clock pin for SMBus interface. See the SMBus Communication with the VT1115M section for additional design information. When not in use, this pin should be connected to VDD.

PWRGD (Pin 48): Power good output pin. This pin indicates whether the output voltage is within regulation. This open-drain output should be externally pulled HIGH with a resistor. See the Power Good and Undervoltage and Overvoltage Programming and Protection sections for additional design information.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

VT1105S (CSP-52) PINOUT



PIN INFORMATION FOR VT1105S SMART SLAVE™

BST (Ball A1): Bootstrap supply for high side drivers.

VDDH (Balls A2-A6): 12V input supply voltage node. These balls connect to the 12V input power supply source.

VX (Balls B1-B6, D1-D6, F1-F6): Switching node. These balls connect the switching node of the power devices to the output inductor.

VSS (Balls C1-C6, E1-E6, G1-G6): Power FETs ground node. These balls connect directly to the ground plane.

VCC (Ball H1): 3.3V supply for low side drivers.

VDD (Balls H2, J1): 3.3V supply for control circuits.

GND (Balls H5, J4): Ground for control circuits.

SPHASE (Ball H6): SPHASE clock input from VT1115M master controller.

IDES_N (Ball J2): Negative input side of differential desired current signal.

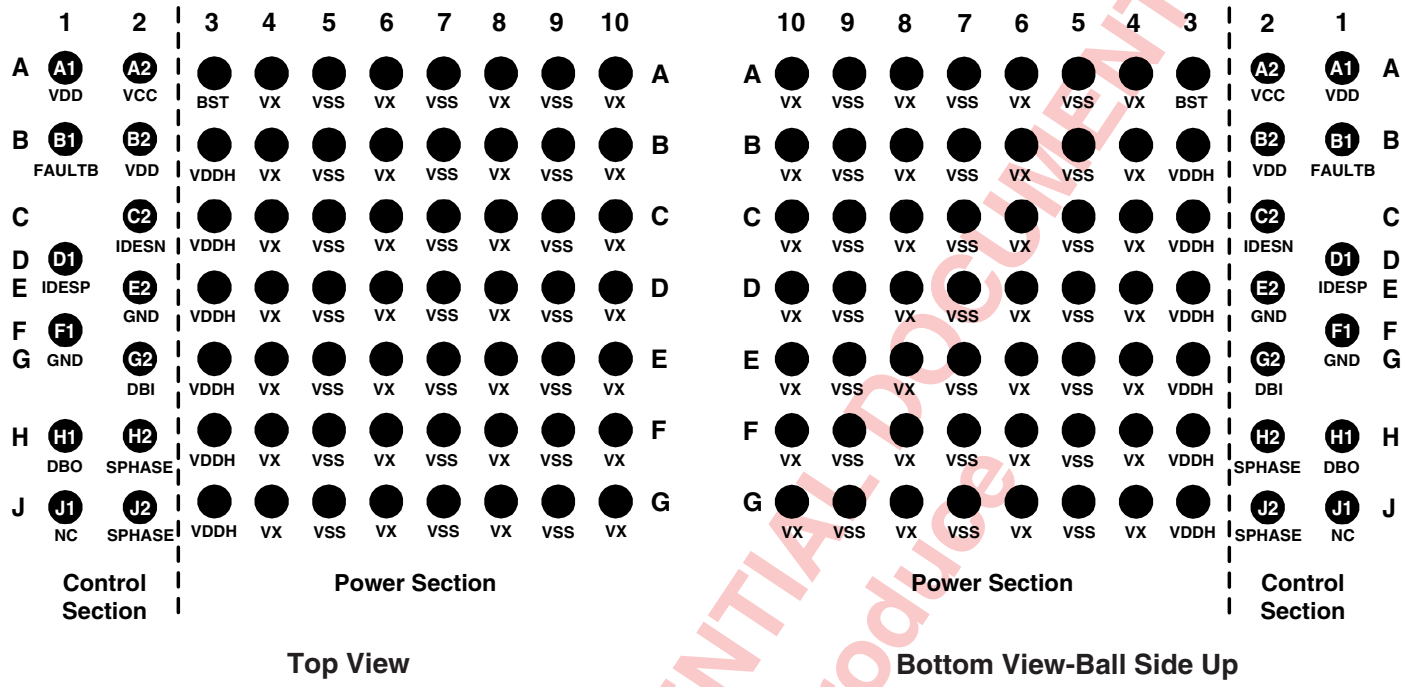
IDES_P (Ball J3): Positive input side of differential desired current signal.

DBI (Ball J5): Digital control bus input.

DBO (Ball J6): Digital control bus output.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

VT1125S (CSP-69) PINOUT



PIN INFORMATION FOR VT1125S SMART SLAVE™

VDD (Balls A1, B2): 3.3V supply for control circuits.

VCC (Ball A2): 3.3V supply for low side drivers.

BST (Ball A3): Bootstrap supply for high side drivers.

VX (Balls A4-G4, A6-G6, A8-G8, A10-G10): Switching node. These balls connect the switching node of the power devices to the output inductor.

VSS (Balls A5-G5, A7-G7, A9-G9): Power FETs ground node. These balls connect directly to the ground plane.

FAULTB (Ball B1): Fault signal. Active low.

VDDH (Balls B3-G3): 12V input supply voltage node. These balls connect to the 12V input power supply source.

IDES_N (Ball C2): Negative input side of differential desired current signal.

IDES_P (Ball D1): Positive input side of differential desired current signal.

GND (Balls E2, F1): Ground for control circuits.

DBI (Ball G2): Digital control bus input.

DBO (Ball H1): Digital control bus output.

SPHASE (Balls H2, J2): SPHASE clock input from VT1115M master controller. A 150Ω resistor is recommended in series with each slave's SPHASE line.

NC (Ball J1): No connect.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

OPERATION

The VT1115M chipset provides a high frequency, highly integrated, compact multiphase solution for high performance, low-voltage power conversion. The basic system architecture consists of a master controller and multiple Smart Slave™ devices. These integrated circuits, along with a small number of external components, provide a complete solution for multiphase buck voltage regulation.

Synchronous Rectification

Each Smart Slave™ utilizes the full benefits of a synchronous rectification topology. Both the Sync FET and Control FET Power FETs are integrated on-chip and no external power components (MOSFETs or Schottky diodes) are required. During normal device operation, the bottom side switch acts as a synchronous rectifier, carrying the current that would normally flow through an external catch diode. This technique reduces losses associated with the diode's forward voltage drop. The resulting power savings are especially important in low-output-voltage applications.

Control Architecture

The Generation 4 architecture used in the VT1115M chipset has a fully differential voltage feedback path with excellent common mode rejection and adjustable gain and compensation. The remote output voltage is connected directly to the VT1115M at the SENSE+ and SENSE- pins. The gain of the error amplifier can be set by two external resistor values across the VAMP pins (VAMP_IN, VAMP_OUT1, VAMP_OUT2). Additional resistors and capacitors in parallel with these resistors can provide additional poles and zeros for different compensation schemes.

Desired output current (I_{DES}) is a differential signal communicated to the slaves by an Idesired bus (IDES_N, IDES_P). The slaves respond to the Idesired signal by producing a DC current proportional to the differential Idesired voltage, with zero volts commanding zero amps and 1.6V corresponding to the full scale current of the slave. The value of the full scale current is programmable via a selection resistor. The slaves use their own internal control and current sense to switch their own FETs to control their inductor currents at the correct DC level, phase, and frequency.

Configuration and Programmability

Configuration settings for the VR are set up via programmable resistors on the VT1115M. Details of the options and the programmability are detailed below. A proprietary communication bus (DBI, DBO) sends out the configuration settings for the VT1115M to the Smart Slave™ devices. The control bus is also used to communicate slave status information back to the VT1115M. The system clock (SPHASE) is also broadcast from the VT1115M to each Smart Slave™.

Volterra provides standard reference designs with all of the programmable parameters optimized for common VR applications.

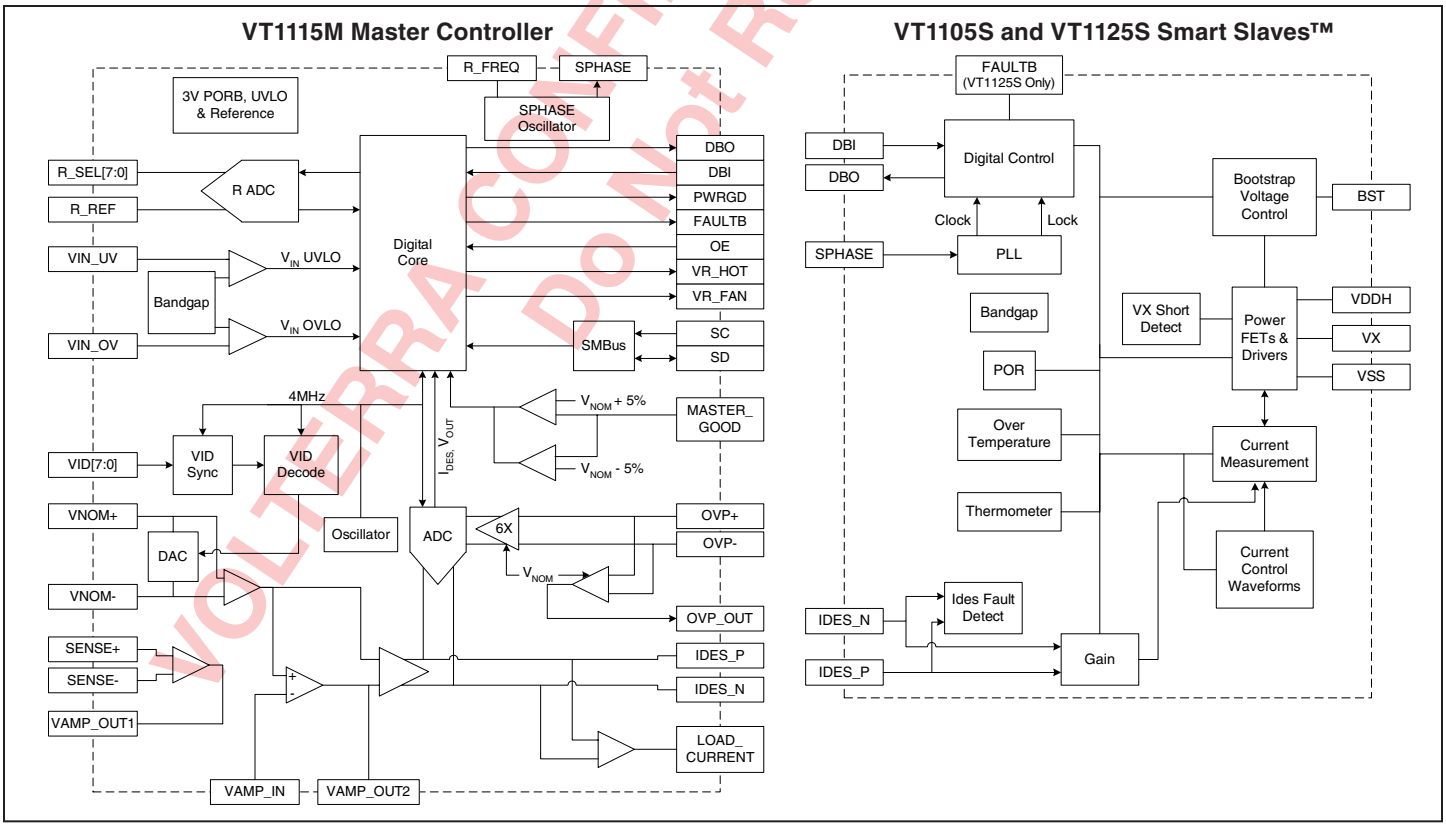


Figure 16. VT1115M Chipset Block Diagram

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

Output Current Scalability

Each Smart Slave™ incorporates all MOSFETs, gate drivers, control and sense circuitry required to implement a single phase of a multiphase buck regulation system. The output current of each slave is user programmable via the R_SEL4 resistor of the master controller. Each master controller supports up to 8 phase shifted slaves, controlled via the differential current signal (I_{DES}). Thus with one basic topology the load supplied can be scaled to any output current level and the total maximum output current equals the slave count times the maximum output current setting of each slave. No more than eight slaves should be connected to a single master, due to fan-out limitations. Up to 16 phase slots are available from the control architecture.

Because the architecture requires no additional components or other modifications to support different output currents, a single PCB layout can support a wide range of load currents with simple loading (or unloading) options. The VT1115M supports all Smart Slave™ devices in Volterra's fourth generation architecture.

The maximum output current of each slave is selected by connecting a resistor between the R_SEL4 pin and ground. Table 1 provides a list of typical values for R_SEL4 and I_{MAX}. For example, for systems where the maximum operating current per slave is 20A, then setting I_{MAX} = 24A is the recommended setting to provide headroom for excursions around the 20A operating value.

The R_SEL4 resistor also controls an internal slave setting which affects the current control algorithm during an unloading transient. For typical applications, internal setting "1" is recommended to minimize the output voltage overshoot during a transient event.

Table 1: I_{MAX} Programming

R_SEL4 (Ω)	I_{MAX} (A)	Internal Slave Setting
340	24	1
1.02k	24	2
1.74k	24	3
2.43k	24	4
3.09k	20	4
3.74k	20	3
4.42k	20	2
5.11k	20	1
5.90k	32	1
6.49k	32	2
7.15k	32	3
7.87k	32	4
8.66k	28	4
9.31k	28	3
10.0k	28	2
10.7k	28	1

Output Voltage Programming

The output voltage of the VT1115M chipset is digitally programmable from 0.600V to 1.60V. The master controller provides built-in support for the industry standard VID codes as follows:

- VR 10.X specification (0.83125V to 1.600V)
- Extended (7 bit) VR 10 specification
- VR 11 specification (0.60V to 1.60V)
- Opteron™ VID code specification (0.800V to 1.550V)

See Tables 15, 16 and 17 for VID tables.

VID code selection is accomplished by connecting a resistor between the R_SEL3 pin and ground. The value of this resistor determines the VID code selected, as shown in Table 2. In conjunction with the R_SEL3 pin, the VID[7:0] pins program an internal DAC that sets the regulator's output voltage. External pull-up resistors can be used for VID[7:0]. At zero output load, the output voltage is equal to the nominal voltage value. This value depends on the VID standard, VID code and setpoint value. Table 2 shows the nominal voltage for each VID standard.

Table 2: VID Code Selection

R_SEL3 (Ω)	VID Code	V_{NOM} Value (V)
340 or 1.02k	VR 10.X	VID - 18.75mV + SP
23.7k or 27.4k	VR 11	VID - 15.625mV + SP
5.9k or 6.49k	Opteron™	VID + 25mV + SP

Programmable Setpoint

The regulator's output voltage setpoint can be adjusted by connecting a resistor from the R_SEL1 pin to ground. The value of this resistor determines the magnitude of the setpoint adjustment, as summarized in Table 3. Overcurrent protection mode (OCP) is also programmable using the R_SEL1 pin. Overcurrent protection is discussed in more detail in the Overcurrent Protection Mode section.

Programmable Droop

The Generation 4 architecture enables flexibility in matching system load lines. To achieve the correct system load line, the proper system gain must be chosen via resistor settings on the VT1115M.

System gain relates total system current to output voltage droop where the system gain (in current per droop voltage) is described in the following equation.

$$\frac{I_{SLAVE}}{V_{DROOP}} = \frac{R2}{R1} \bullet \left(\frac{I_{MAX}}{1.6}\right) \bullet \{6,13,20\}$$

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

Table 3: Setpoint and Overcurrent Programmability

RSEL_1 (Ω)	Setpoint Adjust (mV) (VID_SEL = VR 10 or Opteron™)	Setpoint Adjust (mV) (VID_SEL = VR 11)	OCP Action (VID_SEL = Opteron™)	OCP Action (VID_SEL = VR 10 or VR 11)
340 (GND)	11.0	5.5	Latch off	Hiccup
1.02k	9.4	4.7	Latch off	Hiccup
1.74k	7.8	3.9	Latch off	Hiccup
2.43k	6.2	3.1	Latch off	Hiccup
3.09k	4.8	2.4	Latch off	Hiccup
3.74k	3.2	1.6	Latch off	Hiccup
4.42k	1.6	0.8	Latch off	Hiccup
5.11k	0.0	0.0	Latch off	Hiccup
5.90k	-1.6	-0.8	Latch off	Hiccup
6.49k	-3.2	-1.6	Latch off	Hiccup
7.15k	-4.8	-2.4	Latch off	Hiccup
7.87k	-6.2	-3.1	Latch off	Hiccup
8.66k	-7.8	-3.9	Latch off	Hiccup
9.31k	-9.4	-4.7	Latch off	Hiccup
10.0k	-11.0	-5.5	Latch off	Hiccup
10.7k	-11.0	-5.5	Latch off	Hiccup
11.3k	-11.0	-5.5	Latch off	CCM
12.1k	-9.4	-4.7	Latch off	CCM
13.0k	-7.8	-3.9	Latch off	CCM
14.0k	-6.2	-3.1	Latch off	CCM
15.4k	-4.8	-2.4	Latch off	CCM
16.9k	-3.2	-1.6	Latch off	CCM
18.7k	-1.6	-0.8	Latch off	CCM
20.5k	0.0	0.0	Latch off	CCM
23.7k	1.6	0.8	Latch off	CCM
27.4k	3.2	1.6	Latch off	CCM
31.6k	4.8	2.4	Latch off	CCM
39.2k	6.2	3.1	Latch off	CCM
49.9k	7.8	3.9	Latch off	CCM
69.8k	9.4	4.7	Latch off	CCM
118k	11.0	5.5	Latch off	CCM
348k (VDD)	FAULT			

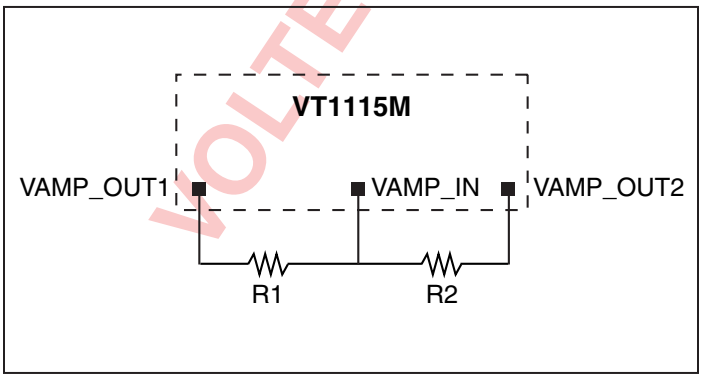


Figure 17. Amplifier Gain Programmability Resistors

Where I_{SLAVE} is the current per slave. For a total slave count of N_{SLAVES} the total regulator current is simply given by:

$$I_{OUT} = N_{SLAVES} \bullet I_{SLAVE}$$

R2 and R1 are external resistors connected around the error amplifier as shown in Figure 17. For best performance, the ratio of R2/R1 should be between 0.5 and 5. The recommended value for R1 is 500Ω.

I_{MAX} is selectable via R_SEL4 as described previously in Table 1. The choice of system gain (6 or 13 or 20) is made with R_SEL7 as shown in Table 4.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

Table 4: VR_FAN/VR_HOT, System Gain, and Master Good Feature

R_SEL7 (Ω)	Gain	VR_FAN (°C)	VR_HOT (°C)	Master Good Feature Enabled?
340	20	125	135	No
1.02k	20	115	125	No
1.74k	20	105	115	No
2.43k	20	95	105	No
3.09k	13	125	135	No
3.74k	13	115	125	No
4.42k	13	105	115	No
5.11k	13	95	105	No
5.90k	6	125	135	No
6.49k	6	115	125	No
7.15k	6	105	115	No
7.87k	6	95	105	No
8.66k	20	125	135	Yes
9.31k	20	115	125	Yes
10.0k	20	105	115	Yes
10.7k	20	95	105	Yes
11.3k	13	125	135	Yes
12.1k	13	115	125	Yes
13.0k	13	105	115	Yes
14.0k	13	95	105	Yes
15.4k	6	125	135	Yes
16.9k	6	115	125	Yes
18.7k	6	105	115	Yes
20.5k	6	95	105	Yes

Example Droop Calculation

Consider a system with 120A, 1.25mΩ load line, with 6 slaves and 20A per slave.

1. In order to ensure that there is some tolerance for current ripple, then choose I_{MAX} = 24. So based on Table 1, use R_SEL4 = 1.02kΩ.
2. Note that with 120A and 1.25mΩ load line, the voltage droop at full load is 150mV.
3. Using the equation above and 150mV and I_{MAX} = 24, R2/R1 • {6,13,20} = 8.89.
4. Choose gain of 6. Thus R_SEL7 is 7.15kΩ (according to VR_FAN/VR_HOT as shown in Table 4).
5. The remaining gain is R2/R1 = 1.48. Choose R1 = 500Ω, R2 = 732Ω for a standard 1% resistor.

Programmable VR_FAN and VR_HOT

The Volterra architecture provides for VR temperature measurements to be made directly in the slave devices. This information is communicated to the VT1115M where VR_FAN and VR_HOT signals can be flagged. The temperature thresholds for VR_FAN and VR_HOT are offset from each other by 10°C as shown in Table 4.

The programmable resistor R_SEL7 sets thresholds for VR_FAN and VR_HOT. This programmable resistor is also used for setting system gain {6,13,20}, as described in the Programmable Droop section previously. The values for R_SEL7 are selected according to Table 4.

On-the-Fly VID

The VT1115M chipset meets AMD Opteron™, Intel® VR 10.X and Intel® VR 11 'VID on the fly' VID specifications.

Output Enable

The OE pin enables or disables the regulator's output voltage. It should be pulled HIGH using an external pull-up resistor. When forced LOW, the output voltage is disabled.

Power Good

The Power Good (PWRGD) pin provides an open drain output that indicates the status of the output voltage. This pin is externally pulled HIGH using a pull-up resistor of 10kΩ or higher. The signal remains high during normal regulator operation. A low signal indicates an output voltage deviation above or outside of the power good window for at least 12µs. The deviation threshold is user programmable and can be adjusted using R_SEL2 as shown in Table 8.

SMBus COMMUNICATION WITH THE VT1115M

The following sections assume basic familiarity with the SMBus interface. Additional background information is available at http://www.smbus.org. The SMBus interface supports the following subset of the SMBus 2.0 specification (appropriate section numbers in parentheses):

- Compliant with 3.3V to 5V ±10% supply levels (2.0)
- SMBus slave support only
- No packet error checking (PEC) (5.4)
- No support for Address Resolution Protocol (5.6)
- Resistor setting allows unique addressing of 16 modules per bus
- Supports SMBus protocols:
  - Write byte/word (5.5.4)
  - Read byte/word (5.5.5)

The following regulator monitoring information is available over the SMBus interface:

- Average regulator output current
- Peak regulator output current (max of averages)
- Sample-by-sample peak regulator output current (cleared after each read)
- Average V_{OUT} error voltage
- Individual slave junction temperature
- Number of active regulator phases
- Slave status reporting (VX short, over-temperature)

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- Status of power good signal
- Status of input undervoltage monitor
- Status of input overvoltage monitor
- Status of output overvoltage monitor
- Status of output enable signal
- Status of output overcurrent monitor
- Status of digital bus monitor
- Status of VR_HOT and VR_FAN
- VID code settings
- Controller ID number
- Controller revision number

The following regulator control capabilities are supported over the SMBus interface:

- Override the VID code settings to program the output voltage
- Override the OE signal to shutdown the regulator
- Override the setpoint and OVP threshold voltages

Up to 16 VT1115M masters can be uniquely addressed via the SMBus. R_SEL0 is used to identify each VT1115M master's address on the SMBus. Addresses are defined as shown in Table 5.

Table 5: Programmable VT1115M Addresses via SMBus

R_SEL0 (Ω)	SMBus Address
340 (GND)	0
1.02k	1
1.74k	2
2.43k	3
3.09k	4
3.74k	5
4.42k	6
5.11k	7
5.90k	8
6.49k	9
7.15k	10
7.87k	11
8.66k	12
9.31k	13
10.0k	14
10.7k	15

Start Up

With VID_SEL set to VR 11, the VT1115M follows VR 11 start-up sequences as shown in Figure 18. Timing specifications are included in the Electrical Characteristics section of this datasheet.

ADDITIONAL PROGRAMMABLE FEATURES AND SETTINGS

Programmable features for the regulator system are read by the VT1115M at startup as detailed in each section of this datasheet. Table 6 shows how the programmable features are related to the R_SEL pins. For calibration, the reference resistor R_{REF} must be 11kΩ with an accuracy of ±0.5%. For setting programmable features, the variable resistors (R_SEL[0:7]) must be accurate to ±1%. Temperature coefficient mismatch between the reference and variable resistors must not exceed 100ppm/°C.

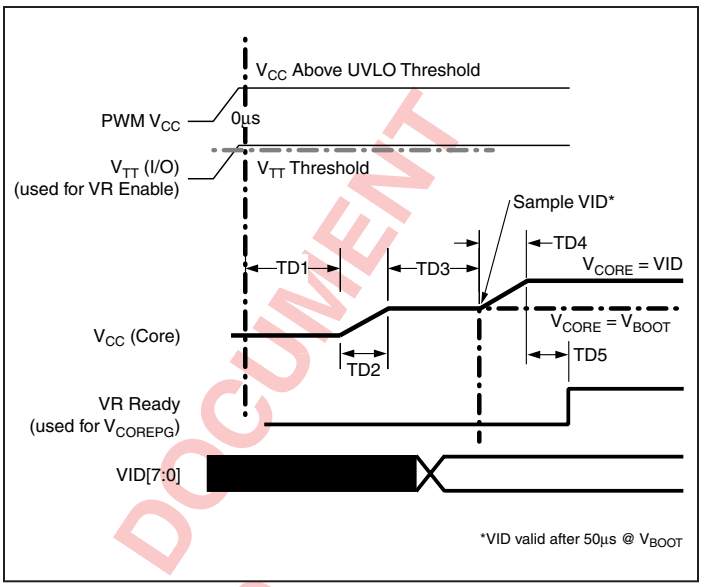


Figure 18. VR 11 Start Up Timing

Table 6: Programmable Features

Feature	R_SEL[7:0]
SMBus Address	0
Setpoint	1
OCP Behavior	1
Power Good Thresholds	2
OVP Threshold	2
VID Select	3
Slave Configuration	4-6
System Gain	7
VR_HOT/VR_FAN Threshold	7

Programmable Switching Frequency

The per-phase switching frequency of the regulator is determined by connecting a resistor between the R_FREQ pin and ground. Nominal per phase switching frequencies are selected by choosing an appropriate resistor value as specified in Table 7 or the equation below. Interleaved, multiphase operation results in an effective switching frequency equal to the number of phases times the per-phase switching frequency.

$$freq = 1/(48 \bullet 10^{-9} + R_{FREQ} \bullet 46 \bullet 10^{-12})$$

Higher switching frequencies enable smaller and faster regulator solutions; lower switching frequencies maximize system efficiency.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

Table 7: Nominal Switching Frequency Programmability	
R_{FREQ} (kΩ)	F_{SPHASE} (kHz)
14	1448
17.8	1154
22.6	918.8
28.7	730.3
36.5	578.9

Undervoltage and Overvoltage Programming and Protection

Programming for Power Good and OVP thresholds is determined via R_SEL2 as shown in Table 8.

The master controller provides programmable input and undervoltage and overvoltage protection. Lockout thresholds for the primary 12V input supply are programmed using the VIN_UV and VIN_OV pins as shown in Figure 19.

The master controller includes programmable output overvoltage protection (OVP). Overvoltage events are detected by monitoring the OVP+ OVP- pin voltages. The system enters OVP mode when OVP+ exceeds VNOM for 500ns by a user-defined amount. Refer to Table 8 for appropriate R_SEL2 values to set the percentage over VNOM for the OVP threshold.

The lower Power Good threshold is set in absolute numbers of mV below V_{NOM} using R_SEL2 (see Table 8). The upper Power Good threshold is set as a percentage above

Table 8: Power Good and OVP Threshold Programmability

R_SEL2 (Ω)	Lower Power Good Threshold (mV below V_{NOM})	Uppoer Power Good Threshold (mV above V_{NOM})	OVP Threshold (% above V_{NOM})	Do VR 11 Start-Up Sequence?*
340 (GND)	240	115	130	Yes
1.02k	240	115	120	Yes
1.74k	240	107.5	112.5	Yes
2.43k	240	105	110	Yes
3.09k	180	115	130	Yes
3.74k	180	115	120	Yes
4.42k	180	107.5	112.5	Yes
5.11k	180	105	110	Yes
5.90k	120	115	130	Yes
6.49k	120	115	120	Yes
7.15k	120	107.5	112.5	Yes
7.87k	120	105	110	Yes
8.66k	60	115	130	Yes
9.31k	60	115	120	Yes
10.0k	60	107.5	112.5	Yes
10.7k	60	105	110	Yes
11.3k	240	115	130	No
12.1k	240	115	120	No
13.0k	240	107.5	112.5	No
14.0k	240	105	110	No
15.4k	180	115	130	No
16.9k	180	115	120	No
18.7k	180	107.5	112.5	No
20.5k	180	105	110	No
23.7k	120	115	130	No
27.4k	120	115	120	No
31.6k	120	107.5	112.5	No
39.2k	120	105	110	No
49.9k	60	115	130	No
69.8k	60	115	120	No
118k	60	107.5	112.5	No
348k (VDD)	60	105	110	No

*__NOTE:__ Only applicable if VR 11 VID code is selected. VR 11 start-up with never occur if another VID code is selected.

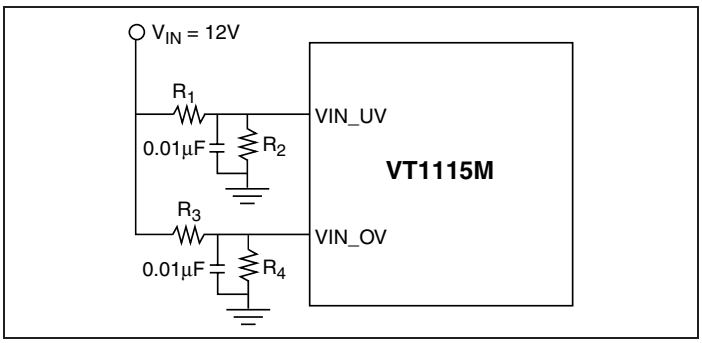


Figure 19. Programming Voltage Lockout Thresholds

V_{NOM}, also shown in the table. OVP thresholds are set as a percentage above V_{NOM}, all via appropriate choice of the value of R_SEL2.

Overvoltage protection is incorporated as part of normal system operation. When the output voltage rises above its nominal value, the slaves turn on their lower MOSFETs and conduct current to ground in an effort to lower the output voltage. If the output voltage continues to rise and the programmable overvoltage threshold is reached, the master controller flags this event on the OVP_OUT pin and the chipset immediately enters a latched shutdown state. The OVP flag can also be read through the SMBus (see SMBus Application Note 11 for details). Restarting the regulator then requires cycling the input and 3.3V power supplies.

The input undervoltage falling threshold is set using the equation:

$$VIN\_UV_1 = \left(1 + \frac{R_1}{R_2}\right) V_{BG}$$

The input overvoltage falling threshold is set using the equation:

$$VIN\_OV_1 = \left(1 + \frac{R_3}{R_4}\right) V_{BG}$$

The input undervoltage rising threshold is set using the equation:

$$VIN\_UV_2 = \left(1 + \frac{R_1}{R_2}\right) (V_{BG} + 0.059)$$

The input overvoltage rising threshold is set using the equation:

$$VIN\_OV_2 = \left(1 + \frac{R_3}{R_4}\right) (V_{BG} + 0.059)$$

where V_{BG} is the bandgap voltage (equal to 1.23V). Both thresholds have roughly 60mV of hysteresis. Typical values of the two resistors used to program each threshold should sum to approximately 100kΩ. A 0.01µF capacitor should also be used to bypass the VIN_UV and VIN_OV pins.

The master controller also incorporates internal circuitry to monitor the 3.3V input supply through its VDD pin to detect undervoltage conditions.

During startup, the master controller monitors these pin voltages to ensure that both the 3.3V and 12V supplies are valid before initiating its startup sequence. If, at any time, the input supplies violate one of these lockout thresholds, the system turns off. Once the supplies become valid again, the system resumes normal operation.

Overcurrent Protection Mode

When the I_{DES} signal indicates a max current command for more than 11ms, the VT1115M master enters one of two available OCP protection modes as shown in Table 3. The OCP strategy used is programmable and can either force the system to a constant current mode (CCM) or a Hiccup OCP mode. The mode is selected via R_SEL1 (in combination with the regulator set-pint adjustment) as specified in Table 3. When VID_SEL = AMD, the OCP action is always to latch the system off.

In the hiccup OCP mode, the master controller alternately enables and disables the output voltage with a 10% duty cycle. Initially, the controller attempts to charge the output node for a period of approximately 5.5ms. If the output voltage has not recovered within this interval, the output is disabled for approximately 50ms and the cycle repeats. Once the output voltage becomes valid, the system self-recovers. The purpose of this “hiccup” mode is to minimize stresses during fault conditions, such as those of a short circuit.

Integrated Thermal Protection (Slave)

Each Smart Slave™ includes integrated thermal protection circuitry. When the slave’s junction temperature exceeds 155°C, the device enters a latched shutdown state, and a fault condition is reported to the master. This fault flag is indicated by the associated master’s FAULTB pin going low and can also be read through the SMBus. For the VT1125S slave, the slave fault is directly indicated on the slave’s FAULTB ball as well. Cycling either the 3.3V or the 12V input power supply resets the slave and clears the fault condition.

Slave Configuration Resistors

Two additional configuration resistors need to be added for the recommended system set-up. R_SEL5 and R_SEL6 should be grounded or connected to ground with 340Ω resistors for normal operation.

MASTER-SLAVE DIGITAL INTERFACE

The Generation 4 slaves are configured and monitored via a digital daisy chain interface between the master and all slaves where all devices are connected in a ring. Digital_Bus_Out (DBO) is the first output from the VT1115M, and is connected to the Digital_Bus_In of the first slave (DBI). The DBO of each slave is then daisy-chain connected to the DBI of each subsequent slave. After all slaves are connected, the ring

is terminated back at the DBI of the VT1115M. The master controller automatically detects the number of phases present and then sets the phase spacing appropriately. Each slave is assigned its own sequential number via the daisy chain control bus and switches in accordance to its required phase offset to the SPHASE signal. For example, with only two slaves, phase spacing is 180 degrees; with three slaves, spacing is 120 degrees.

Each slave's phase offset and other configuration settings are communicated over the digital bus during startup. Fault conditions are communicated from slave to master during normal operation.

Second Level Redundancy

The VT1115M system is equipped with a "Master Good" feature that enhances the reliability of the power system. In order to guard against master controller failures, the VT1115M monitors a precision external reference connected to the EXT_REF pin. The external reference should be programmed to equal the V_{NOM} of the VT1115M.

The VT1115M will continuously measure the external reference. If the measured voltage falls outside a specified tolerance around V_{NOM}, the system latches off. In order to prevent false Master Good fault assertion, the VT1115M has a built-in digital filter. Master Good fault will not be asserted unless the voltage on the EXT_REF pin is outside the tolerance band for 1µs. Master Good shutdown requires power cycle for system restart. This feature can be enabled by using the appropriate R_SEL7 resistor settings (see Table 4).

EXTERNAL COMPONENT SELECTION

Table 9 provides a list of external components required to complete the VT1115M regulation system. More detailed component selection information is provided in the following sections.

Bleed Resistor

A small 100Ω bleed resistor should be connected between the output of the regulator and ground for applications with very low output current loads in shutdown. This pull-down resistor ensures that the output is in a known low-voltage state during shutdown.

Inductor Selection

The output inductor has an important influence on the overall size, cost, and efficiency of the voltage regulator. Smaller inductor values usually correspond to larger saturation current ratings, smaller physical sizes, or both. Since the inductor is typically one of the larger components in the system, a minimum inductor value is particularly important in space-constrained applications. Smaller inductor values also permit faster transient response.

Table 9: Recommended External Components

Master Components			
Description	**Value**	**Package**	**Quantity**
VDD Capacitor	1µF / 6.3V	0603	1
VNOM Capacitor	6800pF / 6.3V	0603	1
UV/OV Capacitors	0.1µF / 6.3V	0603	2
UV/OV Resistors	Varies	0603	4
R2/R1 Resistors	Varies	0603	2
Configuration Resistor	Varies, 1% tolerance	0603	7
Configuration Reference Resistor	11kΩ, 0.5% tolerance	0603	1
Frequency Resistor	Varies	0603	1
PG Pullup Resistor	10kΩ	0603	1
Fault Pullup Resistor	10kΩ	0603	1
SC/SD Pullup Resistor	10kΩ	0603	2
VID[0:5], OE Resistor	10kΩ	0603	7
Bleed Resistor	100Ω	0603	1
Slave Components			
Description	**Value**	**Package**	**Quantity**
VDD 3.3V Capacitor	1µF / 6.3V / 125°C	0603	1
VCC 3.3V Capacitor	1µF / 6.3V / 125°C	0603	1
Boost Capacitor	1µF / 6.3V / 125°C	0603	1
VDD12V HF Capacitor	1µF / 16V / 125°C	0603	3*
VDD12V Bulk Capacitor	10µF* / 16V / 125°C	1206	2

***NOTE:** Under review - Volterra may relax these recommendations.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

The current slew rate through the output inductor is given by:

$$\text{Slew Rate} = \frac{dI_L}{dt} = \frac{V_L}{L}$$

where I_L is the inductor current, L is the output inductance, and V_L is the voltage drop across the inductor. This equation implies that larger inductor values limit the regulator's ability to slew current through the output inductor in response to step load transients. Consequently, more output capacitors are required to supply (or store) sufficient charge to maintain regulation while the inductor current "catches up" to the load.

In contrast, smaller inductor values increase the regulator's maximum achievable slew rate and decrease the necessary capacitance, at the expense of higher ripple current. The peak-to-peak ripple current for a single slave is given by the following equation:

$$I_{PP} = \frac{1}{fL}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)(V_{OUT})$$

where f is the switching frequency, L is the output inductor value, V_{IN} is the input voltage, and V_{OUT} is the output voltage. From this equation, it is clear that for the same switching frequency, ripple current increases inversely as L decreases. This increased ripple current results in increased AC loss, larger peak current and, for the same output capacitance, results in increased output voltage ripple.

The saturation current rating of the inductor is another important consideration. At steady-state full load, the peak inductor current is given by:

$$I_{PK} = I_{MAX} + \frac{I_{PP}}{2}$$

where I_{MAX} is the desired, maximum DC load current per slave (see the Slave Output Current Programming section) and I_{PP} is the peak-to-peak inductor current ripple, defined above. For proper operation of the regulator, it is important that I_{PK} never exceeds the saturation current rating of the inductor, I_{SAT}, during steady-state operation. It is recommended that a margin of at least 20% is included between I_{PK} and I_{SAT}:

$$I_{SAT} > 1.2 \bullet I_{PK}$$

For example, in a 12V to 1.2V application with f = 1MHz and L = 100nH, I_{PP} = 10.8A. With I_{MAX} programmed to 24A, the peak inductor current is I_{PK} = 29.4A, and an inductor with a saturation current rating of at least 36A is recommended. Also note that the saturation current of an inductor is generally smaller at high temperature than at room temperature. It is therefore recommended that the saturation current of the inductor be specified at the maximum case temperature of 125°C.

Finally, the power dissipation of the inductor influences the regulation efficiency. Losses in the inductor include core loss, DC resistance loss, and AC resistance loss. For the best efficiency, inductors with ferrite core material exhibiting low loss in the range of 0.5MHz to 2MHz, DC winding

Table 10: Inductor Contacts

Company	Phone	Website
Cooper Electronics	(561) 752-5000	www.cooperet.com
ICE Components	(800) 729-2099	www.icecomponents.com
Pulse	(858) 674-8159	www.pulseeng.com
Vitec	(760) 918-8831	www.viteccorp.com

Table 11: Output Inductors

Inductor	Vendor	Part Number	Value (nH)	I_{SAT} (A)	R_{DC} (mΩ)	Footprint (mm)	Height (mm)
100nH	Cooper Electronics	FP4-100	100	44	0.59	10.2 x 6.8	5
	ICE Components	LP02-101-2	100	45	0.43	9.0 x 7.0	5
	Pulse	PA0511.101	120	41	0.55	10.2 x 7.0	5
	Vitec	59P9011	120	41	0.37	10.4 x 7.0	5
70nH	ICE Components	LP02-800-1S	85	44	0.35	7.2 x 6.5	5
	Pulse	PA0512.700	72	48	0.45	7.0 x 7.0	5.2
	Vitec	59P9003	70	45	0.30	7.6 x 7.5	5
50nH	Cooper Electronics	FP2-V050	50	60 [3]	0.46	7.2 x 6.7	5
	ICE	LP02-500-1S	50	60 [3]	0.37	7.2 x 6.5	5.2
	Vitec	59P9002	50	52	0.29	7.6 x 7.5	5

NOTE 3: Inductance drop less than 20% for I_{DC} up to 60A.
NOTE 4: Saturation current (I_{SAT}) and DC winding resistance (R_{DC}) as characterized by Volterra at 125°C.
NOTE 5: I_{SAT} is defined by Volterra as a 20% drop in zero-bias inductance at 125°C.

resistance below 1mΩ, and AC winding resistance below 10mΩ at 2MHz are recommended.

Table 10 and Table 11 provide a summary of recommended inductor suppliers and part numbers. Each inductor meets the electrical requirements of VT1115M applications and has been characterized and guard-banded by Volterra to specify minimum saturation current at 125ºC over part-to-part and lot-to-lot variations. In addition, most of these inductors share a common printed circuit board (PCB) footprint, simplifying parts procurement.

The choice of 100nH inductors with per-phase switching frequencies in the range of 700kHz to 1MHz are generally recommended as a good trade-off between efficiency, transient response, current ripple, voltage ripple, and overall system size in a typical 12V to low-voltage application with large load steps and transient windows greater than 100mV. For applications with more demanding transient requirements, 70nH or 50nH inductors and switching frequencies above 1MHz are recommended.

Output Capacitor Selection

Output capacitance is selected to provide suitable transient tolerance and output voltage ripple. For the best performance, lowest cost, and smallest size of the VT1115M system, multilayer ceramic chip (MLCC) capacitors with 1206 or smaller case sizes, capacitance values of 47µF or smaller, 6.3V or 4V voltage ratings, and X5R or better temperature characteristics are recommended.

In VT1115M systems with large transient load steps and MLCC output capacitors, it is generally the value of capacitance, rather than the series parasitics of those capacitors, that determines the transient tolerance. An all-MLCC capacitance value of 160µF (per slave) guarantees that the output voltage will not deviate by more than 150mV peak-to-peak for 12.5A/slave unloading and loading transients with 1A/ns load current slew rates and a 120nH inductor (per slave).

If desired, more capacitance can be added at the output to tighten transient tolerance at the expense of increased size, cost, and component count. For a given load step magnitude ΔI_{LOAD}, output inductor value L, peak-to-peak ripple current I_{PP}, input voltage V_{IN}, and output voltage V_{OUT}, the transient overshoot and undershoot generally scale inversely with the value of output capacitance, C_{OUT}. For larger load steps with the same tolerance, capacitance should be increased with load step magnitude and peak-to-peak ripple current according to the following relationship:

$$C_{OUT} \propto \left(\Delta I_{LOAD} + \frac{I_{PP}}{2}\right)^2$$

The voltage undershoot associated with a loading transient generally scales inversely with (V_{IN} - V_{OUT}). Similarly, the voltage overshoot associated with an unloading transient scales inversely with V_{OUT}. For the same transient tolerance, C_{OUT} generally scales linearly with L (see the Inductor Selection section).

Output voltage ripple is another important consideration in the selection of output capacitors. For a single-phase buck regulator operating in continuous conduction mode, the total voltage ripple across the output capacitor bank can be approximated as the sum of three voltage waveforms: 1) the triangle wave that results from multiplying the AC ripple current by the ESR, 2) the square wave that results from multiplying the ripple current slew rate by the ESL, and 3) the piecewise quadratic waveform that results from charging and discharging the output capacitor:

$$V_{PP} = (ESR)(I_{PP}) + (ESL)\left(\frac{V_{IN}}{L}\right) + \left(\frac{I_{PP}}{8fC_{OUT}}\right)$$

where ESR is the equivalent series resistance at the output, I_{PP} is the peak-to-peak inductor current ripple, ESL is the high-frequency equivalent series inductance at the output, V_{IN} is the input voltage, L is the output inductance, f is the switching frequency, and C_{OUT} is the output capacitance. In a typical VT1115M application with a bank of 1206, X5R, 6.3V, 22µF output capacitors, these three components are roughly equal.

In a multiphase regulation system, however, this equation represents only a worst-case upper bound. The actual output voltage ripple depends on the relative phasing of the individual slaves and the PCB parasitics between the output capacitors. In the worst case (when N slave contributions add constructively), the net I_{PP} and ripple current slew rate are N times larger than for a single slave. However, the parallel combination of the output capacitance of N slaves results in a net C_{OUT} which is N times larger, and net ESR and ESL, which are N times smaller than for a single slave. This leads to an identical expression for the absolute worst-case output voltage ripple of the system. Of course, typical phasing of the slaves dramatically improves this ripple.

The ESL effect of an output capacitor on output voltage ripple cannot be estimated from the resonant frequency, but from the high-frequency (10MHz or above) impedance of that capacitor. The contribution to ESL of a single 1206 22µF output capacitor is between 0.3 and 0.4nH, rather than the 1.2nH usually quoted. PCB traces and vias in the V_{OUT} / GND loop contribute additional parasitic inductance.

The final considerations in the selection of output capacitors are ripple current rating and power dissipation. Using a conservative design approach, the output capacitors should be designed to handle the maximum peak-to-peak AC ripple current experienced in the worst case. Because the recommended output capacitors have extremely low

ESR values, they easily satisfy this ripple current requirement. For the triangular AC ripple current at the output, the total RMS current that needs to be handled is calculated as:

$$I_{RMS_{COUT}} = \frac{I_{PP}}{\sqrt{12}}$$

and the total power dissipation in the output capacitors is:

$$P_{COUT} = I^2_{RMS_{COUT}} \cdot ESR$$

where ESR is the equivalent series resistance of the entire output capacitor bank. In a 12V to 1.2V application using a 100nH output inductor and switching at 1MHz, the peak-to-

Table 12: Capacitor Contacts

Company	Phone	Website
AVX	(843) 448-9411	www.avxcorp.com
Murata	(770) 436-1300	www.murata.co.jp
Panasonic	(714) 373-7334	www.panasonic.com
Taiyo Yuden	(408) 753-4150	www.taiyo-yuden.com
TDK	(847) 803-6100	www.component.tdk.com

Table 13: MLCC Output Capacitors

Case Size	Value (µF)	Temperature Rating	Voltage Rating	t [6] (mm)	Vendor	Part Number
1206	10	X5R	6.3V	1.6	AVX Murata Taiyo Yuden TDK	1206D106MAT2A GRM31CR60J106KA01L JMK316BJ226ML C3216X5R0J106M
1206	10	X6S	4V 6.3V 4V	1.6	AVX Murata TDK	12064W106MAT2A GRM319C80J106KE19D C3216X6S0G106M
1206	22	X5R	6.3V	1.6	AVX Murata Taiyo Yuden TDK	12066D226MAT2A GRM31CR60J226KE19L JMK316BJ226ML C3216X5R0J226M
1206	22	X6S	4V	1.6	AVX Murata TDK	12064W226MAT2A GRM31CC80G226KE19L C3216X6S0G226M
1206	47	X5R	4V 6.3V	1.6	AVX Murata Taiyo Yuden TDK	12064D476MAT2A GRM31CR60J476ME19L JMK316BJ476ML C3216X5R0J476M
1206	47	X6S	4V	1.6	TDK	C3216X6S0G476M
0805	10	X5R	6.3V	1.25 1.25 0.85 1.25	AVX Murata Taiyo Yuden TDK	08056D106MAT2A GRM21BR60J106KE19L JMK212BJ106MD C2012X5R0J106M
0805	10	X6S	4V 6.3V 4V	1.6	AVX Murata TDK	08054W106MAT2A GRM21BC80J106KE19L C2012X6S0G106M
0805	22	X5R	6.3V	1.25 1.25 1.25 1.25	AVX Murata Taiyo Yuden TDK	08056D226MAT2A GRM21BR60J226ME39L JMK212BJ226MG C2012X5R0J226M
0805	22	X6S	4V 6.3V 4V	1.6	AVX Murata TDK	08054W226MAT2A GRM21BC80J226ME51L C2012X6S0G226M

NOTE 6: t indicates nominal thickness in mm.

peak ripple current is 10.8A per slave, yielding an RMS ripple current of 3.1A. With eight 22µF output capacitors in the 1206 case size, each capacitor must handle a worst-case RMS ripple current of (3.1/8 = 0.39A). This RMS current level corresponds to a total power dissipation of less than 15mW and surface temperature rise of less than 3°C, and thus falls well within the ripple current rating for the parts. Operation under such conservative conditions extends the lifetime of the capacitors and improves system reliability.

Table 12 and Table 13 provide a list of recommended capacitor suppliers and MLCC output capacitors for VT1115M systems. Each capacitor has 1206 or smaller case size, X5R or better temperature rating, 6.3V or 4V voltage rating, and value of 47µF or smaller.

In applications where transient tolerance is more constraining than output voltage ripple, the replacement of some MLCC output capacitors with one or more bulk capacitors may be cost effective. Panasonic's 220µF, 9mΩ, 2V SX series of SP-cap (part number EEFSX0D221R) is recommended for these applications.

Input Capacitor Selection

The selection and placement of input capacitors are important considerations. High-frequency input capacitors serve to control switching noise. For the best high-frequency noise suppression, three pieces of 0603, 1µF, 16V, 125°C MLCC input capacitors are recommended per slave. Bulk input capacitors are designed to absorb the pulsed DC current that is drawn by the regulator. For the best performance, lowest cost, and smallest size of the VT1115M system, multilayer ceramic chip (MLCC) capacitors with 1210 or smaller case sizes, capacitance values of 22µF or smaller, 16V voltage ratings, and X7R or X7S temperature characteristics are recommended as bulk. The minimum required value of bulk capacitance is strongly influenced by the parasitic inductance in the loop, which includes the +12V supply.

Because they must source the pulsed DC input current of the regulator, the power dissipation and self-heating of the bulk input capacitors are far more important than those for the output capacitors. In a conventional single-phase buck regulator, the magnitude of the RMS input capacitor current can be approximated using the following equation:

$$I_{RMS_{CIN}} = \frac{I_{LOAD}\sqrt{V_{OUT}\left(V_{IN} - V_{OUT}\right)}}{V_{IN}}$$

where I_{LOAD} is the output DC load current per slave. With an equivalent series resistance of the bulk input capacitor bank, ESR_{CIN}, the total power dissipation in these input capacitors is:

$$P_{CIN} = I^2_{RMS_{CIN}} \cdot ESR_{CIN}$$

For a multiphase system, however, this expression for RMS input current represents only a worst-case upper bound. Typical phasing among slaves reduces the overall ripple current demand on each slave's input capacitors. In practice, the ripple cancellation depends strongly on PCB layout parasitics, operating frequencies, load dynamics,

Table 14: MLCC Input Capacitors

Case Size	Value (µF)	Temperature Rating	Voltage Rating	t [7] (mm)	Vendor	Part Number
0603	1	X7S X7S X7R	6.3V 10V 6.3V	0.8 [8]	AVX Murata TDK	06036Z105KAT GRM188C71A105KA12D C1608X7R0J105K
0603	1	X7S X7R	16V	0.8 [8]	Murata TDK	GRM188C71C105KA12D C1608X7R1C105K
0805	2.2	X7R	25V 16V	1.25 1.25	Murata TDK	GRM21BR71E225KA73L C2012X7R1C225M
0805	4.7	X7R	16V	1.25	Murata TDK	Expected in Q4'04 Expected in Q4'04
1206	4.7	X7R	16V	1.6	AVX Murata Taiyo	Expected in 1Q04 GRM31CR71C475KA01L Expected in 4Q04
1206	10	X7R	16V	1.6	Murata TDK	GRM31CR71C106KAC7L C3216X7R1C106M
1210	10	X7R	16V 25V	2.0 2.5	Murata TDK	GRM32DR71C106KA01L C3225X7R1E106M
1210	22	X7R	16V	2.5	Murata TDK	Expected in Q4'04 C3225X7R1C226M

NOTE 7: t indicates nominal thickness in mm.
NOTE 8: Indicates capacitors with nominal thickness smaller than the minimum CSP package thickness.

and output to input voltage ratios. So the actual RMS current through each slave's input capacitors lies somewhere between these two extremes.

A conservative approach uses the worst-case upper bound to determine the power dissipation and self-heating of the input capacitors. For a VT1115M system converting 12V to 1.2V with 18A of sustained load current per slave, the worst-case RMS current flowing through each slave's input capacitor bank is equal to 5.4A. If two 10µF input capacitors in 1206 cases are used, the overall ESR is 4mΩ. The power dissipation in the input capacitors is 120mW, yielding nearly 12°C in case temperature rise, which are acceptable numbers for most applications. For better efficiency and increased reliability, the number of input capacitors can be increased to three or more.

The proximity of the input capacitors to the Smart Slaves™ can have an important impact on efficiency and regulation. Please see the PCB Layout section that follows for a description of the best design practices.

Table 14 provides a list of recommended input capacitors for VT1115M systems. Each capacitor has 1210 or smaller case size, 125°C temperature rating, and 16V voltage rating. In some applications, the Smart Slaves™ may require a heatsink. The typical heatsink construction includes an extrusion for the Smart Slaves™ slaves. Capacitors with thickness less than the minimum height of the CSP package are indicated in Table 14. These capacitors are likely to fit within the same extrusion as the CSP package, minimizing the cost and complexity of the heatsink design.

PCB Layout

The printed circuit board layout can dramatically affect the performance of the regulator. A poorly designed board can degrade efficiency, noise performance, and even control loop stability. At higher switching frequencies, layout issues are especially critical.

As a general guideline, the input capacitors and output inductor should be placed in close proximity to each slave IC, while the output capacitors should be lumped together as close to the load as possible. **Input bypass capacitors should be placed on the same PCB side as the CSPs, all referenced to a common ground plane directly beneath. High-frequency capacitors with maximum thickness of 0.95mm or less should be used to clear heatsink restrictions, so that capacitors are as close to the CSPs as possible.** Traces to these components should be kept as short and wide as possible to minimize parasitic inductance and resistance. Traces connecting the input capacitors and internal FETs on each slave IC require particular attention since they carry currents with the largest RMS values and fastest slew rates. The input capacitors should be placed as close to the input supply pins as possible. An uninterrupted ground plane is required immediately underneath these high-frequency current paths, with the ground plane located no more than 5 mils below the top layer. By keeping the flow of this high-frequency AC current localized to a tight loop at the regulator, electromagnetic interference (EMI) can be minimized.

A low impedance ground plane is essential to keep all voltages referenced to a common ground and to minimize stray inductance in all high-frequency loops. Multiple vias are recommended for all paths that carry high currents (i.e., ground, VDD, VX). Vias should be placed close to the chips to create the shortest possible current loops. But it should be insured that via placement does not obstruct the flow of currents or the mirror currents induced in the ground plane.

Careful attention should also be paid to the VX traces to minimize noise coupling into surrounding circuits. These traces include large voltage swings (greater than 12V) with dv/dt greater than 10V/ns. It is recommended that these traces are not only kept short, but are shielded with a GND plane immediately beneath.

Voltage sense lines should be routed differentially directly from the load points. They should be routed in parallel and in close proximity to each other. The ground plane can be used as a shield for these or other sensitive signals to protect them from capacitive or magnetic coupling of high-frequency noise.

For remote-sense applications where the load and VT1115M controller IC are separated by a significant distance or impedance, it is important to place the majority of the output capacitors directly at the load. Ideally, for system stability, all of the output capacitors should be placed as close as possible to the load.

Gerber files with layout information and complete reference designs can be obtained by contacting a Volterra account representative.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

Table 15: VR 10 with 6.25mV Extension VID Codes - Programmable Output Voltage Settings (R_SEL = 0.34kΩ)

VID 4 400mV	VID 3 200mV	VID 2 100mV	VID 1 50mV	VID 0 25mV	VID 5 12.5mV	VID 6 6.25mV	Voltage (V)	VID 4 400mV	VID 3 200mV	VID 2 100mV	VID 1 50mV	VID 0 25mV	VID 5 12.5mV	VID 6 6.25mV	Voltage (V)
0	1	0	1	0	1	1	1.60000	1	1	0	1	0	1	1	1.20000
0	1	0	1	0	1	0	1.59375	1	1	0	1	0	1	0	1.19375
0	1	0	1	1	0	1	1.58750	1	1	0	1	1	0	1	1.18750
0	1	0	1	1	0	0	1.58125	1	1	0	1	1	0	0	1.18125
0	1	0	1	1	1	1	1.57500	1	1	0	1	1	1	1	1.17500
0	1	0	1	1	1	0	1.56875	1	1	0	1	1	1	0	1.16875
0	1	1	0	0	0	1	1.56250	1	1	1	0	0	0	1	1.16250
0	1	1	0	0	0	0	1.55625	1	1	1	0	0	0	0	1.15625
0	1	1	0	0	1	1	1.55000	1	1	1	0	0	1	1	1.15000
0	1	1	0	0	1	0	1.54375	1	1	1	0	0	1	0	1.14375
0	1	1	0	1	0	1	1.53750	1	1	1	0	1	0	1	1.13750
0	1	1	0	1	0	0	1.53125	1	1	1	0	1	0	0	1.13125
0	1	1	0	1	1	1	1.52500	1	1	1	0	1	1	1	1.12500
0	1	1	0	1	1	0	1.51875	1	1	1	0	1	1	0	1.11875
0	1	1	1	0	0	1	1.51250	1	1	1	1	0	0	1	1.11250
0	1	1	1	0	0	0	1.50625	1	1	1	1	0	0	0	1.10625
0	1	1	1	0	1	1	1.50000	1	1	1	1	0	1	1	1.10000
0	1	1	1	0	1	0	1.49375	1	1	1	1	0	1	0	1.09375
0	1	1	1	0	0	1	1.48750	1	1	1	1	1	0	1	OFF
0	1	1	1	0	0	0	1.48125	1	1	1	1	1	0	0	OFF
0	1	1	1	1	1	1	1.47500	1	1	1	1	1	1	1	OFF
0	1	1	1	1	1	0	1.46875	1	1	1	1	1	1	0	OFF
1	0	0	0	1	0	1	1.46250	0	0	0	0	0	0	1	1.08750
1	0	0	0	1	0	0	1.45625	0	0	0	0	0	0	0	1.08125
1	0	0	0	0	1	1	1.45000	0	0	0	0	0	1	1	1.07500
1	0	0	0	0	1	0	1.44375	0	0	0	0	0	1	0	1.06875
1	0	0	0	0	0	1	1.43750	0	0	0	0	1	0	1	1.06250
1	0	0	0	0	0	0	1.43125	0	0	0	0	1	0	0	1.05625
1	0	0	0	1	1	1	1.42500	0	0	0	0	1	1	1	1.05000
1	0	0	0	1	1	0	1.41875	0	0	0	0	1	1	0	1.04375
1	0	0	1	1	0	1	1.41250	0	0	0	1	0	0	1	1.03750
1	0	0	1	1	0	0	1.40625	0	0	0	1	0	0	0	1.03125
1	0	0	1	0	1	1	1.40000	0	0	0	1	0	1	1	1.02500
1	0	0	1	0	1	0	1.39375	0	0	0	1	0	1	0	1.01875
1	0	0	1	0	0	1	1.38750	0	0	0	1	1	0	1	1.01250
1	0	0	1	0	0	0	1.38125	0	0	0	1	1	0	0	1.00625
1	0	0	1	1	1	1	1.37500	0	0	0	1	1	1	1	1.00000
1	0	0	1	1	1	0	1.36875	0	0	0	1	1	1	0	0.99375
1	0	1	0	1	0	1	1.36250	0	0	1	0	0	0	1	0.98750
1	0	1	0	1	0	0	1.35625	0	0	1	0	0	0	0	0.98125
1	0	1	0	0	1	1	1.35000	0	0	1	0	0	1	1	0.97500
1	0	1	0	0	1	0	1.34375	0	0	1	0	0	1	0	0.96875
1	0	1	0	0	0	1	1.33750	0	0	1	0	1	0	1	0.96250
1	0	1	0	0	0	0	1.33125	0	0	1	0	1	0	0	0.95625
1	0	1	0	1	1	1	1.32500	0	0	1	0	1	1	1	0.95000
1	0	1	0	1	1	0	1.31875	0	0	1	0	1	1	0	0.94375
1	0	1	1	1	0	1	1.31250	0	0	1	1	0	0	1	0.93750
1	0	1	1	1	0	0	1.30625	0	0	1	1	0	0	0	0.93125
1	0	1	1	0	1	1	1.30000	0	0	1	1	0	1	1	0.92500
1	0	1	1	0	1	0	1.29375	0	0	1	1	0	1	0	0.91875
1	0	1	1	0	0	1	1.28750	0	0	1	1	1	0	1	0.91250
1	0	1	1	0	0	0	1.28125	0	0	1	1	1	0	0	0.90625
1	0	1	1	1	1	1	1.27500	0	0	1	1	1	1	1	0.90000
1	0	1	1	1	1	0	1.26875	0	0	1	1	1	1	0	0.89375
1	1	0	0	1	0	1	1.26250	0	1	0	0	0	0	1	0.88750
1	1	0	0	1	0	0	1.25625	0	1	0	0	0	0	0	0.88125
1	1	0	0	0	1	1	1.25000	0	1	0	0	0	1	1	0.87500
1	1	0	0	0	1	0	1.24375	0	1	0	0	0	1	0	0.86875
1	1	0	0	0	0	1	1.23750	0	1	0	0	1	0	1	0.86250
1	1	0	0	0	0	0	1.23125	0	1	0	0	1	0	0	0.85625
1	1	0	0	1	1	1	1.22500	0	1	0	0	1	1	1	0.85000
1	1	0	0	1	1	0	1.21875	0	1	0	0	1	1	0	0.84375
1	1	0	1	0	0	1	1.21250	0	1	0	1	0	0	1	0.83750
1	1	0	1	0	0	0	1.20625	0	1	0	1	0	0	0	0.83125

NOTE: VID[0] must be set high for standard VR10.X VID codes.

Table 16: VR 11 8-Bit VID Codes - Programmable Output Voltage Settings (R_SEL = 27.4kΩ)

VID HEX1 VID[7:4]	VID HEX2 VID[3:0]	Voltage (V)	VID HEX1 VID[7:4]	VID HEX2 VID[3:0]	Voltage (V)	VID HEX1 VID[7:4]	VID HEX2 VID[3:0]	Voltage (V)	VID HEX1 VID[7:4]	VID HEX2 VID[3:0]	Voltage (V)	VID HEX1 VID[7:4]	VID HEX2 VID[3:0]	Voltage (V)
0	0	OFF	3	4	1.28750	6	7	0.96875	9	A	0.65000	*C*	*D*	*0.33125*
0	1	OFF	3	5	1.28125	6	8	0.96250	9	B	0.64375	*C*	*E*	*0.32500*
0	2	1.60000	3	6	1.27500	6	9	0.95625	9	C	0.63750	*C*	*F*	*0.31875*
0	3	1.59375	3	7	1.26875	6	A	0.95000	9	D	0.63125	*D*	*0*	*0.31250*
0	4	1.58750	3	8	1.26250	6	B	0.94375	9	E	0.62500	*D*	*1*	*0.30625*
0	5	1.58125	3	9	1.25625	6	C	0.93750	9	F	0.61875	*D*	*2*	*0.30000*
0	6	1.57500	3	A	1.25000	6	D	0.93125	A	0	0.61250	*D*	*3*	*0.29375*
0	7	1.56875	3	B	1.24375	6	E	0.92500	A	1	0.60625	*D*	*4*	*0.28750*
0	8	1.56250	3	C	1.23750	6	F	0.91875	*A*	*2*	*0.60000*	*D*	*5*	*0.28125*
0	9	1.55625	3	D	1.23125	7	0	0.91250	*A*	*3*	*0.59375*	*D*	*6*	*0.27500*
0	A	1.55000	3	E	1.22500	7	1	0.90625	*A*	*4*	*0.58750*	*D*	*7*	*0.26875*
0	B	1.54375	3	F	1.21875	7	2	0.90000	*A*	*5*	*0.58125*	*D*	*8*	*0.26250*
0	C	1.53750	4	0	1.21250	7	3	0.89375	*A*	*6*	*0.57500*	*D*	*9*	*0.25625*
0	D	1.53125	4	1	1.20625	7	4	0.88750	*A*	*7*	*0.56875*	*D*	*A*	*0.25000*
0	E	1.52500	4	2	1.20000	7	5	0.88125	*A*	*8*	*0.56250*	*D*	*B*	*0.24375*
0	F	1.51875	4	3	1.19375	7	6	0.87500	*A*	*9*	*0.55625*	*D*	*C*	*0.23750*
1	0	1.51250	4	4	1.18750	7	7	0.86875	*A*	*A*	*0.55000*	*D*	*D*	*0.23125*
1	1	1.50625	4	5	1.18125	7	8	0.86250	*A*	*B*	*0.54375*	*D*	*E*	*0.22500*
1	2	1.50000	4	6	1.17500	7	9	0.85625	*A*	*C*	*0.53750*	*D*	*F*	*0.21875*
1	3	1.49375	4	7	1.16875	7	A	0.85000	*A*	*D*	*0.53125*	*E*	*0*	*0.21250*
1	4	1.48750	4	8	1.16250	7	B	0.84375	*A*	*E*	*0.52500*	*E*	*1*	*0.20625*
1	5	1.48125	4	9	1.15625	7	C	0.83750	*A*	*F*	*0.51875*	*E*	*2*	*0.20000*
1	6	1.47500	4	A	1.15000	7	D	0.83125	*B*	*0*	*0.51250*	*E*	*3*	*0.19375*
1	7	1.46875	4	B	1.14375	7	E	0.82500	*B*	*1*	*0.50625*	*E*	*4*	*0.18750*
1	8	1.46250	4	C	1.13750	7	F	0.81875	*B*	*2*	*0.50000*	*E*	*5*	*0.18125*
1	9	1.45625	4	D	1.13125	8	0	0.81250	*B*	*3*	*0.49375*	*E*	*6*	*0.17500*
1	A	1.45000	4	E	1.12500	8	1	0.80625	*B*	*4*	*0.48750*	*E*	*7*	*0.16875*
1	B	1.44375	4	F	1.11875	8	2	0.80000	*B*	*5*	*0.48125*	*E*	*8*	*0.16250*
1	C	1.43750	5	0	1.11250	8	3	0.79375	*B*	*6*	*0.47500*	*E*	*9*	*0.15625*
1	D	1.43125	5	1	1.10625	8	4	0.78750	*B*	*7*	*0.46875*	*E*	*A*	*0.15000*
1	E	1.42500	5	2	1.10000	8	5	0.78125	*B*	*8*	*0.46250*	*E*	*B*	*0.14375*
1	F	1.41875	5	3	1.09375	8	6	0.77500	*B*	*9*	*0.45625*	*E*	*C*	*0.13750*
2	0	1.41250	5	4	1.08750	8	7	0.76875	*B*	*A*	*0.45000*	*E*	*D*	*0.13125*
2	1	1.40625	5	5	1.08125	8	8	0.76250	*B*	*B*	*0.44375*	*E*	*E*	*0.12500*
2	2	1.40000	5	6	1.07500	8	9	0.75625	*B*	*C*	*0.43750*	*E*	*F*	*0.11875*
2	3	1.39375	5	7	1.06875	8	A	0.75000	*B*	*D*	*0.43125*	*F*	*0*	*0.11250*
2	4	1.38750	5	8	1.06250	8	B	0.74375	*B*	*E*	*0.42500*	*F*	*1*	*0.10625*
2	5	1.38125	5	9	1.05625	8	C	0.73750	*B*	*F*	*0.41875*	*F*	*2*	*0.10000*
2	6	1.37500	5	A	1.05000	8	D	0.73125	*C*	*0*	*0.41250*	*F*	*3*	*0.09375*
2	7	1.36875	5	B	1.04375	8	E	0.72500	*C*	*1*	*0.40625*	*F*	*4*	*0.08750*
2	8	1.36250	5	C	1.03750	8	F	0.71875	*C*	*2*	*0.40000*	*F*	*5*	*0.08125*
2	9	1.35625	5	D	1.03125	9	0	0.71250	*C*	*3*	*0.39375*	*F*	*6*	*0.07500*
2	A	1.35000	5	E	1.02500	9	1	0.70625	*C*	*4*	*0.38750*	*F*	*7*	*0.06875*
2	B	1.34375	5	F	1.01875	9	2	0.70000	*C*	*5*	*0.38125*	*F*	*8*	*0.06250*
2	C	1.33750	6	0	1.01250	9	3	0.69375	*C*	*6*	*0.37500*	*F*	*9*	*0.05625*
2	D	1.33125	6	1	1.00625	9	4	0.68750	*C*	*7*	*0.36875*	*F*	*A*	*0.05000*
2	E	1.32500	6	2	1.00000	9	5	0.68125	*C*	*8*	*0.36250*	*F*	*B*	*0.04375*
2	F	1.31875	6	3	0.99375	9	6	0.67500	*C*	*9*	*0.35625*	*F*	*C*	*0.03750*
3	0	1.31250	6	4	0.98750	9	7	0.66875	*C*	*A*	*0.35000*	*F*	*D*	*0.03125*
3	1	1.30625	6	5	0.98125	9	8	0.66250	*C*	*B*	*0.34375*	F	E	OFF
3	2	1.30000	6	6	0.97500	9	9	0.65625	*C*	*C*	*0.33750*	F	F	OFF
3	3	1.29375												

Legend

Plain Text	Supported VIDs	VID = 1.0V to 1.6V, Tolerance = ±0.5% 0.8V < VID < 1.0V, Tolerance = ±5mV VID < 0.8V, Tolerance = ±8mV
Italic Text	0.44 < VID < 0.6V	Full device operation to specification is not guaranteed at this output voltage
Shaded Cells	VID < 0.44V	Output voltages below VID = 0.44V are not supported in this device

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

Table 17: AMD Opteron™ VID Codes - Programmable Output Voltage Settings (R_SEL3 = 5.90kΩ)

VID5	VID4	VID3	VID2	VID1	VID0	Output Voltage (V)
N/A	0	0	0	0	0	1.550
N/A	0	0	0	0	1	1.525
N/A	0	0	0	1	0	1.500
N/A	0	0	0	1	1	1.475
N/A	0	0	1	0	0	1.450
N/A	0	0	1	0	1	1.425
N/A	0	0	1	1	0	1.400
N/A	0	0	1	1	1	1.375
N/A	0	1	0	0	0	1.350
N/A	0	1	0	0	1	1.325
N/A	0	1	0	1	0	1.300
N/A	0	1	0	1	1	1.275
N/A	0	1	1	0	0	1.250
N/A	0	1	1	0	1	1.225
N/A	0	1	1	1	0	1.200
N/A	0	1	1	1	1	1.175
N/A	1	0	0	0	0	1.150
N/A	1	0	0	0	1	1.125
N/A	1	0	0	1	0	1.100
N/A	1	0	0	1	1	1.075
N/A	1	0	1	0	0	1.050
N/A	1	0	1	0	1	1.025
N/A	1	0	1	1	0	1.000
N/A	1	0	1	1	1	0.975
N/A	1	1	0	0	0	0.950
N/A	1	1	0	0	1	0.925
N/A	1	1	0	1	0	0.900
N/A	1	1	0	1	1	0.875
N/A	1	1	1	0	0	0.850
N/A	1	1	1	0	1	0.825
N/A	1	1	1	1	0	0.800
N/A	1	1	1	1	1	Shutdown

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

REFERENCE DESIGN

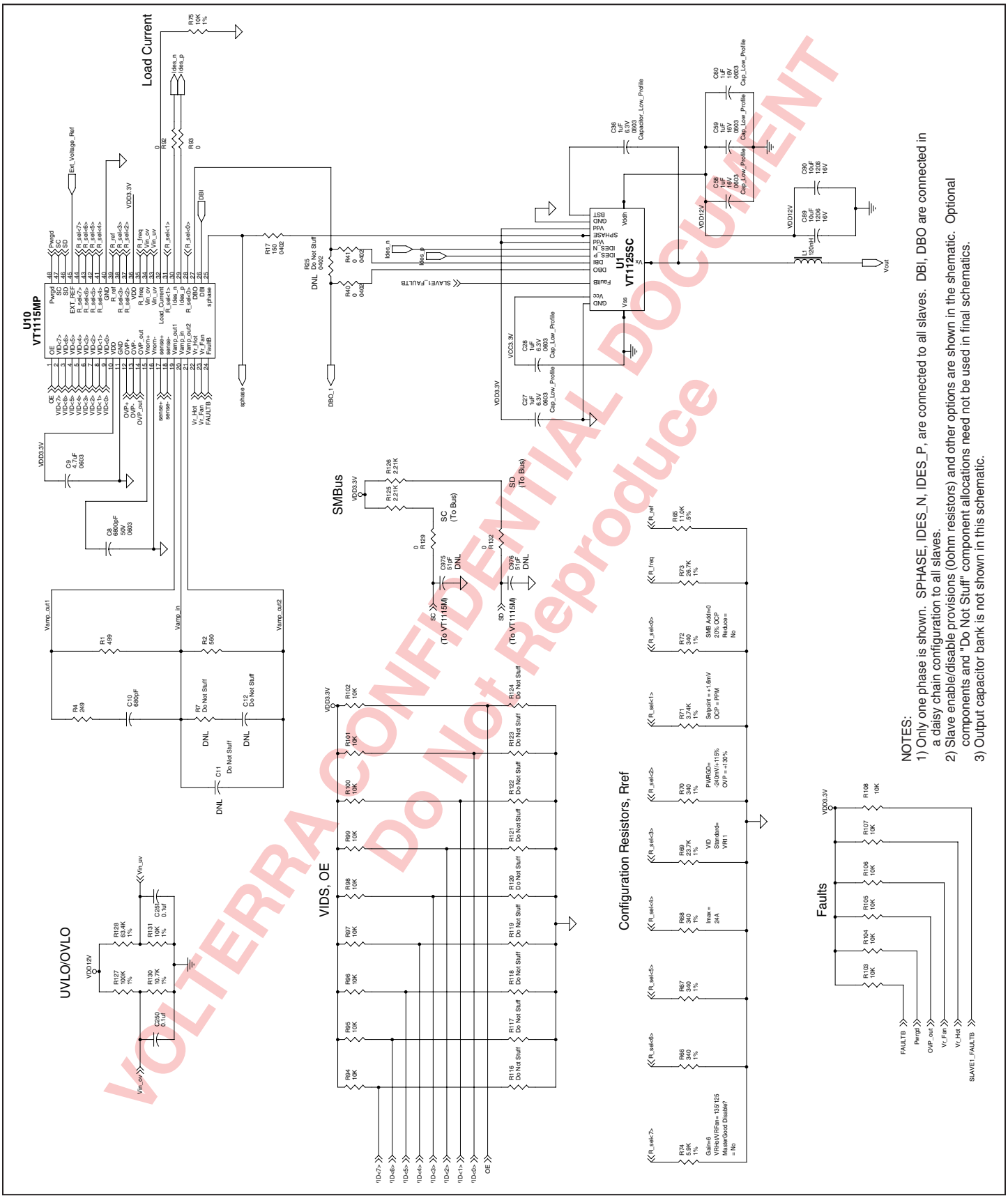
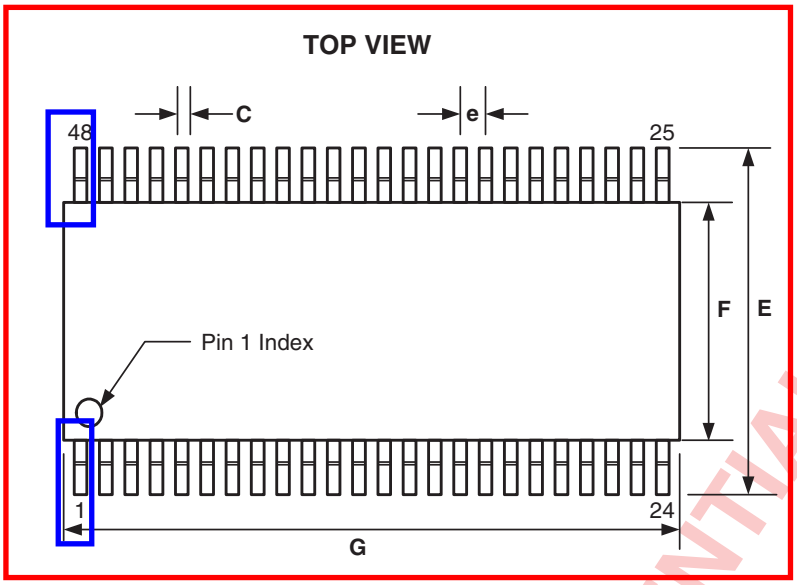


Figure 20. VT1115M/VT1125S Chipset Reference Design Schematic

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

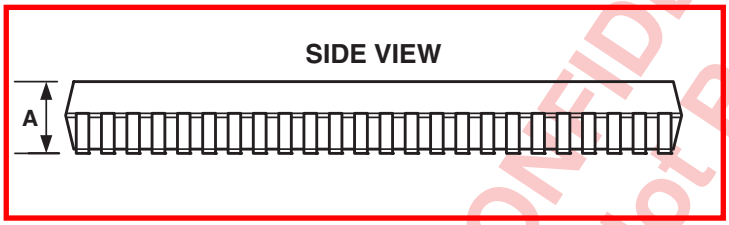
PACKAGE DIMENSIONS - VT1115M

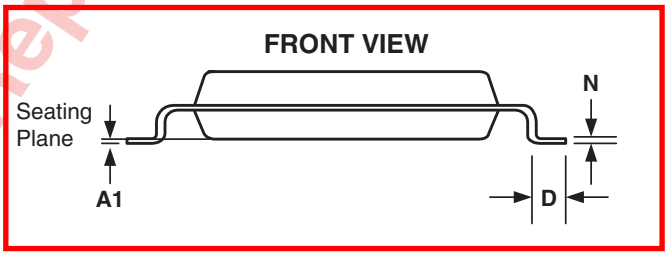
	Title:	Doc No.	Rev.
VOLTERRA	Package Outline - 48 Lead TSSOP	ES AP-0691	1
		Page 1 of 2	

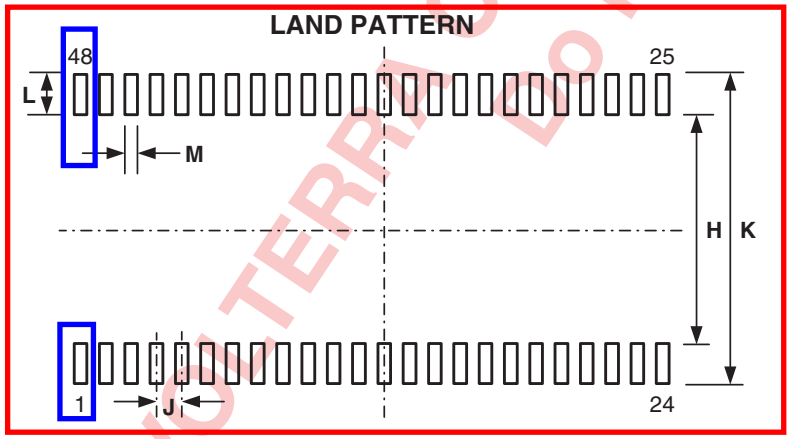


	MILLIMETERS			INCHES*		
DIM	MIN	TYP	MAX	MIN	TYP	MAX
A			1.100			0.0433
A1	0.050		0.150	0.0020		0.0059
C	0.130		0.230	0.0051		0.0091
D	0.500		0.700	0.0197		0.0276
e		0.400			0.157	
E	6.200		6.600	0.2441		0.2598
F	4.300		4.500	0.1693		0.1772
G	9.600		9.800	0.3780		0.3858
H		4.120			0.1622	
J		0.400			0.0157	
K		7.420			0.2921	
L		1.650			0.0650	
M		0.203			0.0080	
N	0.090		0.200	0.0035		0.0079

**Inches provided for reference only.*







Notes
1. Drawings not to scale.
2. Controlling dimensions are in millimeter.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

PACKAGE DIMENSIONS - VT1105S

VOLTERRA	Title: Package Outline - 52 Ball CSP VSC1054 / VSC1072 / VT1105S	Doc No. ES AP-0588	Rev. 1
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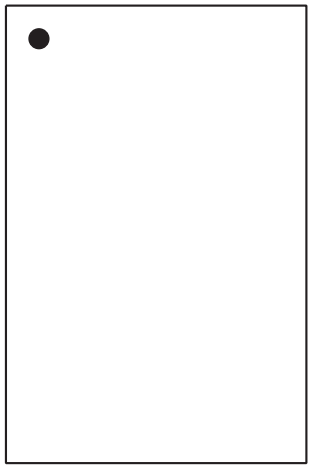
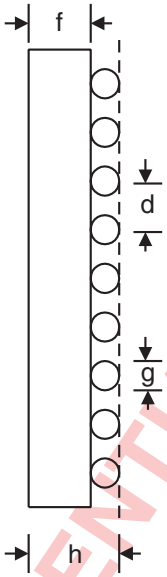
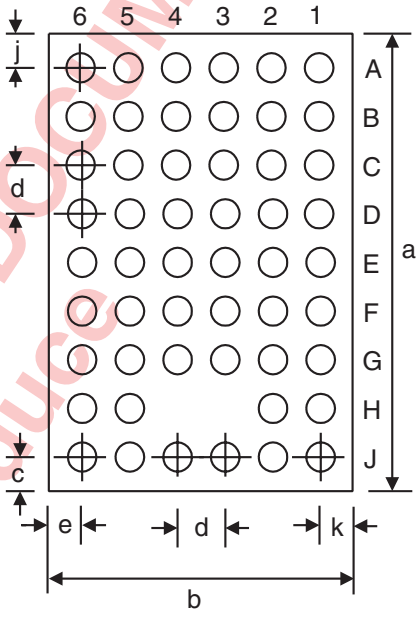
TOP VIEW



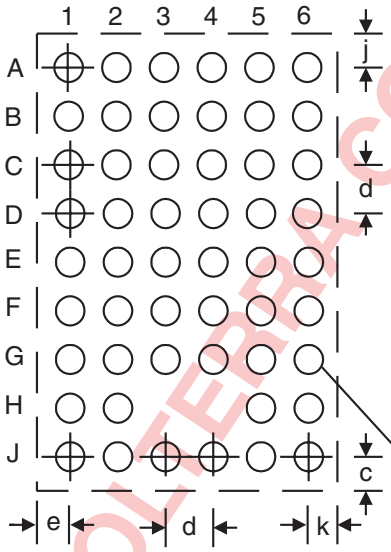
SIDE VIEW



BOTTOM VIEW

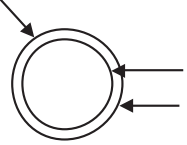


LAND PATTERN



DIM	MILLIMETERS MIN	TYP	MAX	INCHES* MIN	TYP	MAX
a	5.014		5.064	0.1974		0.1994
b	3.174		3.224	0.1250		0.1269
c		0.453			0.0178	
d		0.500			0.0197	
e		0.341			0.0134	
f	0.635		0.685	0.0250		0.0270
g		0.375			0.0148	
h		0.950			0.0374	
j		0.586			0.0231	
k		0.358			0.0141	

** Inches provided for reference only*



TYPICAL PAD DESIGN
0.28mm ±0.05mm Solder Mask Opening
0.350mm Solder Pad Diameter

Notes
1. Drawing not to scale.
2. Controlling dimensions are in millimeters

PACKAGE DIMENSIONS - VT1125S

VOLTERRA	Title: Package Outline - 69 Ball CSP VSC1075 / VT1125S	Doc No. ES AP-0760	Rev. 0
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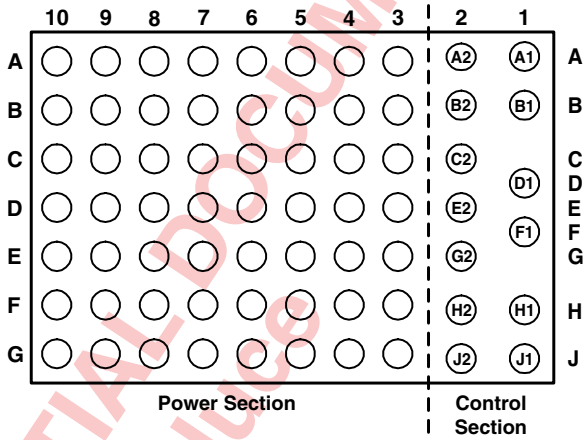
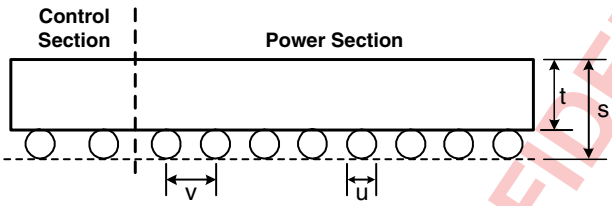
TOP VIEW

BOTTOM VIEW



Note: Rows & columns on the Control Section are NOT on a common grid with the Power Section. See Land Pattern for detailed dimensions.

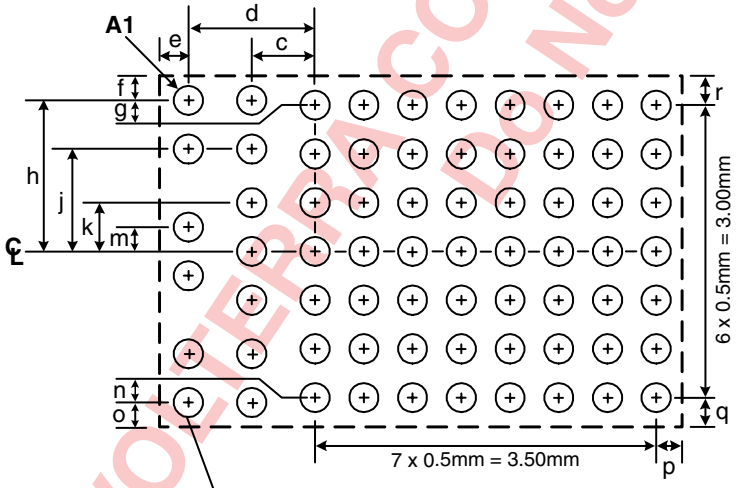
SIDE VIEW



DIM	MILLIMETERS MIN	TYP	MAX	INCHES* MIN	TYP	MAX
a	3.673		3.723	0.1446		0.1466
b	5.503		5.553	0.2167		0.2186
c		0.650			0.0256	
d		1.300			0.0512	
e	0.413		0.463	0.0163		0.0182
f	0.271		0.321	0.0107		0.0126
g		0.075			0.0030	
h		1.575			0.0620	
j		1.075			0.0423	
k		0.500			0.0197	
m		0.250			0.0098	
n		0.075			0.0030	
o	0.226		0.276	0.0089		0.0109
p	0.265		0.315	0.0104		0.0124
q	0.301		0.351	0.0119		0.0138
r	0.346		0.396	0.0136		0.0156
s		0.930			0.0366	
t		0.650			0.0256	
u		0.375			0.0148	
v		0.500			0.0197	

**Inches provided for reference only.*

LAND PATTERN
(Ball Side Down)



TYPICAL PAD DESIGN

Notes
1. Drawing not to scale.
2. Controlling dimensions are in millimeters.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

DATASHEET PHASE DEFINITIONS

PRODUCT PREVIEW: Specifications are to be used as design targets for planning purposes as product is still in development stage.

PRELIMINARY: Specifications are based on limited product and system characterization as product is sampling and has not competed qualification.

NEW PRODUCT: Specifications are based on product and system characterization over all operating conditions as product has passed qualification and released to production.

FINAL: Specifications are based on volume manufacturing data and extensive field data as product has been in production over a year.

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Volterra products have not been designed, tested, or manufactured for use or resale in applications where the failure, malfunction, or any inaccuracy of the products carries a risk of death or serious bodily injury, including, but not limited to, applications such as use in medical devices (as that term is defined in the Medical Device Amendments Act of 1976), use in nuclear facilities, aircraft navigation or communication, emergency systems, or other applications with a similar degree of potential hazard.

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NOTE

Always check with Volterra Semiconductor Corporation for the latest datasheet before completing a design.

North America and Europe Sales
Worldwide Headquarters
Volterra Semiconductor Corporation
3839 Spinnaker Court
Fremont, CA 94538
Tel: +1 (510) 743-1200
Fax: +1 (510) 743-1600
Email: sales@volterra.com

Asia Sales
Volterra Asia Pte. Ltd.
No. 10 Ang Mo Kio Street 65
TechPoint #06-03
Singapore 569059
Tel: +65 6483-2922
Fax: +65 6483-1611
Email: sales@volterra.com

Visit Volterra online at **http://www.volterra.com**