Data Sheet

VT1620A
VinylUSB USB2.0 FS Audio Codec

April 22, 2010
Revision 1.01

Revision History

Rev	Date	Initial	Note
1.0	Dec. 8, 09	TL	Initial external release
1.01	Apr. 22, 10	TL	Corrected typo in functional block diagram Updated legal page

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1 Product Features

VT1620A

VinylUSB USB2.0 FS Audio Codec

- **USB Interface**
  - USB transceiver integrated
  - USB 2.0 full speed compliant
  - USB audio device class specification v1.0 compliant
  - USB Device Firmware Upgrade v1.1 compliant
  - Supports one Control Endpoint, one Isochronous Out Endpoint, one Isochronous In Endpoint, one Feedback Endpoint and one Interrupt Endpoint.
  - Alternative zero bandwidth setting to save USB bus bandwidth while the device in idle status
  - USB HID volume, mute, and GIO support
  - Supports suspend, resume and remote wake-up
  - Adaptive clock generator for audio streaming synchronization
  - USB Feedback endpoint support to enable lossless audio quality
- **MCU**
  - Embedded 8032 with ICE mode support
  - Built-in 16k ROM for firmware; no extra Flash required
  - Optional External Serial Flash for firmware, Max. 64k
  - External Serial Flash for vendor specific VID, PID and Serial Number
- **I²C Interface**
  - Supports both slave mode and master mode
  - Supports wait-states
  - Up to 400 kb/s data transfer rate
- **Audio Capabilities**
  - SPDIF TX audio interface (1 port)
    - Full duplex 16-, 20-, 24-bit mono- or 2-channel
    - 44.1 kHz, 48 kHz, 96 kHz, 192 kHz sampling rates
  - Embedded Audio CODEC
    - ADC SNR 90 dB and THD -80 dB
    - DAC SNR 95 dB and THD -85 dB
    - 2-ch 16/24-bit ADC, supporting 44.1 kHz, 48 kHz, 96 kHz, 192 kHz sampling rates
    - 2-ch 16/24-bit DAC, supporting 44.1 kHz, 48 kHz, 96 KHz, 192 kHz sampling rates
    - Left / Right channel exchange for both ADC and DAC.
    - Noise Gate
    - ALC for ADC
    - Embedded headphone amplifier
- **Audio Device Configuration**
  - MIC-Array: 2-ch microphone
  - MIC-Array & mono speaker: 2-ch microphone & 2-ch stereo output
  - Headset: 1-ch microphone & 2-ch stereo output
  - VoIP: 1-ch microphone & 2-ch stereo output & HID
  - Capless headphone
  - AA path support
- **Specific and General IO Interface**
  - Record-mute LED
  - Device-in-operation LED
  - Buzz output
  - General IO pins
- **Miscellaneous**
  - Single 6-MHz Crystal input with on-chip PLL.
  - USB bus-powered device, with built-in 5-V to 3.3-V and 5-V to 2-V regulator
  - Independent sample rate for playback and recording.

2 Overview

The VT1620A VinylUSB chip is a Universal Serial Bus Audio Codec for intermediate consumer headphone or IP phone applications. It conforms to the USB 2.0 Specification and supports Full-Speed mode. VT1620A supports USB Audio Class 1.0, and hence can enable driverless product. Featuring with S/PDIF TX interface, VT1620A's stereo I/O supports most popular digital audio sampling resolutions. VT1620A requires only one 6-MHz crystal to generate all necessary clock frequencies for internal clock operation. VT1620A also integrates 5-V to 3.3-V and 5-V to 2-V regulator; together with 16-k built-in ROM, it provides customer with extremely cost-competitive BOM solution.

Figure 1 shows the functional block diagram for VT1620A VinylUSB Audio Codec.

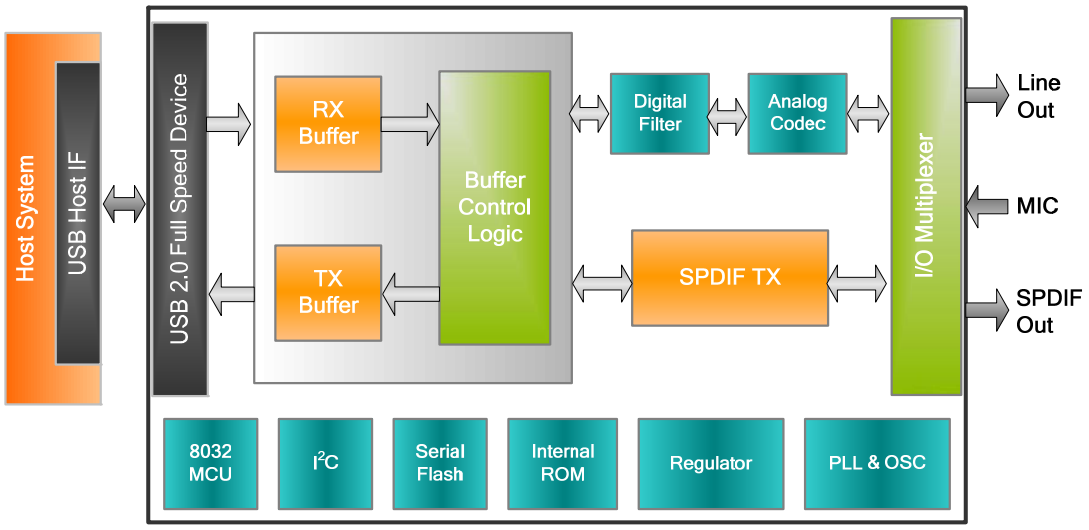


Figure 1 – VT1620A Functional Block Diagram

3 Pinout

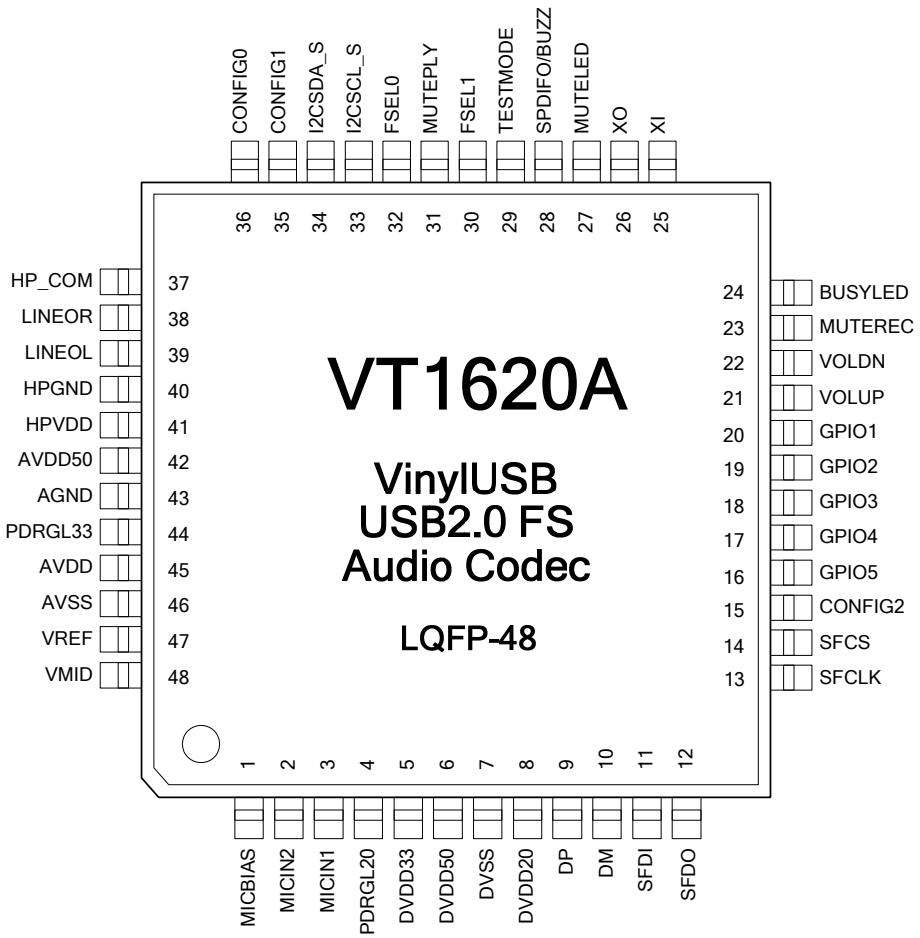


Figure 2 – VT1620A Pin Diagram for LQFP-48 (Top View)

4 Pin List

Table 1 – VT1620A Pin List

Pin	I/O	Pin Name	Pin	I/O	Pin Name	Pin	I/O	Pin Name	Pin	I/O	Pin Name
1	A	MICBIAS	13	O	SFCLK	25	A	XI	37	A	HP_COM
2	A	MICIN2	14	O	SFCS	26	A	XO	38	A	LINEOR
3	A	MICIN1	15	B	CONFIG2	27	B	MUTELED	39	A	LINEOL
4	A	PDRGL20	16	B	GPIO5	28	B	SPDIFO/BUZZ	40	P	HPGND
5	P	DVDD33	17	B	GPIO4	29	I	TESTMODE	41	P	HPVDD
6	P	DVDD50	18	B	GPIO3	30	B	FSEL1	42	P	AVDD50
7	P	DVSS	19	B	GPIO2	31	B	MUTEPLY	43	P	AGND
8	P	DVDD20	20	B	GPIO1	32	B	FSEL0	44	A	PDRGL33
9	A	DP	21	B	VOLUP	33	B	I2CSCL_S	45	P	AVDD
10	A	DM	22	B	VOLDN	34	B	I2CSDA_S	46	P	AVSS
11	I	SFDI	23	B	MUTEREC	35	B	CONFIG1	47	A	VREF
12	O	SFDO	24	B	BUSYLED	36	B	CONFIG0	48	A	VMID

Note:

I = Input;
O = Output
A = Analog
B = Bi-directional
P = Power / Ground

5 Pin Description

5.1 USB Interface

Pin Name	Type	Pin #	Signal Description
DP	A	9	USB Bus DPlus.
DM	A	10	USB Bus DMinus.

5.2 I^2C Interface

Pin Name	Type	Pin #	Signal Description
I2CSCL_S	B	33	I^2C Slaver SCL.
I2CSDA_S	B	34	I^2C Slaver SDA.

5.3 Button & LED Interface

Pin Name	Type	Pin #	Signal Description
VOLUP	B	21	Volume Up.
VOLDN	B	22	Volume Down.
MUTEREC	B	23	Mute Record.
MUTEPLY	B	31	Mute Play.
BUSYLED	B	24	Busy LED.
MUTELED	B	27	Mute LED.

5.4 S/PDIF Interface

Pin Name	Type	Pin #	Signal Description
SPDIFO/BUZZ	B	28	S/PDIF Output Signal; Buzz Output.

5.5 Clock Interface

Pin Name	Type	Pin #	Signal Description
XO	A	26	Clock Out.
XI	A	25	Clock In. 6 MHz.

5.6 SPI Interface

Pin Name	Type	Pin #	Signal Description
SFCS	O	14	Serial Flash Chip Selects. Active-low.
SFDI	I	11	Serial Flash Controller Data Input.
SFDO	O	12	Serial Flash Controller Data Output.
SFCLK	O	13	Serial Flash Clock.

5.7 Codec Interface

Pin Name	Type	Pin #	Signal Description
MICIN1	A	3	Microphone Input 1.
MICIN2	A	2	Microphone Input 2.
MICBIAS	A	1	Microphone Bias.
LINEOR	A	38	Line-out Right.
LINEOL	A	39	Line-out Left.
HP_COM	A	37	Line-out Bias.
VREF	A	47	Reference Voltage Decoupling Capacitor.
VMID	A	48	Mid-rail Voltage Decoupling Capacitor.
PDRGL33	A	44	PD 5 ~ 3.3 V RGL.
PDRGL20	A	4	PD 5 ~ 2.0 V RGL.

5.8 Power & Ground

Pin Name	Type	Pin #	Signal Description
AVDD50	P	42	USB 5 V Power for Analog Part Regulator.
AVDD	P	45	RGL Output for Analog Audio Circuit.
HPVDD	P	41	RGL Output for Headphone Driver Supply.
AVSS	P	46	Analog Ground for Audio Circuit.
AGND	P	43	Reference Ground for Internal Analog Circuit.
DVDD50	P	6	USB 5 V Power for Digital Part Regulator.
DVDD33	P	5	RGL 3.3 V Output for Digital Part.
DVDD20	P	8	RGL 2.0 V Output for Digital Part.
DVSS	P	7	Ground for Digital Part.

5.9 GPIO (General Purpose Input/Output) Interface

Pin Name	Type	Pin #	Signal Description
GPIO[5:1]	B	16; 17; 18; 19; 20	General Purpose Input/Output.
*FSEL[1:0]	B	30; 32	Flash Type Select.
**CONFIG[2:0]	B	15; 35; 36	Device Type Select.

Note:

* Refer to Table 8 – Settings of FSEL [1:0] for VT1620A versus EEPROM Types for detailed EEPROM selection.

** Refer to Table 5 – Settings of CONFIG [2:0] for VT1620A for detailed device type selection.

5.10 Test Mode Interface

Pin Name	Type	Pin #	Signal Description
TESTMODE	I	29	TESTMODE.

6 Memory Map

The 8051 family's memory is organized in a Harvard structure, which means the program memory and data memory are located in the separate address spaces. The 16 address lines can access up to 64k byte space.

6.1 Program Memory Space

Since the 8032 core embedded in VT1620A is a ROMless version of 8051, all the program memories used by VT1620A are considered as "External memory" in the point of view of 8032 core.

Table 2 – Program Memory Space of VT1620A

Byte Address Range	On-chip (Note 1.)	Off-chip (Note 1.)	Size in bytes	Data Access
0x0000 – 0x0FFF	Built-in ROM / EP1/2 Buffer (Note 2.)	Serial Flash	4k	8 bits R/W
0x1000 – 0x3FFF	Built-in ROM	Serial Flash	12k	8 bits R/W
0x4000 – 0xFFFF	--	Serial Flash	48k	8 bits R/W

Note:

1. When boot from ROM is selected by the strapping option, on-chip space will be used as the program memory. When boot from ROM is not selected by the strapping option, off-chip space will be used as the program memory.
2. When updating firmware in the off-chip program memory, EP1/2 SRAM is used as the temporary program memory storage. Under this mode, the lowest 4k address will be mapped to EP1/2 buffer.

6.2 Data Memory Space

The 256 bytes of internal registers and up to 64k bytes of external data memory can be accessed by the 8032 core. (The boundary of internal/external is the 8032 core.)

6.3 MCU Internal Registers

Please refer to the following Table 3 for the memory map of MCU Internal Registers.

Table 3 – Memory Map of MCU Internal Registers

Byte Address Range	On-chip	Off-chip	Size in Bytes	Data Access
0x0000 – 0x001F	4 banks of R0-R7	--	32	8 bits R/W
0x0020 – 0x002F	Bit addressable 0x00-0x7F	--	16	1/8 bits R/W
0x0030 – 0x007F	Rest of lower 128 Direct/indirect addressing	--	80	8 bits R/W
0x0080 – 0x00FF	Upper 128 indirect addressing only	--	128	8 bits R/W
	SFR direct addressing			1/8 bits R/W

6.4 Configuration Registers and Data Memory

Please refer to the following Table 4 for the memory map of Configuration Registers and Data Memory.

Table 4 – Memory Map of Configuration Registers and Data Memory

Byte Address Range	On-chip	Off-chip	Size in bytes	Data Access
0x0000 – 0x00FF	System Configuration	--	256	8 bits R/W
0x0100 – 0x01FF	Interrupt Controller	--	256	8 bits R/W
0x0200 – 0x02FF	USB Controller	--	256	8 bits R/W
0x0300 – 0x03FF	Serial Flash Controller	--	256	8 bits R/W
0x0400 – 0x04FF	Endpoint Data Buffer Controller	--	256	8 bits R/W
0x0500 – 0x05FF	I^2S Audio Controller	--	256	8 bits R/W
0x0600 – 0x06FF	I^2C Controller	--	256	8 bits R/W
0x0700 – 0x07FF	SPDIF Register Set	--	256	8 bits R/W
0x0800 – 0x09FF	RESERVED	RESERVED	512	8 bits R/W
0x0A00 – 0x0AFF	CODEC Register Set	--	256	8 bits R/W
0x0B00 – 0x0DFF	RESERVED	RESERVED	768	8 bits R/W
0x0E00 – 0x0EFF	GPIO Controller	--	256	8 bits R/W
0x0F00 – 0x0FFF	RESERVED	RESERVED	256	8 bits R/W
0x1000 – 0x10FF	UGM	--	256	8 bits R/W
0x1100 – 0x3FFF	RESERVED	RESERVED	8K	8 bits R/W
0x4000 – 0x47FF	EP1 Buffer	--	2k	8 bits R/W
0x4800 – 0x4FFF	EP2 Buffer	--	2k	8 bits R/W
0x5000 – 0xFFFF	RESERVED	RESERVED	44K	8 bits R/W

7 Audio Capabilities

7.1 Multiple Audio Configuration Support

VT1620A integrates two channel audio ADC and two channel audio DAC. VT1620A supports various audio sample rates. Table 5 shows the settings of CONFIG [2:0] that allows VT1620A to be configured for applications of different product categories. Table 6 shows the detailed configuration options of VT1620A.

Table 5 – Settings of CONFIG [2:0] for VT1620A

Configuration	CONFIG2	CONFIG1	CONFIG0
USB Dongle	0	0	0
USB Headset	0	0	1
USB Speaker	0	1	0
USB Microphone	0	1	1
USB MicArray	1	0	0

Note:

USB Dongle is the default configuration. For the values not included in the above table, i.e. 101, 110, and 111, VT1620 will be configured as USB Dongle.

Table 6 – VT1620A Configuration Options

		USB Dongle 2-In/2-Out	**USB Headset** 1-In/2-Out	**USB Speaker** 2-Out	**USB Mic** 2-In	**USB Mic-Array** 2-In/2-Out
Playback	SPDIF	●	N/A	N/A	N/A	N/A
	Channel	Stereo	Stereo	Stereo	N/A	Stereo
	Sample Rate/ Bit Width	44.1/48k 16 bit 44.1/48k 24 bit 96k 16 bit 96k 24 bit 192k 16 bit	44.1/48k 16 bit 44.1/48k 24 bit 96k 16 bit 96k 24 bit 192k 16 bit	44.1/48k 16 bit 44.1/48k 24 bit 96k 16 bit 96k 24 bit 192k 16 bit	N/A	44.1/48k 16 bit
Record	Channel	Stereo	Mono	N/A	Stereo	Stereo
	Sample Rate/ Bit Width	44.1/48k 16 bit 44.1/48k 24 bit 96k 16 bit 96k 24 bit	44.1/48k 16 bit 44.1/48k 24 bit 96k 16 bit 96k 24 bit	N/A	44.1k/48k 16 bit	44.1k/48k 16 bit
A-A Path		●	●	N/A	N/A	N/A
Mic-Array		N/A	N/A	N/A	N/A	●
HID		●	●	●	N/A	●

7.2 Audio Topologies

The following Figure 3 to
Figure 7 illustrate the audio topologies of VT1620A, including USB dongle, USB headset, USB speaker, USB microphone, and USB Mic-Array.

7.2.1 USB Dongle

VT1620A supports volume control (-40 dB ~ 0 dB) and mute control for speaker output path; MIC boost (+20 dB), volume control (0 ~ 30 dB), and mute control for microphone input path; volume control (0 ~ 30 dB) and mute control for AA path in the USB dongle application.

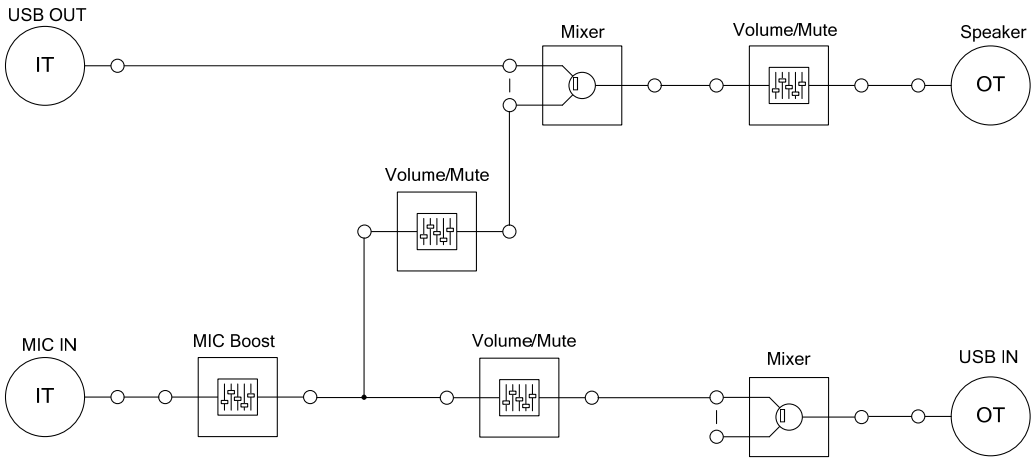


Figure 3 – Audio Topology of USB Dongle

7.2.2 USB Headset

The topology of the USB headset is the same as the USB dongle.

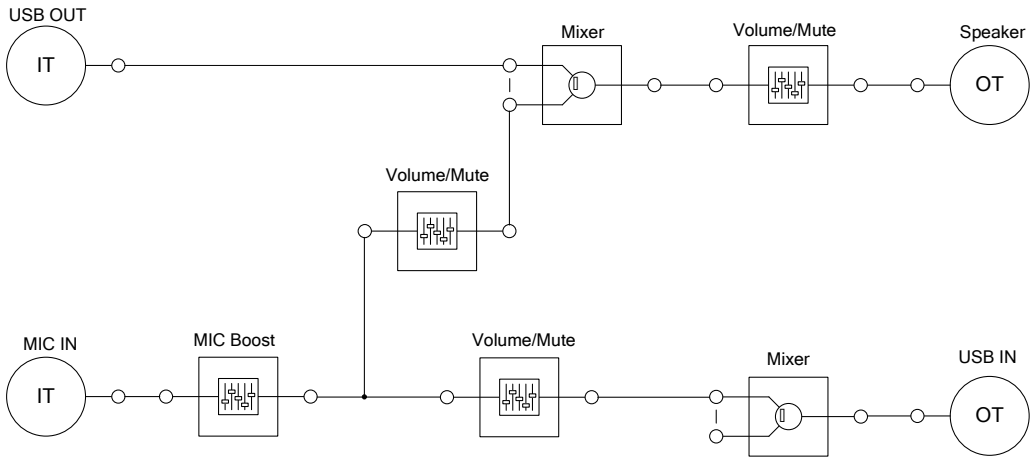


Figure 4 – Audio Topology of USB Headset

7.2.3 USB Speaker

VT1620A supports volume control (-40 dB ~ 0 dB) and mute control in the USB speaker application.

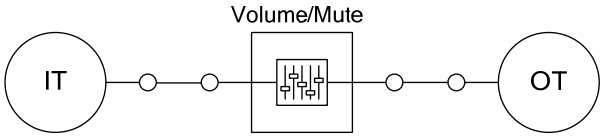


Figure 5 – Audio Topology of USB Speaker

7.2.4 USB Microphone

VT1620A supports the volume control (0 dB ~ 30 dB) and mute control functions in the USB microphone application.

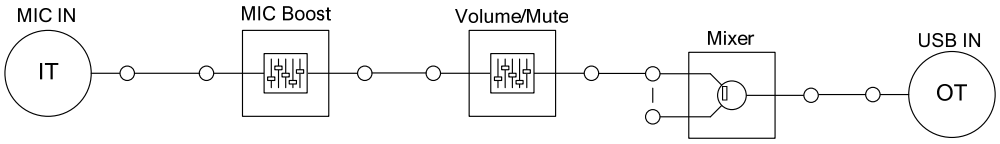
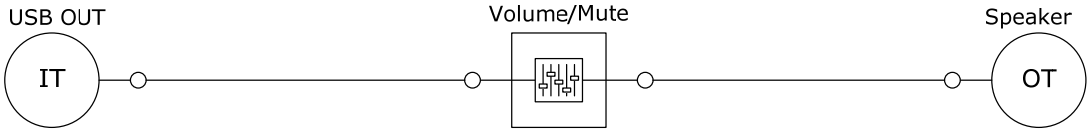


Figure 6 – Audio Topology of USB Microphone

7.2.5 USB Mic-Array

VT1620A supports volume control (-40 dB ~ 0 dB), and mute control for the speaker output path; MIC boost (+20 dB), volume control (0 ~ 30 dB), and mute control for microphone input path in the USB Mic-Array application.



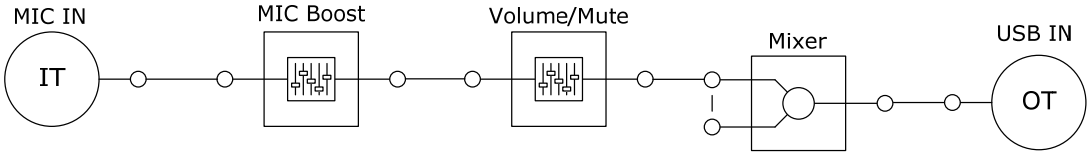


Figure 7 – Audio Topology of USB Mic-Array

7.3 Default Microphone Array Geometry Descriptor

Please refer to the following Table 7 for the register summary information of Microphone Array.

Table 7 – Microphone Array Information

Offset	Field	Size	Value	Description
0	guidMicArrayID	16 bytes	07FE86C1-8948-4db5-B184-C5162D4AD314h	A unique ID that marks the beginning of the microphone array information in the memory.
16	wDescriptorLength	2 bytes	003Ch	The length in bytes of the microphone array information, including the GUID and length fields.
18	wVersion	2 bytes	0100h	The version number of the microphone array specification, followed by this descriptor.
20	bmMicArrayType	2 bytes	0000h	The microphone array type. When the following bits are set to one, it indicates the associated array type: D0: Linear. D1: Planar. D2: 3D. D15...3: Reserved
22	wWorkVertAngBeg	2 bytes	0000h	The start of the work volume vertical angle.
24	wWorkVertAngEnd	2 bytes	0000h	The end of the work volume vertical angle.
26	wWorkHorAngBeg	2 bytes	DDE9h	The beginning of the work volume horizontal angle.
28	wWorkHorAngEnd	2 bytes	2217h	The end of the work volume horizontal angle.
30	wWorkFreqBandLo	2 bytes	0050h	The lower bound of the work frequency range.
32	wWorkFreqBandHi	2 bytes	1D4Ch	The upper bound of the work frequency range.
34	wNumberOfMics	2 bytes	0002h	The number of individual microphone definitions that follow.
36	wMicrophoneType(0)	2 bytes	0000h	A number that uniquely identifies the type of microphone 0: 00: Omni-Directional 01: SubCardioid 02: Cardioid 03: SuperCardioid 04: HyperCardioid 05: 8 Shaped 0F - FF: Vendor defined
38	wXCoordinate(0)	2 bytes	0000h	The x-coordinate of microphone 0.
40	wYCoordinate(0)	2 bytes	FFCEh	The y-coordinate of microphone 0.
42	wZCoordinate(0)	2 bytes	0000h	The z-coordinate of microphone 0.
44	wMicVertAngle(0)	2 bytes	0000h	The main response axis (MRA) vertical angle of microphone 0.
46	wMicHorAngle(0)	2 bytes	0000h	The MRA horizontal angle of microphone 0.
48	wMicType(1)	2 bytes	0000h	A number that uniquely identifies the type of microphone 1: 00: Omni-Directional 01: SubCardioid 02: Cardioid 03: SuperCardioid 04: HyperCardioid 05: 8 Shaped 0F - FF: Vendor defined
50	wXCoordinate(1)	2 bytes	0000h	The x-coordinate of microphone 1.
52	wYCoordinate(1)	2 bytes	0032h	The y-coordinate of microphone 1.
54	wZCoordinate(1)	2 bytes	0000h	The z-coordinate of microphone 1.
56	wMicVertAngle(1)	2 bytes	0000h	The MRA vertical angle of microphone 1.
58	wMicHorAngle(1)	2 bytes	0000h	The MRA horizontal angle of microphone 1.

Note:

1. The offset and size values are in bytes.

2. All angles are expressed in the units of 1/10000 radians. For example, 0.8727 radians is expressed as 8727 (0x2217). The value can range from -31416 to 31416, inclusive.

3. X-y-z coordinates are expressed in millimeters. The value can range from 32767 to 32767, inclusive.

4. The coordinate system's orientation, axes, and the positive directions of the angles are shown in the following Figure 8.

5. Frequency values are expressed in Hz. The range of frequency values is bounded only by the size of the field and assumes that only typical values are used.

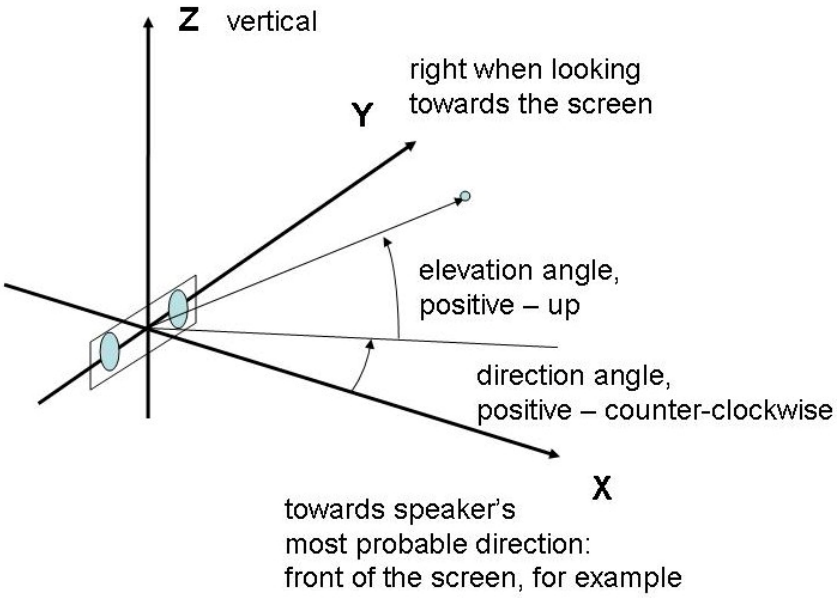


Figure 8 – Microphone Array Coordinate System

7.4 Default Manufacturer String

- Default Manufacturer String: VIA Technologies Inc.

7.5 Default Product String

- USB Dongle: VIA USB Dongle
- USB Headset: VIA USB Headset
- USB Speaker: VIA USB Speaker
- USB Microphone: VIA USB Microphone
- USB Mic-Array: VIA USB MicArray

7.6 User Customization

The manufacturer can change default VID/PID, manufacturer string, product string, serial number string, and microphone array geometry descriptor (for USB Mic-array configuration only) by an external EERPOM. Table 8 shows the settings of FSEL [1:0] for VT1620A versus EEPROM types. The EEPROM data structure is defined in Table 9.

Table 8 – Settings of FSEL [1:0] for VT1620A versus EEPROM Types

EEPROM Type	FSEL1	FSEL0
Internal ROM, without EEPROM	0	0
Internal ROM, with EEPROM of 1-byte address	0	1
Internal ROM, with EEPROM of 2-byte address	1	0
Internal ROM, with EEPROM of 3-byte address	1	1

Note:

According to the size of EEPROM, the address can be 1 byte, 2 bytes, or 3 bytes. For example, usually the EEPROM of 2k-bit or less uses 1-byte address, and the EEPROM of 1M-bit or more uses 3-byte address.
For the EEPROM of 1-byte address, FSEL=01
For the EEPROM of 2-byte address, FSEL=10
For the EEPROM of 3-byte address, FSEL=11

If no customized information is needed, FSEL should be set to 00.

Table 9 – EEPROM Data Structure

Byte Index		Description
0		Magic Number1: “V”, 0x56
1		Magic Number2: “T”, 0x54
2		Total Data Length Low Byte
3		Total Data Length High Byte
4		Bit [3:0]: System Configuration Bit [4]: 1 — — Support remote wakeup; 0 — — Not support remote wakeup Bit [7:5]: Reserved.
5		Reserved
VID Info	6	If Byte 7 Bit [7] == 1, Byte 6 is the offset Bit [7:0] of VID low byte in EEPROM, and VID high byte is the next byte after VID low byte. If Byte 7 Bit [7] == 0, Byte6 is reserved.
	7	If Byte 5 Bit [7] == 1, Byte 7 Bit [6:0] is the offset Bit [14:8] of VID low byte. If Byte 5 Bit [7] == 0, Byte 7 Bit [6:0] is reserved. Bit [7]: 1 —— There is VID in EEPROM; 0 —— No VID in EEPROM
PID Info	8	If Byte 9 Bit [7] == 1, Byte 8 is the offset Bit [7:0] of PID low byte in EEPROM, and PID high byte is the next byte after PID low byte. If Byte 9 Bit [7] == 0, Byte 8 is reserved.
	9	If Byte 9 Bit [7] == 1, Byte 9 Bit [6:0] is the offset Bit [14:8] of PID low byte. If Byte 9 Bit [7] == 0, Byte 9 Bit [6:0] is reserved. Bit [7]: 1 —— There is PID in EEPROM; 0 —— No PID in EEPROM

Byte Index		Description
Device String Info	10	If Byte 11 Bit [7] == 1, Byte 10 is the offset Bit [7:0] of Product string in EEPROM. If Byte 11 Bit [7] == 0, Byte 10 is reserved.
	11	If Byte 11 Bit [7] == 1, Byte 11 Bit [6:0] is the offset Bit [14:8] of Product string. If Byte 11 Bit [7] == 0, Byte 11 Bit [6:0] is reserved. Bit [7]: 1 —— There is Product string in EEPROM; 0 —— No Product string
	12	If Byte 11 Bit [7] == 1, Byte 12 is the length of Product string. If Byte 11 Bit [7] == 0, Byte 12 is reserved.
	13	Reserved
Vendor String Info	14	If Byte 15 Bit [7] == 1, Byte 14 is the offset Bit [7:0] of Manufacturer string. If Byte 15 Bit [7] == 0, Byte 14 is reserved.
	15	If Byte 15 Bit [7] == 1, Byte 15 Bit [6:0] is the offset Bit [14:8] of Manufacturer string. If Byte 15 Bit [7] == 0, Byte 15 Bit [6:0] is reserved. Bit [7]: 1 —— There is Manufacturer string in EEPROM; 0 —— No Manufacturer string
	16	If Byte 15 Bit [7] == 1, Byte 16 is the length of Manufacturer string. If Byte 15 Bit [7] == 0, Byte 16 is reserved.
	17	Reserved
SN Info	18	If Byte 19 Bit [7] == 1, Byte 18 is the offset Bit [7:0] of Serial Number. If Byte 19 Bit [7] == 0, Byte 18 is reserved.
	19	If Byte 19 Bit [7] == 1, Byte 19 Bit [6:0] is the offset Bit [14:8] of Serial Number. If Byte 19 Bit [7] == 0, Byte 19 Bit [6:0] is reserved. Bit [7]: 1 —— There is Serial Number in EEPROM; 0 —— No Serial Number
	20	If Byte 19 Bit [7] == 1, Byte 20 is the length of Serial Number. If Byte 19 Bit [7] == 0, Byte 20 is reserved.
	21	Reserved
Mic-Array Info	22	If Byte 23 Bit [7] == 1, Byte 22 is the offset Bit [7:0] of Microphone Array geometry descriptor. If Byte 23 Bit [7] == 0, Byte 22 is reserved.
	23	If Byte 23 Bit [7] == 1, Byte 23 Bit [6:0] is the offset Bit [14:8] of Microphone Array geometry descriptor. If Byte 23 Bit [7] == 0, Byte 23 Bit [6:0] is reserved. Bit [7]: 1 —— There is Microphone Array geometry descriptor in EEPROM; 0 —— No Microphone Array geometry descriptor
	24	If Byte 23 Bit [7] == 1, Byte 24 is the length of Microphone Array geometry descriptor. If Byte 23 Bit [7] == 0, Byte 24 is reserved.
	25	Reserved
Structure of Patch Register	n	Register Index Low Byte
	n+1	Register Index High Byte
	n+2	Register Patch State
	n+3	Register Content

8 Clock and Crystal Networks

8.1 External Clock Source or Crystal Networks

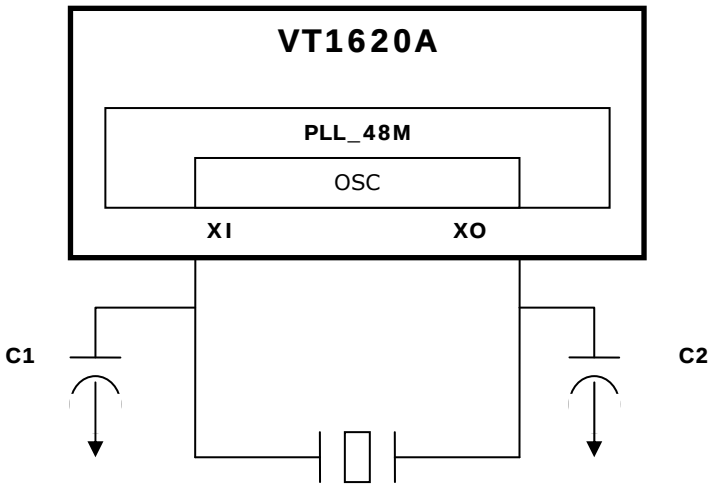
The VT1620A needs one external clock source or crystal networks:

- A 6-MHz clock (or crystal network) provides the fundamental input clock source for the VT1620A. A PLL_48M module takes this 6-MHz clock input, and generates a 48-MHz clock output which is the root of all VT1620A clocks. In this PLL_48M module, an Oscillator and a PLL are integrated together.
- There are two PLLs (PLL24576 and PLL112896) in the system that utilizes the 24-MHz clock source. They use the 48-MHz clock output from PLL_48M divided by 2. The purpose of these two PLLs is to provide clock source for the VT1620A Codec related circuitry to generate accurate clocks for all kinds of popular Audio sample rates.
- PLL24576 generates the 245.76-MHz clock output, base on this clock, the bit clock and 128-fs over sampling clock can be generated for 16-kHz, 48-kHz, 96-kHz, 192-kHz sample rate audio recording.
- PLL112896 generates the 112.896-MHz clock output; base on this clock, the bit clock and 128-fs over sampling clock can be generated for the 44.1-kHz sample rate audio recording.
- All the clocks for the rest functional blocks are generated from the 48-MHz clock.
- The VT1620A can also take the 24.576-MHz and 11.2896-MHz clock directly from the external source. However, this is the backup solution in case there is any problem to generate these two clocks internally.

The Strapping Option Bit [3] determines whether the source of the 6-MHz input clock is supplied by an external clock source or by an external crystal network.

When the Strapping Option value is a one, then an external 6-MHz clock source should drive the XI signal pin of the VT1620A, while the XO signal pin of the VT1620A should be left as No Connection. In such case, the built-in OSC in PLL_48M module will be bypassed and stopped.

When the Strapping Option value is a zero, then the following external 6-MHz crystal network is recommended to provide the 6-MHz clock source for the VT1620A:



C1: 12 pF
C2: 12 pF
Crystal: 6 MHz

Figure 9 – VT1620A Clock and Crystal Networks

8.2 Internal Clock Generation

The following Figure 10 illustrates the clocks generated in the system.

The divisors A to I are all even number clock divisors. They are software programmable. Together with the clock gating control units, VT1620A clock generator module provides FW with methods to fully control each clock and thus enable flexible system support for different applications.

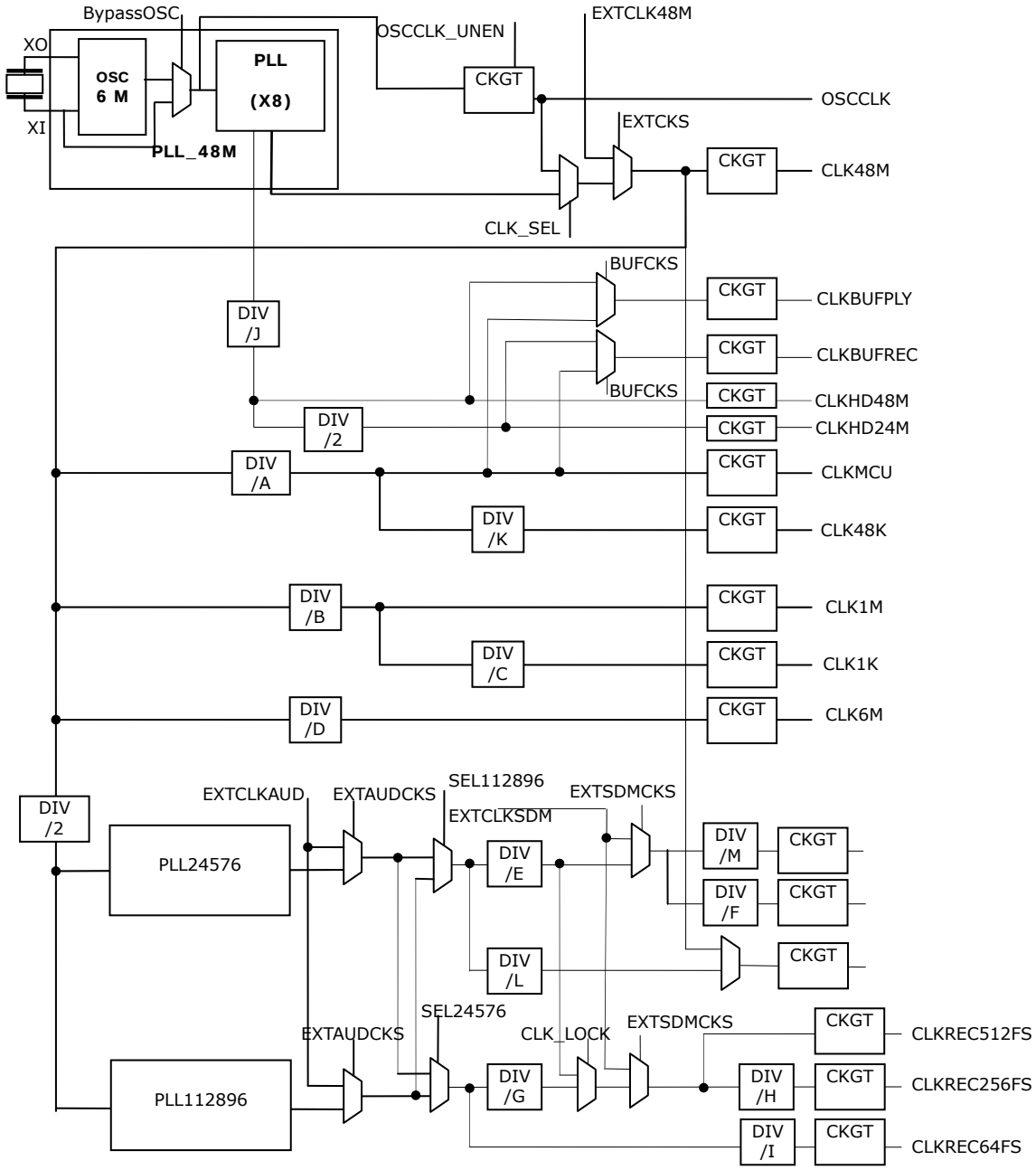


Figure 10 – VT1620A Clock Generator

8.3 Clock Divisor Settings

Refer to the following Table 10 for VT1620A clock divisor settings.

Table 10 – Clock Divisor Settings

Divisor	Clock Division Range	Adaptive Clock	Default Setting	Default Clock Frequency
A	1, 2, 4, 6, …… 62	No	4	12 MHz
B	1, 2, 4, 6, …… 62	No	48	1 MHz
C	1, 2, 4, 6, …… 510	No	256	3.9 kHz
D	1, 2, 4, 6, …… 62	No	8	6 MHz
E	5, 10, 20, 30, …… 310	Yes	10	24.576 MHz
F	1, 2, 4, 6, …… 62	No	4	6.144 MHz
G	5, 10, 20, 30, …… 310	No	10	24.576 MHz
H	1, 2, 4, 6, …… 62	No	2	12.288 MHz
I	5,10,20,30,……310	No	8	3.072 MHz
J	8	Yes	8	48 MHz
K	250	No	250	48 kHz
L	10	No	10	12.288 MHz
M	1, 2, 4, 6, …… 62	No	2	12.288 MHz

9 Electrical Specification

9.1 Absolute Maximum Ratings

Condition	MIN	MAX
Supply Voltage AVDD50, DVDD50.	-0.3 V	6V
Voltage Range Analog Input	AGND-0.3 V	AVDD + 0.3 V
Operating Temperature Range ,TA	-25 °C	+85 °C
Storage Temperature after Soldering	0 °C	+125 °C
ESD (HBM)	2 kV	

9.2 Recommended Operating Conditions

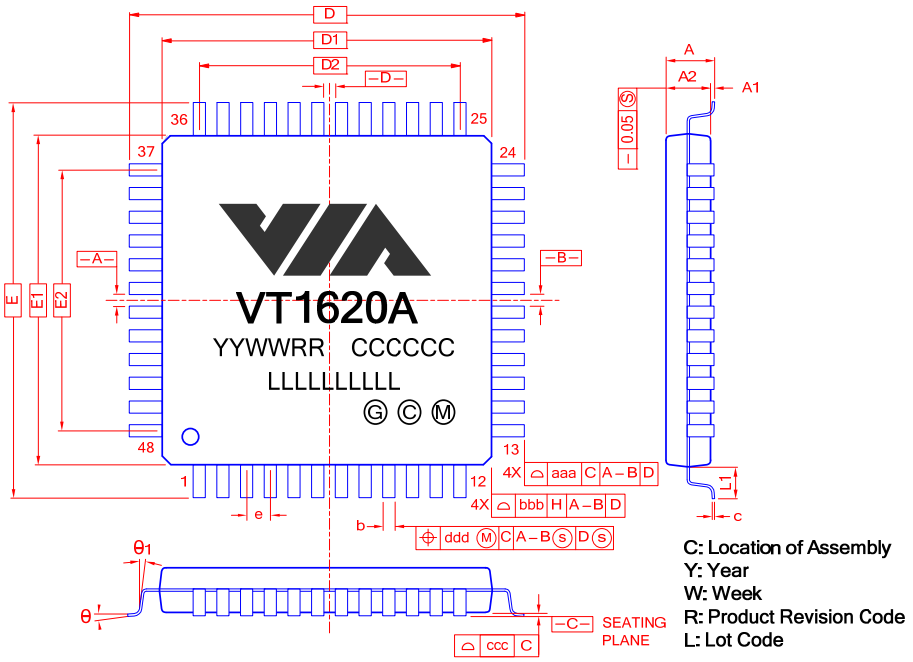
Parameter	Symbol	MIN	NOM	MAX	Unit
Analog Supply Voltage	AVDD50.	4.4	5	5.25	V
Digital Supply Voltage	DVDD50	4.4	5	5.25	V
Analog Supply Voltage	AVDD, HPVDD, DVDD33	3.13	3.3	3.47	V
Digital Supply Voltage	DVDD20	1.9	2.0	2.1	V
Operating Temperature Range	TA	0	25	85	°C

9.3 Electrical Parameters

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Unit
Analog Inputs (MIC INPUT1, MIC INPUT2, to ADC out						
Full Scale Input Signal Level (for ADC 0 dB Input at 0 dB Gain)	VINFS	AVDD=HPVDD = 3.3V		1.0		V rms
Input Resistance		MIC INPUT1 to ADC, MIC BOOST Gain = 0 dB		55		kΩ
		MIC INPUT1 to ADC, MICBOOST Gain = +30 dB		3.4		
Input Capacitance				10		pF
Signal to Noise Ratio (A-weighted)	SNR	AVDD=HPVDD = 3.3 V		90	92	dB
Dynamic Range		-60 dBFs		90	92	dB
Total Harmonic Distortion	THD	-1 dBFs Input, AVDD=HPVDD = 3.3V		-80		dB
ADC Channel Separation		1 kHz Signal		94		dB

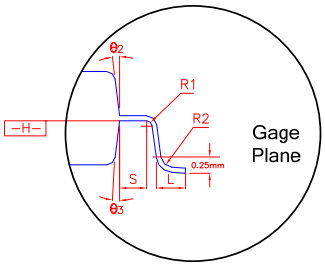
Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Unit
Analog In to Analog Outputs (LOUT, ROUT)						
0 dB Full Scale Output Voltage				HPVDD/ 3.3		Vrms
Mute Attenuation		1 kHz, Full Scale Signal		96		dB
Channel Separation		Analog in to Analog out		100		dB
Signal to Noise Ratio (A-weighted)	SNR	AVDD=HPVDD = 3.3 V		97		dB
Total Harmonic Distortion	THD	AVDD=HPVDD = 3.3V		-91		dB
DAC to Line-Out (LOUT with 10 k~ / 50 pF Load)						
Signal to Noise Ratio (A-weighted)	SNR	AVDD=HPVDD = 3.3 V		95		dB
Total Harmonic Distortion	THD	AVDD=HPVDD = 3.3 V	55	-85		dB
Channel Separation		10 kHz Signal		93		dB
DAC to Headphone Output (LOUT/ROUT, Using Capacitors)						
Output Power per Channel	PO	Output power is highly correlated with THD.				
Total Harmonic plus Noise	THD+N	HPVDD=3.3 V, RL=32~ , -3 dBFS Input (FS=515 mV)		-85		
		HPVDD=3.3 V, RL=16~ , -3 dBFS Input (FS=334 mV)		-82		
Signal to Noise Ratio (A-weighted)	SNR	HPVDD = 3.3 V		95		dB
Channel Separation		10 kHz Signal		66		dB
Analogue Reference Levels						
USB Bus Power	VBUS		4.4	5	5.25	V
Middle Rail Reference Voltage	VMID		–3%	AVDD/HPVDD	+3%	V
Buffered Reference Voltage	VREF		–3%	AVDD/HPVDD	+3%	V
Microphone Bias						
Bias Voltage	VMICBIAS	3 mA Load Current	–5%	0.9×AVDD	+ 5%	V
Bias Current Source	IMICBIAS				3	mA
Output Noise Voltage	Vn	1 k to 20 kHz		15		nV/~Hz
Digital Input / Output						
Input HIGH Level	VIH		0.7×DVDD33			V
Input LOW Level	VIL				0.3×DVDD33	V
Output HIGH Level	VOH	IOL=1 mA	0.9×DVDD33			V
Output LOW Level	VOL	IOH-1 mA			0.1×DVDD33	V

10 Mechanical Specification



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	–	–	1.60	–	–	0.063
A1	0.05	–	0.15	0.002	–	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BSC.			0.354 BSC.		
D1	7.00 BSC.			0.276 BSC.		
E	9.00 BSC.			0.354 BSC.		
E1	7.00 BSC.			0.276 BSC.		
R1	0.08	–	–	0.003	–	–
R2	0.08	–	0.20	0.003	–	0.008
Θ	0°	3.5°	7°	0°	3.5°	7°
Θ1	0°	–	–	0°	–	–
Θ2	11°	12°	13°	11°	12°	13°
Θ3	11°	12°	13°	11°	12°	13°
c	0.09	–	0.20	0.004	–	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	–	–	0.008	–	–
48L						
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	5.50			0.217		
E2	5.50			0.217		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		



NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 11 – VT1620A LQFP-48 Package (7 mm×7 mm)

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