Data Sheet

VT1702S
High Definition Audio Codec

November 13, 2009

Preliminary Revision 1.0

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1 Product Features

VT1702S

High Definition Audio Codec

1.1 Hardware Features

- **Compliant with Intel High Definition Audio Specification Rev. 1.0**
- **Exceeds Microsoft Windows Logo Program (WLP 3.10) Requirements**
- **Two stereo digital-to-analog converters**
  - 16-, 20-, 24-bit resolution
  - Audio sampling rates: 48 kHz, 96 kHz, 192 kHz, 44.1 kHz, and 88.2 kHz
  - DAC SNR: 100 dB
  - THD+N: 85 dB
- **Two stereo analog-to-digital converters**
  - 16-, 20-, 24-bit resolution
  - Audio sampling rates: 48 kHz, 96 kHz, 192 kHz, and 44.1 kHz
  - ADC SNR: 98 dB
  - THD+N: 80 dB
- **One stereo digital microphone**
  - Supports mono and stereo interface
  - 16-, 20-, 24-bit resolution
  - Sampling rates: 16 kHz, 32 kHz, 44.1 kHz, and 48 kHz
- **Two independent SPDIF output channels; the second is for digital audio output to a HDMI transmitter**
  - Supports 16-, 20-, 24-bit data format
  - Sampling rates: 48 kHz, 96 kHz, 192 kHz, 44.1 kHz, and 88.2 kHz
- **Jack presence detection**
  - Two jack detection pins; each detects up to four jacks plugging
  - Jack-detect circuit with unsolicited response
- **Analog microphone**
  - Software selectable boost gain (10/20/30 dB) for analog microphone input
  - 3 sets of adjustable Vref Out pins for microphone bias.
- **Supports external analog PCBEEP input**
- **Hardware volume control**
- **High performance analog mixer for AA-path**
- **Four general-purpose IO (GPIO) pins for customized applications**
- **Supports External Amplifier Power Down (EAPD)**
- **HPF in ADC path for DC removal**
- **Supports 1.5 ~ 3.3V I/O for HD audio link**
- **Optimized management for Pop Mitigation**
- **Supports cap-less headphone on Port A**
- **Functionality of pins:**
  - Line Out, Headphone
    - Pins 39 and Pin 41 (Port A)
  - Line In, Microphone
    - Pin 21 and Pin 22 (Port B)
    - Pin 23 and Pin 24 (Port C)
    - Pin 16 and Pin 17 (Port F)
  - Line Out
    - Pin 35 and Pin 36 (Port D)
- **Package**
  - Available in 48-Pin LQFP lead-free Package

1.2 Software Features

- **Meets Microsoft WLK1.2 and conforms to the requirements of Windows Hardware Quality Labs testing (WHQL)**

- **Functions of Speaker Device**
  - Equalizer (EQ)
  - Room Correction (RC)
  - Bass Management (BM)
  - Environment Modeling (EM)
  - Loudness Equalization (LE)
  - Speaker Fill (SF)

- **General features for Mic-Array Application**
  - Acoustic Echo Cancellation (AEC)
  - Noise Suppression (NS)
  - Beam Forming (BF)

- **Recording Control for Microphone Input**

- **Digital Output Control UI**

- **VIA Vendor Driver Support**

- **Supports various operating systems**
  - Microsoft Windows 2000
  - Microsoft Windows Server 2003
  - Microsoft Windows XP
  - Microsoft Windows Vista (32-bit/64-bit)
  - Microsoft WinCE4.2 / 5.0 / 6.0
  - Linux (Fedora Core 7, 8 / Suse SLED Desktop 10SP1 / UBUNTU 7.1 / Redhat)

- **Optional Sound Effect**
  - QSound 3D audio effects
  - DTS CONNECT / DTS Surround Sensation
  - Dolby[1] PCEE program
  - Creative audio program
  - 3rd party Microphone Array technology

- **Optional Software Feature**
  - Karaoke Mode for Home Entertainment
  - Dynamic range control with adjustable parameters

[1] Supply of this Implementation of Dolby technology does not convey a license nor imply a right under any patent, or any other industrial or intellectual property right of Dolby Laboratories, to use this Implementation in any finished end-user or ready-to-use final product. It is hereby notified that a license for such use is required from Dolby Laboratories.

2 Overview

The VT1702S is a low power, high-fidelity High Definition Audio Codec that is designed for laptops. It integrates the 4-channel digital-to-analog converters (DAC) and 4-channel analog-to-digital converters (ADC). It is compatible with Intel High Definition Audio specification, and conforms to or exceeds Microsoft Windows Logo Program (WLP3.10) requirements.

The VT1702S features two independent stereo DACs, and two independent stereo ADCs. Both of them can support sound resolution up to 24 bits and sample rates up to 192 kHz. A high quality analog mixer is used to support A-A path. It can achieve 100 dB Signal-to-Noise Ratio (SNR) for DACs and 98 dB SNR for ADCs.

The VT1702S provides one stereo digital microphone interface that supports 16 kHz, 32 kHz, 44.1 kHz, and 48 kHz sampling rate. The stereo ADCs and microphone array can support Acoustic Echo Cancellation (AEC), Beam Forming (BF), and Noise Suppression (NS) technologies. The hardware volume control function provides a wide range of gain control and audio signals. The VT1702S also features two independent SPDIF output channels for use of consumer audio applications. The second is for digital audio output to a HDMI transmitter. The SPDIF transmitters support sampling rates of 44.1 kHz, 48 kHz, 88.2 KHz, 96 kHz, and 192 kHz. The VT1702S uses two jack detection pins for presence detection on up to eight audio jacks. This function allows software to determine if there is a device plugged into the circuit.

The analog microphone input features three sets of adjustable Vref Out pins for microphone bias, and can be programmed with 10-dB, 20-dB, and 30-dB boost gain by Vendor driver. VT1702S features high-pass-filter (HPF) in analog-to-digital converter (ADC) path for removing DC offset signals. VT1702S supports 1.5V and 3.3V HDA signaling. In addition, VT1702S supports Capless Headphone feature that eliminates the need for external capacitors and saves the board space and cost.

The VT1702S is embedded with software utilities such as environment emulation, EQ, extender, and the optional sound effects, including QSound, DTS Connect, Dolby Digital Live, Dolby PCEE program, and Creative audio program. VT1702S is available in a 48-Pin LQFP Pb-free and RoHS compliant package. VT1702S is a high quality audio solution that provides outstanding performance and design flexibility.

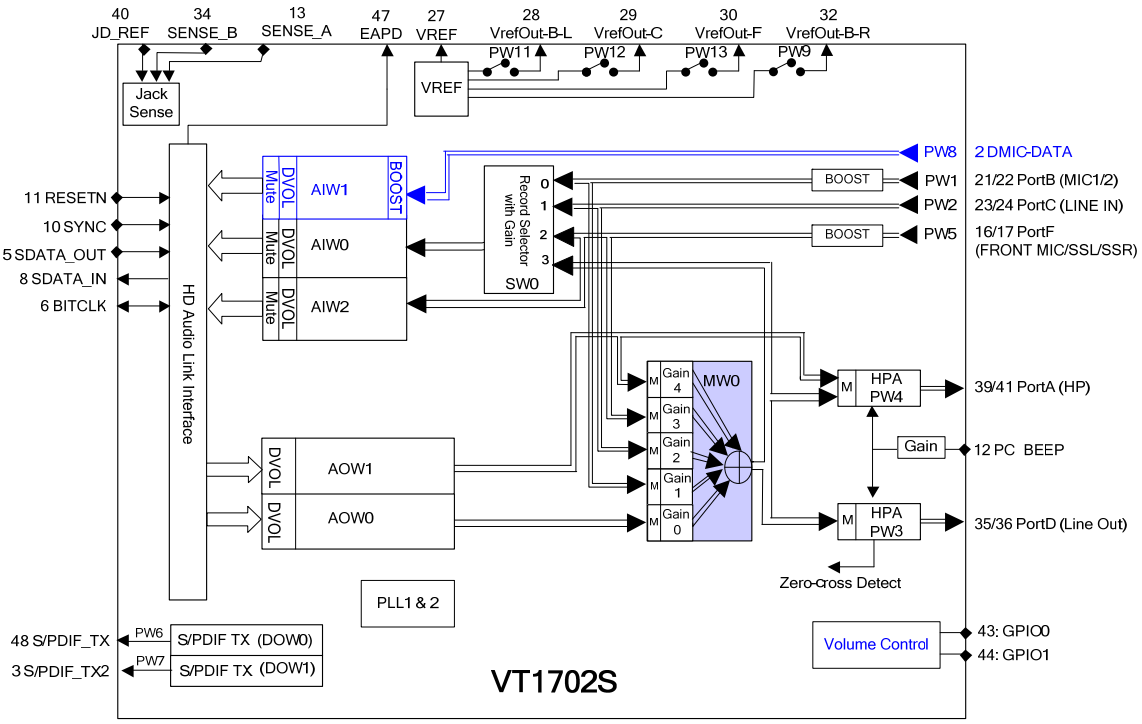


Figure 1 – VT1702S Functional Block Diagram

3 Pinout

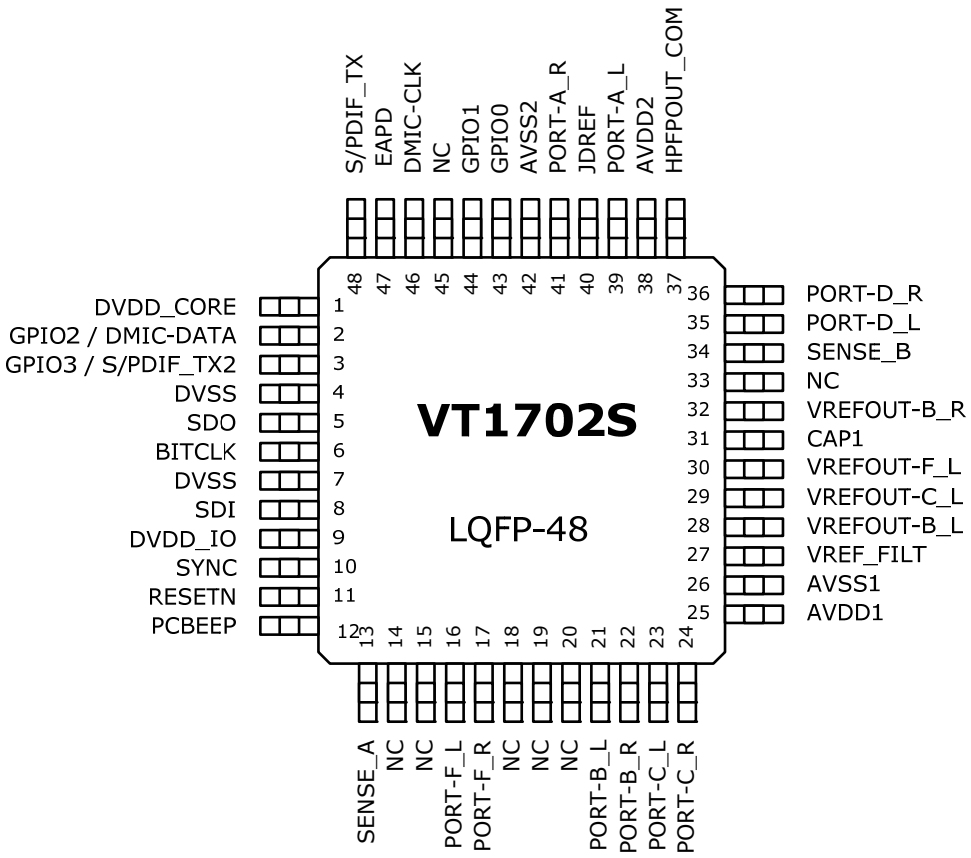


Figure 2 – VT1702S Pin Diagram for LQFP-48 (Top View)

4 Pin List

Table 1 – VT1702S Pin List

Pin	Pin Name	Pin	Pin Name
1	DVDD_CORE	25	AVDD1
2	GPIO2 / DMIC-DATA	26	AVSS1
3	GPIO3 / S/PDIF_TX2	27	VREF_FILT
4	DVSS	28	VREFOUT-B_L
5	SDO	29	VREFOUT-C_L
6	BITCLK	30	VREFOUT-F_L
7	DVSS	31	CAP1
8	SDI	32	VREFOUT-B_R
9	DVDD_IO	33	NC
10	SYNC	34	SENSE_B
11	RESETN	35	PORT-D_L (Front Left)
12	PCBEEP	36	PORT-D_R (Front Right)
13	SENSE_A	37	HPFPOUT_COM
14	NC	38	AVDD2
15	NC	39	PORT-A_L (HP Left)
16	PORT-F_L (Front MIC)	40	JDREF
17	PORT-F_R (Front MIC)	41	PORT-A_R (HP Right)
18	NC	42	AVSS2
19	NC	43	GPIO0
20	NC	44	GPIO1
21	PORT-B_L (MIC)	45	NC
22	PORT-B_R (MIC)	46	DMIC-CLK
23	PORT-C_L (LINE IN L)	47	EAPD
24	PORT-C_R (LINE IN R)	48	S/PDIF_TX

5 Pin Description

Table 2 – Signal Type Definitions

Type	Description
I	**Input.** Standard input-only signal.
O	**Output.** Standard active output driver.
I/O	**Input/output.** An input/output signal.

5.1 Digital I/O Pins

Pin Name	Pin #	I/O	Signal Description
GPIO2 / DMIC-DATA	2	IO	General Purpose Input/Output 2 / PDM Data from Digital Microphone
GPIO3 / S/PDIF_TX2	3	IO	General Purpose Input/Output 3 / The Second S/PDIF Output
SDO	5	I	Serial Data Input from Controller
BITCLK	6	I	24MHz Bit Clock from Controller
SDI	8	IO	Serial Data Output to Controller
SYNC	10	I	Sample SYNC from Controller
RESETN	11	I	Hardware Reset from Controller
GPIO0	43	IO	General Purpose Input/Output 0
GPIO1	44	IO	General Purpose Input/Output 1
DMIC-CLK	46	O	Clock Output to Digital Microphone
EAPD	47	O	External Amplifier Power-Down
S/PDIF_TX	48	O	S/PDIF Output

5.2 Analog I/O Pins

Pin Name	Pin #	I/O	Signal Description
SENSE_A	13	I	Jack Detect Pin 1
SENSE_B	34	I	Jack Detect Pin 2
HPFPOUT_COM	37	O	Analog Output for Capless Headphone Driver
PORT-A_L	39	O	Analog Output for HP Out Left
PORT-A_R	41	O	Analog Output for HP Out Right
PORT-F_L	16	I	Analog Input for front MIC
PORT-F_R	17	I	Analog Input for front MIC
PORT-B_L	21	I	Analog Input for MIC1 Left
PORT-B_R	22	I	Analog Input for MIC1 Right
PORT-C_L	23	I	Analog Input for Line-in Left
PORT-C_R	24	I	Analog Input for Line-in Right
PORT-D_L	35	O	Analog Output for Line-out Left
PORT-D_R	36	O	Analog Output for Line-out Right
PCBEEP	12	I	PC Beep Signal Input
VREF_FILT	27	O	Reference Voltage Capacitor
VREFOUT-B_L	28	O	Reference Voltage Output for Port B (L)
VREFOUT-C_L	29	O	Reference Voltage Output for Port C
VREFOUT-F_L	30	O	Reference Voltage Output for Port F
CAP1	31	O	Optional Capacitor for ADC Reference
VREFOUT-B_R	32	O	Reference Voltage Output for Port B (R)
JDREF	40	O	External Resistor for Jack Detect Circuit

5.3 Power and Ground

Pin Name	Pin #	I/O	Signal Description
DVDD_CORE	1	P	Digital Core Power. 3.3V
DVDD_IO	9	P	Digital Power for HDA Link: 3.3V ~ 1.5V
DVSS	4	P	Digital VSS
DVSS	7	P	Digital VSS
AVDD1	25	P	Analog VDD
AVDD2	38	P	Analog VDD
AVSS1	26	P	Analog VSS
AVSS2	42	P	Analog VSS

6 High Definition Audio Link Protocol

6.1 Link Signaling

The link protocol defines the digital serial interface that connects High Definition Audio codec to the audio controller, and is not compatible with the previous AC97 protocol. The link is controller synchronous, based on a fixed 24MHz BITCLK and is purely isochronous without any flow control.

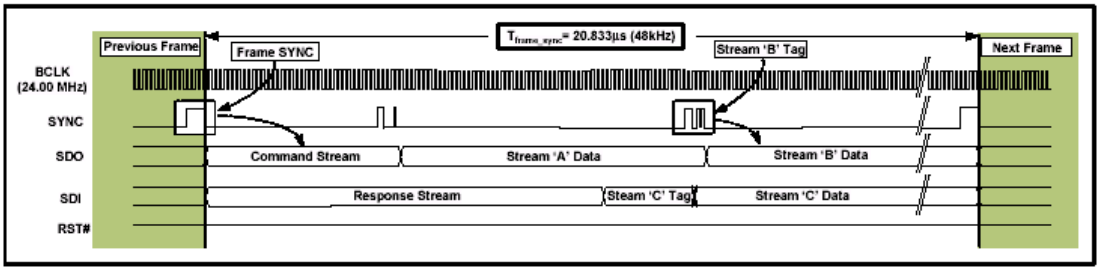


Figure 3 – High Definition Audio Link Conceptual View

6.2 Signal Definitions

Table 3 – High Definition Audio Link Conceptual View

Signal Name	Source	Type	Description
BITCLK	Controller	I	24MHz clock.
SYNC	Controller	I	Global 48KHz Frame Sync and outbound tag signal.
SDO	Controller	I	Bussed serial data output from controller.
SDI	Codec & controller	I/O	Point-to-point serial data. Controller has a weak pull down.
RESETN	Controller	I	Global active low reset signal.

BITCLK is the 24MHz clock sourced from the controller and connecting to all codec on the link.

SYNC marks input and output frame boundaries (Frame Sync) as well as identifying outbound data streams (stream tags). SYNC is always sourced from the controller and connects to all codec on the link.

SDO is driven by the controller to all codec on the link. Compared with AC97, the SDO is double pumped with respect to both rising and falling edges of BITCLK in order to increase the bandwidth required for High Definition Audio link.

SDI is a point-to-point data signal driven by the codec to the controller. Because the bandwidth requirement is not that high compared to SDO, data is single pumped with respect to only the rising edge of BITCLK. The controller is required to implement weak pull-down on all SDI signals.

RESETN is sourced from the controller and connects to all codec on the link. Assertion of RESETN results I null link interface logic being reset to Default power on state.

The following figure shows the timing diagram of BITCLK, SYNC, SDO and SDI.

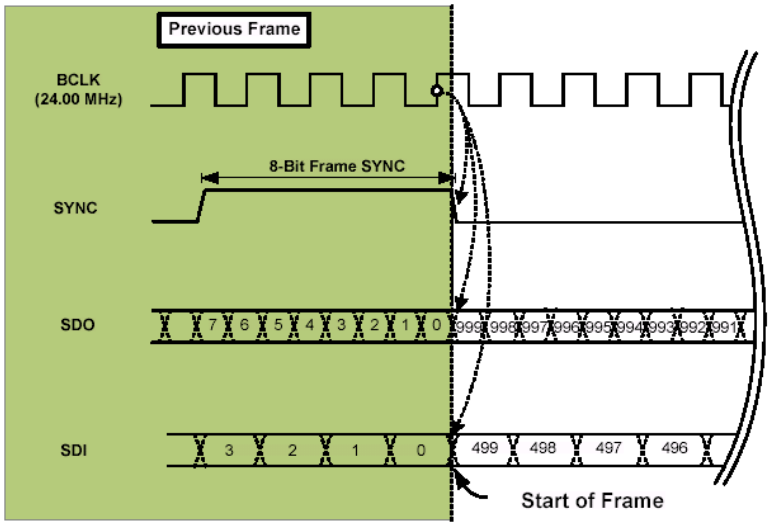


Figure 4 – Bit Timing Diagram

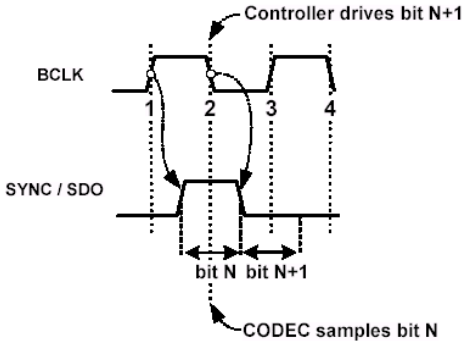


Figure 5 – SYNC and SDO Timing Relative to BITCLK

Figure 5 shows that both SYNC and SDO may be toggled with respect to either edge of BITCLK. In particular, bit cell n+1 is driven by the controller on SDO with respect to clock edge #2, and is sampled by the codec with respect to the subsequent clock edge, #3, and so forth.

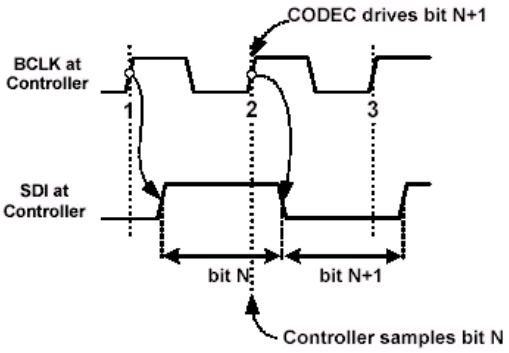


Figure 6 – SDI Timing Relative to BITCLK

Figure 6 shows that SID may only be toggled with respect to the rising edge of BITCLK. In particular, bit cell n+1 is driven by the codec on SDI with respect to rising clock edge #2 and is sampled by the controller with respect to the subsequent rising clock edge, #3, and so forth.

6.3 Signaling Topology

The following diagram shows a typical system with one controller and its associated codec.

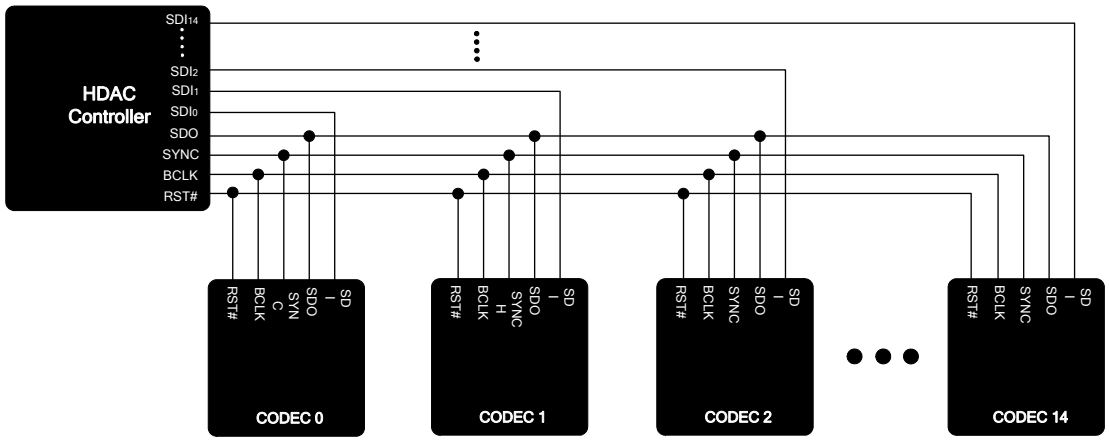


Figure 7 – Basic High Definition Audio System

6.4 Frame Composition

A frame is defined as a 20.833us window of time marked by the falling edge of the Frame Sync marker, which identifies the start of each frame. The controller is responsible for generating the Frame Sync marker, which is a high-going pulse on SYNC, exactly four BITCLK in width.

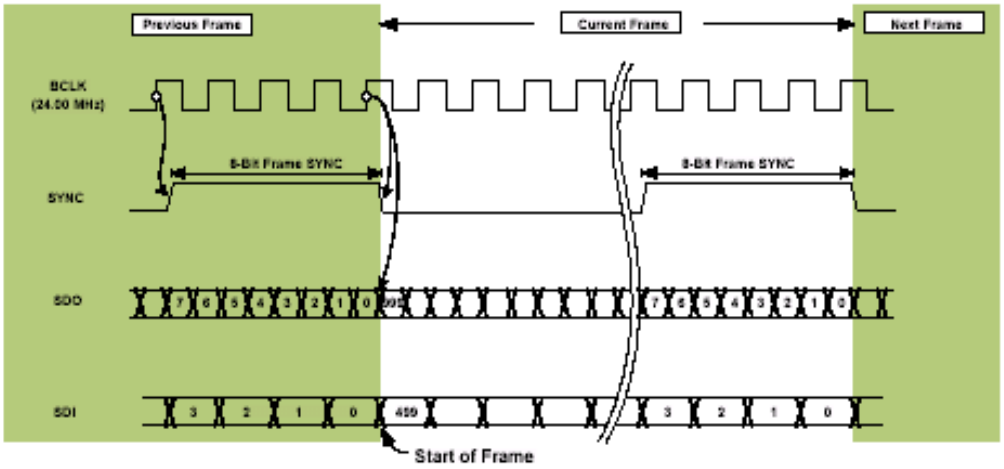


Figure 8 – Frames Demarcation

Both inbound and outbound frames are made up of three major components, specifically:

- A single Command / Response Field
- Zero or more Stream Packets
- A Null Field to fill out the frame

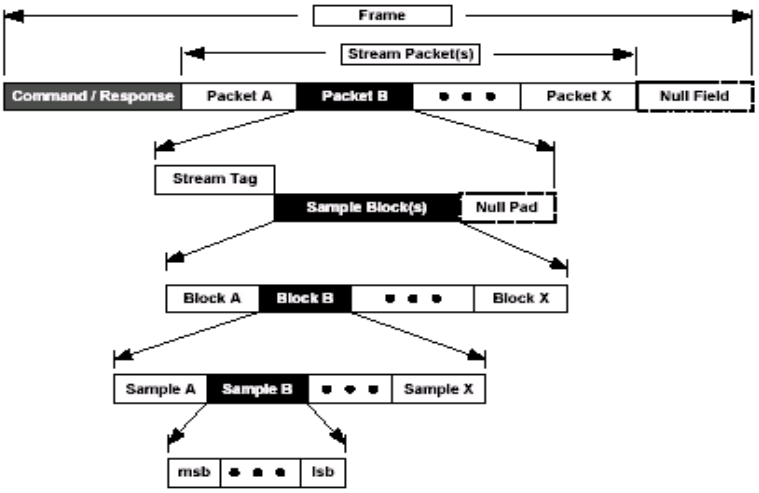


Figure 9 – Frame Composition

Command / Response Field is used for link and codec management. One of these fields appears exactly once per frame, MSB first, and is always the first field in the frame. It is composed of a 40-bit Command Field on each outbound frame from the controller and a 36-bit Response Field on each inbound frame from the codec.

Stream Tag is the label at the beginning of each stream packet that provides the associated stream ID. All data in one stream packet belongs to a single stream.

Sample Block is a set of one or more samples, the number of which is specified by the "Channels" field of the Stream Descriptor Format registers. Samples in a given sample block are associated with a single given stream, have the same sample size, and have the same time reference. And no padding is permitted between samples.

Ordering of samples within a block is always the same for all blocks in a given stream.

Sample is a set of bits providing a single sample point of a single analog waveform.

Null Field is used to fill up the remainder of the bits in each frame that are not used for Command / Response or packets. A null field must be transmitted as logical 0's.

6.5 Output Frame

6.5.1 Stream Tags

Outbound stream tags are 8 bits in length and are transmitted at a double pumped rate as side band information on SYNC. It is composed of a 4-bit preamble which is signaled as three SDO bit times high followed by one SDO bit time low. This is immediately followed by a 4-bit Stream ID. Outbound stream tags are transmitted on SYNC so as to align with the last eight data bits of the preceding stream packet or Command Field.

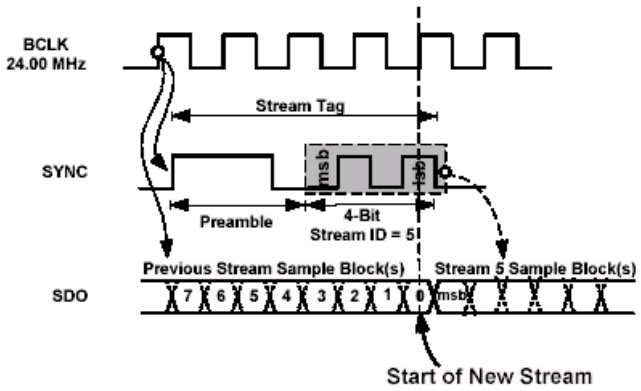


Figure 10 – Outbound Stream Tag Format and Transmission

6.5.2 Outbound Frames

Outbound frames start and end between the falling edges of successive Frame Syncs. The first 40 bits are dedicated for the Command field and are sued to send commands to codec. The controller transmits the tag for the first outbound packet on SYNC during the last eight bit times of the Command field. The sample blocks for the first packet are transmitted on SDO immediately following the Command field. There's no proscribed order in which the different stream packets are to be transmitted. Controllers are required to transmit a null field fro the remaining bits within an outbound frame when the transmission of the stream packets completes before the end of the frame.

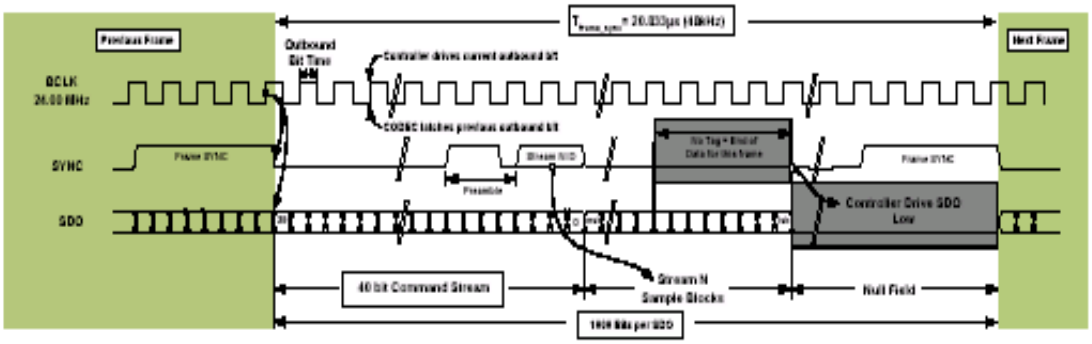


Figure 11 – Outbound Frame with Null Field

6.6 Input Frame

6.6.1 Stream Tags

An inbound stream tag is 10 bits in length, and is transmitted "in-line" at a single pumped rate on SDI, immediately preceding the associated inbound sample blocks. It is composed of a 4-bit stream ID, followed by a 6-bit data length field that provides the length, in bytes, of all sample blocks with the given stream packet.

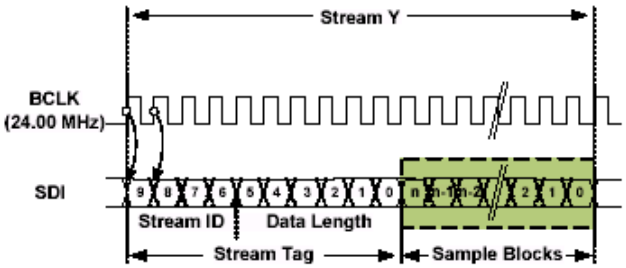


Figure 12 – Inbound Tag Format and Transmission

6.6.2 Inbound Frames

Inbound frames start and end between the falling edges of successive Frame Syncs. The first 36 bits of an inbound frame are dedicated for the Response Field, which codec use for sending responses to controller commands. The codec transmits the first stream packet on SID immediately following the Response Field. A stream tag indicating a packet length of zero must immediately follow the last stream packet to be transmitted. Such a stream tag marks the completion of data transmission within that frame, and the remaining valid bit positions are set to the null field. In the event there are less than 10 valid bit positions remaining in the frame after the last stream packet, then no termination tag is transmitted, and the remaining bits are the null field.

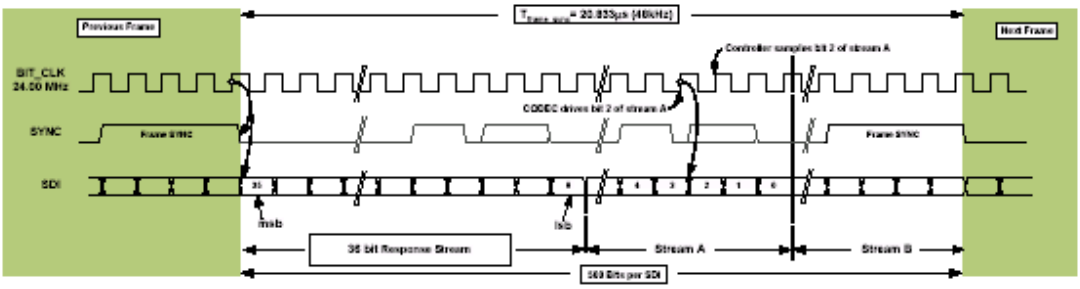


Figure 13 – Inbound Frame with No Null Field

6.7 Reset and Initialization

6.7.1 Link Reset

A link reset is signaled on the link by assertion of the RESETN signal, and results in all Link interface logic in both codec and controller, including registers, being initialized to their Default state. The controller drives all SDO and SYNC outputs low when entering or exiting link reset.

A controller may only initiate the link reset entry sequence after completing any currently pending initialization or state change requests.

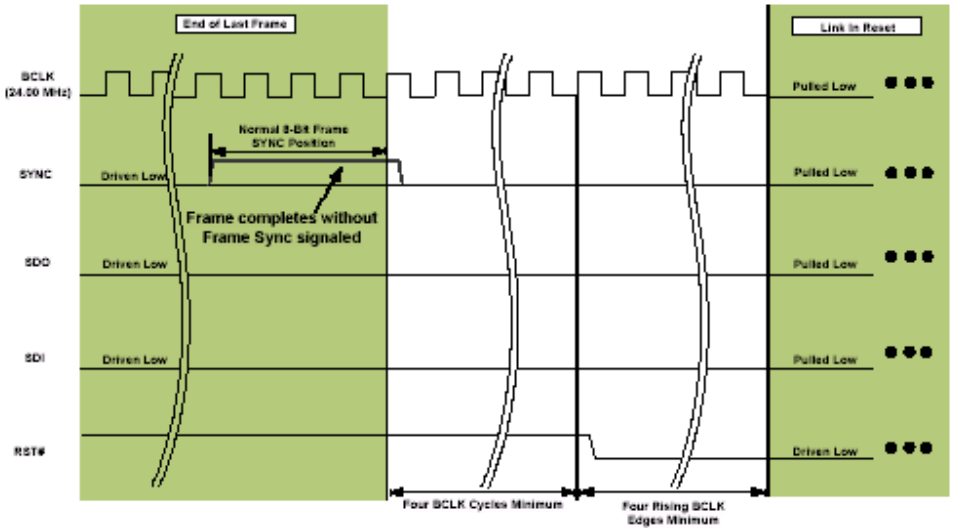


Figure 14 – Link Reset Entry Sequence

The sequence when entering link reset is described in the following.

1. The controller synchronously completes the current frame but does not signal Frame Sync during the last eight SDO bit times.
2. The Controller synchronously asserts RESETN four or more BITCLK cycles after the completion of the current frame.
3. BITCLK is stopped a minimum of four clocks after the assertion of RESETN.

In the event of a host bus reset, the above sequence does not complete, and RESETN is asynchronously asserted immediately and unconditionally.

Regardless of the reason for entering Link Reset, it may be exited only under software control and in a synchronous manner.

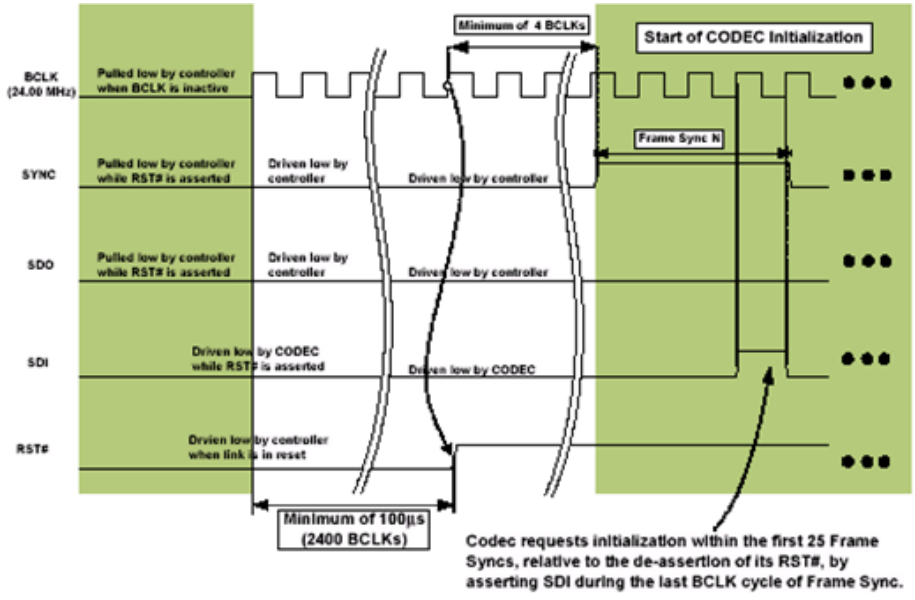


Figure 15 – Link Reset Exit Sequence

The sequence when exiting link reset is described in the following.

1. The controller provides a properly running BITCLK for a minimum of 100us (2400 BITCLK cycles or more) before the de-assertion of RESETN. This allows time for codec PLLs to lock.
2. The RESETN signal is de-asserted.
3. The SYNC commences signaling valid frames on the link with the first Frame Sync generating at a minimum of four BITCLK cycles after the de-assertion of RESETN.
4. The codec must signal an initialization request via SID within the first 25 Frame Syncs relative to the de-assertion of their respective RESETN signal.

6.7.2 Codec Function Group Reset

A codec function group reset is initiated via the Function_Reset verb and results in all logic within the targeted function group being driven to its Default or reset state. By Default VT1702S does not signal a state change and initialization request on SDI after the Function_Reset verb, and still keeps its codec address previously assigned by the controller. This behavior can be changed by setting a vendor defined register bit for backward compatible with the Rev. 0.7 Azalia Spec. See the Vendor Defined verbs in the Audio Function Group for the detail.

6.7.3 Codec Initialization

Immediately following the completion of Link Reset sequence (or Function_Reset verb, if enabled by the vendor-defined verb), VT1702S proceed through a codec initialization sequence, which is provide each codec with a unique address by which it can thereafter be referenced with Commands on the SDO signal. During this sequence, the controller provides each requesting codec with a unique address using its attached SDI signals.

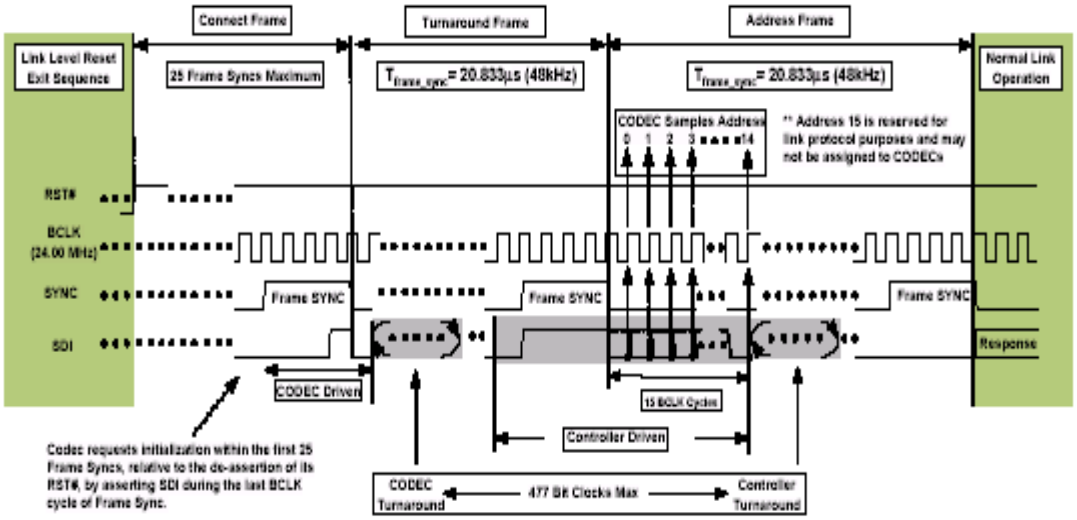


Figure 16 – Codec Initialization Sequence

The codec initialization sequence occurs across three contiguous frames immediately following any reset sequence. During these three frames, codec are required to ignore all outbound traffic present on SYNC & SDO. These three frames, labeled the “Connect Frame”, the “Turnaround Frame”, and the “Address Frame”, are described below.

6.7.3.1 Connect and Turnaround Frames

In the Connect and Turnaround Frames, the codec signals its request for initialization on SDI and then releases SDI (turnaround) to be driven by the controller in the subsequent address frame.

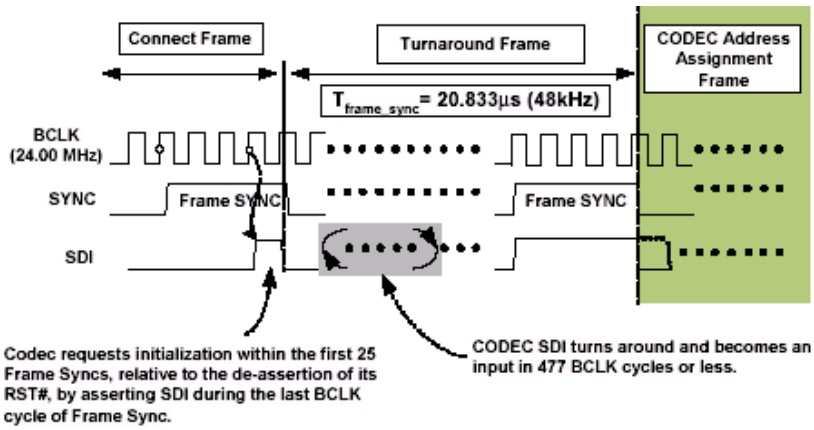


Figure 17 – Connect and Turnaround Frames

The codec signals an initialization request by synchronously driving SDI high during last bit clock cycle of Frame Sync. SDI must be asserted for the entire BITCLK cycle and must be synchronously de-asserted o the same rising edge of BITCLK as the de-assertion of the Frame Sync. The codec are only permitted to signal an initialization request on a null input frame, a frame in which no response stream or input streams are being sent.

In the Turnaround Frame, codec and controllers are required to turn SDI around upon the completion of the Connect Frame. To do this, the codec actively drives SDI low for one BITCLK cycle immediately following the de-assertion of SYNC at the end of the Connect Frame. The codec then puts its SDI drivers in a high impedance state at the end of the first BITCLK cycle in the Turnaround Frame. Four BITCLK cycles before the end of the Turnaround Frame, SYNC and SID are driven high by the controller. The SDI remains driven high through the end of the Turnaround Frame in preparation for the subsequent address frame.

6.7.3.2 Address Frames

During the Address Frame, SDI is a codec input and is driven by the controller beginning in the last four BITCLK periods (Frame Sync) of the Turnaround Frame. The falling edge of Frame Sync marks the start of codec address assignment. Address assignment is indicated by the controller holding each SDI high for the number of BITCLK cycles equal to the numeric ID of that particular SDI. Thus the unique address of the codec becomes the ID of its attached SDI.

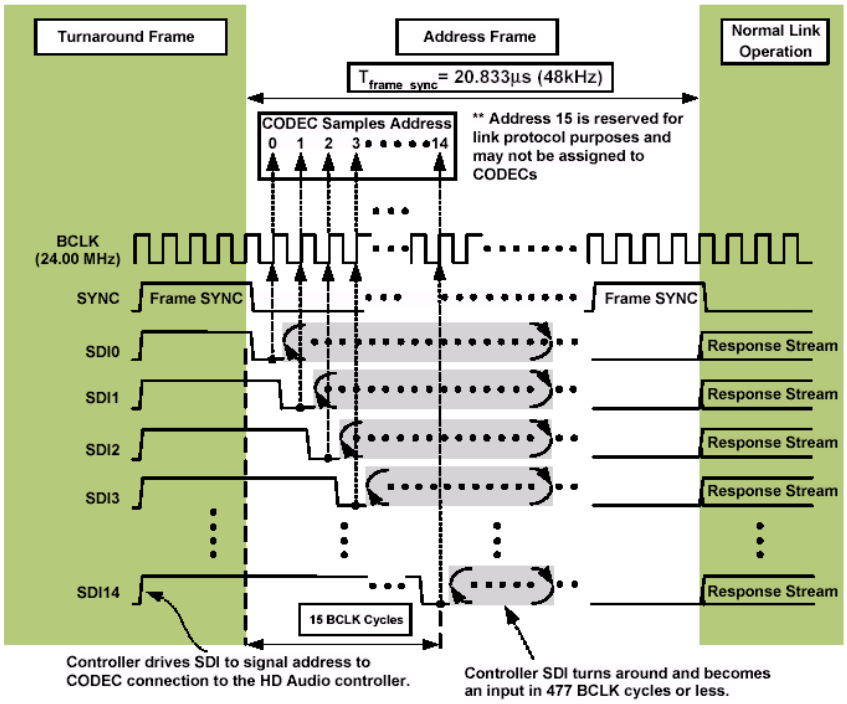


Figure 18 – Address Frame

Codec count from zero to fourteen starting on the rising edge of BITCKL following the de-assertion of Frame Sync, and sample the value of this count for their unique address on the first rising edge of BITCLK in which SYNC and SDI are both sampled low.

The controller must put its SDI drivers in a high impedance state by the rising edge of the 18th BITCLK of the address frame but not before driving each SDI low for at least one clock cycle. The SDI then becomes an input to the controller. Normal link operation starts on the frame following the completion of the Address Frame, and the codec is required to actively drive a valid response field and to be ready to accept commands in this and subsequent frames.

6.8 Handling Stream Independent Sample Rates

Unlike AC97, the Link is source synchronous and has no codec initiated flow control, the controller generates all sample transfer timing.

6.8.1 Codec Sample Rendering Timing

VT1702S supports the all the multiples and submultiples of the base rates of 48 kHz and 44.1 kHz, up to the maximum rate respectively of the DAC and ADC. For DAC, up to 192 kHz sample rate is supported. For ADC, the maximum rate is 96 kHz.

Table 4 – Sample Rate Supported

Multiple	Base Rate 48 kHz	Base Rate 44.1 kHz
1/6	8 kHz	
1/4		11.025 kHz
1/3	16 kHz	
1/2		22.05 kHz
2/3	32 kHz	
1	48 kHz	44.1 kHz
2	96 kHz	88.2 kHz
4	192 kHz	176.4 kHz

6.8.2 Link Sample Delivering Timing

For streams whose sample rate is a natural harmonic of 48 kHz, the timing is relatively straightforward. The rates in multiple (N) of 48 kHz are containing N sample blocks in one frame. For the rates in sub-multiple (1/N) of 48 kHz, there must be one sample block transmitted every one in N frames, and the intervening N-1 frames will contain no sample for this stream.

Since the link frame rate is fixed at 48 kHz, streams using a base rate of 44.1 kHz must have samples transmitted on a cadence creating the slightly lower aggregate transmission rate to match the slightly lower rendering rate. For streams running at a sample rate of 44.1 kHz, there're occasional frames that will not contain a sample generating the following cadence.

12-11-11-12-11-11-12-11-11-12-11-11-11- (repeat)

The dashes indicate frames that do not contain a sample block. The cadence repeats continuously generating exactly 147 sample blocks every 160 frames, and avoids any long term drift between sample delivery and rendering clock.

Sample rates that are integral multiples of 44.1 kHz apply the "12-11" cadence rule just as a 44.1 kHz sample rate would, except that non-empty frames contain multiple (2 or 4) sample blocks, instead of just one.

For a sample rate of 22.05 kHz, the transmission pattern becomes:

{12}-*{11}-*{11}-*{12}-*{11}-*{11}-*{12}-*{11}-*{11}-*{12}-*{11}-*{11}-*{11}-* (repeat)
where
{12} = 1*1*1*1*1*1*1*1*1*1*1*1*
{11} = 1*1*1*1*1*1*1*1*1*1*1*

and the asterisks * represent a frame in which there is no sample block.

For a sample rate of 11.025 kHz, the transmission pattern becomes:

[12]-*[11]-***[11]-***[12]-***[11]-***[11]-***[12]-***[11]-***[11]-***[12]-***[11]-***[11]-***[11]-*** (repeat)**
where
[12] = 1*1***1***1***1***1***1***1***1***1***1***1*****
[11] = 1*1***1***1***1***1***1***1***1***1***1*****

and the asterisks * represent a frame in which there is no sample block.

These framing sequences apply only to the outbound (SDO) data from the controller. Inbound (SDI) data transmitted by the codec is permitted to deviate for minimizing codec buffer management.

6.9 Power Management

Whenever the Link is commanded to enter a low power state, it enters the link-reset state. This state is only exited in response to a software command and follows all link rules for exiting the link reset state. The Audio Function Group and the analog input / output converter widgets support power control. Whole chip power states can be controlled through the Audio Function Group, while individual DACs and ADCs can also be controlled through the corresponding power state control verbs. The following table describes the definitions of the power-state.

Power States	Definitions	Referenced with AC97
D0	All power on. Individual ADCs & DACs can be controlled.	
D1	All amplifiers and analog converters are powered down. Register values maintained, and analog reference voltage is still on.	PR0 & PR1 & PR2
D2	Register values maintained, but analog reference voltage is also down.	PR3
D3	Same as D2 state.	PR3

6.10 Unsolicited Response Behavior Description

- As jack plug in, and jack pull out, "unsolicited response" occurs.
- As initial state (boot-up or wake-up), jack already plugged-in, 'unsolicited response does not report. Bit 31 of pin sense register needs to correctly report whether anything is plugged in.
- All pin widgets except SPDIF TX (PW6), only analog jacks externally exposed, and of the 3.55mm (1/8'') mini jack type need "unsolicited response".
- "Unsolicited response" is a capability that could be reported by any type of widgets. Microsoft class driver only takes advantage of pin widget on this because it's not clear to us what other widget types (AOW, AIW and MW) are going to use this response.
- While Microsoft spec. is not very clear about what its Default should be, Microsoft recommendation is set it to disabled by Default. Class driver will enable it before using unsolicited response.

7 Widget Description

7.1 Node ID List

Table 5 – Node ID List

Node ID	Name	Input Connection List	Note
00	Root Node	N/A	
01	AFG	N/A	Audio Function Group
10	AOW0	N/A	Analog Output Widget
11	DOW0	N/A	Digital Output Widget for S/PDIF TX
12	AIW0	13	Analog Input Widget
13	SW0	14, 15, 18, 1A	ADC Input Selection
14	PW1	N/A	Port B
15	PW2	N/A	Port C
16	PW3	10	Port D
17	PW4	10, 1D	Port A
18	PW5	N/A	Port F
19	PW6	11	Pin Widget 6 for S/PDIF TX
1A	MW0	10, 14, 15, 18, 1D	Analog Mixer
1B	DOW1	N/A	Digital Output Widget for S/PDIF TX2
1C	PW7	1B	HDMI Audio Output
1D	AOW1	N/A	Analog Output Widget
1E	PW8	N/A	Pin Widget for DigMic DATA
1F	AIW1	1E	Widget for DigMic
20	AIW2	18	Analog Input Widget

7.2 Root Node (Node ID = 00)

7.2.1 Get Parameter Verb (Verb ID = F00h)

Get Vendor ID (Payload = 00h) Response: 1106 n398h

Bit	Attribute	Description
31-16	R	Vendor ID
15-0	R	Device ID (n: 0-7)

Get Revision ID (Payload = 02h) Response: 0010 0000h

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	MajRev The major revision number (left of the decimal) of the Azalia spec to which the codec is fully compliant. 0001b
19:16	R	MinRev The minor revision number (right of the decimal) of the Azalia spec to which the codec is fully compliant. 0000b
15:8	R	Revision ID 0000 0000b
7:0	R	Stepping ID 0000 0000b

Get Subordinate Node Count (Payload = 04h) Response: 0001 0001h

Bit	Attribute	Description
31:24	R	Reserved
23:16	R	Starting Node Number 01h
15:8	R	Reserved
7:0	R	Total Number of Nodes. 01h (Only 1 Audio Function Group in the codec)

7.3 Audio Function Group (Node ID = 01)

7.3.1 Get Parameter Verb (Verb ID = F00h)

Get Subordinate Node Count (Payload = 04h) Response: 0010 0011h

Bit	Attribute	Description
31:24	R	Reserved
23:16	R	Starting Node Number 10h
15:8	R	Reserved
7:0	R	Total Number of Nodes 11h

Get Function Group Type (Payload = 05h) Response: 0000 0001h

Bit	Attribute	Description
31:9	R	Reserved
8	R	0b: Not support unsolicited response.
7:0	R	01h: Audio function group.

Get Function Group Capabilities (Payload = 08h) Response: 0000 0306h

Bit	Attribute	Description
31:17	R	Reserved
16	R	Beep Gen 0b
15:12	R	Reserved
11:8	R	Input Delay 3h
7:4	R	Reserved
3:0	R	Output Delay 6h

Get Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	D3Sup
2	R	D2Sup
1	R	D1Sup
0	R	D0Sup

Get GPIO Capabilities (Payload = 11h) Response: 4000 0002h

Bit	Attribute	Description
31	R	GPIWake=0 (Not support GPIO wake up function)
30	R	GPIUnso=1 (Support GPIO unsolicited response)
29:24	R	Reserved
23:16	R	NumGPIs=00h (No GPI pin is supported)
15:8	R	NumGPOs=00h (No GPO pin is supported)
7:0	R	NumGPIOs=02h (Four GPIO pins are supported)

7.3.2 Unsolicited Response Control Verb (Verb ID = F08h & 708h)

	Description	Verb ID	Payload
Get	Get the UnsRes ability of AFG	F08h	8'b0
Set	Set the UnsRes ability of AFG	708h	EnableUnsol

Response

Bit	Attribute	Description
31:8	R	Reserved
7	RW	Enable Unsolicited Response 0: Disable 1: Enable
6	R	Reserved
5:0	RW	Tag for Unsolicited Response The value is opaque to codec and used by software to determine which codec node generate unsolicited response.

7.3.3 GPIO Data Verbs (Verb ID = F15h & 715h)

	Description	Verb ID	Payload
Get	Get GPIO data	F15h	8'b0
Set	Set GPIO data	715h	Data

Response

Bit	Attribute	Description
31:8	R	Reserved
7:4	R	GPIO[7:2] Data Not supported here.
3:0	RW	GPIO[1:0] Data

7.3.4 GPIO Enable Mask Verbs (Verb ID = F16h & 716h)

	Description	Verb ID	Payload
Get	Get the status of GPIO pin	F16h	8'b0
Set	Enable/ Disable GPIO pin	716h	Enable

Response

Bit	Attribute	Description
31:8	R	Reserved
7:4	R	GPIO[7:2] Enable Mask Not supported here.
3:0	RW	GPIO[1:0].Enable Mask 0: The corresponding GPIO pin is disabled and is Hi-Z state. 1: The corresponding GPIO pin is enabled. Its behavior is determined by the GPIO direction control.

Note: When disabled, the value returned on a read will still reflect the value that would be driven if the GPIO pin is enabled.

7.3.5 GPIO Direction Verbs (Verb ID = F17h & 717h)

	Description	Verb ID	Payload
Get	Get the direction of GPIO pin	F17h	8'b0
Set	Set the direction of GPIO pin	717h	Control

Response

Bit	Attribute	Description
31:8	R	Reserved
7:4	R	GPIO[7:2] Direction Control Not supported here.
3:0	RW	GPIO[1:0] Direction Control 0: The corresponding GPIO pin is configured as an input pin. 1: The corresponding GPIO pin is configured as an output pin.

7.3.6 GPIO Unsolicited Enable Mask (Verb ID = F19h & 719h)

	Description	Verb ID	Payload
Get	Get unsolicited ability of GPIO	F19h	8'b0
Set	Set unsolicited ability of GPIO	719h	UnsolEnable

Response

Bit	Attribute	Description
31:8	R	Reserve
7:4	R	GPIO[7:2] Unsolicited Enable Mask Not supported here.
3:0	RW	GPIO[1:0] Unsolicited Enable Mask 0: Unsolicited response will not be sent on link. 1: Unsolicited response will be sent on link when corresponding GPIO is configured as input and changes state.

Note: The unsolicited response of corresponding GPIO (configured as input) is enabled as the "Enable Mask" and verb "Unsolicited Response" for NID=01 are enabled.

7.3.7 Subsystem ID Control Verbs (Verb ID = F20h & 720h – 723h)

	Description	Verb ID	Payload
Get	Get Subsystem ID	F20h	8'b0
Set1	Set Subsystem ID[7:0]	720h	Subsystem ID [7:0]
Set2	Set Subsystem ID[15:8]	721h	Subsystem ID [15:8]
Set3	Set Subsystem ID[23:16]	722h	Subsystem ID [23:16]
Set4	Set Subsystem ID[31:24]	723h	Subsystem ID [31:24]

Response 32'h11060000

Bit	Attribute	Description
31:16	RW	Manufacturer ID 1106h
15:8	RW	Board SKU 00h
7:0	RW	Assembly ID 00h

Note: All 32 bits in the Subsystem ID register are writeable, with the power-on default value of 1106 0000h. The system board BIOS can change the values during power up sequence to precisely describe the information about the motherboard so that the OS can load the correct driver.

7.3.8 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Note: For whole chip power down control.
Response

Bit	Attribute	Description
31:8	R	Reserved
7:4	R	PS-Act Same as PS-Set for AFG.
3:0	RW	PS-Set

7.3.9 Vendor Defined Verbs (Verb ID = F70h – F74h) - Reserved

7.3.10 Function Reset Verb (Verb ID = 7FFh)

	Description	Verb ID	Payload
Function Reset	Function Reset	7FFh	8'b0

7.4 Audio Analog Output Converter Widget (Node ID = 10h, 1Dh)

7.4.1 Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) Response: 0000 041Dh

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0000b: Audio output converter widget.
19:16	R	0000b: Delay.
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	0: Analog widget, not digital.
8	R	0: Connection list is not present.
7	R	0: Does not support unsolicited response.
6	R	0: No Processing control.
5	R	Reserved
4	R	1: Contains format information.
3	R	1: Amplifier parameter.
2	R	1: Out amp presented.
1	R	0: In amp not present.
0	R	1: Stereo.

Supported PCM Size, Rates (Payload = 0Ah) Response: 000E 05E0h

Bit	Attribute	Description
31:21	R	Reserved
20	R	0: No 32-bit audio format support.
19	R	1: 24-bit audio format support.
18	R	1: 20-bit audio format support.
17	R	1: 16-bit audio format support.
16	R	0: No 8-bit audio format support.
15:12	R	Reserved
11	R	0: 384 kHz not supported.
10	R	1: 192 kHz supported.
9	R	0: 176.4 kHz not supported.
8	R	1: 96 kHz supported.
7	R	1: 88.2 kHz supported.
6	R	1: 48 kHz supported.
5	R	1: 44.1 kHz supported.
4	R	0: 32 kHz not supported.
3	R	0: 22.05 kHz not supported.
2	R	0: 16 kHz not supported.
1	R	0: 11.025 kHz not supported.
0	R	0: 8 kHz not supported.

Supported Stream Formats (Payload = 0Bh) Response: 0000 0001h

Bit	Attribute	Description
31:3	R	Reserved
2	R	0: No AC3 support.
1	R	0: No Float32 support.
0	R	1: PCM supported.

Output Amplifier Capabilities (Payload =12h) Response: 0005 2A2Ah

Bit	Attribute	Description
31	R	0: No mute capability.
30:23	R	Reserved
22:16	R	Step Size 0000101b: Step size is 1.5dB.
15	R	Reserved
14:8	R	Number of steps 0101010b: Number of steps is 43 (-63dB – 0dB).
7	R	Reserved
6:0	R	Offset 0101010b: Offset 2Ah is 0dB.

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R	1: D0Sup

7.4.2 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Note: For DAC power down control.
Response

Bit	Attribute	Description
31:8	R	Reserved
7:4	R	PS-Act Reports the actual power state of the widget.
3:0	RW	PS-Set

7.4.3 Converter Stream, Channel Verbs (Verb ID = F06h & 706h)

	Description	Verb ID	Payload
Get	Get Converter Stream/ Channel	F06h	8'b0
Set	Set Converter Stream/ Channel	706h	Stream is in bit[7:4] Channel is in bit[3:0]

7.4.4 Converter Format Verbs (Verb ID = Ah & 2h)

	Description	Verb ID	Payload
Get	Get Converter Format	Ah	16'b0
Set	Set Converter Format	2h	Format

Converter Format

Bit	Attribute	Description
15	R	Stream Type 0: PCM 1: Non-PCM (Not supported)
14	RW	Sample Base Rate 0: 48 kHz 1: 44.1 kHz
13:11	RW	Sample Base Rate Multiple 000 = x1: 48 kHz, 44.1 kHz 001 = x2: 96 kHz, 88.2 kHz 010 = x3: 144 kHz (Not supported) 011 = x4: 192 kHz, 176.4 kHz 100-111: Reserved
10:8	RW	Sample Base Rate Divisor 000 = /1: 48 kHz Others: Not supported
7	R	Reserved
6:4	RW	Bits Per Sample 000: 8-bit (Not supported) 001: 16-bit 010: 20-bit 011: 24-bit 100: 32-bit (Not supported)
3:0	RW	Number of Channels (CHAN) Number of channels for this stream in each "sample block" of the "packets" in each "frame" on the link. 0000: 1 0001: 2 …… 1111: 16

7.4.5 Amplifier Gain / Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/ Mute	Bh	Format
Set	Set Amplifier Gain/ Mute	3h	Format

Get Payload Format

Bit	Attribute	Description
15	W	0: The input amplifier is being requested. (Ignored) 1: The output amplifier is being requested.
14	W	Reserved
13	W	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	Reserved
3:0	W	Index

Get Response format

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Amplifier is un-muted.
6:0	R	Amplifier Gain Setting 0101010b: Offset 2Ah is 0dB. (Default)

Set Payload Format

Bit	Attribute	Description
15	W	1: The output amplifier is being set.
14	W	1: The input amplifier is being set. (Ignored)
13	W	1: The left amplifier is being set.
12	W	1: The right amplifier is being set.
11:8	W	Index Ignored
7	W	0: Un-muted.
6:0	W	Gain Setting

7.5 Audio Digital Output Converter (S/PDIF TX) Widget (Node ID = 11h, 1Bh)

7.5.1 Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) Response: 0000 0611h

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0000b: Audio output converter widget.
19:16	R	0000b: Delay.
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	1: Digital widget, not analog.
8	R	0: Connection list is not present.
7	R	0: Does not support unsolicited response.
6	R	0: No processing control.
5	R	Reserved
4	R	1: Contains format information.
3	R	0: Contains no amplifier parameter.
2	R	0: Out amp not present.
1	R	0: In amp not present.
0	R	1: Stereo.

Supported PCM Size, Rates (Payload = 0Ah) Response: 000E 05E0h

Bit	Attribute	Description
31:21	R	Reserved
20	R	0: No 32-bit audio format support.
19	R	1: 24-bit audio format support.
18	R	1: 20-bit audio format support.
17	R	1: 16-bit audio format support.
16	R	0: No 8-bit audio format support.
15:12	R	Reserved
11	R	0: 384 kHz not supported.
10	R	1: 192 kHz not supported.
9	R	0: 176.4 kHz not supported.
8	R	1: 96 kHz supported.
7	R	1: 88.2 kHz supported.
6	R	1: 48 kHz supported.
5	R	1: 44.1 kHz supported.
4	R	0: 32 kHz not supported.
3	R	0: 22.05 kHz not supported.
2	R	0: 16 kHz not supported.
1	R	0: 11.025 kHz not supported.
0	R	0: 8 kHz not supported.

Supported Stream Formats (Payload = 0Bh) Response: 0000 0001h

Bit	Attribute	Description
31:3	R	Reserved
2	R	0: No AC3 support.
1	R	0: No Float32 support.
0	R	1: PCM supported.

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R	1: D0Sup

7.5.2 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Note: For S/PDIF TX power down control.

Response

Bit	Attribute	Description
31:8	R	Reserved
7:4	R	PS-Act Reports the actual power state of the widget.

7.5.3 Converter Stream, Channel Verbs (Verb ID = F06h & 706h)

	Description	Verb ID	Payload
Get	Get Converter Stream/ Channel	F06h	8'b0
Set	Set Converter Stream/ Channel	706h	Stream is in bit[7:4], Channel bit[3:0]

7.5.4 S/PDIF Converter Control 1 & 2 Verbs (Verb ID = F0Dh & 70Dh, 70Eh)

	Description	Verb ID	Payload
Get	Get Converter Control State	F0Dh	8'b0
Set	Set Converter Control 1	70Dh	SIC[7:0]
Set	Set Converter Control 2	70Eh	SIC[15:8]

S/PDIF IEC Control Bits Format

Bit	Attribute	Description
15	R	Reserved
14:8	RW	CC[6:0] Category Code
7	RW	L: Generation level.
6	RW	PRO 0: Consumer mode. 1: Professional mode.
5	RW	AUDIO 0: Data is PCM format. 1: Data is non PCM format.
4	RW	Copy 0: Copyright is not asserted. 1: Copyright is asserted.
3	RW	Pre 0: Pre-emphasis is none. 1: Filter pre-emphasis is 50/15 μs.
2	RW	VCFG Determine S/PDIF transmitter behavior when data is not being transmitted.
1	RW	Validity Flag
0	RW	DigEn 0: S/PDIF TX disabled. 1: S/PDIF TX enabled.

7.5.5 Converter Format Verbs (Verb ID = Ah & 2h)

	Description	Verb ID	Payload
Get	Get Converter Format	Ah	16'b0
Set	Set Converter Format	2h	Format

Converter Format

Bit	Attribute	Description
15	RW	Stream Type 0: PCM 1: Non-PCM
14	RW	Sample Base Rate 0: 48 kHz 1: 44.1 kHz
13:11	RW	Sample Base Rate Multiple 000 = x1: 48 kHz, 44.1 kHz 001 = x2: 96 kHz, 88.2 kHz 010 = x3: 144 kHz (Not supported) 011 = x4: 192 kHz, 176.4 kHz (176.4 kHz not support) 100-111: Reserved
10:8	RW	Sample Base Rate Divisor 000 = /1: 48 kHz Others: Not supported
7	R	Reserved
6:4	RW	Bits per Sample 000: 8-bit (Not supported) 001: 16-bit 010: 20-bit 011: 24-bit 100: 32-bit (Not supported)
3:0	RW	Number of Channels (CHAN) Number of channels for this stream in each "sample block" of the "packets" in each "frame" on the link. 0000: 1 0001: 2 …… 1111: 16

7.6 Audio Analog Input Converter Widget AIW0(Node ID = 12h)

7.6.1 Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) Response: 0010 051Bh

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0001: Audio input converter widget.
19:16	R	0000: Delay.
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	0: Analog widget, not digital.
8	R	1: Connection list is present.
7	R	0: Does not support unsolicited response.
6	R	0: No processing control.
5	R	Reserved
4	R	1: Contains format information.
3	R	1: Contains amplifier parameter.
2	R	0: Out amp not presented.
1	R	1: In amp present.
0	R	1: Stereo.

Supported PCM Size, Rates (Payload = 0Ah) Response: 000E 0560h

Bit	Attribute	Description
31:21	R	Reserved
20	R	0: No 32-bit audio format support.
19	R	1: 24-bit audio format support.
18	R	1: 20-bit audio format support.
17	R	1: 16-bit audio format support.
16	R	0: No 8-bit audio format support.
15:12	R	Reserved
11	R	0: 384 kHz not supported.
10	R	1: 192 kHz supported.
9	R	0: 176.4 kHz not supported.
8	R	1: 96 kHz supported.
7	R	0: 88.2 kHz not supported.
6	R	1: 48 kHz supported.
5	R	1: 44.1 kHz supported.
4	R	0: 32 kHz not supported.
3	R	0: 22.05 kHz not supported.
2	R	0: 16 kHz not supported.
1	R	0: 11.025 kHz not supported.
0	R	0: 8 kHz not supported.

Supported Stream Formats (Payload = 0Bh) Response: 0000 0001h

Bit	Attribute	Description
31:3	R	Reserved
2	R	0: No AC3 support.
1	R	0: No Float32 support.
0	R	1: PCM supported.

Amplifier Capabilities (Payload = 0Dh) Response: 8005 1F0Bh

Bit	Attribute	Description
31	R	1: Mute capable.
30:23	R	Reserved
22:16	R	Step Size 0000101b: Step size is 1.5 dB.
15	R	Reserved
14:8	R	Number of Steps 0011111b: Number of steps is 32 (-16.5 dB – 30 dB).
7	R	Reserved
6:0	R	Offset 0001011b: Offset Bh is 0 dB.

Connection List Length (Payload = 0Eh) Response: 0000 0001h

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Short form.
6:0	R	0000001b: 1 input available.

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R`	1: D0Sup

7.6.2 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Response 32'h00000013

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Independent NID.
6:0	R	0010011b: From SW0 (NID = 13h).

7.6.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Note: For ADC power down control.
Response

Bit	Attribute	Description
31:8	R	Reserved
7:4	R	PS-Act Reports the actual power state of the widget.
3:0	RW	PS-Set

7.6.4 Converter Stream, Channel Verbs (Verb ID = F06h & 706h)

	Description	Verb ID	Payload
Get	Get Converter Stream/ Channel	F06h	8'b0
Set	Set Converter Stream/ Channel	706h	Stream is in bit[7:4], Channel bit[3:0]

7.6.5 Converter Format Verbs (Verb ID = Ah & 2h)

	Description	Verb ID	Payload
Get	Get Converter Format	Ah	16'b0
Set	Set Converter Format	2h	Format

Converter Format

Bit	Attribute	Description
15	R	Stream Type 0: PCM 1: Non-PCM (Not supported)
14	RW	Sample Base Rate 0: 48 kHz 1: 44.1 kHz
13:11	RW	Sample Base Rate Multiple 000: x1: 48 kHz, 44.1 kHz 001: x2: 96 kHz, 010: x3: 144 kHz (Not supported) 011: x4: 192 kHz 100~111: Reserved
10:8	RW	Sample Base Rate Divisor 000 = /1: 48 kHz Others: Not supported
7	R	Reserved
6:4	RW	Bits per Sample 000: 8-bit (Not supported) 001: 16-bit 010: 20-bit 011: 24-bit 100: 32-bit (Not supported)
3:0	RW	Number of Channels (CHAN) Number of channels for this stream in each "sample block" of the "packets" in each "frame" on the link. 0000: 1 0001: 2 …… 1111: 16

7.6.6 Amplifier Gain / Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/ Mute	Bh	Format
Set	Set Amplifier Gain/ Mute	3h	Format

Get Payload Format

Bit	Attribute	Description
15	W	0: The input amplifier is being requested. 1: The output amplifier is being requested. (Ignored)
14	W	Reserved (Read as 0.)
13	W	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	Reserved (Read as 0.)
3:0	W	Index Ignored

Get Response format

Bit	Attribute	Description
31:8	R	Reserved (Read as 0.)
7	R	0: Amplifier is un-muted. 1: Amplifier is muted.
6:0	R	Amplifier Gain Setting 0001011b: Offset Bh is 0dB. (Default)

Set Payload Format

Bit	Attribute	Description
15	W	1: The output amplifier is being set. (Ignored)
14	W	1: The input amplifier is being set.
13	W	1: The left amplifier is being set.
12	W	1: The right amplifier is being set.
11:8	W	Index Ignored
7	W	0: Un-mute 1: Mute
6:0	W	Gain Setting

7.7 Selector Widget SW0 (Node ID = 13h)

7.7.1 Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) Response: 0030 0501h

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0011b: Audio selector widget.
19:16	R	0000b: Delay.
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	0: Analog widget, not digital.
8	R	1: Connection list is present.
7	R	0: Does not support unsolicited response.
6	R	0: No processing control.
5	R	Reserved
4	R	0: No format information.
3	R	0: Amplifier parameter.
2	R	0: Out amp not presented.
1	R	0: In amp not present.
0	R	1: Stereo.

Connection List Length (Payload = 0Eh) Response: 0000 0004h

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Short form.
6:0	R	0000100b: 4 input available.

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R	1: D0Sup

7.7.2 Connection Select Control Verbs (Verb ID = F01h & 701h)

	Description	Verb ID	Payload
Get	Get Connection Select	F01h	8'b0
Set	Set Connection Select	701h	The connection index value to be set

7.7.3 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Response 32'h1A181514 (n=0) or 32'h00000000 (n=4)

Bit	Attribute	Description	
		Offset index n = 0	**Offset index n = 4**
31:24	R	Connection List Entry n+3 8'h1A (MW0)	8'h00
23:16	R	Connection List Entry n+2 8'h18 (PW5, Port F)	8'h00
15:8	R	Connection List Entry n+1 8'h15 (PW2, PortC)	8'h00
7:0	R	Connection List Entry n 8'h14 (PW1, PortB)	8'h00

7.7.4 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Note: For SW0 power down control.
Response

Bit	Attribute	Description
31:8	R	Reserved (Read as 0.)
7:4	R	PS-Act Reports the actual power state of the widget.
3:0	RW	PS-Set

7.8 Pin Widget PW1, PW5 (Node ID = 14h, 18h)

7.8.1 Get Parameter Verb (Verb ID = F00h)

Function Group Type (Payload = 05h) Response: 0000 0101h

Bit	Attribute	Description
31:9	R	Reserved
8	R	1: Unsolicited capable.
7:0	R	0000 0001: Audio function group.

Audio Widget Capabilities (Payload = 09h) Response: 0040 0481h

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0100: Pin widget.
19:16	R	0000: Delay.
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	0: Analog widget, not digital.
8	R	0: Connection list is not present.
7	R	1: Support unsolicited response.
6	R	0: No processing control.
5:	R	Reserved
4	R	0: Doesn’t contain format information.
3	R	0: Contain amplifier parameter.
2	R	0: Out amp not presented.
1	R	0: In amp not presented.
0	R	1: Stereo.

Pin Capabilities (Payload = 0Ch) Response: 0000 2324h

Bit	Attribute	Description	
31:17	R	Reserved	
16	R	EAPD Capable	Read as 0.
15:8	R	VRef Control	Read as 23h. (100%, 50%, and Hi-Z)
7	R	Reserved	
6	R	Balanced I/O Pins	Read as 0.
5	R	Input Capable	Read as 1.
4	R	Output Capable	Read as 0.
3	R	Headphone Drive Capable	Read as 0.
2	R	Presence Detect Capable	Read as 1.
1	R	Trigger Required	Read as 0.
0	R	Impedance Sense Capable	Read as 0.

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R`	1: D0Sup

7.8.2 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Note: For PW1, PW2, PW5 power down control.

Response

Bit	Attribute	Description
31:8	R	Reserved (Read as 0.)
7:4	R	PS-Act Reports the actual power state of the widget.
3:0	RW	PS-Set

7.8.3 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

PinCntl Format

Bit	Attribute	Description
7	R	Headphone Enable 0: Disabled
6	RW	Output Enable 0: Disabled 1: Output enabled
5	RW	Input Enable 0: Disabled 1: Input enabled
4:3	R	Reserved (Read as 0.)
2:0	RW	VRef Enable These bits control the VRef signal associated with the pin widget. 000: Hi-Z 001: 50% (Half of AVdd) 010: 0V (Not supported) 101: AVdd Others: Reserved

7.8.4 Unsolicited Response Control (Verb ID = F08h & 708h)

	Description	Verb ID	Payload
Get	Get Unsolicited Response Control	F08h	8'b0
Set	Set Unsolicited Response Control	708h	Enable unsolicited response

Unsolicited Format

Bit	Attribute	Description
7	RW	0: Unsolicited response disabled. 1: Unsolicited response enabled.
6	R	Reserved
5:0	RW	Tag Used by software to determine which node generated the unsolicited response.

7.8.5 Pin Sense Control Verbs (Verb ID = F09h & 709h)

	Description	Verb ID	Payload
Get	Get Pin Sense Control	F09h	8'b0
Set	Set Pin Sense Control	709h	PinCntl

PinCntl Format

Bit	Attribute	Description
7:1	R	Reserved
0	R	Right Channel Sense (Not supported)

Response

Bit	Attribute	Description
31	R	Presence Detect 0: Nothing plugged in. 1: Jack plugged in.
30:0	R	Reserved

7.8.6 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Config Bits Format (Default: 32'h01A19026 for PW1, 32'h02A19027 for PW5)

Bit	Attribute	Description
31:30	RW	Port Connectivity 00
29:24	RW	Location 000001: PW1 000010: PW5
23:20	RW	Default Device 1010: PW1 1010: PW5
19:16	RW	Connection Type 0001
15:12	RW	Color 1001: PW1 1001: PW5
11:8	RW	Misc. 0000
7:4	RW	Default Association 0010: PW1 0010: PW5
3:0	RW	Sequence 0110: PW1 0111: PW5

7.9 Pin Widget PW2 (Node ID = 15h)

7.9.1 Get Parameter Verb (Verb ID = F00h)

Function Group Type (Payload = 05h) Response: 0000 0101h

Bit	Attribute	Description
31:9	R	Reserved
8	R	1: Unsolicited capable.
7:0	R	0000 0001: Audio function group.

Audio Widget Capabilities (Payload = 09h) Response: 0040 0481h

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0100: Pin widget.
19:16	R	0000: Delay.
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power Control supported.
9	R	0: Analog widget, not digital.
8	R	0: Connection list is not present.
7	R	1: Support unsolicited response.
6	R	0: No processing control.
5:	R	Reserved
4	R	0: Doesn’t contain format information.
3	R	0: Contain amplifier parameter.
2	R	0: Out amp not presented.
1	R	0: In amp not presented.
0	R	1: Stereo.

Pin Capabilities (Payload = 0Ch) Response: 0000 2324h

Bit	Attribute	Description	
31:17	R	Reserved	
16	R	EAPD Capable	Read as 0.
15:8	R	VRef Control	Read as 8’h23. (100% & 50% & Hi-Z)
7	R	Reserved	
6	R	Balanced I/O Pins	Read as 0.
5	R	Input Capable	Read as 1.
4	R	Output Capable	Read as 0.
3	R	Headphone Drive Capable	Read as 0.
2	R	Presence Detect Capable	Read as 1.
1	R	Trigger Required	Read as 0.
0	R	Impedance Sense Capable	Read as 0.

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R`	1: D0Sup

7.9.2 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Note: For PW1, PW2, PW5 power down control.

Response

Bit	Attribute	Description
31:8	R	Reserved (Read as 0.)
7:4	R	PS-Act Reports the actual power state of the widget.
3:0	RW	PS-Set

7.9.3 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

PinCntl Format

Bit	Attribute	Description
7	R	Headphone Enable 0: Disabled
6	RW	Output Enable 0: Disabled 1: Output enabled
5	RW	Input Enable 0: Disabled 1: Input enabled
4:3	R	Reserved (Read as 0.)
2:0	RW	VRef Enable These bits control the VRef signal associated with the pin widget. 3'b000: Hi-Z 3'b001: 50% (Half of AVdd) 3'b010: 0V (Not supported) 3'b101: AVdd Others: Reserved

7.9.4 Unsolicited Response Control (Verb ID = F08h & 708h)

	Description	Verb ID	Payload
Get	Get Unsolicited Response Control	F08h	8'b0
Set	Set Unsolicited Response Control	708h	Enable unsolicited response

Unsolicited Format

Bit	Attribute	Description
7	RW	0: Unsolicited response disabled. 1: Unsolicited response enabled.
6	R	Reserved
5:0	RW	Tag Used by software to determine the node that generated the unsolicited response.

7.9.5 Pin Sense Control Verbs (Verb ID = F09h & 709h)

	Description	Verb ID	Payload
Get	Get Pin Sense Control	F09h	8'b0
Set	Set Pin Sense Control	709h	PinCntl

PinCntl Format

Bit	Attribute	Description
7:1	R	Reserved
0	R	Right Channel Sense (Not supported)

Response

Bit	Attribute	Description
31	R	Presence Detect 0: Nothing plugged in. 1: Jack plugged in.
30:0	R	Reserved

7.9.6 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Config bits Format: 32'h0181302E

Bit	Attribute	Description
31:30	RW	Port Connectivity 00
29:24	RW	Location 000001
23:20	RW	Default Device 1000
19:16	RW	Connection Type 0001
15:12	RW	Color 0011
11:8	RW	Misc. 0000
7:4	RW	Default Association 0010
3:0	RW	Sequence 1110

7.10 Pin Widget PW3 (Node ID =16h)

7.10.1 Get Parameter Verb (Verb ID = F00h)

Function Group Type (Payload = 05h) Response: 0000 0101h

Bit	Attribute	Description
31:9	R	Reserved
8	R	1: Unsolicited capable.
7:0	R	0000 0001: Audio function group.

Audio Widget Capabilities (Payload = 09h) Response: 0040 058Dh

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0100: Pin widget.
19:16	R	0000: Delay.
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	0: Analog widget, not digital.
8	R	1: Connection list is present.
7	R	1: Support unsolicited response.
6	R	0: No processing control.
5	R	Reserved
4	R	0: Doesn’t contain format information.
3	R	1: Contain amplifier parameter.
2	R	1: Out amp Present.
1	R	0: In amp not present.
0	R	1: Stereo.

Pin Capabilities (Payload = 0Ch)) Response: 0001 001Ch

Bit	Attribute	Description	
31:17	R	Reserved	
16	R	EAPD Capable	Read as 1.
15:8	R	VRef Control	Read as 8’h00.
7	R	Reserved	
6	R	Balanced I/O Pins	Read as 0.
5	R	Input Capable	Read as 0.
4	R	Output Capable	Read as 1.
3	R	Headphone Drive Capable	Read as 1.
2	R	Presence Detect Capable	Read as 1.
1	R	Trigger Required	Read as 0.
0	R	Impedance Sense Capable	Read as 0.

Connection List Length (Payload = 0Eh) Response: 0000 0001h

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Short form.
6:0	R	0000001: Only 1 input available.

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R`	1: D0Sup

Amplifier Capabilities (Payload = 12h) Response: 8000 0000h

Bit	Attribute	Description
31	R	1: Mute capable.
30:23	R	Reserved
22:16	R	Step Size 0000000: Step size is 0dB.
15	R	Reserved
14:8	R	Number of Steps 0000000: Number of steps is 1.
7	R	Reserved
6:0	R	Offset 0000000: Offset 00h is 0dB.

7.10.2 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Response 32'h0000001A

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Independent NID.
6:0	R	0011010b. (From MW0, NID = 1Ah)

7.10.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Note: For PW3 power down control.
Response

Bit	Attribute	Description
31:8	R	Reserved (Read as 0.)
7:4	R	PS-Act Reports the actual power state of the widget.
3:0	RW	PS-Set

7.10.4 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

PinCntl Format

Bit	Attribute	Description
7	RW	Headphone Enable (Default value is 1'b0) 0: Headphone disabled 1: Headphone enabled
6	RW	Output Enable 0: Disabled 1: Output enabled (Default)
5	R	Input Enable 0: Disabled 1: Input enabled (Not supported)
4:0	R	Reserved

7.10.5 Unsolicited Response Control (Verb ID = F08h & 708h)

	Description	Verb ID	Payload
Get	Get Unsolicited Response Control	F08h	8'b0
Set	Set Unsolicited Response Control	708h	Enable unsolicited response

Unsolicited Format

Bit	Attribute	Description
7	RW	0: Unsolicited Response Disabled 1: Unsolicited Response Enabled
6	R	Reserved
5:0	RW	Tag Used by software to determine the node that generated the unsolicited response.

7.10.6 Pin Sense Control Verbs (Verb ID = F09h & 709h)

	Description	Verb ID	Payload
Get	Get Pin Sense Control	F09h	8'b0
Set	Set Pin Sense Control	709h	PinCntl

PinCntl Format

Bit	Attribute	Description
7:1	R	Reserved
0	R	Right Channel Sense (Not supported)

Response

Bit	Attribute	Description
31	R	Presence Detect 1: Jack plugged in 0: Nothing plugged in
30:0	R	Reserved

7.10.7 EAPD Enable Verbs (Verb ID = F0C & 70Ch)

	Description	Verb ID	Payload
Get	EAPD Control	F0Ch	8'b0
Set		70Ch	Bit 1 is EAPD (Default: 1'b0)

7.10.8 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Config bits Format (Default: 32'h01014010)

Bit	Attribute	Description	
31:30	RW	Port Connectivity	00
29:24	RW	Location	000001
23:20	RW	Default Device	0000
19:16	RW	Connection Type	0001
15:12	RW	Color	0100
11:8	RW	Misc	0000
7:4	RW	Default Association	0001
3:0	RW	Sequence	0000

7.10.9 Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	
Set	Set Amplifier Gain/Mute	3h	

Get Payload Format

Bit	Attribute	Description
15	W	0: The input amplifier is being requested. (Ignored) 1: The output amplifier is being requested.
14	W	Reserved (Read as 0.)
13	W	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	Reserved (Read as 0.)
3:0	W	Index

Get Response format

Bit	Attribute	Description	
31:8	R	Reserved (Read as 0.)	
7	R	0: Amplifier is unmated.	1: Amplifier is muted.
6:0	R	Amplifier gain setting 0000000: Offset 00h is 0dB. (Default)	

Set Payload Format

Bit	Attribute	Description
15	W	1: The output amplifier is being set.
14	W	1: The input amplifier is being set. (Ignored)
13	W	1: The left amplifier is being set.
12	W	1: The right amplifier is being set.
11:8	W	Index Ignored
7	W	1: Mute 0: Un-mute
6:0	W	Gain Setting

7.11 Pin Widget PW4 (Node ID =17h)

7.11.1 Get Parameter Verb (Verb ID = F00h)

Function Group Type (Payload = 05h) Response: 0000 0101h

Bit	Attribute	Description
31:9	R	Reserved
8	R	1: Unsolicited capable.
7:0	R	0000 0001: Audio function group.

Audio Widget Capabilities (Payload = 09h) Response: 0040 058Dh

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0100: Pin widget.
19:16	R	0000: Delay.
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	0: Analog widget, not digital.
8	R	1: Connection list is present.
7	R	1: Support unsolicited response.
6	R	0: No processing control.
5	R	Reserved
4	R	0: Doesn’t contain format information.
3	R	1: Contain amplifier parameter.
2	R	1: Out amp Present.
1	R	0: In amp not present.
0	R	1: Stereo.

Pin Capabilities (Payload = 0Ch) Response: 0000 001Ch

Bit	Attribute	Description	
31:17	R	Reserved	
16	R	EAPD Capable	Read as 0.
15:8	R	VRef Control	Read as 00h.
7	R	Reserved	
6	R	Balanced I/O Pins	Read as 0.
5	R	Input Capable	Read as 0.
4	R	Output Capable	Read as 1.
3	R	Headphone Drive Capable	Read as 1
2	R	Presence Detect Capable	Read as 1.
1	R	Trigger Required	Read as 0.
0	R	Impedance Sense Capable	Read as 0.

Connection List Length (Payload = 0Eh) Response: 0000 0002h

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Short form.
6:0	R	0000010: 2 inputs available.

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R`	1: D0Sup

Amplifier Capabilities (Payload = 12h) Response: 8000 0000h

Bit	Attribute	Description
31	R	1: Mute capable.
30:23	R	Reserved
22:16	R	Step Size 0000000: Step size is 0dB.
15	R	Reserved
14:8	R	Number of Steps 0000000: Number of steps is 1.
7	R	Reserved
6:0	R	Offset 0000000: Offset 00h is 0dB.

7.11.2 Connection Select Control Verbs (Verb ID = F01h & 701h)

	Description	Verb ID	Payload
Get	Get Connection Select	F01h	8'b0
Set	Set Connection Select	701h	The connection index value to be set

7.11.3 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Response 32'h00001A1D (n=0) or 32'h00000000 (n=4)

Bit	Attribute	Description	
		Offset index n = 0	Offset index n = 4
31:24	R	Connection List Entry n+3 8'h00	8'h00
23:16	R	Connection List Entry n+2 8'h00	8'h00
15:8	R	Connection List Entry n+1 8'h1A (MW0)	8'h00
7:0	R	Connection List Entry n 8'h1D (AOW1)	8'h00

7.11.4 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Note: For PW3 power down control.
Response

Bit	Attribute	Description
31:8	R	Reserved (Read as 0.)
7:4	R	PS-Act Reports the actual power state of the widget.
3:0	RW	PS-Set

7.11.5 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

PinCntl Format

Bit	Attribute	Description
7	RW	Headphone Enable 0: Disabled 1: Headphone enabled
6	RW	Output Enable 0: Disabled 1: Output enabled (Default)
5	R	Input Enable 0: Disabled 1: Input enabled (Not supported)
4:0	R	Reserved

7.11.6 Unsolicited Response Control (Verb ID = F08h & 708h)

	Description	Verb ID	Payload
Get	Get Unsolicited Response Control	F08h	8'b0
Set	Set Unsolicited Response Control	708h	Enable unsolicited response

Unsolicited Format

Bit	Attribute	Description
7	RW	0: Unsolicited Response Disabled. 1: Unsolicited Response Enabled.
6	R	Reserved
5:0	RW	Tag Used by software to determine the node that generated the unsolicited response.

7.11.7 Pin Sense Control Verbs (Verb ID = F09h & 709h)

	Description	Verb ID	Payload
Get	Get Pin Sense Control	F09h	8'b0
Set	Set Pin Sense Control	709h	PinCntl

PinCntl Format

Bit	Attribute	Description
7:1	R	Reserved
0	R	Right Channel Sense (Not supported)

Response

Bit	Attribute	Description
31	R	Presence Detect 1: Jack plugged in 0: Nothing plugged in
30:0	R	Reserved

7.11.8 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Config bits Format (Default: 32'h0221401F)

Bit	Attribute	Description
31:30	RW	Port Connectivity 00
29:24	RW	Location 000010
23:20	RW	Default Device 0010
19:16	RW	Connection Type 0001
15:12	RW	Color 0100
11:8	RW	Misc. 0000
7:4	RW	Default Association 0001
3:0	RW	Sequence 1111

7.11.9 Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	
Set	Set Amplifier Gain/Mute	3h	

Get Payload Format

Bit	Attribute	Description
15	W	0: The input amplifier is being requested. (Ignored) 1: The output amplifier is being requested.
14	W	Reserved
13	W	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	Reserved (Read as 0.)
3:0	W	Index

Get Response format

Bit	Attribute	Description
31:8	R	Reserved (Read as 0.)
7	R	0: Amplifier is unmated. 1: Amplifier is muted.
6:0	R	Amplifier Gain Setting 0000000: Offset 00h is 0dB. (Default)

Set Payload Format

Bit	Attribute	Description
15	W	1: The output amplifier is being set.
14	W	1: The input amplifier is being set. (Ignored)
13	W	1: The left amplifier is being set.
12	W	1: The right amplifier is being set.
11:8	W	Index Ignored
7	W	1: Mute 0: Un-mute
6:0	W	Gain Setting

7.12 Pin Widget PW6 (Node ID = 19h) S/PDIF TX Pin

7.12.1 Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) Response: 0040 0701h

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0100: Pin widget.
19:16	R	0000: Delay.
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	1: Digital widget.
8	R	1: Connection list is present.
7	R	0: Does not support unsolicited response.
6	R	0: No processing control.
5	R	Reserved
4	R	0: Doesn’t contain format information.
3	R	0: Doesn’t contain amplifier parameter.
2	R	0: Out amp not presented.
1	R	0: In amp not presented.
0	R	1: Stereo.

Pin Capabilities (Payload = 0Ch) Response: 0000 0010h

Bit	Attribute	Description	
31:17	R	Reserved	
16	R	EAPD Capable	Read as 0.
15:8	R	VRef Control	Read as 8’b0.
7	R	Reserved	
6	R	Balanced I/O Pins	Read as 0.
5	R	Input Capable	Read as 0.
4	R	Output Capable	Read as 1.
3	R	Headphone Drive Capable	Read as 0.
2	R	Presence Detect Capable	Read as 0.
1	R	Trigger Required	Read as 0.
0	R	Impedance Sense Capable	Read as 0.

Connection List Length (Payload = 0Eh) Response: 0000 0001h

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Short form.
6:0	R	0000001: Only 1 input available.

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R	1: D0Sup

7.12.2 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Response 32'h00000011

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Independent NID
6:0	R	0010001 (From DOW0, NID = 11h)

7.12.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Note: For PW9 power down control.
Response

Bit	Attribute	Description
31:8	R	Reserved (Read as 0.)
7:4	R	PS-Act Reports the actual power state of the widget.
3:0	RW	PS-Set

7.12.4 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

PinCntl Format

Bit	Attribute	Description
7	R	Headphone Enable 0: Disabled
6	RW	Output Enable 0: Disabled 1: Output enabled
5	R	Input Enable 0: Disabled
4:3	R	Reserved
2:0	R	VRef Enable 000

7.12.5 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Config bits Format (Default: 32'h074411F0)

Bit	Attribute	Description
31:30	RW	Port Connectivity 00
29:24	RW	Location 000111
23:20	RW	Default Device 0100 (SPDIF Out)
19:16	RW	Connection Type 0100
15:12	RW	Color 0001
11:8	RW	Misc 0001
7:4	RW	Default Association 1111
3:0	RW	Sequence 0000

7.13 Mixer Widget (Node ID = 1Ah)

7.13.1 Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) Response: 0020 050Bh

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0010: Audio mixer widget.
19:16	R	0000: Delay.
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	0: Analog widget, not digital.
8	R	1: Connection List is present.
7	R	0: Does not support unsolicited response.
6	R	0: No processing control.
5	R	Reserved
4	R	0: No format information.
3	R	1: Amplifier parameter.
2	R	0: Out amp not presented.
1	R	1: In amp present.
0	R	1: Stereo.

Input Amplifier Capabilities (Payload = 0Dh) Response: 8005 1F17h

Bit	Attribute	Description
31	R	1: Mute capable.
30:23	R	Reserved
22:16	R	Step Size 0000101: Step size is 1.5dB. (No effect)
15	R	Reserved
14:8	R	Number of Steps 0011111: Number of steps is 32 (-34.5dB – 12dB). (Default) 0010111: Number of steps is 24 (-34.5dB – 0dB).
7	R	Reserved
6:0	R	Offset 0010111: Offset 17h is 0dB.

Connection List Length (Payload = 0Eh) Response: 0000 0004h

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Short form.
6:0	R	0000100: 4 inputs available.

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R`	1: D0Sup

7.13.2 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Response 32'h18151410 (n=0) or 32'h00000000 (n=4)

Bit	Attribute	Description	
		Offset index n = 0	Offset index n = 4
31:24	R	Connection List Entry n+3 8'h18 (PW5, PortF)	8'h00
23:16	R	Connection List Entry n+2 8'h15 (PW2, PortC)	8'h00
15:8	R	Connection List Entry n+1 8'h14 (PW1, PortB)	8'h00
7:0	R	Connection List Entry n 8'h10 (AOW0)	8'h00

7.13.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Note: For Mixer power down control.
Response

Bit	Attribute	Description
31:8	R	Reserved (Read as 0.)
7:4	R	PS-Act Reports the actual power state of the widget.
3:0	RW	PS-Set

7.13.4 Amplifier Gain/ Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain /Mute	Bh	Format
Set	Set Amplifier Gain Mute	3h	Format

Get Payload Format

Bit	Attribute	Description
15	W	0: The input amplifier is being requested. 1: The output amplifier is being requested. (Ignored)
14	W	Reserved (Read as 0.)
13	W	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	Reserved (Read as 0.)
3:0	W	Index

Get Response format

Bit	Attribute	Description
31:8	R	Reserved (Read as 0.)
7	R	0: Amplifier is un-muted. 1: Amplifier is muted. (Default, it's "0" to analog)
6:0	R	Amplifier Gain Setting 0010111: Offset 17h is 0dB. (Default)

Set Payload Format

Bit	Attribute	Description
15	W	1: The output amplifier is being set. (Ignored)
14	W	1: The input amplifier is being set.
13	W	1: The left amplifier is being set.
12	W	1: The right amplifier is being set.
11:8	W	Index Ignored
7	W	0: Un-mute 1: Mute
6:0	W	Gain Setting

7.14 Pin Widget PW7 (Node ID = 1Ch) HDMI Audio Output Pin

7.14.1 Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) Response: 0040 0701h

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0100: Pin widget.
19:16	R	0000: Delay.
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	1: Digital widget.
8	R	1: Connection list is present.
7	R	0: Does not support unsolicited response.
6	R	0: No processing control.
5	R	Reserved
4	R	0: Doesn't contain format information.
3	R	0: Doesn't contain amplifier parameter.
2	R	0: Out amp not presented.
1	R	0: In amp not presented.
0	R	1: Stereo.

Pin Capabilities (Payload = 0Ch) Response: 0000 0010h

Bit	Attribute	Description	
31:17	R	Reserved	
16	R	EAPD Capable	Read as 0.
15:8	R	VRef Control	Read as 00h.
7	R	Reserved	
6	R	Balanced I/O Pins	Read as 0.
5	R	Input Capable	Read as 0.
4	R	Output Capable	Read as 1.
3	R	Headphone Drive Capable	Read as 0.
2	R	Presence Detect Capable	Read as 0.
1	R	Trigger Required	Read as 0.
0	R	Impedance Sense Capable	Read as 0.

Connection List Length (Payload = 0Eh) Response: 0000 0001h

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Short form.
6:0	R	0000001: Only 1 input available.

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R`	1: D0Sup

7.14.2 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Response 32'h0000001B

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Independent NID
6:0	R	0011011 (From DOW1, NID = 1Bh)

7.14.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Note: For PW9 power down control.
Response

Bit	Attribute	Description
31:8	R	Reserved (Read as 0.)
7:4	R	PS-Act Reports the actual power state of the widget.
3:0	RW	PS-Set

7.14.4 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

PinCntl Format

Bit	Attribute	Description
7	R	Headphone Enable 0: Disabled
6	RW	Output Enable 0: Disabled 1: Output enabled
5	R	Input Enable 0: Disabled
4:3	R	Reserved
2:0	R	VRef Enable 000

7.14.5 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Config bits Format (Default: 32'h985601F0)

Bit	Attribute	Description
31:30	RW	Port Connectivity 10
29:24	RW	Location 011000
23:20	RW	Default Device 0101 (SPDIF Out)
19:16	RW	Connection Type 0110
15:12	RW	Color 0000
11:8	RW	Misc 0001
7:4	RW	Default Association 1111
3:0	RW	Sequence 0000

7.15 Pin Widget PW8 (Node ID = 1Eh)

7.15.1 Get Parameter Verb (Verb ID = F00h)

Function Group Type (Payload = 05h) Response: 0000 0001h

Bit	Attribute	Description
31:9	R	Reserved
8	R	0: Unsolicited Capable.
7:0	R	00000001: Audio function group.

Audio Widget Capabilities (Payload = 09h) Response: 0040 040Bh

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0100: Pin widget.
19:16	R	0000: Delay.
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	0: Analog widget, not digital.
8	R	0: Connection list is not present.
7	R	0: Not support unsolicited response.
6	R	0: No processing control.
5:	R	Reserved
4	R	0: Doesn’t contain format information.
3	R	1: Contain amplifier parameter.
2	R	0: Out amp not presented.
1	R	1: In amp presented.
0	R	1: Stereo.

Pin Capabilities (Payload = 0Ch) Response: 0000 0020h

Bit	Attribute	Description	
31:17	R	Reserved	
16	R	EAPD Capable	Read as 0.
15:8	R	VRef Control	Read as 8’b0.
7	R	Reserved	
6	R	Balanced I/O Pins	Read as 0.
5	R	Input Capable	Read as 1.
4	R	Output Capable	Read as 0.
3	R	Headphone Drive Capable	Read as 0.
2	R	Presence Detect Capable	Read as 0.
1	R	Trigger Required	Read as 0.
0	R	Impedance Sense Capable	Read as 0.

Amplifier Capabilities (Payload = 0Dh) Response: 002F 0300h

Bit	Attribute	Description	
31	R	0: Mute capable.	
30:23	R	Reserved	
22:16	R	Step Size	0101111: Step size is 12 dB.
15	R	Reserved	
14:8	R	Number of Steps	0000011: Number of steps is 4 (0 dB – 36 dB).
7	R	Reserved	
6:0	R	Offset	0000000: Offset 00h is 0 dB.

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R`	1: D0Sup

7.15.2 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

For PW8 power down control
Response

Bit	Attribute	Description
31:8	R	Reserved (Read as 0.)
7:4	R	PS-Act Reports the actual power state of the widget.
3:0	RW	PS-Set

7.15.3 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

PinCntl Format

Bit	Attribute	Description	
7	R	Headphone Enable 0: Disabled	
6	R	Output Enable 0: Disabled	
5	RW	Input Enable 0: Disabled	1: Input enabled
4:3	R	Reserved (Read as 0.)	
2:0	R	VRef Enable These bits control the VRef signal associated with the pin widget. 000: Hi-Z	

7.15.4 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Config bits Format (Default: 32'h50A601F0)

Bit	Attribute	Description	
31:30	RW	Port Connectivity	01
29:24	RW	Location	010000
23:20	RW	Default Device	1010
19:16	RW	Connection Type	0110
15:12	RW	Color	0000
11:8	RW	Misc	0001
7:4	RW	Default Association	1111
3:0	RW	Sequence	0000

7.15.5 Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	Format
Set	Set Amplifier Gain/Mute	3h	Format

Get Payload Format

Bit	Attribute	Description
15	W	0: The input amplifier is being requested. 1: The output amplifier is being requested. (Ignored)
14	W	Reserved (Read as 0.)
13	W	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	Reserved (Read as 0.)
3:0	W	Index Ignored

Get Response format

Bit	Attribute	Description
31:8	R	Reserved (Read as 0.)
7	R	0: Amplifier is un-muted.
6:0	R	Amplifier Gain Setting 0000000: Offset 00h is 0 dB. (Default)

Set Payload Format

Bit	Attribute	Description
15	W	1: The output amplifier is being set. (Ignored)
14	W	1: The input amplifier is being set.
13	W	1: The left amplifier is being set.
12	W	1: The right amplifier is being set.
11:8	W	Index Ignored
7	W	0: Un-mute
6:0	W	Gain Setting

7.16 Audio Analog Input Converter Widget AIW1 (Node ID = 1Fh)

7.16.1 Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) Response: 0010 051Bh

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0001: Audio input converter widget.
19:16	R	0000: Delay.
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	0: Analog widget, not digital.
8	R	1: Connection list is present.
7	R	0: Does not support unsolicited response.
6	R	0: No processing control.
5	R	Reserved
4	R	1: Contains format information.
3	R	1: Contains amplifier parameter.
2	R	0: Out amp not presented.
1	R	1: In amp present.
0	R	1: Stereo.

Supported PCM Size, Rates (Payload = 0Ah) Response: 0002 0074h

Bit	Attribute	Description
31:21	R	Reserved
20	R	0: No 32-bit audio format support.
19	R	0: No 24-bit audio format support.
18	R	0: No 20-bit audio format support.
17	R	1: 16-bit audio format support.
16	R	0: No 8-bit audio format support.
15:12	R	Reserved
11	R	0: No 384 kHz support.
10	R	0: No 192 kHz support.
9	R	0: No 176.4 kHz support.
8	R	0: No 96 kHz support.
7	R	0: No 88.2 kHz (not supported).
6	R	1: 48 kHz support.
5	R	1: 44.1kHz support.
4	R	1: 32 kHz support.
3	R	0: No 22.05 kHz support.
2	R	1: 16 kHz support.
1	R	0: No 11.025 kHz support.
0	R	0: No 8 kHz support.

Supported Stream Formats (Payload = 0Bh) Response: 0000 0001h

Bit	Attribute	Description
31:3	R	Reserved
2	R	0: No AC3 support.
1	R	0: No Float32 support.
0	R	1: PCM supported.

Amplifier Capabilities (Payload = 0Dh) Response: 8005 0C00h

Bit	Attribute	Description
31	R	1: Mute capable.
30:23	R	Reserved
22:16	R	Step Size 0000101: Step size is 1.5 dB.
15	R	Reserved
14:8	R	Number of Steps 0001100: Number of steps is 13 (0 dB – 18 dB).
7	R	Reserved
6:0	R	Offset 0000000: Offset 00h is 0 dB.

Connection List Length (Payload = 0Eh) Response: 0000 0001h

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Short form.
6:0	R	0000001: 1 input available.

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Description
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R`	1: D0Sup

7.16.2 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Response 32'h0000001E

Bit	Attribute	Description
31:8	R	Reserved
7	R	0: Independent NID
6:0	R	0011110: From PW8 (NID = 1Eh)

7.16.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

For DigMic power down control
Response

Bit	Attribute	Description
31:8	R	Reserved (Read as 0.)
7:4	R	PS-Act. Reports the actual power state of the widget.
3:0	RW	PS-Set

7.16.4 Converter Stream, Channel Verbs (Verb ID = F06h & 706h)

	Description	Verb ID	Payload
Get	Get Converter Stream / Channel	F06h	8'b0
Set	Set Converter Stream / Channel	706h	Stream is in bit[7:4] Channel is in bit[3:0]

7.16.5 Converter Format Verbs (Verb ID = Ah & 2h)

	Description	Verb ID	Payload
Get	Get Converter Format	Ah	16'b0
Set	Set Converter Format	2h	Format

Converter Format

Bit	Attribute	Description
15	R	Stream Type 0: PCM 1: Non-PCM (Not supported)
14	RW	Sample Base Rate 0: 48 kHz 1: 44.1 kHz
13:11	RW	Sample Base Rate Multiple 000 = x1: 48 kHz / 44.1 kHz or less 001 = x2: 96 kHz, 88.2 kHz, 32 kHz (96 kHz, 88.2 kHz Not support) 010 = x3: 144 kHz (Not supported) 011 = x4: 192 kHz (Not supported) 100-111: Reserved
10:8	RW	Sample Base Rate Divisor 000 = /1: 48 kHz, 44.1 kHz 001 = /2: 24 kHz, 22.05 kHz (Not supported) 010 = /3: 16 kHz, 32 kHz Others: Not supported
7	R	Reserved
6:4	RW	Bits per Sample 000: 8-bit (Not supported) 001: 16-bit 010: 20-bit (Not supported) 011: 24-bit (Not supported) 100: 32-bit (Not supported)
3:0	RW	Number of Channels (CHAN) Number of channels for this stream in each "sample block" of the "packets" in each "frame" on the link. 0000: 1 0001: 2 …… 1111: 16

7.16.6 Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	Format
Set	Set Amplifier Gain/Mute	3h	Format

Get Payload Format

Bit	Attribute	Description
15	W	0: The input amplifier is being requested. 1: The output amplifier is being requested. (Ignored)
14	W	Reserved (Read as 0.)
13	W	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	Reserved (Read as 0.)
3:0	W	Index Ignored

Get Response format

Bit	Attribute	Description
31:8	R	Reserved (Read as 0.)
7	R	0: Amplifier is un-muted. 1: Amplifier is muted.
6:0	R	Amplifier Gain Setting 0000000: Offset 00h is 0dB. (Default)

Set Payload Format

Bit	Attribute	Description
15	W	1: The output amplifier is being set. (Ignored)
14	W	1: The input amplifier is being set.
13	W	1: The left amplifier is being set.
12	W	1: The right amplifier is being set.
11:8	W	Index Ignored
7	W	1: Mute 0: Un-mute
6:0	W	Gain Setting

7.17 Audio Analog Input Converter Widget AIW2 (Node ID = 20h)

7.17.1 Get Parameter Verb (Verb ID = F00h)

Audio Widget Capabilities (Payload = 09h) Response: 0010 051Bh

Bit	Attribute	Description
31:24	R	Reserved
23:20	R	0001: Audio input converter widget.
19:16	R	0000: Delay
15:12	R	Reserved
11	R	0: No L-R swap.
10	R	1: Power control supported.
9	R	0: Analog widget, not digital.
8	R	1: Connection list is present.
7	R	0: Does not support unsolicited response.
6	R	0: No processing control.
5	R	Reserved
4	R	1: Contains format information.
3	R	1: Contains amplifier parameter.
2	R	0: Out amp not presented.
1	R	1: In amp present.
0	R	1: Stereo.

Supported PCM Size, Rates (Payload = 0Ah) Response: 000E 0560h

Bit	Attribute	Description
31:21	R	Reserved
20	R	0: No 32-bit audio format support.
19	R	1: 24-bit audio format support.
18	R	1: 20-bit audio format support.
17	R	1: 16-bit audio format support.
16	R	0: No 8-bit audio format support.
15:12	R	Reserved
11	R	0: 384 kHz not supported.
10	R	1: 192 kHz supported.
9	R	0: 176.4 kHz not supported.
8	R	1: 96 kHz supported.
7	R	0: 88.2 kHz not supported.
6	R	1: 48 kHz supported.
5	R	1: 44.1 kHz supported.
4	R	0: 32 kHz not supported.
3	R	0: 22.05 kHz not supported.
2	R	0: 16 kHz not supported.
1	R	0: 11.025 kHz not supported.
0	R	0: 8 kHz not supported.

Supported Stream Formats (Payload = 0Bh)		Response: 0000 0001h
Bit	**Attribute**	**Description**
31:3	R	Reserved
2	R	0: No AC3 support.
1	R	0: No Float32 support.
0	R	1: PCM supported.

Amplifier Capabilities (Payload = 0Dh)		Response: 8005 1F0Bh
Bit	**Attribute**	**Description**
31	R	1: Mute capable.
30:23	R	Reserved
22:16	R	Step Size 0000101: Step size is 1.5 dB.
15	R	Reserved
14:8	R	Number of Steps 0011111: Number of steps is 32 (-16.5 dB – 30 dB).
7	R	Reserved
6:0	R	Offset 0001011: Offset Bh is 0 dB.

Connection List Length (Payload = 0Eh)		Response: 0000 0001h
Bit	**Attribute**	**Description**
31:8	R	Reserved
7	R	0: Short form.
6:0	R	0000001: 1 input available.

Supported Power States (Payload = 0Fh)		Response: 0000 000Fh
Bit	**Attribute**	**Description**
31:4	R	Reserved
3	R	1: D3Sup
2	R	1: D2Sup
1	R	1: D1Sup
0	R`	1: D0Sup

7.17.2 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	**Verb ID**	**Payload**
Get	Get Connection List Entry	F02h	Offset index n
Response 32'h00000018			
Bit	**Attribute**	**Description**	
31:8	R	Reserved	
7	R	0: Independent NID	
6:0	R	0011000: From PW5 (NID = 18h)	

7.17.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

For ADC power down control
Response

Bit	Attribute	Description
31:8	R	Reserved
7:4	R	PS-Act Reports the actual power state of the widget.
3:0	RW	PS-Set

7.17.4 Converter Stream, Channel Verbs (Verb ID = F06h & 706h)

	Description	Verb ID	Payload
Get	Get Converter Stream / Channel	F06h	8'b0
Set	Set Converter Stream / Channel	706h	Stream is in bit[7:4] Channel is in bit[3:0]

7.17.5 Converter Format Verbs (Verb ID = Ah & 2h)

	Description	Verb ID	Payload
Get	Get Converter Format	Ah	16'b0
Set	Set Converter Format	2h	Format

Converter Format

Bit	Attribute	Description
15	R	Stream Type 0: PCM 1: Non-PCM (Not supported)
14	RW	Sample Base Rate 0: 48 kHz 1: 44.1 kHz
13:11	RW	Sample Base Rate Multiple 000: x1: 48 kHz, 44.1 kHz 001: x2: 96 kHz 010: x3: 144 kHz (Not supported) 011: x4: 192 kHz 100-111: Reserved
10:8	RW	Sample Base Rate Divisor 000 = /1: 48 kHz Others: Not supported
7	R	Reserved
6:4	RW	Bits per Sample 000: 8-bit (Not supported) 001: 16-bit 010: 20-bit 011: 24-bit 100: 32-bit (Not supported)
3:0	RW	Number of Channels (CHAN) Number of channels for this stream in each "sample block" of the "packets" in each "frame" on the link. 0000: 1 0001: 2 …… 1111: 16

7.17.6 Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	Format
Set	Set Amplifier Gain/Mute	3h	Format

Get Payload Format

Bit	Attribute	Description
15	W	0: The input amplifier is being requested. 1: The output amplifier is being requested. (Ignored)
14	W	Reserved (Read as 0.)
13	W	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	Reserved (Read as 0.)
3:0	W	Index Ignored

Get Response format

Bit	Attribute	Description
31:8	R	Reserved (Read as 0.)
7	R	0: Amplifier is un-muted. 1: Amplifier is muted.
6:0	R	Amplifier Gain Setting 0001011: Offset Bh is 0 dB. (Default)

Set Payload Format

Bit	Attribute	Description
15	W	1: The output amplifier is being set. (Ignored)
14	W	1: The input amplifier is being set.
13	W	1: The left amplifier is being set.
12	W	1: The right amplifier is being set.
11:8	W	Index Ignored
7	W	0: Un-mute 1: Mute
6:0	W	Gain Setting

8 Functional Descriptions

8.1 Clock Control

One of the major differences between Azalia and AC97 is the clock source. The Azalia controller provides a 24MHz clock (BITCLK). An internal PLL (PLL1) in the codec uses BITCLK (24MHz) as the reference clock and generates 49.152 MHz clocks for internal use. A second PLL (PLL2) also takes the 24MHz BITCLK and generates 22.5792 MHz clock for 44.1 kHz based rates. The PLLs can be powered down by the Power Widget for power management. **Both PLL output clocks can be routed to pin 48 by a vendor defined verb for testing**.

The interface signals between digital block and the 2 PLLs are listed below.

PLL1 (49.152 MHz)		
Pin Name	**Direction (From PLL)**	**Pin Description**
REFCLK	I	Connect to a 24-MHz clock input.
CLK49152	O	49.152-MHz clock output.
RST	I	When RST is high, the PLL enters a low power mode and all internal states are reset.
PWRPD	I	When PWRPD is high, the PLL enters a power-down mode.
VDD	IO	Digital power supply for PFD and Dividers. Nominally 3.3V.
GND	IO	Ground for PFD and Dividers.
VCOPWR	IO	Analog power supply for VCO. Nominally 3.3V.
VCOGND	IO	Ground for VCO.
CHGPPWR	IO	Analog power supply for Bias and Charge Pump. Nominally 3.3V.
CHGPGND	IO	Ground for Bias and Charge Pump.

22.5792 MHz		
Pin Name	**Direction (From PLL)**	**Pin Description**
REFCLK	I	Connect to a 24-MHz clock input.
CLK225792	O	22.5792-MHz clock output.
RST	I	When RST is high, the PLL enters a low power mode and all internal states are reset.
PWRPD	I	When PWRPD is high, the PLL enters a power-down mode.
VDD	IO	Digital power supply for PFD and Dividers. Nominally 3.3V.
GND	IO	Ground for PFD and Dividers.
VCOPWR	IO	Analog power supply for VCO. Nominally 3.3V.
VCOGND	IO	Ground for VCO.
CHGPPWR	IO	Analog power supply for Bias and Charge Pump. Nominally 3.3V.
CHGPGND	IO	Ground for Bias and Charge Pump.

8.2 Interpolation / Decimation

To take advantage the high bandwidth provided by the new audio interface, the hardware only supports native 44.1-, 48-, 88.2-, 96-, and 192 kHz sample rates, and the driver is responsible for converting the data to / from 192 kHz. This way the large area previously required for implementing the digital interpolation / decimation filters can be saved.

8.3 HPF for ADC DC Removal

The built-in high-pass filter for each ADC can remove the DC component in the ADC data.

8.4 Audio Jack Detection Circuits

Based on the jack detection circuit defined in the HD audio specification, the figure below summarizes the equivalent resistance values to the SENSE pin in different scenario.

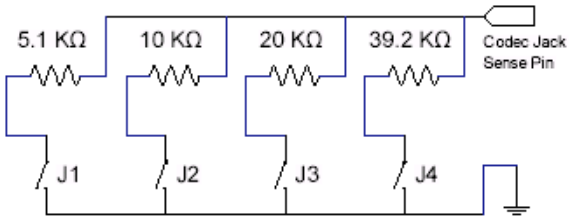


Figure 19 – Jack Detect Circuit

8.5 Internal Loop-back and Peak Detection for Low Cost Production Test

Internal loop-back paths can be used to test all DACs and ADCs functions. The output of each DAC can be routed back to the input of the ADC. The ADC output data is analyzed by a specially designed block to detect the zero-crossing point and the peak values. These information can be read back to decide whether the digital & analog functions are normal. Refer to the descriptions in the Vendor-Defined Verbs in the Audio Function Group.

8.6 Digital Microphone Implementation

Codec provides a clock signal to digital microphone. Digital microphone converts the external analog signal into 1-bit digital signal. 1-bit signal is the output of a sigma-delta modulator. Codec receives 1-bit data and converter it to PCM data by decimation filter. The PCM data is sent to the HAD controller through HAD link.

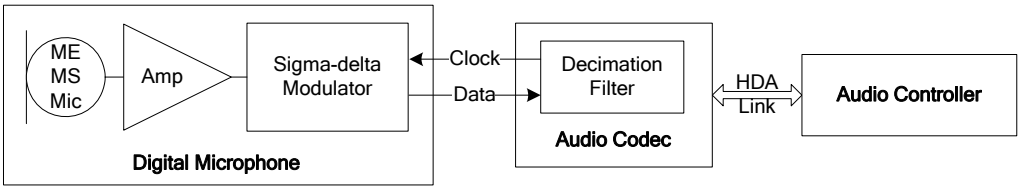
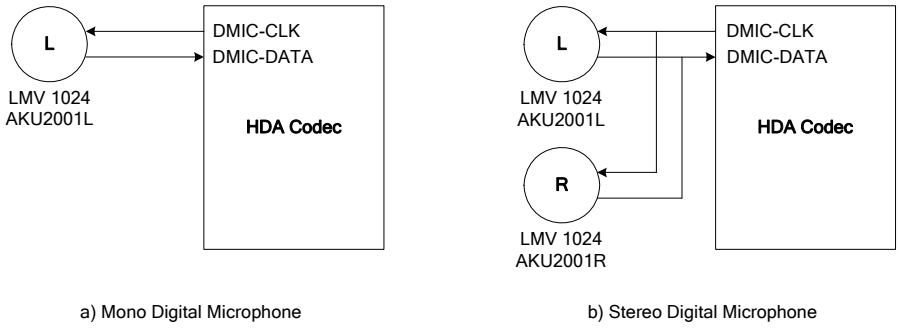


Figure 20 – Digital Microphone Implementation 1

This codec supports a two-wire interface for the digital microphone and operates in single channel (mono type) or stereo channels (stereo mode) of digital microphones. One pin is clock output to the digital microphone, and the other is a serial pin.



a) Mono Digital Microphone

b) Stereo Digital Microphone

Figure 21 – Digital Microphone Implementation 2

8.7 GPIO Implementation

- GPIO Application
  - Volume Control (Up, Down, Mute) Via GPIO0 / GPIO1
    Detect low pulses generated at GPIO0 and GPIO1, and use them to calculate the Up and Down count into 6 bits of volume steps. "Mute" is also sampled by 0.1 ms to toggle the mute status. Hardware will not adjust volume. The count value will be reported via unsolicited response to software to control the master volume.

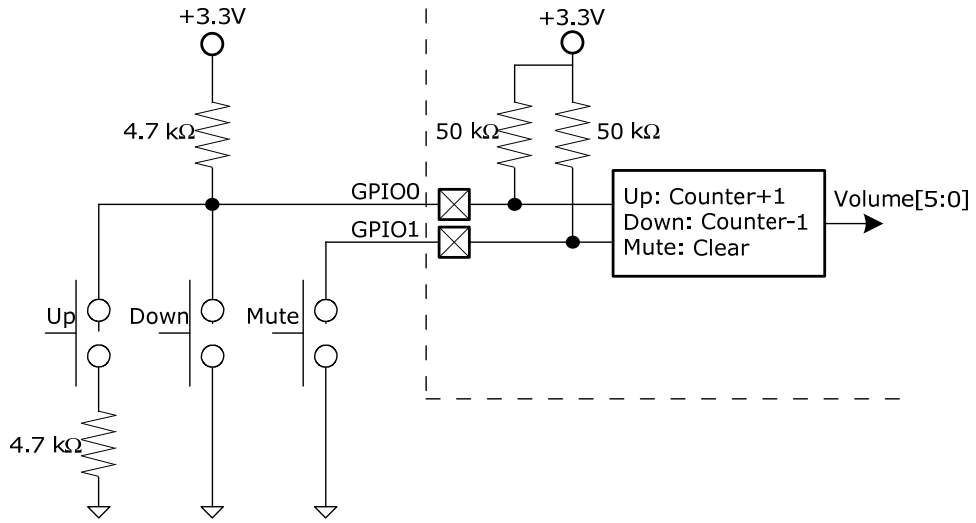


Figure 22 – Digital Volume Control Implementation

  - Front Panel Sense
  - De-pop or EAPD via GPIO

9 Electrical Specification

Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit	Note
T_S	Storage Temperature	-55	125	°C	—
T_A	Ambient Operating Temperature	0	85	°C	—
V_{ESD}	Electrostatic Discharge (human body model)	—	2	kV	—

Note: Stress above conditions may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit	Note
DVDD	Digital Power Supplies	3.135	3.3	3.465	V
AVDD	Analog Power Supplies (preferred)	–	5	–	V
AVDD	Analog Power Supplies (for low-power apps)	–	3.3	–	V

Digital DC and AC Characteristics

DC Performance Characteristic

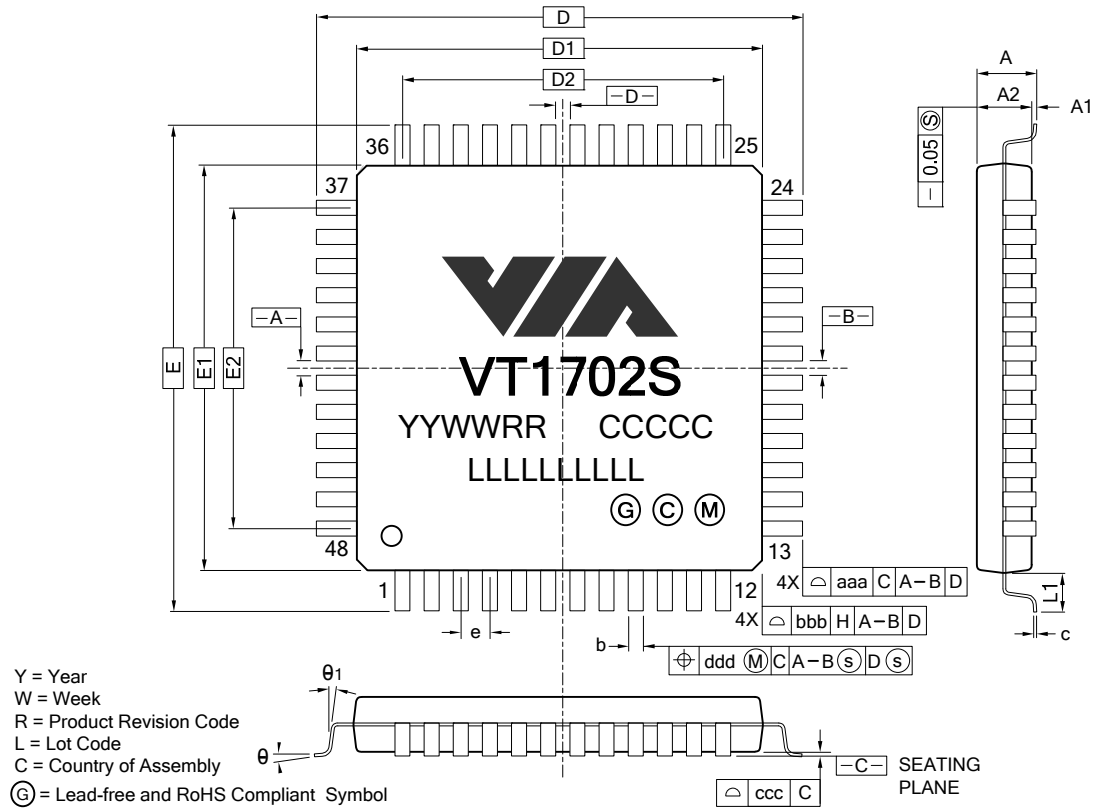
Symbol	Parameter	Min	Max	Unit	Note
V_{IN}	Input Voltage Range	-0.3	–	DVDD+0.3	V
V_{IL}	Low Level Input Voltage	–	–	0.35xDVDD	V
V_{IH}	High Level Input Voltage	0.65xDVDD	–	–	V
V_{OH}	High Level Output Voltage	0.9xDVDD	–	–	V
V_{OL}	Low Level Output Voltage	–	–	0.1xDVDD	V
	Input Leakage Current (AC-Link inputs)	-10	–	10	µA
	Output Leakage Current (Hi-Z'd AC-Link outputs)	-10	–	10	µA
	Input / Output Pin Capacitance	–	–	7.5	pF

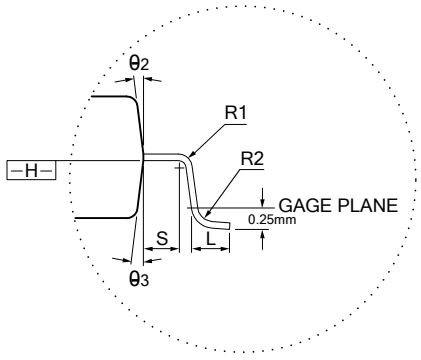
Analog Performance Characteristics

Parameter	Min	Type	Max	Unit
Analog Input				
Full Scale Input Voltage	–		–	
Line Inputs		1.0		Vrms
Mic Inputs with 20dB Gain		0.1		
Mic inputs with 0dB Gain		1		
Input Impedance	10	–	–	kΩ
Input Capacitance	–	7.5	–	pF
Analog Output				
Full Scale Output Voltage	–			
Line Output		1.0		Vrms
Headphone Output			1.41	
Analog S/N	–		–	
Other to LINE_OUT		100		dB
Analog Frequency Response	20	–	20,000	Hz
Vrefout	–	2.25-2.75	–	V
ADC Converters				
Digital S/N	–	100	–	dB
Total Harmonic Distortion	–	–	0.003	%
Frequency Response	20	–	19,200	Hz
Transition Band	19,200	–	28,800	Hz
Stop Band	28,800	–	–	Hz
Stop Band Rejection	-74	–	–	dB
Out-of-Band Rejection	–	-40	–	dB
Spurious Tone Reduction	–	-100	–	dB
Attenuation, Gain Step Size	–	1.5	–	dB
DAC Converters				
Digital S/N	–	100	–	dB
Total Harmonic Distortion	–	–	0.003	%
Frequency Response	20	–	19,200	Hz
Transition Band	19,200	–	28,800	Hz
Stop Band	28,800	–	–	Hz
Stop Band Rejection	-74	–	–	dB
Out-of-Band Rejection	–	-40	–	dB
Channel Separation	–	-90	–	dB
Spurious Tone Reduction	–	-100	–	dB
Attenuation, Gain Step Size	–	1.5	–	dB

Note: The frequency response, transition band and stop band specified in the table is based on fs = 48 kHz, and scale with fs.

10 Mechanical Specification





NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

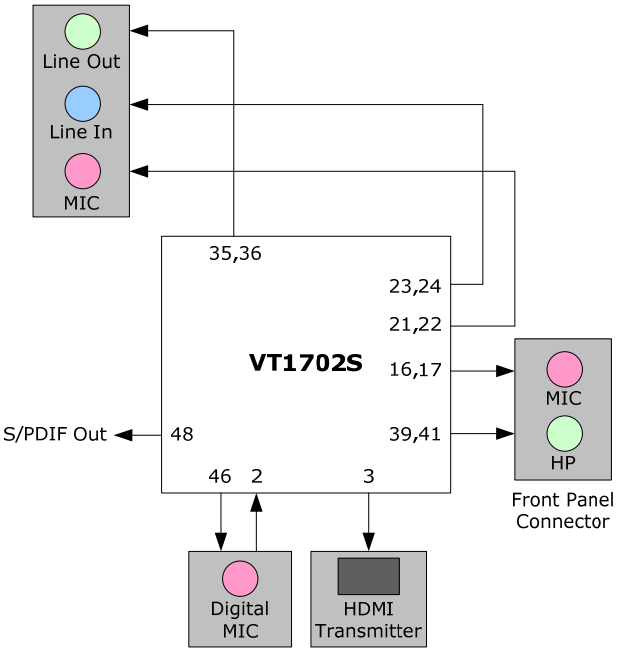
CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BASIC			0.354 BASIC		
E	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E1	7.00 BASIC			0.276 BASIC		
D2	5.50 BASIC			0.217 BASIC		
E2	5.50 BASIC			0.217 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

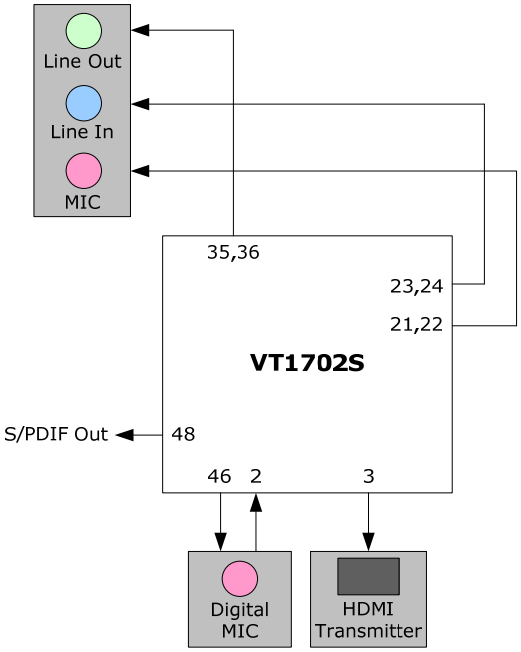
Figure 23 – VT1702S LQFP-48 Package (7 mm×7 mm)

11 Application Circuit

11.1 The System with Front Panel Design



11.2 The System without Front Panel Design



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