



## Data Sheet

VT1705  
High Definition Audio Codec

June 11, 2009  
Revision 1.1



## Table of Contents

Revision History .....	i
Table of Contents .....	ii
List of Figures .....	iii
List of Tables .....	iii
1 Product Features .....	1
1.1 Hardware Features .....	1
1.2 Software Features .....	2
2 Overview .....	3
3 Functional Block Diagram .....	4
4 Pinout .....	5
5 Pin List .....	6
6 Pin Description .....	7
6.1 Digital I/O Pins .....	7
6.2 Analog I/O Pins .....	7
6.3 Power and Ground .....	8
6.4 NC Pins (Pins with No Connection) .....	8
7 High Definition Audio Link Protocol .....	9
7.1 Link Signaling .....	9
7.2 Signal Definitions .....	9
7.3 Signaling Topology .....	11
7.4 Frame Composition .....	11
7.5 Output Frame .....	13
7.6 Input Frame .....	14
7.7 Reset and Initialization .....	15
7.8 Handling Stream Independent Sample Rates .....	19
7.9 Power Management .....	20
7.10 Unsolicited Response Behavior Description .....	20
8 Widget Description .....	21
8.1 Node ID List .....	21
8.2 Root Node (Node ID = 00) .....	22
8.3 Audio Function Group (Node ID = 01) .....	23
8.4 Audio Analog Output Converter Widget (Node ID = 10h, 11h, 25h) .....	27
8.5 Audio Digital Output Converter (S/PDIF TX) Widget (Node ID = 12h, 15h) .....	31
8.6 Audio Analog Input Converter Widget (Node ID = 13h, 14h) .....	35
8.7 Mixer Widget (Node ID = 16h) .....	40
8.8 Selector Widget SW0 (Node ID = 17h) .....	43
8.9 Selector Widget SW1-SW2 (Node ID = 18h, 27h) .....	45
8.10 Pin Widget PW0 (Node ID = 19h) .....	48
8.11 Pin Widget PW3 (Node ID = 1Ch) .....	52
8.12 Pin Widget PW4 (Node ID = 1Dh) .....	57
8.13 Pin Widget PW7 (Node ID = 23h) .....	63
8.14 Pin Widget PW1, PW2 (Node ID = 1Ah, 1Bh) .....	67
8.15 Pin Widget PW5 (Node ID = 1Eh) .....	73
8.16 Pin Widget PW8 (Node ID = 1Fh) CD Analog Input .....	79
8.17 Pin Widget PW9 (Node ID = 20h ) S/PDIF TX Pin .....	82
8.18 Pin Widget PW10 (Node ID = 21h ) HDMI Audio Output Pin .....	85
9 Functional Descriptions .....	88
9.1 Clock Control .....	88
9.2 Interpolation / Decimation .....	88
9.3 HPF for ADC DC Removal .....	88
9.4 Audio Jack Detection Circuits .....	89
9.5 Internal Loop-back and Peak Detection for Low Cost Production Test .....	89
9.6 GPIO Implementation .....	89
10 Electrical Specification .....	90
11 Mechanical Specification .....	92
12 Application Circuit .....	93

## List of Figures

Figure 1 – VT1705 Functional Block Diagram .....	4
Figure 2 – VT1705 Pin Diagram for LQFP-48 (Top View) .....	5
Figure 3 – High Definition Audio Link Conceptual View .....	9
Figure 4 – Bit Timing Diagram .....	10
Figure 5 – SYNC and SDO Timing Relative to BITCLK .....	10
Figure 6 – SDI Timing Relative to BITCLK .....	10
Figure 7 – Basic High Definition Audio System .....	11
Figure 8 – Frames Demarcation .....	11
Figure 9 – Frame Composition .....	12
Figure 10 – Outbound Stream Tag Format and Transmission .....	13
Figure 11 – Outbound Frame with Null Field .....	13
Figure 12 – Inbound Tag Format and Transmission .....	14
Figure 13 – Inbound Frame with No Null Field .....	14
Figure 14 – Link Reset Entry Sequence .....	15
Figure 15 – Link Reset Exit Sequence .....	15
Figure 16 – Codec Initialization Sequence .....	16
Figure 17 – Connect and Turnaround Frames .....	17
Figure 18 – Address Frame .....	18
Figure 19 – Jack Detect Circuit .....	89
Figure 20 – VT1705 LQFP-48 Package (7 mm×7 mm) .....	92
Figure 21 – The System with Front Panel Design .....	93
Figure 22 – The System without Front Panel Design .....	93
Figure 23 – The System with Only One Back Panel Connector Design .....	94

## List of Tables

Table 1 – VT1705 Pin List .....	6
Table 2 – Signal Type Definitions .....	7
Table 3 – High Definition Audio Link Signal Description .....	9
Table 4 – Sample Rate Supported .....	19
Table 5 – Node ID List .....	21







### 3 Functional Block Diagram

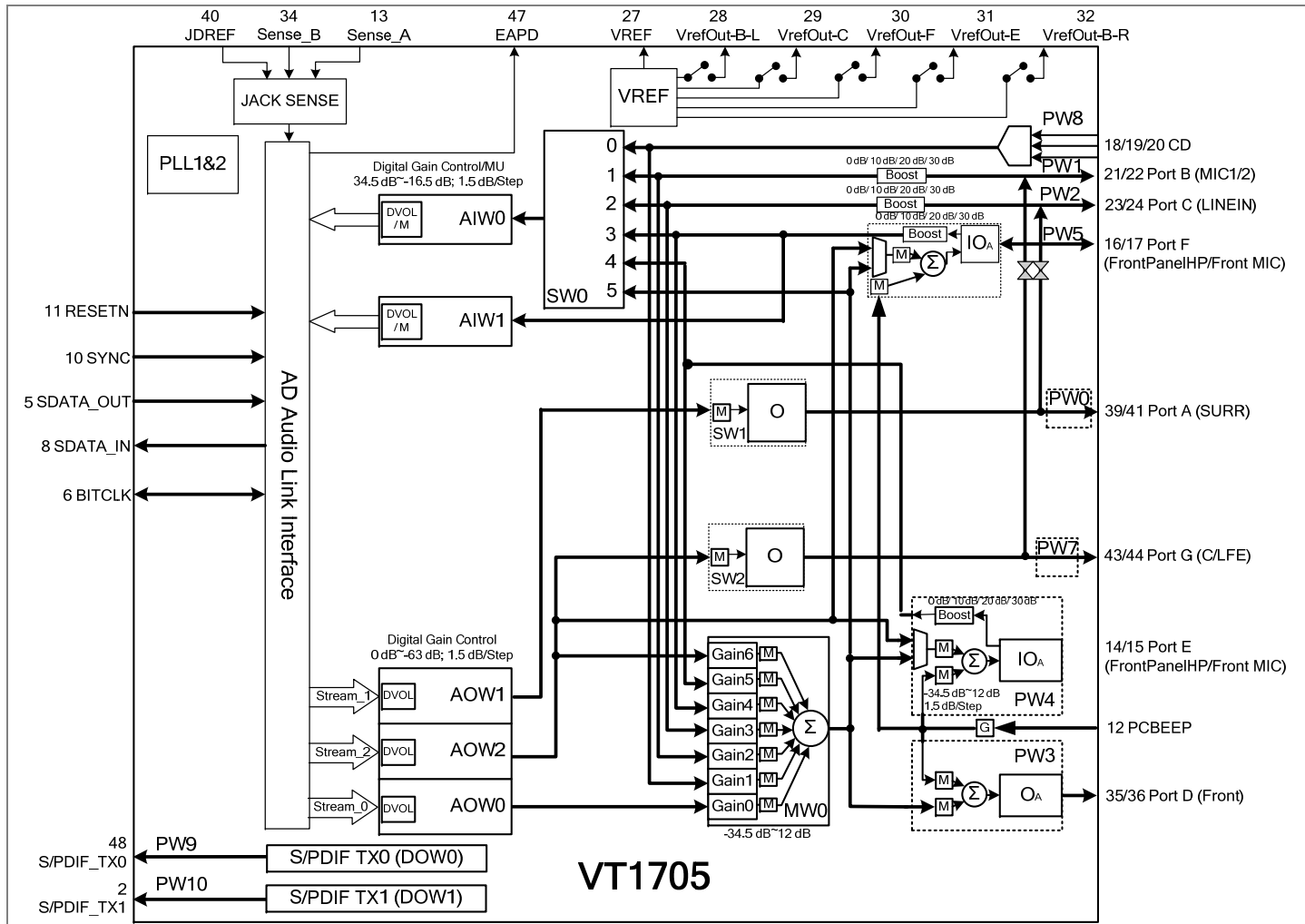


Figure 1 – VT1705 Functional Block Diagram



## 4 Pinout

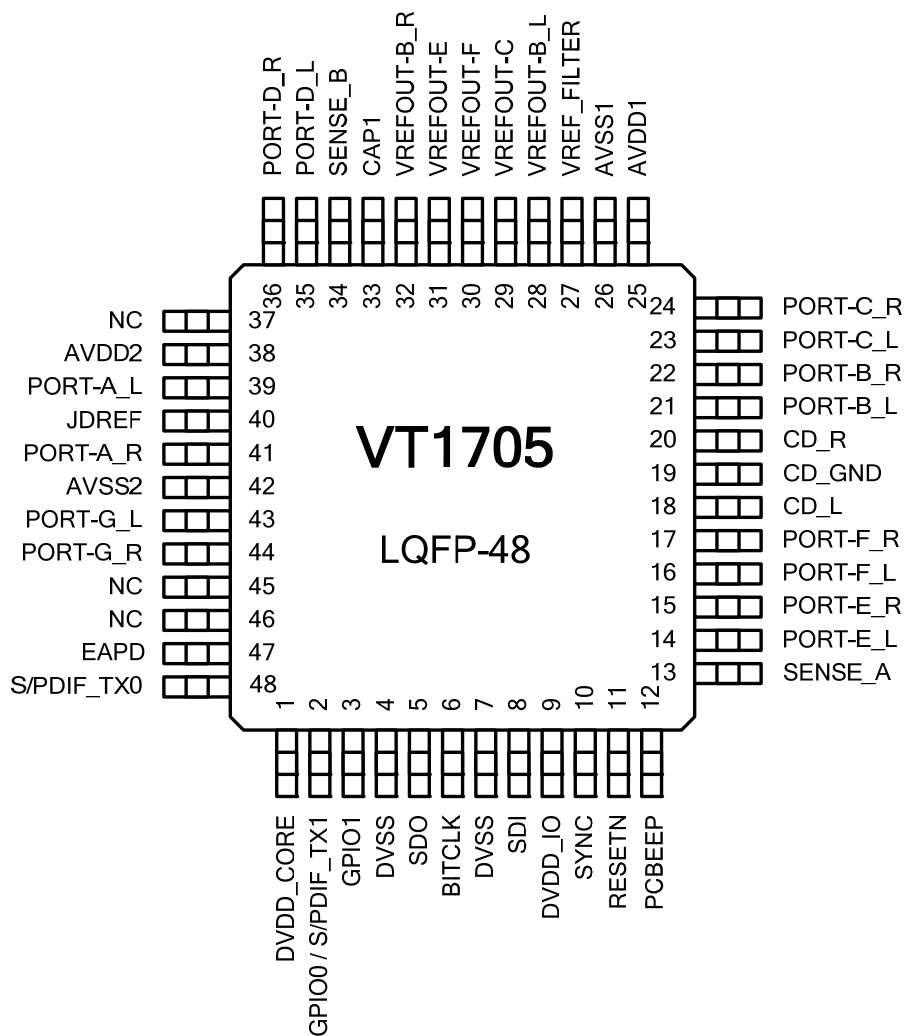


Figure 2 – VT1705 Pin Diagram for LQFP-48 (Top View)

## 5 Pin List

Table 1 – VT1705 Pin List

<b>Pin</b>	<b>Pin Name</b>	<b>Pin</b>	<b>Pin Name</b>
1	DVDD_CORE	25	AVDD1
2	GPIO0 / S/PDIF_TX1	26	AVSS1
3	GPIO1	27	VREF_FILTER
4	DVSS	28	VREFOUT-B_L
5	SDO	29	VREFOUT-C
6	BITCLK	30	VREFOUT-F
7	DVSS	31	VREFOUT-E
8	SDI	32	VREFOUT-B_R
9	DVDD_IO	33	CAP1
10	SYNC	34	SENSE_B
11	RESETN	35	PORT-D_L (Front Left)
12	PCBEEP	36	PORT-D_R (Front Right)
13	SENSE_A	37	NC
14	PORT-E_L (Front HP Left)	38	AVDD2
15	PORT-E_R (Front HP Right)	39	PORT-A_L (Surround Left)
16	PORT-F_L (Front MIC 1)	40	JDREF
17	PORT-F_R (Front MIC 2)	41	PORT-A_R (Surround Right)
18	CD_L	42	AVSS2
19	CD_GND	43	PORT-G_L (Center / LFE)
20	CD_R	44	PORT-G_R (LFE / Center)
21	PORT-B_L (Mic 1)	45	NC
22	PORT-B_R (Mic 2)	46	NC
23	PORT-C_L (Line in L)	47	EAPD
24	PORT-C_R (Line in R)	48	S/PDIF_TX0

## 6 Pin Description

Table 2 – Signal Type Definitions

Type	Description
I	<b>Input.</b> Standard input-only signal.
O	<b>Output.</b> Standard active output driver.
IO	<b>Input/output.</b> An input/output signal.
P	<b>Power.</b>

### 6.1 Digital I/O Pins

Pin Name	Pin #	I/O	Signal Description
GPIO0 / S/PDIF_TX1	2	IO	General Purpose Input/Output 0 / The Second S/PDIF Output
GPIO1	3	IO	General Purpose Input/Output 1
SDO	5	I	Serial Data Input from Controller
BITCLK	6	I	24 MHz Bit Clock from Controller
SDI	8	IO	Serial Data Output to Controller
SYNC	10	I	Sample SYNC from Controller
RESETN	11	I	Hardware Reset from Controller
EAPD	47	O	External Amplifier Power-Down
S/PDIF_TX0	48	O	The First S/PDIF Output

### 6.2 Analog I/O Pins

Pin Name	Pin #	I/O	Signal Description
SENSE_A	13	I	Jack Detect Pin 1
SENSE_B	34	I	Jack Detect Pin 2
PORT-E_L	14	IO	Analog I/O. The default setting is output for Front Panel HP Out Left.
PORT-E_R	15	IO	Analog I/O. The default setting is output for Front Panel HP Out Right.
PORT-F_L	16	IO	Analog I/O. The default setting is input for Front MIC.
PORT-F_R	17	IO	Analog I/O. The default setting is input for Front MIC.
CD-L	18	I	CD Input Left Channel
CD-R	20	I	CD Input Right Channel
PORT-B_L	21	IO	Analog I/O. The default setting is input for MIC1 Left.
PORT-B_R	22	IO	Analog I/O. The default setting is input for MIC1 Right.
PORT-C_L	23	IO	Analog I/O. The default setting is input for Line-in Left.
PORT-C_R	24	IO	Analog I/O. The default setting is input for Line-in Right.
PORT-D_L	35	O	Analog Output for Line-out Left
PORT-D_R	36	O	Analog Output for Line-out Right
PORT-A_L	39	O	Analog Output for Surround-out Left
PORT-A_R	41	O	Analog Output for Surround-out Right
PORT-G_L	43	O	Analog Output for Center Line Out.
PORT-G_R	44	O	Analog Output for LFE (Low-Frequency Effect) Line Out
PCBEEP	12	I	PC Beep Signal Input
VREF_FILTER	27	O	Reference Voltage Capacitor
VREFOUT-B_L	28	O	Reference Voltage Output for Port B Left

VREFOUT-C	29	O	Reference Voltage Output for Port C
VREFOUT-F	30	O	Reference Voltage Output for Port F
VREFOUT-E	31	O	Reference Voltage Output for Port E
VREFOUT-B_R	32	O	Reference Voltage Output for Port B Right
CAP1	33	O	Optional Capacitor for ADC Reference
JDREF	40	O	External Resistor for Jack Detect Circuit

### 6.3 Power and Ground

Pin Name	Pin #	I/O	Signal Description
DVDD_CORE	1	P	Digital Core Power. 3.3V
DVDD_IO	9	P	Digital Power for HDA Link. 1.5V~3.3V
DVSS	4	P	Digital VSS
DVSS	7	P	Digital VSS
CD_GND	19	-	CD Ground
AVDD1	25	P	Analog VDD
AVDD2	38	P	Analog VDD
AVSS1	26	P	Analog VSS
AVSS2	42	P	Analog VSS

### 6.4 NC Pins (Pins with No Connection)

Pin Name	Pin #	I/O	Signal Description
NC	37	-	No Connection
NC	45	-	No Connection
NC	46	-	No Connection

## 7 High Definition Audio Link Protocol

### 7.1 Link Signaling

The link protocol defines the digital serial interface that connects High Definition Audio codec to the audio controller, and is not compatible with the previous AC97 protocol. The link is controller synchronous, based on a fixed 24MHz BITCLK and is purely isochronous without any flow control.

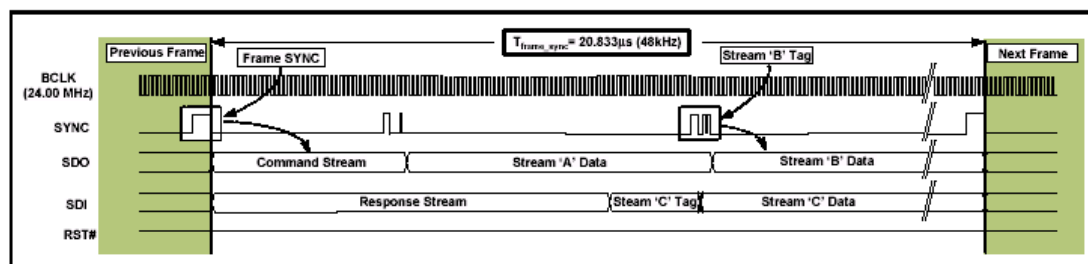


Figure 3 – High Definition Audio Link Conceptual View

### 7.2 Signal Definitions

Table 3 – High Definition Audio Link Signal Description

Signal Name	Source	Type	Description
BITCLK	Controller	I	24 MHz Clock
SYNC	Controller	I	Global 48 kHz Frame Sync and Outbound Tag Signal.
SDO	Controller	I	Bussed Serial Data Output from Controller.
SDI	Codec & controller	IO	Point-to-point Serial Data. The controller has a weak pull down.
RESETN	Controller	I	Global Active Low Reset Signal.

**BITCLK** is the 24 MHz clock sourced from the controller and connecting to all codec on the link.

**SYNC** marks input and output frame boundaries (Frame Sync) as well as identifying outbound data streams (stream tags). SYNC is always sourced from the controller and connects to all codec on the link.

**SDO** is driven by the controller to all codec on the link. Compared with AC97, the SDO is double pumped with respect to both rising and falling edges of BITCLK in order to increase the bandwidth required for High Definition Audio link.

**SDI** is a point-to-point data signal driven by the codec to the controller. Because the bandwidth requirement is not that high compared with SDO, the data is single pumped with respect to only the rising edge of BITCLK. The controller is required to implement weak pull-down on all SDI signals.

**RESETN** is sourced from the controller and connects to all codec on the link. Assertion of RESETN results in all link interface logic being reset to Default power on state.

The following figure shows the timing diagram of BITCLK, SYNC, SDO and SDI.

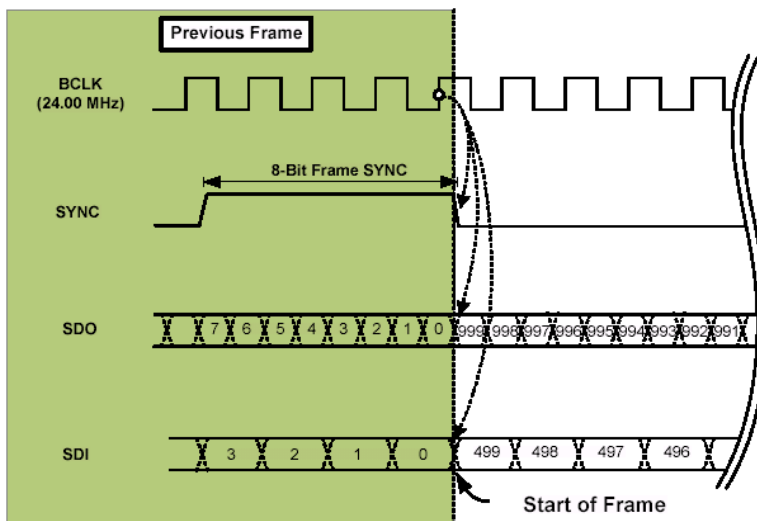


Figure 4 – Bit Timing Diagram

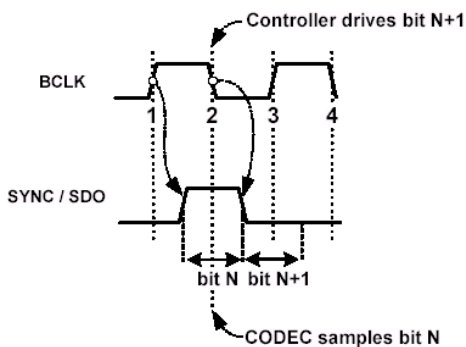


Figure 5 – SYNC and SDO Timing Relative to BITCLK

Figure 5 shows that both SYNC and SDO may be toggled with respect to either edge of BITCLK. In particular, bit cell n+1 is driven by the controller on SDO with respect to clock edge #2, and is sampled by the codec with respect to the subsequent clock edge, #3, and so forth.

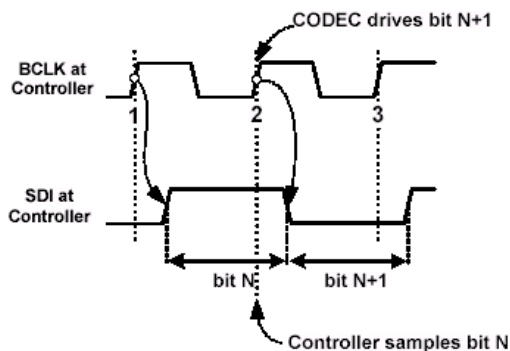


Figure 6 – SDI Timing Relative to BITCLK

Figure 6 shows that SID may only be toggled with respect to the rising edge of BITCLK. In particular, bit cell n+1 is driven by the codec on SDI with respect to rising clock edge #2 and is sampled by the controller with respect to the subsequent rising clock edge, #3, and so forth.

### 7.3 Signaling Topology

The following diagram shows a typical system with one controller and its associated codec.

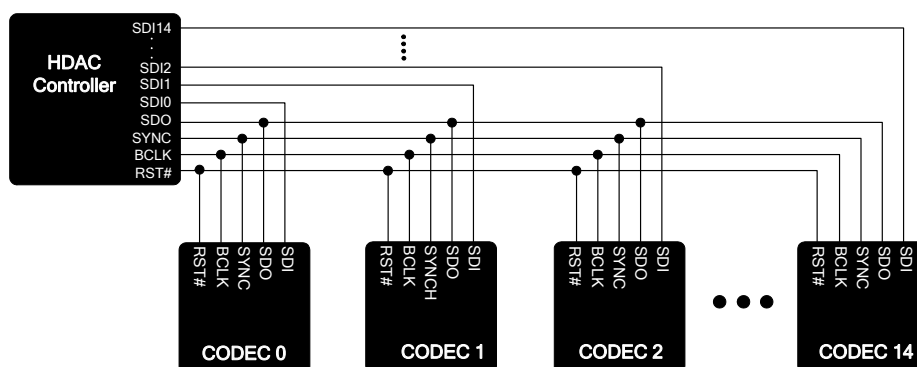


Figure 7 – Basic High Definition Audio System

### 7.4 Frame Composition

A frame is defined as a 20.833  $\mu$ s window of time marked by the falling edge of the Frame Sync marker, which identifies the start of each frame. The controller is responsible for generating the Frame Sync marker, which is a high-going pulse on SYNC, exactly four BITCLK in width.

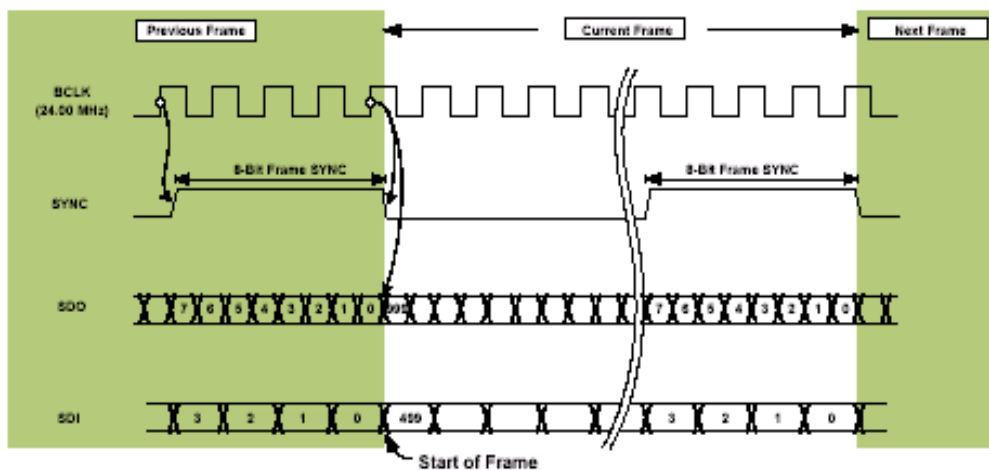


Figure 8 – Frames Demarcation

Both inbound and outbound frames are made up of three major components, specifically:

- A single Command / Response Field
- Zero or more Stream Packets
- A Null Field to fill out the frame

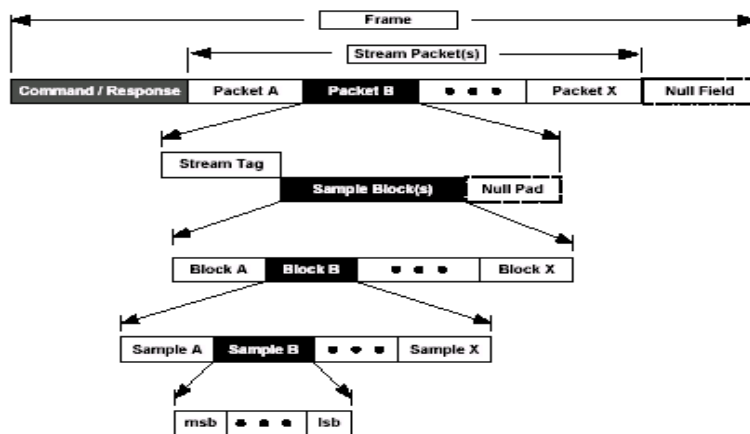


Figure 9 – Frame Composition

**Command / Response Field** is used for link and codec management. One of these fields appears exactly once per frame, MSB first, and is always the first field in the frame. It is composed of a 40-bit Command Field on each outbound frame from the controller and a 36-bit Response Field on each inbound frame from the codec.

**Stream Tag** is the label at the beginning of each stream packet that provides the associated stream ID. All data in one stream packet belongs to a single stream.

**Sample Block** is a set of one or more samples, the number of which is specified by the “Channels” field of the Stream Descriptor Format registers. Samples in a given sample block are associated with a single given stream, have the same sample size, and have the same time reference. And no padding is permitted between samples.

Ordering of samples within a block is always the same for all blocks in a given stream.

**Sample** is a set of bits providing a single sample point of a single analog waveform.

**Null Field** is used to fill up the remainder of the bits in each frame that are not used for Command / Response or packets. A null field must be transmitted as logical 0’s.



## 7.5 Output Frame

### 7.5.1 Stream Tags

Outbound stream tags are 8 bits in length and are transmitted at a double pumped rate as side band information on SYNC. It is composed of a 4-bit preamble which is signaled as three SDO bit times high followed by one SDO bit time low. This is immediately followed by a 4-bit Stream ID. Outbound stream tags are transmitted on SYNC so as to align with the last eight data bits of the preceding stream packet or Command Field.

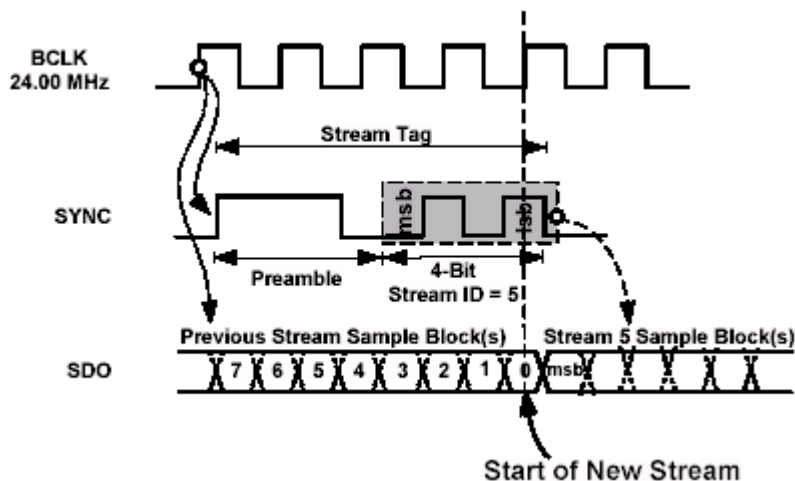


Figure 10 – Outbound Stream Tag Format and Transmission

### 7.5.2 Outbound Frames

Outbound frames start and end between the falling edges of successive Frame Syncs. The first 40 bits are dedicated for the Command field and are used to send commands to codec. The controller transmits the tag for the first outbound packet on SYNC during the last eight bit times of the Command field. The sample blocks for the first packet are transmitted on SDO immediately following the Command field. There's no proscribed order in which the different stream packets are to be transmitted. Controllers are required to transmit a null field for the remaining bits within an outbound frame when the transmission of the stream packets completes before the end of the frame.

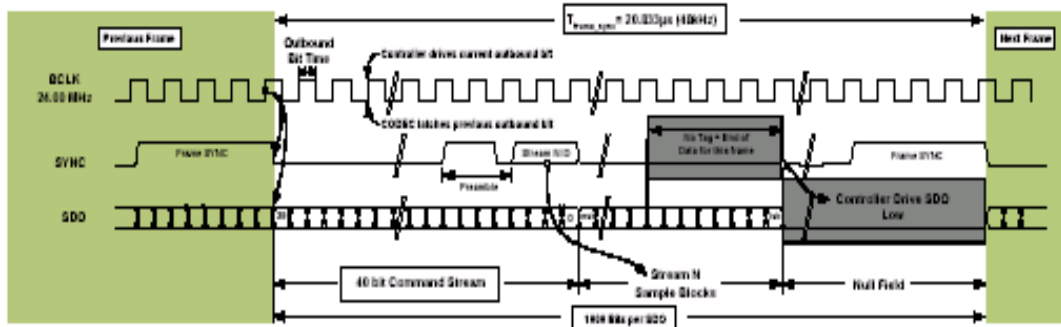


Figure 11 – Outbound Frame with Null Field

## 7.6 Input Frame

### 7.6.1 Stream Tags

An inbound stream tag is 10 bits in length, and is transmitted "in-line" at a single pumped rate on SDI, immediately preceding the associated inbound sample blocks. It is composed of a 4-bit stream ID, followed by a 6-bit data length field that provides the length, in bytes, of all sample blocks with the given stream packet.

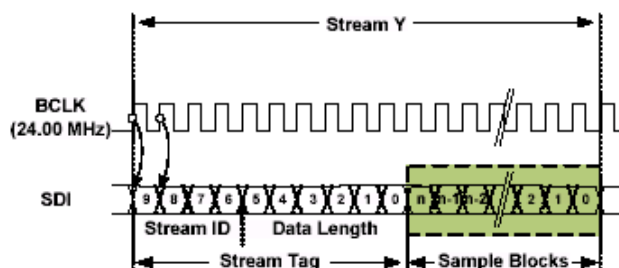


Figure 12 – Inbound Tag Format and Transmission

### 7.6.2 Inbound Frames

Inbound frames start and end between the falling edges of successive Frame Syncs. The first 36 bits of an inbound frame are dedicated for the Response Field, which codec use for sending responses to controller commands. The codec transmits the first stream packet on SID immediately following the Response Field. A stream tag indicating a packet length of zero must immediately follow the last stream packet to be transmitted. Such a stream tag marks the completion of data transmission within that frame, and the remaining valid bit positions are set to the null field. In the event there are less than 10 valid bit positions remaining in the frame after the last stream packet, then no termination tag is transmitted, and the remaining bits are the null field.

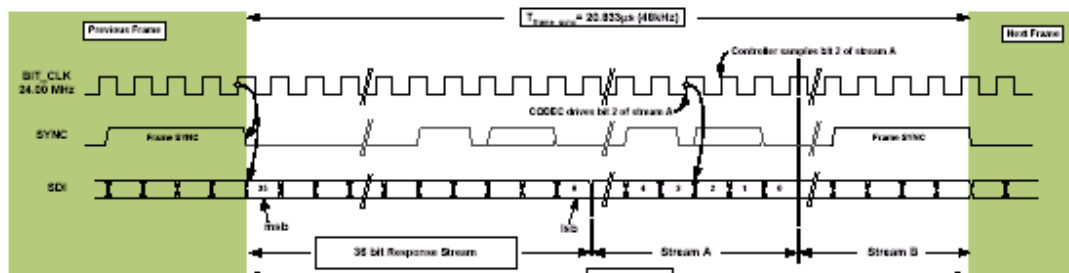


Figure 13 – Inbound Frame with No Null Field



The sequence when exiting link reset is described in the following.

1. The controller provides a properly running BITCLK for a minimum of 100  $\mu$ s (2400 BITCLK cycles or more) before the de-assertion of RESETN. This allows time for codec PLLs to lock.
2. The RESETN signal is de-asserted.
3. The SYNC commences signaling valid frames on the link with the first Frame Sync that occurs at a minimum of four BITCLK cycles after the de-assertion of RESETN.
4. Codec must signal an initialization request via SDI within the first 25 Frame Syncs relative to the de-assertion of their respective RESETN signal.

### 7.7.2 Codec Function Group Reset

A codec function group reset is initiated via the Function\_Reset verb and results in all logic within the targeted function group being driven to its Default or reset state. By Default VT1705 does not signal a state change and initialization request on SDI after the Function\_Reset verb, and still keeps its codec address previously assigned by the controller. This behavior can be changed by setting a vendor defined register bit for backward compatible with the High Definition Audio Spec. See the Vendor Defined verbs in the Audio Function Group for the detail.

### 7.7.3 Codec Initialization

Immediately following the completion of Link Reset sequence ( or Function\_Reset verb, if enabled by the vendor-defined verb), VT1705 proceeds through a codec initialization sequence, which provides each codec with a unique address by which it can thereafter be referenced to Commands on the SDO signal. During this sequence, the controller provides each requesting codec with a unique address using its attached SDI signals.

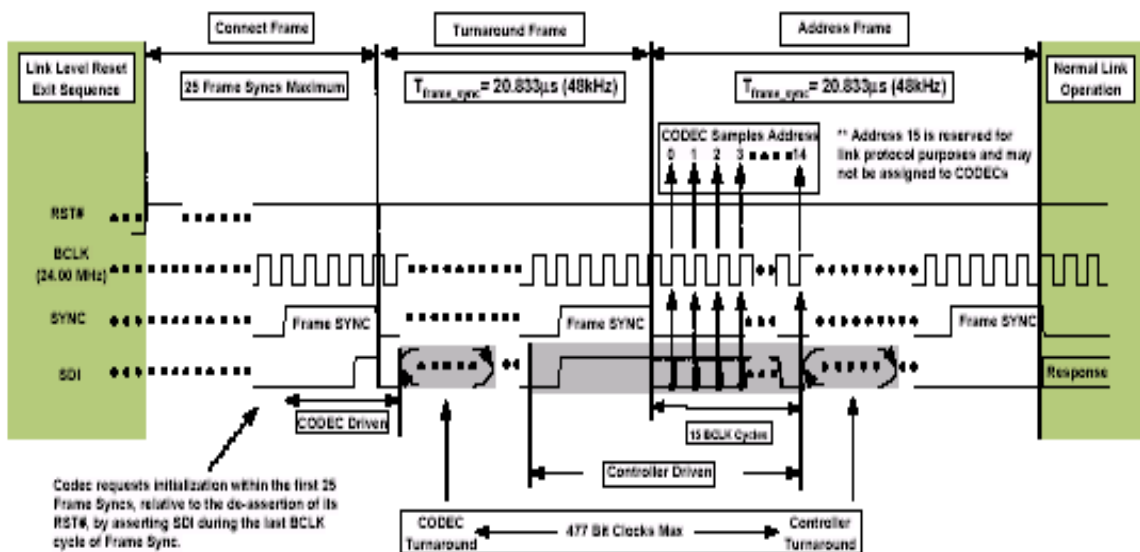


Figure 16 – Codec Initialization Sequence

The codec initialization sequence occurs across three contiguous frames immediately following any reset sequence. During these three frames, the codec is required to ignore all outbound traffic present on SYNC & SDO. These three frames, labeled as the “Connect Frame”, the “Turnaround Frame”, and the “Address Frame”, are described in the following sub-section.

### 7.7.3.1 Connect and Turnaround Frames

In the Connect and Turnaround Frames, the codec signals its request for initialization on SDI and then releases SDI (turnaround) to be driven by the controller in the subsequent address frame.

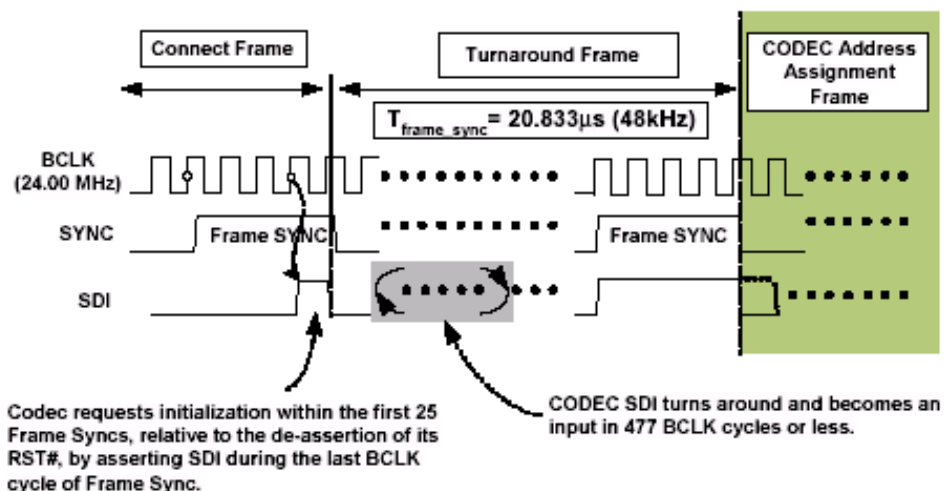


Figure 17 – Connect and Turnaround Frames

The codec signals an initialization request by synchronously driving SDI high during last bit clock cycle of Frame Sync. SDI must be asserted for the entire BITCLK cycle and must be synchronously de-asserted the same rising edge of BITCLK as the de-assertion of the Frame Sync. The codec are only permitted to signal an initialization request on a null input frame, a frame in which no response stream or input streams are being sent.

In the Turnaround Frame, the codec and controllers are required to turn SDI around upon the completion of the Connect Frame. To do this, the codec actively drives SDI low for one BITCLK cycle immediately following the de-assertion of SYNC at the end of the Connect Frame. The codec then puts its SDI drivers in a high impedance state at the end of the first BITCLK cycle in the Turnaround Frame. Four BITCLK cycles before the end of the Turnaround Frame, SYNC and SID are driven high by the controller. The SDI remains driven high through the end of the Turnaround Frame in preparation for the subsequent address frame.

### 7.7.3.2 Address Frames

During the Address Frame, SDI is a codec input and is driven by the controller beginning in the last four BITCLK periods (Frame Sync) of the Turnaround Frame. The falling edge of Frame Sync marks the start of codec address assignment. Address assignment is indicated by the controller holding each SDI high for the number of BITCLK cycles equal to the numeric ID of that particular SDI. Thus, the unique address of the codec becomes the ID of its attached SDI.

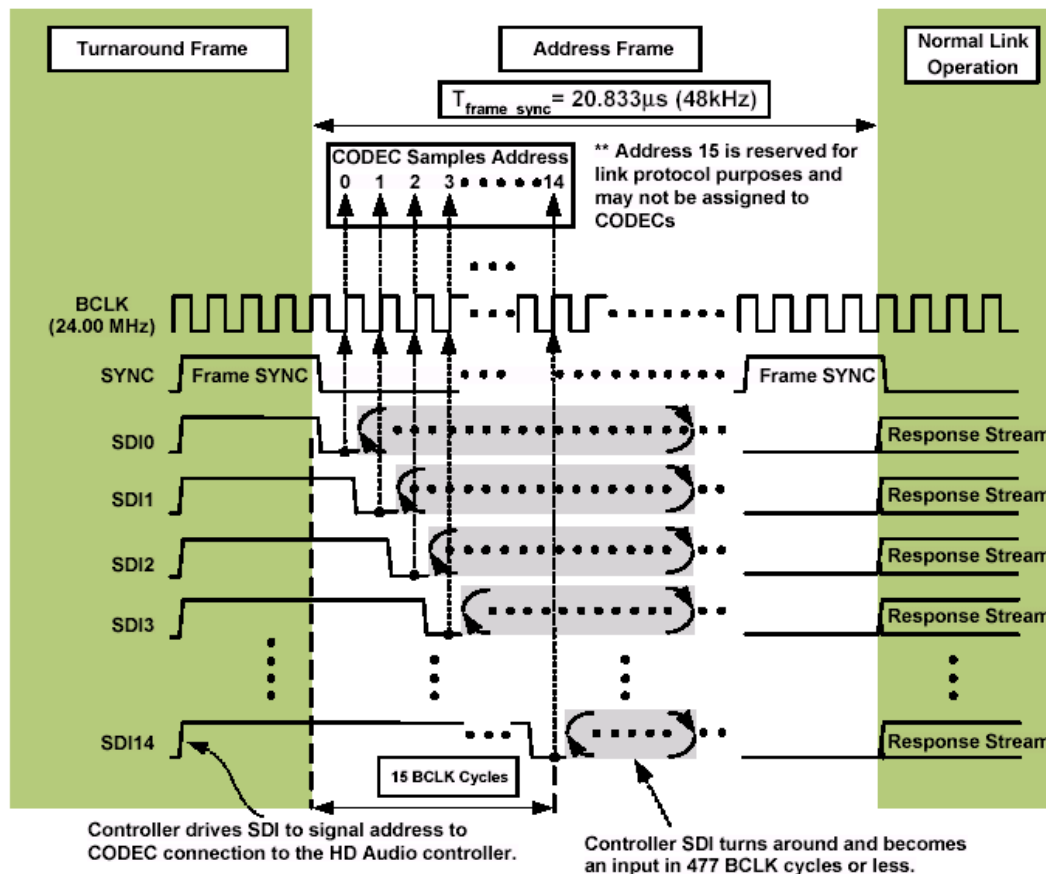


Figure 18 – Address Frame

The codec counts from zero to fourteen starting on the rising edge of BITCLK following the de-assertion of Frame Sync, and samples the value of this count for their unique address on the first rising edge of BITCLK in which SYNC and SDI are both sampled low.

The controller must put its SDI drivers in a high impedance state by the rising edge of the 18<sup>th</sup> BITCLK of the address frame but not before driving each SDI low for at least one clock cycle. The SDI then becomes an input to the controller. Normal link operation starts on the frame following the completion of the Address Frame, and the codec is required to actively drive a valid response field and to be ready to accept commands in this and subsequent frames.

## 7.8 Handling Stream Independent Sample Rates

Unlike AC97, the Link is source synchronous and has no codec initiated flow control, the controller generates all sample transfer timing.

### 7.8.1 Codec Sample Rendering Timing

VT1705 supports the all the multiples and submultiples of the base rates of 48 kHz & 44.1 kHz, up to the maximum rate respectively of the DAC and ADC. For DAC, up to 192 kHz sample rate is supported. For ADC, the maximum rate is 96 kHz.

Table 4 – Sample Rate Supported

Multiple	Base Rate 48 kHz	Base Rate 44.1 kHz
1/6	8 kHz	
1/4		11.025 kHz
1/3	16 kHz	
1/2		22.05 kHz
2/3	32 kHz	
1	48 kHz	44.1 kHz
2	96 kHz	88.2 kHz
4	192 kHz	176.4 kHz

### 7.8.2 Link Sample Delivering Timing

For streams whose sample rate is a natural harmonic of 48 kHz, the timing is relatively straightforward. The rates in multiple (N) of 48 kHz are containing N sample blocks in one frame. For the rates in sub-multiple (1/N) of 48 kHz, there must be one sample block transmitted every one in N frames, and the intervening N-1 frames will contain no sample for this stream.

Since the link frame rate is fixed at 48 kHz, streams using a base rate of 44.1 kHz must have samples transmitted on a cadence creating the slightly lower aggregate transmission rate to match the slightly lower rendering rate. For streams running at a sample rate of 44.1 kHz, there're occasional frames that will not contain a sample generating the following cadence.

**12-11-11-12-11-11-12-11-11-12-11-11-11- (repeat)**

The dashes indicate frames that do not contain a sample block. The cadence repeats continuously generating exactly 147 sample blocks every 160 frames, and avoids any long term drift between sample delivery and rendering clock.

Sample rates that are integral multiples of 44.1KHz apply the "12-11" cadence rule just as a 44.1KHz sample rate would, except that non-empty frames contain multiple ( 2 or 4 ) sample blocks, instead of just one.

For a sample rate of 22.05 kHz, the transmission pattern becomes:

**{12}-\*{11}-\*{11}-\*{12}-\*{11}-\*{11}-\*{12}-\*{11}-\*{11}-\*{12}-\*{11}-\*{11}-\*{11}-\* (repeat)**

where

**{12} = 1\*1\*1\*1\*1\*1\*1\*1\*1\*1\*1\*1\*1\*1\*1\***

**{11} = 1\*1\*1\*1\*1\*1\*1\*1\*1\*1\*1\***

and the asterisks \* represent a frame in which there is no sample block.

For a sample rate of 11.025 kHz, the transmission pattern becomes:

**[12]-\*\*\*[11]-\*\*\*[11]-\*\*\*[12]-\*\*\*[11]-\*\*\*[11]-\*\*\*[12]-\*\*\*[11]-\*\*\*[11]-\*\*\*[12]-\*\*\*[11]-\*\*\*[11]-\*\*\*[11]-\*\*\* (repeat)**

where

**[12] = 1\*\*\*1\*\*\*1\*\*\*1\*\*\*1\*\*\*1\*\*\*1\*\*\*1\*\*\*1\*\*\*1\*\*\*1\*\*\*1\*\*\*1\*\*\***

**[11] = 1\*\*\*1\*\*\*1\*\*\*1\*\*\*1\*\*\*1\*\*\*1\*\*\*1\*\*\*1\*\*\*1\*\*\***

and the asterisks \* represent a frame in which there is no sample block.

These framing sequences apply only to the outbound (SDO) data from the controller. Inbound (SDI) data transmitted by the codec is permitted to deviate for minimizing codec buffer management.





## 8 Widget Description

### 8.1 Node ID List

Table 5 – Node ID List

Node ID	Name	Input Connection List	Note
00	Root Node	N/A	
01	AFG	N/A	Audio Function Group
10	AOW0	N/A	Analog Output Widget 0
11	AOW1	N/A	Analog Output Widget 1
12	DOW0	N/A	Digital Output Widget 0 for S/PDIF TX0
13	AIW0	17	Analog Input Widget 0
14	AIW1	1E	Analog Input Widget 1
15	DOW1	N/A	Digital Output Widget 1 for S/PDIF TX1
16	MW0	10, 1A, 1B, 1D, 1E, 1F, 25	Analog Mixer
17	SW0	16, 1A, 1B, 1D, 1E, 1F	ADC Input Selection
18	SW1	11	AOW1 Mute
19	PW0	18	Port A
1A	PW1	27	Port B
1B	PW2	18	Port C
1C	PW3	16	Port D
1D	PW4	16, 25	Port E
1E	PW5	16, 25	Port F
1F	PW8	N/A	Pin Widget 8 for CD Input
20	PW9	12	Pin Widget 9 for S/PDIF TX0
21	PW10	15	Pin Widget 10 for S/PDIF TX1
22	VD4	N/A	Vendor Widget 4
23	PW7	27	Port G
24	VD5	N/A	Vendor Widget 5
25	AOW2	N/A	Analog Output Widget 2
26	VD6	N/A	Vendor Widget 6
27	SW2	25	AOW2 Mute

## 8.2 Root Node (Node ID = 00)

### 8.2.1 Get Parameter Verb (Verb ID = F00h)

#### Offset

##### Get Vendor ID (Payload = 00h)

Response: 1106 4397h

Bit	Attribute	Default	Description
31:16	R	1106h	Vendor ID
15:0	R	4397h	Device ID

#### Offset

##### Get Revision ID (Payload = 02h)

Response: 0010 0000h

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0001b	MajRev The major revision number (left of the decimal) of the High Definition Audio Spec to which the codec is fully compliant.
19:16	R	0	MinRev The minor revision number (right of the decimal) of the High Definition Audio Spec to which the codec is fully compliant.
15:8	R	0	Revision ID
7:0	R	0	Stepping ID

#### Offset

##### Get Subordinate Node Count (Payload = 04h)

Response: 0001 0001h

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:16	R	01h	Starting Node Number
15:8	R	0	Reserved
7:0	R	01h	Total Number of Nodes (Only 1 Audio Function Group in the Codec )

### 8.3 Audio Function Group (Node ID = 01)

#### 8.3.1 Get Parameter Verb (Verb ID = F00h)

##### Offset

**Get Subordinate Node Count (Payload = 04h)** Response: 0010 0018h

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:16	R	10h	Starting Node Number.
15:8	R	0	Reserved
7:0	R	18h	Total Number of Nodes

##### Offset

**Get Function Group Type (Payload = 05h)** Response: 0000 0001h

Bit	Attribute	Default	Description
31:9	R	0	Reserved
8	R	0	Unsolicited Response (Not supported)
7:0	R	01h	Audio Function Group

##### Offset

**Get Function Group Capabilities (Payload = 08h)** Response: 0000 0306h

Bit	Attribute	Default	Description
31:17	R	0	Reserved
16	R	0	Beep Gen
15:12	R	0	Reserved
11:8	R	3h	Input Delay
7:4	R	0	Reserved
3:0	R	6h	Output Delay

##### Offset

**Get Supported Power States (Payload = 0Fh)** Response: 0000 0000h

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	0	D3Sup
2	R	0	D2Sup
1	R	0	D1Sup
0	R	0	D0Sup

##### Offset

**Get GPIO Capabilities (Payload = 11h)** Response: 0000 0001h

Bit	Attribute	Default	Description
31	R	0	GPIOWake= 0
30	R	0	GPIOUnsol= 0, GPIO Unsolicited Response Supported.
29:24	R	0	Reserved
23:16	R	0	NumGPIs= 00h. No GPI Pin Supported
15:8	R	0	NumGPOs= 00h. No GPO Pin Supported
7:0	R	01h	NumGPIOs =01h. One GPIO Pin Supported When pin 2 is not configured as SPDIF_TX1 (F83h, bit4=0), the number of GPIO will be 2.

### 8.3.2 Subsystem ID Control Verb (Verb ID = F20h & 720h-723h)

	Description	Verb ID	Payload
Get	Get Subsystem ID	F20h	8'b0
Set1	Set Subsystem ID[7:0]	720h	Subsystem ID [7:0]
Set2	Set Subsystem ID[15:8]	721h	Subsystem ID [15:8]
Set3	Set Subsystem ID[23:16]	722h	Subsystem ID [23:16]
Set4	Set Subsystem ID[31:24]	723h	Subsystem ID [31:24]

#### Offset

#### Subsystem ID Register

Response: 1106 0000h

Bit	Attribute	Default	Description
31:16	RW	1106h	Manufacturer ID
15:8	RW	00h	Board SKU
7:0	RW	00h	Assembly ID

Note: All 32 bits in the Subsystem ID register are writeable, with the power-on default value of 1106 0000h. The system board BIOS can change the values during power up sequence to precisely describe the information about the motherboard so that the OS can load the correct driver.

### 8.3.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

#### Offset

#### The Whole Chip Power-down Control Register

Response: 0000 0000h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7:4	R	0	PS-Act. Same as PS-Set for AFG.
3:0	RW	0	PS-Set

### 8.3.4 GPIO Unsolicited Response (Verb ID = F08h & 708h)

	Description	Verb ID	Payload
Get	Get Unsolicited Response	F08h	8'b0
Set	Set Unsolicited Response	708h	Enable unsolicited response

#### Offset

#### GPIO Unsolicited Format

Response: 0000 0000h

Bit	Attribute	Default	Description
7	RW	0	Unsolicited Response Control 0: Unsolicited Response Disabled 1: Unsolicited Response Enabled
6	R	0	Reserved
5:0	RW	0	Tag Used by software to determine which node generated the unsolicited response.



### 8.3.8 GPIO Unsolicited Response Enable Mask (Verb ID = F19h & 719h)

	Description	Verb ID	Payload
Get	Get GPIO Unsolicited Response Enable Mask Response	F19h	8'b0
Set	Set GPIO Unsolicited Response Enable Mask	719h	GPIO Unsolicited Response Enable Mask[7:0]

#### Offset

#### Get/ Set GPIO Unsolicited Response Enable Mask Format

Response: 0000 0000h

Bit	Attribute	Default	Description
31:2	R	0	Reserved
1	RW	0	0: An unsolicited response will NOT be sent when a GPIO1 line changes state. 1: An unsolicited response will be sent when a GPIO1 line changes state.
0	RW	0	0: An unsolicited response will NOT be sent when a GPIO0 line changes state. 1: An unsolicited response will be sent when a GPIO0 line changes state.

### 8.3.9 Vendor Defined Verbs (Verb ID = F70h – F74h) - Reserved

### 8.3.10 Vendor Defined Verbs (Verb ID = F78h – F7Ch) - Reserved

### 8.3.11 Vendor Defined Verbs (Verb ID = F80h – F84h) - Reserved

### 8.3.12 Vendor Defined Verbs (Verb ID = F88h – F8Ch) – Reserved

### 8.3.13 Vendor Defined Verbs (Verb ID = F90h – F94h) - Reserved

### 8.3.14 Vendor Defined Verbs (Verb ID = F98h – F9Ch) - Reserved

### 8.3.15 Vendor Defined Verbs (Verb ID = FA0h – FA4h) - Reserved

### 8.3.16 Vendor Defined Verbs (Verb ID = FA8h – FACH) - Reserved

### 8.3.17 Function Reset Verb (Verb ID = 7FFh)

	Description	Verb ID	Payload
Set	Function Reset	7FFh	8'b0

## 8.4 Audio Analog Output Converter Widget (Node ID = 10h, 11h, 25h)

### 8.4.1 Get Parameter Verb (Verb ID = F00h)

#### Offset

#### Audio Widget Capabilities (Payload = 09h)

Response: 0000 041Dh

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0	Audio Output Converter Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	0	Analog Widget, not Digital
8	R	0	Connection List is not Present
7	R	0	Does not Support Unsolicited Response
6	R	0	No Processing Control
5	R	0	Reserved
4	R	1b	Contain Format Information
3	R	1b	Contain Amplifier Parameter
2	R	1b	Out Amp Presented
1	R	0	In Amp not Present
0	R	1b	Stereo

#### Offset

#### Supported PCM Size, Rates (Payload = 0Ah)

Response: 000E 05E0h

Bit	Attribute	Default	Description
31:21	R	0	Reserved
20	R	0	No 32-bit Audio Format Support
19	R	1b	24-bit Audio Format Support
18	R	1b	20-bit Audio Format Support
17	R	1b	16-bit Audio Format Support
16	R	0	8-bit Audio Format Support
15:12	R	0	Reserved
11	R	0	384 kHz not Supported
10	R	1b	192 kHz Supported
9	R	0	176.4 kHz Supported
8	R	1b	96 kHz Supported
7	R	1b	88.2 kHz Supported
6	R	1b	48 kHz Supported
5	R	1b	44.1 kHz Supported
4	R	0	32 kHz not Supported
3	R	0	22.05 kHz not Supported
2	R	0	16 kHz not Supported
1	R	0	11.025 kHz not Supported
0	R	0	8 kHz not Supported





### 8.4.3 Converter Stream, Channel Verbs (Verb ID = F06h & 706h)

	Description	Verb ID	Payload
Get	Get Converter Stream / Channel	F06h	8'b0
Set	Set Converter Stream / Channel	706h	Stream is in bit [7:4], and Channel in bit [3:0].

### 8.4.4 Converter Format Verbs (Verb ID = Ah & 2h)

	Description	Verb ID	Payload
Get	Get Converter Format	Ah	16'b0
Set	Set Converter Format	2h	Format

#### Offset

#### Converter Format

Response: 0000 0031h

Bit	Attribute	Default	Description
15	R	0	Stream Type 0: PCM 1: Non-PCM ( Not supported )
14	RW	0	Sample Base Rate 0: 48 kHz 1: 44.1 kHz
13:11	RW	0	Sample Base Rate Multiple 000: x1: 48 kHz, 44.1 kHz 001: x2: 96 kHz, 88.2 kHz 010: x3: 144 kHz ( Not supported ) 011: x4: 192 kHz 100-111: Reserved
10:8	RW	0	Sample Base Rate Divisor 000: /1; 48 kHz Others: Not supported
7	R	0	Reserved
6:4	RW	011b	Bits per Sample 000: 8-bit ( Not supported ) 001: 16-bit 010: 20-bit 011: 24-bit 100: 32-bit ( Not supported )
3:0	RW	0001b	Number of Channels (CHAN) Refers to the number of channels for the stream in each "sample block" of the "packets" in each "frame" on the link. 0000: 1 0001: 2 ..... 1111: 16

#### 8.4.5 Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	Format
Set	Set Amplifier Gain/Mute	3h	Format

##### Offset

##### Get Payload Format

Bit	Attribute	Default	Description
15	W	-	0: The input amplifier is being requested (Ignored). 1: The output amplifier is being requested.
14	W	-	Reserved
13	W	-	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	-	Reserved
3:0	W	-	Index

##### Offset

##### Get Response Format

Response: 0000 002Ah

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Amplifier is Un-muted.
6:0	R	0101010b	Amplifier Gain Setting 0101010b: Offset 2Ah is 0 dB.

##### Offset

##### Set Payload Format

Response: 0000 0000h

Bit	Attribute	Default	Description
15	W	-	The Output Amplifier is being Set.
14	W	-	The Input Amplifier is being Set (Ignored).
13	W	-	The Left Amplifier is being Set.
12	W	-	The Right Amplifier is being Set.
11:8	W	-	Index Ignored
7	W	-	Un-mute
6:0	W	-	Gain Setting

## 8.5 Audio Digital Output Converter (S/PDIF TX) Widget (Node ID = 12h, 15h)

### 8.5.1 Get Parameter Verb (Verb ID = F00h)

#### Offset

#### Audio Widget Capabilities (Payload = 09h)

Response: 0000 0611h

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0	Audio Output Converter Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	1b	Digital Widget, not Analog
8	R	0	Connection List is not Present.
7	R	0	Does not Support Unsolicited Response.
6	R	0	No Processing Control
5	R	0	Reserved
4	R	1b	Contains Format Information.
3	R	0	Contains Amplifier Parameter.
2	R	0	Out Amp Present
1	R	0	In Amp not Present
0	R	1b	Stereo

#### Offset

#### Supported PCM Size, Rates (Payload = 0Ah)

Response: 000E 05E0h

Bit	Attribute	Default	Description
31:21	R	0	Reserved
20	R	0	No 32-Bit Audio Format Support
19	R	1b	24-Bit Audio Format Support
18	R	1b	20-Bit Audio Format Support
17	R	1b	16-Bit Audio Format Support
16	R	0	8-Bit Audio Format Support
15:12	R	0	Reserved
11	R	0	384 kHz not Supported
10	R	1b	192 kHz not Supported
9	R	0	176.4 kHz not Supported
8	R	1b	96 kHz Supported
7	R	1b	88.2 kHz Supported
6	R	1b	48 kHz Supported
5	R	1b	44.1 kHz Supported
4	R	0	32 kHz not Supported
3	R	0	22.05 kHz not Supported
2	R	0	16 kHz not Supported
1	R	0	11.025 kHz not Supported
0	R	0	8 kHz not Supported

**Offset**

**Supported Stream Formats (Payload = 0Bh)**

Response: 0000 0001h

Bit	Attribute	Default	Description
31:3	R	0	Reserved
2	R	0	No AC3 Support
1	R	0	No Float32 Support
0	R	1b	PCM Supported

**Offset**

**Supported Power States (Payload = 0Fh)**

Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

**8.5.2 Power State Verbs (Verb ID = F05h & 705h)**

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

**Offset**

**S/PDIF TX Power-down Control**

Response: 0000 0400h

Bit	Attribute	Default	Description
31:11	R	0	Reserved
10	R	1b	PS-SettingsReset
9:8	R	0	Reserved
7:4	R	0	PS-Act Reports the actual power state of the widget.
3:0	RW	0	PS-Set

**8.5.3 Converter Stream, Channel Verbs (Verb ID = F06h & 706h)**

	Description	Verb ID	Payload
Get	Get Converter Stream / Channel	F06h	8'b0
Set	Set Converter Stream / Channel	706h	Stream is in bit[7:4]; Channel bit[3:0]

#### 8.5.4 S/PDIF Converter Control 1 & 2 Verbs (Verb ID = F0Dh & 70Dh, 70Eh)

	Description	Verb ID	Payload
Get	Get Converter Control State	F0Dh	8'b0
Set	Set Converter Control 1	70Dh	SIC[7:0]
Set	Set Converter Control 2	70Eh	SIC[15:8]

#### Offset

#### S/PDIF IEC Control Bits Format

Response: 0000 0000h

Bit	Attribute	Default	Description
15	R	0	Reserved
14:8	RW	0	CC[6:0] Category Code
7	RW	0	L: Generation Level
6	RW	0	PRO 0: Consumer mode.                   1: Professional mode.
5	RW	0	AUDIO 0: Data is PCM format.               1: Data is non PCM format.
4	RW	0	Copy 0: Copyright is not asserted.       1: Copyright is asserted.
3	RW	0	Pre 0: Pre-emphasis is none.           1: Filter pre-emphasis is 50/ 15 µs
2	RW	0	VCFG Determine S/PDIF transmitter behavior when data is not being transmitted.
1	RW	0	Validity Flag
0	RW	0	DigEn 0: S/PDIF TX disabled.               1: S/PDIF TX enabled.

**8.5.5 Converter Format Verbs (Verb ID = Ah & 2h)**

	Description	Verb ID	Payload
Get	Get Converter Format	Ah	16'b0
Set	Set Converter Format	2h	Format

**Offset**

**Converter Format** Response: 0000 0031h

Bit	Attribute	Default	Description
15	RW	0	Stream Type 0: PCM <span style="float: right;">1: Non-PCM</span>
14	RW	0	Sample Base Rate 0: 48 kHz <span style="float: right;">1: 44.1 kHz</span>
13:11	RW	0	Sample Base Rate Multiple 000: x1; 48 kHz, 44.1 kHz 001: x2; 96 kHz, 88.2 kHz 010: x3; 144 kHz (Not supported) 011: x4; 192 kHz, 176.4 kHz (176.4 kHz not support) 100-111: Reserved
10:8	RW	0	Sample Base Rate Divisor 000 = /1: 48 kHz <span style="float: right;">Others: Not supported</span>
7	R	0	Reserved
6:4	RW	011b	Bits per Sample 000: 8-bit (Not supported) <span style="float: right;">001: 16-bit</span> 010: 20-bit <span style="float: right;">011: 24-bit</span> 100: 32-bit (Not supported)
3:0	RW	0001b	Number of Channels (CHAN) Refers to number of channels for this stream in each "sample block" of the "packets" in each "frame" on the link. 0000: 1 <span style="float: right;">0001: 2</span> ..... <span style="float: right;">1111: 16</span>

## 8.6 Audio Analog Input Converter Widget (Node ID = 13h, 14h)

### 8.6.1 Get Parameter Verb (Verb ID = F00h)

#### Offset

#### Audio Widget Capabilities (Payload = 09h)

Response: 0010 051Bh

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0001b	Audio Input Converter Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	0	Analog Widget, not Digital
8	R	1b	Connection List is Present.
7	R	0	Does not Support Unsolicited Response.
6	R	0	No Processing Control
5	R	0	Reserved
4	R	1b	Contains Format Information
3	R	1b	Contains Amplifier Parameter
2	R	0	Out Amp is not Present.
1	R	1b	In Amp is Present.
0	R	1b	Stereo

#### Offset

#### Supported PCM Size, Rates (Payload = 0Ah)

Response: 000E 0560h

Bit	Attribute	Default	Description
31:21	R	0	Reserved
20	R	0	No 32-bit Audio Format Support
19	R	1b	24-bit Audio Format Support
18	R	1b	20-bit Audio Format Support
17	R	1b	16-bit Audio Format Support
16	R	0	8-bit Audio Format Support
15:12	R	0	Reserved
11	R	0	384 kHz not Supported
10	R	1b	192 kHz Supported
9	R	0	176.4 kHz not Supported
8	R	1b	96 kHz Supported
7	R	0	88.2 kHz not Supported
6	R	1b	48 kHz Supported
5	R	1b	44.1 kHz Supported
4	R	0	32 kHz not Supported
3	R	0	22.05 kHz not Supported
2	R	0	16 kHz not Supported
1	R	0	11.025 kHz not Supported
0	R	0	8 kHz not Supported

**Offset**

**Supported Stream Formats (Payload = 0Bh)**

Response: 0000 0001h

Bit	Attribute	Default	Description
31:3	R	0	Reserved
2	R	0	No AC3 Support
1	R	0	No Float32 Support
0	R	1b	PCM Supported

**Offset**

**Input Amplifier Capabilities (Payload = 0Dh)**

Response: 8005 1F0Bh

Bit	Attribute	Default	Description
31	R	1b	Mute Capable
30:23	R	0	Reserved
22:16	R	0000101b	Step Size 0000101b: Step size is 1.5 dB.
15	R	0	Reserved
14:8	R	0011111b	Number of steps 0011111b: Number of steps is 32 (-16.5 dB – 30 dB).
7	R	0	Reserved
6:0	R	0001011b	Offset 0001011b: Offset 0Bh is 0dB.

**Offset**

**Connection List Length (Payload = 0Eh)**

Response: 0000 0001h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Short Form
6:0	R	0000001b	1 Input Available

**Offset**

**Supported Power States (Payload = 0Fh)**

Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup



### 8.6.2 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

#### Offset

Response: 0000 0017h  
or 0000 001Eh

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Independent NID
6:0	R	-	0010111b: From SW0 (NID = 17h) for AIW0 0011110b: From PW5 (NID = 1Eh) for AIW1

### 8.6.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

#### Offset

#### ADC Power-down Control

Response: 0000 0000h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7:4	R	0	PS-Act. Report the Actual Power State of the Widget.
6:0	R	0	PS-Set

### 8.6.4 Converter Stream, Channel Verbs (Verb ID = F06h & 706h)

	Description	Verb ID	Payload
Get	Get Converter Stream / Channel	F06h	8'b0
Set	Set Converter Stream / Channel	706h	Stream is in bit [7:4]. Channel is in bit [3:0].

### 8.6.5 Converter Format Verbs (Verb ID = Ah & 2h)

	Description	Verb ID	Payload
Get	Get Converter Format	Ah	16'b0
Set	Set Converter Format	2h	Format

#### Offset

#### Converter Format

Response: 0000 0031h

Bit	Attribute	Default	Description
15	R	0	Stream Type 0: PCM 1: Non-PCM (Not supported)
14	RW	0	Sample Base Rate 0: 48 kHz 1: 44.1 kHz
13:11	RW	0	Sample Base Rate Multiple 000: x1; 48 kHz, 44.1 kHz 001: x2; 96 kHz 010: x3; 144 kHz ( Not supported ) 011: x4; 192 kHz 100-111: Reserved
10:8	RW	0	Sample Base Rate Divisor 000: /1; 48 kHz Others : Not supported
7	R	0	Reserved
6:4	RW	011b	Bits per Sample 000: 8-bit ( Not supported ) 001: 16-bit 010: 20-bit 011: 24-bit 100: 32-bit ( Not supported )
3:0	RW	0001b	Number of Channels (CHAN) Refers to the number of channels for this stream in each "sample block" of the "packets" in each "frame" on the link. 0000: 1 0001: 2 ..... 1111: 16

### 8.6.6 Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	Format
Set	Set Amplifier Gain/Mute	3h	Format

#### Offset

##### Get Payload Format

Bit	Attribute	Default	Description
15	W	-	0: The input amplifier is being requested. 1: The output amplifier is being requested (ignored).
14	W	-	Reserved
13	W	-	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	-	Reserved
3:0	W	-	Index Ignored

#### Offset

##### Get Response format

Response: 0000 008Bh

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	1b	0: Amplifier is un-muted. 1: Amplifier is muted.
6:0	R	0001011b	Amplifier Gain Setting 0001011b: 0 dB

#### Offset

##### Set Payload Format

Response: 0000 0000h

Bit	Attribute	Default	Description
15	W	-	The Output Amplifier is being Set (Ignored).
14	W	-	The Input Amplifier is being Set.
13	W	-	The Left Amplifier is being Set.
12	W	-	The Right Amplifier is being Set.
11:8	W	-	Index Ignored
7	W	-	0: Un-mute 1: Mute
6:0	W	-	Gain Setting

## 8.7 Mixer Widget (Node ID = 16h)

### 8.7.1 Get Parameter Verb (Verb ID = F00h)

#### Offset

#### Audio Widget Capabilities (Payload = 09h)

Response: 0020 050Bh

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0010b	Audio Mixer Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	0	Analog Widget, not Digital
8	R	1b	Connection List is Present.
7	R	0	Does not Support Unsolicited Response
6	R	0	No Processing Control
5	R	0	Reserved
4	R	0	No Format Information
3	R	1b	Amplifier Parameter
2	R	0	Out Amp not Presented
1	R	1b	In Amp Present
0	R	1b	Stereo

#### Offset

#### Input Amplifier Capabilities (Payload = 0Dh)

Response: 8005 1F17h

Bit	Attribute	Default	Description
31	R	1b	Mute Capable
30:23	R	0	Reserved
22:16	R	0000101b	Step Size 0000101b: Step size is 1.5 dB.
15	R	0	Reserved
14:8	R	0011111b	Number of Steps 0011111b: Number of steps is 31 (-34.5 dB - 12 dB).
7	R	0	Reserved
6:0	R	0010111b	Offset 0010111b: Offset 17h is 0 dB.

#### Offset

#### Connection List Length (Payload = 0Eh)

Response: 0000 0007h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Short Form
6:0	R	0000111b	7 Inputs Available

**Offset**

**Supported Power States (Payload = 0Fh)**

Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

**8.7.2 Connection List Entry Control Verbs (Verb ID = F02h)**

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

**Offset**

Response: 1B1A 1F10h (n=0)  
or 0025 1D1Eh (n=4)

Bit	Attribute	Default	Description	
			Offset index n = 0	Offset index n = 4
31:24	R	1Bh or 00h	Connection List Entry n+3 1Bh: (PW2, Port C)	- 00h
23:16	R	1Ah or 25h	Connection List Entry n+2 1Ah: (PW1, Port B)	Connection List Entry n+2 25h: (AOW2)
15:8	R	1Fh or 1Dh	Connection List Entry n+1 1Fh: (PW8, CD)	Connection List Entry n+1 1Dh: (PW4)
7:0	R	10h or 1Eh	Connection List Entry n 10h: (AOW0)	Connection List Entry n 1Eh: (PW5, Port F)

**8.7.3 Power State Verbs (Verb ID = F05h & 705h)**

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

**Offset**

**Mixer Power-down Control**

Response: 0000 0000h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7:4	R	0	PS-Act. Reports the Actual Power State of the Widget.
3:0	RW	0	PS-Set

#### 8.7.4 Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	Format
Set	Set Amplifier Gain/Mute	3h	Format

##### Offset

##### Get Payload Format

Bit	Attribute	Default	Description
15	W	-	0: The input amplifier is being requested. 1: The output amplifier is being requested (ignored).
14	W	-	Reserved
13	W	-	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	-	Reserved
3:0	W	-	Index

##### Offset

##### Get Response Format

Response: 0000 0097h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	1b	0: Amplifier is un-muted. 1: Amplifier is muted.
6:0	R	0010111b	Amplifier Gain Setting 0010111b: Offset 17h is 0dB.

##### Offset

##### Set Payload Format

Response: 0000 0000h

Bit	Attribute	Default	Description
15	W	-	The Output Amplifier is being Set (ignored).
14	W	-	The Input Amplifier is being Set.
13	W	-	The Left Amplifier is being Set.
12	W	-	The Right Amplifier is being Set.
11:8	W	-	Index Ignored
7	W	-	0: Un-mute 1: Mute
6:0	W	-	Gain Setting

## 8.8 Selector Widget SW0 (Node ID = 17h)

### 8.8.1 Get Parameter Verb (Verb ID = F00h)

#### Offset

#### Audio Widget Capabilities (Payload = 09h)

Response: 0030 0501h

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0011b	Audio Selector Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	0	Analog Widget, not Digital
8	R	1b	Connection List is Present
7	R	0	Does not Support Unsolicited Response
6	R	0	No Processing Control
5	R	0	Reserved
4	R	0	No Format Information
3	R	0	Amplifier Parameter
2	R	0	Out Amp not Presented
1	R	0	In Amp not Present
0	R	1b	Stereo

#### Offset

#### Connection List Length (Payload = 0Eh)

Response: 0000 0006h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Short Form
6:0	R	0000110b	6 Inputs Available

#### Offset

#### Supported Power States (Payload = 0Fh)

Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

### 8.8.2 Connection Select Control Verbs (Verb ID = F01h & 701h)

	Description	Verb ID	Payload
Get	Get Connection Select	F01h	8'b0 Default: 00000001h (MIC)
Set	Set Connection Select	701h	The connection index value to be set

### 8.8.3 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

#### Offset

Response: 1E1B 1A1Fh (n=0)  
or 0000 161Dh (n=4)

Bit	Attribute	Default	Description	
			Offset index n = 0	Offset index n = 4
31:24	R	1Eh or 00h	Connection List Entry n+3 1Eh: (PW5, Port F)	Connection List Entry n+3 00h
23:16	R	1Bh or 00h	Connection List Entry n+2 1Bh: (PW2, Port C)	Connection List Entry n+2 00h
15:8	R	1Ah or 16h	Connection List Entry n+1 1Ah: (PW1, Port B)	Connection List Entry n+1 16h: (MW)
7:0	R	1Fh or 1Dh	Connection List Entry n 1Fh: (PW8, CD)	Connection List Entry n 1Dh: (PW4, Port E)

### 8.8.4 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

#### Offset

#### SW0 Power-down Control

Response: 0000 0000h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7:4	R	0	PS-Act. Report the Actual Power State of the Widget.
3:0	RW	0	PS-Set



## 8.9 Selector Widget SW1-SW2 (Node ID = 18h, 27h)

### 8.9.1 Get Parameter Verb (Verb ID = F00h)

#### Offset

#### Audio Widget Capabilities (Payload = 09h)

Response: 0030 050Dh

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0011b	Audio Selector Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	0	Analog Widget, not Digital
8	R	1b	Connection List is Present
7	R	0	Does not Support Unsolicited Response
6	R	0	No Processing Control
5	R	0	Reserved
4	R	0	No Format Information
3	R	1b	Amplifier Parameter
2	R	1b	Out Amp Present
1	R	0	In Amp not Present
0	R	1b	Stereo

#### Offset

#### Connection List Length (Payload = 0Eh)

Response: 0000 0001h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Short Form
6:0	R	0000001b	1 Input Available

#### Offset

#### Supported Power States (Payload = 0Fh)

Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

#### Offset

#### Output Amplifier Capabilities (Payload = 12h)

Response: 8000 0000h

Bit	Attribute	Default	Description
31	R	1b	Mute Capable
30:23	R	0	Reserved
22:16	R	0	Step Size 0000000b: Step size is 0 dB.
15	R	0	Reserved

14:8	R	0	Number of Steps 0000000b: Number of steps is 0.
7	R	0	Reserved
6:0	R	0	Offset

### 8.9.2 Connection Select Control Verbs (Verb ID = F01h & 701h)

	Description	Verb ID	Payload
Get	Get Connection Select	F01h	8'b0
Set	Set Connection Select	701h	The connection index value to be set.

### 8.9.3 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

#### Offset

Response: 0000 0011h  
or 0000 0025h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7:0	R	0	Connection List Entry n 11h: (AOW1) for SW1 25h: (AOW2) for SW2

### 8.9.4 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

#### Offset

#### SW1 ~ SW2 Power-down Control

Response: 0000 0000h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7:4	R	0	PS-Act. Report the Actual Power State of the Widget.
3:0	RW	0	PS-Set

### 8.9.5 Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	Format
Set	Set Amplifier Gain/Mute	3h	Format

#### Offset

##### Get Payload Format

Bit	Attribute	Default	Description
15	W	-	0: The input amplifier is being requested (Ignored). 1: The output amplifier is being requested.
14	W	-	Reserved
13	W	-	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	-	Reserved
3:0	W	-	Index Ignored

#### Offset

##### Get Response Format

Response: 0000 0080h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	1b	0: Amplifier is un-muted. 1: Amplifier is muted.
6:0	R	0	Amplifier Gain Setting

#### Offset

##### Set Payload Format

Response: 0000 0000h

Bit	Attribute	Default	Description
15	W	-	The Output Amplifier is being Set.
14	W	-	The Input Amplifier is being Set (Ignored).
13	W	-	The Left Amplifier is being Set.
12	W	-	The Right Amplifier is being Set.
11:8	W	-	Index Ignored
7	W	-	0: Un-mute 1: Mute
6:0	W	-	Gain Setting

## 8.10 Pin Widget PW0 (Node ID = 19h)

### 8.10.1 Get Parameter Verb (Verb ID = F00h)

#### Offset

#### Audio Widget Capabilities (Payload = 05h)

Response: 0000 0101h

Bit	Attribute	Default	Description
31:9	R	0	Reserved
8	R	1b	Unsolicited Capable
7:0	R	00000001b	Audio Function Group

#### Offset

#### Audio Widget Capabilities (Payload = 09h)

Response: 0040 0581h

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0100b	Pin Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	0	Analog Widget, not Digital
8	R	1b	Connection List is Present
7	R	1b	Support Unsolicited Response
6	R	0	No Processing Control
5	R	0	Reserved
4	R	0	Doesn't Contain Format Information
3	R	0	Contain Amplifier Parameter
2	R	0	Out Amp not Present
1	R	0	In Amp not Present
0	R	1b	Stereo

#### Offset

#### Pin Capabilities (Payload = 0Ch)

Response: 0000 0014h

Bit	Attribute	Default	Description
31:17	R	0	Reserved
16	R	0	EAPD Capable
15:8	R	0	Vref Control
7	R	0	Reserved
6	R	0	Balanced I/O Pins
5	R	0	Input Capable
4	R	1b	Output Capable
3	R	0	Headphone Drive Capable
2	R	1b	Presence Detect Capable
1	R	0	Trigger Required
0	R	0	Impedance Sense Capable.

**Offset**

**Connection List Length (Payload = 0Eh)** Response: 0000 0001h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Short Form
6:0	R	0000001b	Only 1 Input Available

**Offset**

**Supported Power States (Payload = 0Fh)** Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

**8.10.2 Connection List Entry Control Verbs (Verb ID = F02h)**

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

**Offset**

Response: 0000 0018h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Independent NID
6:0	R	0011000b	From SW1

**8.10.3 Power State Verbs (Verb ID = F05h & 705h)**

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	Offset index n
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

**Offset**

**PWO Power-down Control** Response: 0000 0000h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7:4	R	0	PS-Act. Report the Actual Power State of the Widget.
3:0	R	0	PS-Set

#### 8.10.4 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

##### Offset

Response: 0000 0000h

Bit	Attribute	Default	Description
7	RW	0	Headphone Enable 0: Disabled 1: Headphone enabled (Not supported)
6	RW	0	Output Enable 0: Disabled (default) 1: Output enabled
5	R	0	Input Enable 0: Disabled 1: Input enabled (Not supported).
4:0	R	0	Reserved

#### 8.10.5 Unsolicited Response Control (Verb ID = F08h & 708h)

	Description	Verb ID	Payload
Get	Get Unsolicited Response Control	F08h	8'b0
Set	Set Unsolicited Response Control	708h	Enable unsolicited response

##### Offset

##### Unsolicited Format

Response: 0000 0000h

Bit	Attribute	Default	Description
7	RW	0	0: Unsolicited Response Disabled 1: Unsolicited Response Enabled
6	R	0	Reserved
5:0	RW	0	Tag Used by software to determine the node that generated the unsolicited response.

#### 8.10.6 Right Channel Sense (Verb ID = F09h & 709h)

	Description	Verb ID	Payload
Get	Get Pin Sense Control	F09h	8'b0
Set	Set Pin Sense Control	709h	PinCntl

##### Offset

##### PinCntl Format

Response: 0000 0000h

Bit	Attribute	Default	Description
7:1	R	0	Reserved
0	R	0	Right Channel Sense ( Not supported )

**Offset**

**Presence Detect**

Response: 0000 0000h

Bit	Attribute	Default	Description
31	R	0	Presence Detect 0: Nothing plugged in. 1: Jack plugged in.
30:0	R	0	Reserved

**8.10.7 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)**

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

**Offset**

**Configuration Bits Format**

Response: 0101 1012h

Bit	Attribute	Default	Description
31:30	RW	0	Port Connectivity 00: Connected to a jack
29:24	RW	000001b	Location
23:20	RW	0	Default Device 0000b: Line-out
19:16	RW	0001b	Connection Type
15:12	RW	0001b	Color
11:8	RW	0	Misc.
7:4	RW	0001b	Default Association
3:0	RW	0010b	Sequence 0010b: Surround out in association # 1

## 8.11 Pin Widget PW3 (Node ID = 1Ch)

### 8.11.1 Get Parameter Verb (Verb ID = F00h)

#### Offset

#### Audio Widget Capabilities (Payload = 05h)

Response: 0000 0101h

Bit	Attribute	Default	Description
31:9	R	0	Reserved
8	R	1b	Unsolicited Capable
7:0	R	00000001b	Audio Function Group

#### Offset

#### Audio Widget Capabilities (Payload = 09h)

Response: 0040 058Dh

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0100b	Pin Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	0	Analog Widget, not Digital
8	R	1b	Connection List is Present.
7	R	1b	Support Unsolicited Response
6	R	0	No Processing Control
5	R	0	Reserved
4	R	0	Does not Contain Format Information.
3	R	1b	Contain Amplifier Parameter
2	R	1b	Out Amp Present
1	R	0	In Amp not Present.
0	R	1b	Stereo

#### Offset

#### Pin Capabilities (Payload = 0Ch)

Response: 0001 001Ch

Bit	Attribute	Default	Description
37:17	R	0	Reserved
16	R	1b	EAPD Capable
15:8	R	0	VRef Control
7	R	0	Reserved
6	R	0	Balanced I/O Pins
5	R	0	Input Capable
4	R	1b	Output Capable
3	R	1b	Headphone Drive Capable.
2	R	1b	Presence Detect Capable
1	R	0	Trigger Required
0	R	0	Impedance Sense Capable



**Offset**

**Connection List Length (Payload = 0Eh)** Response: 0000 0001h

Bit	Attribute	Default	Description
37:8	R	0	Reserved
7	R	0	Short Form
6:0	R	0000001b	Only 1 Input Available

**Offset**

**Supported Power States (Payload = 0Fh)** Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

**Offset**

**Output Amplifier Capabilities (Payload = 12h)** Response: 8000 0000h

Bit	Attribute	Default	Description
31	R	1b	Mute Capable
30:23	R	1b	Reserved
22:16	R	0	Step Size 0000000b: Step size is 0 dB.
15	R	0	Reserved
14:8	R	0	Number of Steps 0000000b: Number of steps is 0h.
7	R	0	Reserved
6:0	R	0	Offset

**8.11.2 Connection List Entry Control Verbs (Verb ID = F02h)**

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

**Offset**

Response: 0000 0016h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Independent NID
6:0	R	0010110b	From MW0

### 8.11.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

#### Offset

#### PW3 Power-down Control

Response: 0000 0000h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7:4	R	0	PS-Act. Reports the Actual Power State of the Widget.
3:0	RW	0	PS-Set

### 8.11.4 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

#### Offset

#### PinCntl Format

Response: 0000 0000h

Bit	Attribute	Default	Description
7	RW	0	Headphone Enable 0: Disabled 1: Headphone enabled
6	RW	0	Output Enable 0: Disabled 1: Output enabled
5	RW	0	Input Enable 0: Disabled 1: Input enabled (Not supported)
4:0	R	0	Reserved

### 8.11.5 Unsolicited Response Control (Verb ID = F08h & 708h)

	Description	Verb ID	Payload
Get	Get Unsolicited Response Control	F08h	8'b0
Set	Set Unsolicited Response Control	708h	Enable unsolicited response

#### Offset

#### Unsolicited Format

Response: 0000 0000h

Bit	Attribute	Default	Description
7	RW	0	0: Unsolicited Response Disabled 1: Unsolicited Response Enabled
6	R	0	Reserved
5:0	RW	0	Tag Used by software to determine which node generated the unsolicited response.

### 8.11.6 Pin Sense Control Verbs (Verb ID = F09h & 709h)

	Description	Verb ID	Payload
Get	Get Pin Sense Control	F09h	8'b0
Set	Set Pin Sense Control	709h	PinCntl

#### Offset

**PinCntl Format** Response: 0000 0000h

Bit	Attribute	Default	Description
7:1	R	0	Reserved
0	R	0	Right Channel Sense (Not supported)

#### Offset

Response: 0000 0000h

Bit	Attribute	Default	Description
31	R	0	Presence Detect 0: Nothing plugged in 1: Jack plugged in
30:0	R	0	Reserved

### 8.11.7 EAPD Enable Verbs (Verb ID = F0Ch & 70Ch)

	Description	Verb ID	Payload
Get	EAPD Control	F0Ch	8'b0
Set		70Ch	Bit 1 is EAPD

### 8.11.8 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

#### Offset

Response: 0101 4010h

Bit	Attribute	Default	Description
31:30	RW	0	Port Connectivity
29:24	RW	000001b	Location
23:20	RW	0	Default Device
19:16	RW	0001b	Connection Type
15:12	RW	0100b	Color
11:8	RW	0	Misc.
7:4	RW	0001b	Default Association
3:0	RW	0	Sequence

### 8.11.9 Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	
Set	Set Amplifier Gain/Mute	3h	

#### Offset

##### Get Payload Format

Bit	Attribute	Default	Description
15	W	-	0: The input amplifier is being requested (Ignored). 1: The output amplifier is being requested.
14	W	-	Reserved
13	W	-	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	-	Reserved
3:0	W	-	Index

#### Offset

##### Get Response Format

Response: 0000 0080h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	1b	0: Amplifier is unmuted. 1: Amplifier is muted.
6:0	R	0	Amplifier Gain Setting

#### Offset

##### Set Payload Format

Response: 0000 0000h

Bit	Attribute	Default	Description
15	W	-	The Output Amplifier is being Set.
14	W	-	The Input Amplifier is being Set (ignored).
13	W	-	The Left Amplifier is being Set.
12	W	-	The Right Amplifier is being Set.
11:8	W	-	Index Ignored
7	W	-	0: Un-Mute 1: Mute
6:0	W	-	Gain Setting

## 8.12 Pin Widget PW4 (Node ID = 1Dh)

### 8.12.1 Get Parameter Verb (Verb ID = F00h)

Offset

Audio Widget Capabilities (Payload = 05h)

Response: 0000 0101h

Bit	Attribute	Default	Description
31:9	R	0	Reserved
8	R	1b	Unsolicited Capable
7:0	R	00000001b	Audio Function Group

Offset

Audio Widget Capabilities (Payload = 09h)

Response: 0040 058Dh

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0100b	Pin Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	0	Analog Widget, not Digital
8	R	1b	Connection List is Present.
7	R	1b	Support Unsolicited Response
6	R	0	No Processing Control
5	R	0	Reserved
4	R	0	Doesn't Contain Format Information.
3	R	1b	Contain Amplifier Parameter
2	R	1b	Out Amp Present
1	R	0	In Amp Present
0	R	1b	Stereo

Offset

Pin Capabilities (Payload = 0Ch)

Response: 0000 233Ch

Bit	Attribute	Default	Description
31:17	R	0	Reserved
16	R	0	EAPD Capable
15:8	R	23h	Vref Control 23h: 100% & 50% & Hi-Z
7	R	0	Reserved
6	R	0	Balanced I/O Pins
5	R	1b	Input Capable
4	R	1b	Output Capable
3	R	1b	Headphone Drive Capable
2	R	1b	Presence Detect Capable
1	R	0	Trigger Required
0	R	0	Impedance Sense Capable

**Offset**

**Connection List Length (Payload = 0Eh)**

Response: 0000 0002h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Short Form
6:0	R	2h	2 Input Available

**Offset**

**Supported Power States (Payload = 0Fh)**

Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

**Offset**

**Input Amplifier Capabilities (Payload = 0Dh)**

Response: 0000 0000h

Bit	Attribute	Default	Description
31	R	0	Mute Capable
30:23	R	0	Reserved
22:16	R	0	Step Size 0000000b: Step size is 0 db.
15	R	0	Reserved
14:8	R	0	Number of Steps 0000000b: Number of steps is 0h.
7	R	0	Reserved
6:0	R	0	Offset 000000b: Offset 00h is 0 dB.

**Offset**

**Output Amplifier Capabilities (Payload = 12h)**

Response: 8000 0000h

Bit	Attribute	Default	Description
31	R	1b	Mute Capable
30:23	R	0	Reserved
22:16	R	0	Step Size. 0000000b: Step size is 0 dB.
15	R	0	Reserved
14:8	R	0	Number of Steps 0000000b: Number of steps is 0h.
7	R	0	Reserved
6:0	R	0	Offset

### 8.12.2 Connection Select Control Verbs (Verb ID = F01h & 701h)

	Description	Verb ID	Payload
Get	Get Connection Select	F01h	8'b0
Set	Set Connection Select	701h	The connection index value to be set 8'b0: from MW0 8'b1: form AOW2

#### Offset

**Get Response Format** Response: -h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7:0	R	-	Connection Index Currently Set 00h: Connection from MW0 01h: Connection form AOW2

### 8.12.3 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

#### Offset

Response: 0000 2516h

Bit	Attribute	Default	Description
31:16	R	0	Reserved
15:8	R	00100101b	From AOW2
7	R	0	Independent NID
6:0	R	0010110b	From MW0

### 8.12.4 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

#### Offset

**PW4 Power-down Control** Response: 0000 0000h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7:4	R	0	PS-Act. Report the Actual Power State of the Widget.
3:0	RW	0	PS-Set

### 8.12.5 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

#### Offset

#### PinCntl Format

Response: 0000 0000h

Bit	Attribute	Default	Description
7	RW	0	Headphone Enable 0: Disabled 1: Headphone enabled
6	RW	0	Output Enable 0: Disabled 1: Output enabled
5	RW	0	Input Enable 0: Disabled 1: Input enabled
4:3	R	0	Reserved
2:0	RW	0	VRef Enable These bits control the VRef signal associated with the pin widget. 000b: Hi-Z 001b: 50% (half of AVdd) 010b: 0V (Not supported) 101b: AVdd Others: Reserved

### 8.12.6 Unsolicited Response Control (Verb ID = F08h & 708h)

	Description	Verb ID	Payload
Get	Get Unsolicited Response Control	F08h	8'b0
Set	Set Unsolicited Response Control	708h	Enable unsolicited response

#### Offset

#### Unsolicited Format

Response: 0000 0000h

Bit	Attribute	Default	Description
7	RW	0	0: Unsolicited Response Disabled 1: Unsolicited Response Enabled
6	R	0	Reserved
5:0	RW	0	Tag Used by software to determine the node that generated the unsolicited response.



### 8.12.7 Pin Sense Control Verbs (Verb ID = F09h & 709h)

	Description	Verb ID	Payload
Get	Get Pin Sense Control	F09h	8'b0
Set	Set Pin Sense Control	709h	PinCntl

#### Offset

**PinCntl Format** Response: 0000 0000h

Bit	Attribute	Default	Description
7:1	R	0	Reserved
0	R	0	Right Channel Sense ( Not supported )

#### Offset

Response: -h

Bit	Attribute	Default	Description
31	R	-	Presence Detect 0: Nothing plugged in 1: Jack plugged in
30:0	R	0	Reserved

### 8.12.8 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

#### Offset

**Config Bits Format** Response: 0221 401Fh

Bit	Attribute	Default	Description
31:30	RW	0	Port Connectivity
29:24	RW	000010b	Location
23:20	RW	0010b	Default Device
19:16	RW	0001b	Connection Type
15:12	RW	0100b	Color
11:8	RW	0	Misc.
7:4	RW	0001b	Default Association
3:0	RW	1111b	Sequence

### 8.12.9 Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	
Set	Set Amplifier Gain/Mute	3h	

#### Offset

##### Get Payload Format

Bit	Attribute	Default	Description
15	W	-	0: The input amplifier is being requested. 1: The output amplifier is being requested.
14	W	-	Reserved
13	W	-	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	-	Reserved
3:0	W	-	Index

#### Offset

##### Get Response Format

Response: -h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	-	0: Amplifier is un-muted (input default). 1: Amplifier is muted (output default).
6:0	R	0	Amplifier Gain Setting

#### Offset

##### Set Payload Format

Response: 0000 0000h

Bit	Attribute	Default	Description
15	W	-	The Output Amplifier is being Set
14	W	-	The Input Amplifier is being Set
13	W	-	The Left Amplifier is being Set
12	W	-	The Right Amplifier is being Set
11:8	W	-	Index Ignored
7	W	-	0: Un-mute 1: Mute
6:0	W	-	Gain Setting

### 8.13 Pin Widget PW7 (Node ID =23h)

#### 8.13.1 Get Parameter Verb (Verb ID = F00h)

##### Offset

##### Audio Widget Capabilities (Payload = 05h)

Response: 0000 0101h

Bit	Attribute	Default	Description
31:9	R	0	Reserved
8	R	1b	Unsolicited Capable
7:0	R	00000001b	Audio Function Group

##### Offset

##### Audio Widget Capabilities (Payload = 09h)

Response: 0040 0581b

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0100b	Pin Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	0	Analog Widget, not Digital
8	R	1b	Connection List is Present.
7	R	1b	Support Unsolicited Response
6	R	0	No Processing Control
5	R	0	Reserved
4	R	0	Doesn't Contain Format Information
3	R	0	Contain Amplifier Parameter
2	R	0	Out Amp not Presented
1	R	0	In Amp not Presented
0	R	1b	Stereo

##### Offset

##### Pin Capabilities (Payload = 0Ch)

Response: 0000 0014h

Bit	Attribute	Default	Description
31:17	R	0	Reserved
16	R	0	EAPD Capable
15:8	R	0	VRef Control
7	R	0	Reserved
6	R	0	Balanced I/O Pins
5	R	0	Input Capable
4	R	1b	Output Capable
3	R	0	Headphone Drive Capable
2	R	1b	Presence Detect Capable
1	R	0	Trigger Required
0	R	0	Impedance Sense Capable

**Offset**

**Connection List Length (Payload = 0Eh)** Response: 0000 0001h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Short Form
6:0	R	0000001b	Only 1 Input Available

**Offset**

**Supported Power States (Payload = 0Fh)** Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

**8.13.2 Connection List Entry Control Verbs (Verb ID = F02h)**

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

**Offset**

Response: 0000 0027h (for PW7)

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Independent NID
6:0	R	0100111b	(From SW2) for PW7

**8.13.3 Power State Verbs (Verb ID = F05h & 705h)**

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

**Offset**

**PW7 Power-down Control** Response: 0000 0000h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7:4	R	0	PS-Act. Reports the Actual Power State of the Widget.
3:0	RW	0	PS-Set

### 8.13.4 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

#### Offset

**PinCntl Format** Response: 0000 0000h

Bit	Attribute	Default	Description
7	R	0	Headphone Enable
6	RW	0	Output Enable 0: Disabled <span style="float: right;">1: Output enabled</span>
5	RW	0	Input Enable 0: Disabled 1: Input enabled (not supported)
4:0	R	0	Reserved

### 8.13.5 Unsolicited Response Control (Verb ID = F08h & 708h)

	Description	Verb ID	Payload
Get	Get Unsolicited Response Control	F08h	8'b0
Set	Set Unsolicited Response Control	708h	Enable unsolicited response

#### Offset

**Unsolicited Format** Response: 0000 0000h

Bit	Attribute	Default	Description
7	RW	0	0: Unsolicited Response Disabled 1: Unsolicited Response Enabled
6	R	0	Reserved
5:0	RW	0	Tag Used by software to determine the node that generated the unsolicited response.

### 8.13.6 Pin Sense Control Verbs (Verb ID = F09h & 709h)

	Description	Verb ID	Payload
Get	Get Pin Sense Control	F09h	8'b0
Set	Set Pin Sense Control	709h	PinCntl

#### Offset

**PinCntl Format** Response: - h

Bit	Attribute	Default	Description
7:1	R	-	Reserved
0	R	-	Right Channel Sense ( Not supported )

#### Offset

Response: 0000 0000h

Bit	Attribute	Default	Description
31	R	0	Presence Detect 0: Nothing plugged in 1: Jack plugged in
30:0	R	0	Reserved

### 8.13.7 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

#### Offset

Response: 0101 6011h for PW7

Bit	Attribute	Default	Description
31:30	RW	0	Port Connectivity
29:24	RW	000001b	Location
23:20	RW	0	Default Device
19:16	RW	0001b	Connection Type
15:12	RW	0110b	Color 0110b: for PW7
11:8	RW	0	Misc
7:4	RW	0001b	Default Association
3:0	RW	0001b	Sequence 0001b: for PW7

## 8.14 Pin Widget PW1, PW2 (Node ID = 1Ah, 1Bh)

### 8.14.1 Get Parameter Verb (Verb ID = F00h)

#### Offset

#### Audio Widget Capabilities (Payload = 05h)

Response: 0000 0101h

Bit	Attribute	Default	Description
31:9	R	0	Reserved
8	R	1b	Unsolicited Capable
7:0	R	00000001b	Audio Function Group

#### Offset

#### Audio Widget Capabilities (Payload = 09h)

Response: 0040 0581h

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0100b	Pin Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	0	Analog Widget, not Digital
8	R	1b	Connection List is Present.
7	R	1b	Support Unsolicited Response
6	R	0	No Processing Control
5	R	0	Reserved
4	R	0	Doesn't Contain Format Information
3	R	0	Contain Amplifier Parameter
2	R	0	Out Amp not Presented
1	R	0	In Amp Presented
0	R	1b	Stereo

#### Offset

#### Pin Capabilities (Payload = 0Ch)

Response: 0000 2334h

Bit	Attribute	Default	Description
31:17	R	0	Reserved
16	R	0	EAPD Capable
15:8	R	23h	VRef Control 23h: 100% & 50% & Hi-Z
7	R	0	Reserved
6	R	0	Balanced I/O Pins
5	R	1b	Input Capable
4	R	1b	Output Capable
3	R	0	Headphone Drive Capable
2	R	1b	Presence Detect Capable
1	R	0	Trigger Required
0	R	0	Impedance Sense Capable

**Offset**

**Input Amplifier Capabilities (Payload = 0Dh)**

Response: 0000 0000h

Bit	Attribute	Default	Description
31	R	0	Mute Capable
30:23	R	0	Reserved
22:16	R	0	Step Size 0: Step size is 0 dB
15	R	0	Reserved
14:8	R	0	Number of Steps 0: Number of steps is 0h
7	R	0	Reserved
6:0	R	0	Offset 0000000b: Offset 00h

**Offset**

**Connection List Length (Payload = 0Eh)**

Response: 0000 0001h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Short Form
6:0	R	0000001b	Only 1 Input Available.

**Offset**

**Supported Power States (Payload = 0Fh)**

Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

**8.14.2 Connection List Entry Control Verbs (Verb ID = F02h)**

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

**Offset**

Response: 0000 0027h (for PW1)  
0000 0018h (for PW2)

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Independent NID
6:0	R	-	0100111b: (From SW2, NID = 27h) for PW1 0011000b: (From SW1, NID = 18h) for PW2



### 8.14.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

#### Offset

#### PW1, PW2 Power-down Control

Response: 0000 0000h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7:4	R	0	PS-Act. Report the Actual Power State of the Widget.
3:0	RW	0	PS-Set

### 8.14.4 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

#### Offset

#### PinCntl Format

Response: 0000 0000h

Bit	Attribute	Default	Description
7	R	0	Headphone Enable 0: Disabled (default)
6	RW	0	Output Enable (for Smart 5.1 Configuration) 0: Disabled (default) 1: Output enabled
5	RW	0	Input Enable 0: Disabled (default) 1: Input enabled
4:3	R	0	Reserved
2:0	RW	0	VRef Enable These bits control the VRef signal associated with the pin widget. 000: Hi-Z (default) 001: 50% (half of AVdd) 010: 0V (Not supported) 101: AVdd Others: Reserved

#### 8.14.5 Unsolicited Response Control (Verb ID = F08h & 708h)

	Description	Verb ID	Payload
Get	Get Unsolicited Response Control	F08h	8'b0
Set	Set Unsolicited Response Control	708h	Enable unsolicited response

#### Offset

**Unsolicited Format** Response: - h

Bit	Attribute	Default	Description
7	RW	-	0: Unsolicited Response Disabled 1: Unsolicited Response Enabled
6	R	-	Reserved
5:0	RW	-	Tag Used by software to determine the node that generated the unsolicited response.

#### 8.14.6 Pin Sense Control Verbs (Verb ID = F09h & 709h)

	Description	Verb ID	Payload
Get	Get Pin Sense Control	F09h	8'b0
Set	Set Pin Sense Control	709h	PinCntl

#### Offset

**PinCntl Format** Response: - h

Bit	Attribute	Default	Description
7:1	R	-	Reserved
0	R	-	Right Channel Sense (Not supported)

#### Offset

**Response** Response: - h

Bit	Attribute	Default	Description
31	R	-	Presence Detect 0: Nothing plugged in 1: Jack plugged in
30:0	R	0	Reserved

### 8.14.7 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

#### Offset

#### Config Bits Format

Response: 01A1 9026h for PW1  
0181 302Eh for PW2

Bit	Attribute	Default	Description
31:30	RW	0	Port Connectivity
29:24	RW	-	Location 000001: For PW1 000001: For PW2
23:20	RW	-	Default Device 1010b: For PW1 1000b: For PW2
19:16	RW	0001b	Connection Type
15:12	RW	-	Color 1001b: For PW1 0011b: For PW2
11:8	RW	0	Misc
7:4	RW	-	Default Association 0010b: For PW1 0010b: For PW2
3:0	RW	-	Sequence 0110b: For PW1 1110b: For PW2

### 8.14.8 Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	
Set	Set Amplifier Gain/Mute	3h	

#### Offset

##### Get Payload Format

Bit	Attribute	Default	Description
15	W	-	0: The input amplifier is being requested (ignored). 1: The output amplifier is being requested.
14	W	-	Reserved
13	W	-	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	-	Reserved
3:0	W	-	Index

#### Offset

##### Get Response format

Response: 0000 0000h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	0: Amplifier is un-muted (input default) 1: Amplifier is muted.
6:0	R	0	Amplifier Gain Setting

#### Offset

##### Set Payload Format

Response: 0000 0000h

Bit	Attribute	Default	Description
15	W	-	The Output Amplifier is being Set (Ignored).
14	W	-	The Input Amplifier is being Set.
13	W	-	The Left Amplifier is being Set.
12	W	-	The Right Amplifier is being Set.
11:8	W	-	Index Ignored
7	W	-	0: Un-mute 1: Mute
6:0	W	-	Gain Setting

## 8.15 Pin Widget PW5 (Node ID = 1Eh)

### 8.15.1 Get Parameter Verb (Verb ID = F00h)

#### Offset

#### Audio Widget Capabilities (Payload = 05h)

Response: 0000 0101h

Bit	Attribute	Default	Description
31:9	R	0	Reserved
8	R	1b	Unsolicited Capable
7:0	R	00000001	Audio Function Group

#### Offset

#### Audio Widget Capabilities (Payload = 09h)

Response: 0040 058Dh

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0100b	Pin Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	0	Analog Widget, not Digital
8	R	1b	Connection List is Present.
7	R	1b	Support Unsolicited Response
6	R	0	No Processing Control
5	R	0	Reserved
4	R	0	Doesn't Contain Format Information
3	R	1b	Contain Amplifier Parameter
2	R	1b	Out Amp Presented
1	R	0	In Amp Presented
0	R	1b	Stereo

#### Offset

#### Pin Capabilities (Payload = 0Ch)

Response: 0000 233Ch

Bit	Attribute	Default	Description
31:17	R	0	Reserved
16	R	0	EAPD Capable
15:8	R	23h	VRef Control 23h: 100% & 50% & Hi-Z
7	R	0	Reserved
6	R	0	Balanced I/O Pins
5	R	1b	Input Capable
4	R	1b	Output Capable
3	R	1b	Headphone Drive Capable
2	R	1b	Presence Detect Capable
1	R	0	Trigger Required
0	R	0	Impedance Sense Capable

**Offset**

**Input Amplifier Capabilities (Payload = 0Dh)**

Response: 0000 0000h

Bit	Attribute	Default	Description
31	R	0	Mute Capable
30:23	R	0	Reserved
22:16	R	0	Step Size 0: Step size is 0 dB.
15	R	0	Reserved
14:8	R	0	Number of Steps 0: Number of steps is 0h.
7	R	0	Reserved
6:0	R	0	Offset 0000000b: Offset 00h is 0 dB.

**Offset**

**Connection List Length (Payload = 0Eh)**

Response: 0000 0002h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Short Form
6:0	R	0000002b	Only 2 Input Available

**Offset**

**Supported Power States (Payload = 0Fh)**

Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

**Offset**

**Output Amplifier Capabilities (Payload = 12h)**

Response: 8000 0000h

Bit	Attribute	Default	Description
31	R	1b	Mute Capable
30:23	R	0	Reserved
22:16	R	0	Step Size 0: Step size is 0 dB
15	R	0	Reserved
14:8	R	0	Number of Steps 0: Number of steps is 0h.
7	R	0	Reserved
6:0	R	0	Offset

### 8.15.2 Connection Select Control Verbs (Verb ID = F01h & 701h)

	Description	Verb ID	Payload
Get	Get Connection Select	F01h	8'b0
Set	Set Connection Select	701h	The Connection Index Value to be Set. 8'b0: from MW0 8'b1: form AOW2

#### Offset

**Get Response Format** Response: - h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7:0	R	-	Connection Index Currently Set 00h: Connection from MW0 01h: Connection form AOW2

### 8.15.3 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

#### Offset

Response: 0000 2516h

Bit	Attribute	Default	Description
31:16	R	0	Reserved
15:8	R	00100101b	From AOW2
7	R	0	Independent NID
6:0	R	0010110b	From MW0

### 8.15.4 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

#### Offset

**PW5 Power-down Control** Response: 0000 0000h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7:4	R	0	PS-Act. Report the Actual Power State of the Widget.
3:0	RW	0	PS-Set

### 8.15.5 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

#### Offset

**PinCntl Format** Response: 0000 0000h

Bit	Attribute	Default	Description
7	RW	0	Headphone Enable 0: Disabled 1: Headphone enabled
6	RW	0	Output Enable (for Smart 5.1 Configuration) 0: Disabled <span style="float: right;">1: Output enabled</span>
5	RW	0	Input Enable 0: Disabled <span style="float: right;">1: Input enabled</span>
4:3	R	0	Reserved
2:0	RW	0	VRef Enable These bits control the VRef signal associated with the pin widget. 000: Hi-Z <span style="float: right;">001: 50% (half of AVdd)</span> 010: 0V ( Not supported ) <span style="float: right;">101: AVdd</span> Others: Reserved

### 8.15.6 Unsolicited Response Control (Verb ID = F08h & 708h)

	Description	Verb ID	Payload
Get	Get Unsolicited Response Control	F08h	8'b0
Set	Set Unsolicited Response Control	708h	Enable unsolicited response

#### Offset

**Unsolicited Format** Response: 0000 0000h

Bit	Attribute	Default	Description
7	RW	0	0: Unsolicited Response Disabled 1: Unsolicited Response Enabled
6	R	0	Reserved
5:0	RW	0	Tag Used by software to determine which node generated the unsolicited response.



### 8.15.7 Pin Sense Control Verbs (Verb ID = F09h & 709h)

	Description	Verb ID	Payload
Get	Get Pin Sense Control	F09h	8'b0
Set	Set Pin Sense Control	709h	PinCntl

#### Offset

**PinCntl Format** Response: - h

Bit	Attribute	Default	Description
7:1	R	0	Reserved
0	R	-	Right Channel Sense ( Not supported )

#### Offset

Response: - h

Bit	Attribute	Default	Description
31	R	-	Presence Detect 0 : Nothing plugged in <span style="float: right;">1 : Jack plugged in</span>
30:0	R	0	Reserved

### 8.15.8 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

#### Offset

**Config Bits Format** Response: 02A1 9027h

Bit	Attribute	Default	Description
31:30	RW	0	Port Connectivity
29:24	RW	000010b	Location
23:20	RW	1010b	Default Device
19:16	RW	0001b	Connection Type
15:12	RW	1001b	Color
11:8	RW	0	Misc.
7:4	RW	0010b	Default Association
3:0	RW	0111b	Sequence

### 8.15.9 Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	
Set	Set Amplifier Gain/Mute	3h	

#### Offset

##### Get Payload Format

Bit	Attribute	Default	Description
15	W	-	0: The input amplifier is being requested. 1: The output amplifier is being requested (Ignored).
14	W	-	Reserved
13	W	-	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	-	Reserved
3:0	W	-	Index

#### Offset

##### Get Response format

Response: 0000 0000h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	0: Amplifier is un-muted (input default). 1: Amplifier is muted (output default).
6:0	R	0	Amplifier Gain Setting

#### Offset

##### Set Payload Format

Response: 0000 0000h

Bit	Attribute	Default	Description
15	W	-	The Output Amplifier is being Set.
14	W	-	The Input Amplifier is being Set.
13	W	-	The Left Amplifier is being Set.
12	W	-	The Right Amplifier is being Set.
11:8	W	-	Index Ignored
7	W	-	0: Un-mute 1: Mute
6:0	W	-	Gain Setting

## 8.16 Pin Widget PW8 (Node ID = 1Fh) CD Analog Input

### 8.16.1 Get Parameter Verb (Verb ID = F00h)

#### Offset

#### Audio Widget Capabilities (Payload = 09h)

Response: 0040 0401h

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0100	Pin Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	0	Analog Widget, not Digital
8	R	0	Connection List is not Presented
7	R	0	Does not Support Unsolicited Response
6	R	0	No Processing Control
5	R	0	Reserved
4	R	0	Doesn't Contain Format Information
3	R	0	Doesn't Contain Amplifier Parameter
2	R	0	Out Amp not Presented
1	R	0	In Amp not Presented
0	R	1b	Stereo

#### Offset

#### Pin Capabilities (Payload = 0Ch)

Response: 0000 0020h

Bit	Attribute	Default	Description
31:17	R	0	Reserved
16	R	0	EAPD Capable
15:8	R	0	VRef Control
7	R	0	Reserved
6	R	0	Balanced I/O Pins
5	R	1b	Input Capable
4	R	0	Output Capable.
3	R	0	Headphone Drive Capable
2	R	0	Presence Detect Capable
1	R	0	Trigger Required
0	R	0	Impedance Sense Capable

#### Offset

#### Supported Power States (Payload = 0Fh)

Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

### 8.16.2 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

#### Offset

##### PW8 Power-down Control

Response: 0000 0000h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7:4	R	0	PS-Act. Reports the Actual Power State of the Widget.
3:0	RW	0	PS-Set

### 8.16.3 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

#### Offset

##### PinCntl Format

Response: 0000 0000h

Bit	Attribute	Default	Description
7	R	0	Headphone Enable 0: Disabled
6	R	0	Output Enable 0: Disabled
5	RW	0	Input Enable 0: Disabled 1: Input enabled
4:3	R	0	Reserved
2:0	R	0	VRef Enable

#### 8.16.4 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

#### Offset

#### Config Bits Format

Response: 5933 11F8h

Bit	Attribute	Default	Description
31:30	RW	01b	Port Connectivity
29:24	RW	011001b	Location 011001b: Internal
23:20	RW	0011b	Default Device 0011b: CD
19:16	RW	0011b	Connection Type
15:12	RW	0001b	Color
11:8	RW	0001b	Misc
7:4	RW	1111b	Default Association
3:0	RW	1000b	Sequence

## 8.17 Pin Widget PW9 (Node ID = 20h ) S/PDIF TX Pin

### 8.17.1 Get Parameter Verb (Verb ID = F00h)

#### Offset

#### Audio Widget Capabilities (Payload = 09h)

Response: 0040 0701h

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0100b	Pin Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	1b	Digital Widget
8	R	1b	Connection List is Present.
7	R	0	Does not Support Unsolicited Response.
6	R	0	No Processing Control
5	R	0	Reserved
4	R	0	Not Containing Format Information
3	R	0	Not Containing Amplifier Parameter
2	R	0	Out amp not Presented
1	R	0	In amp not Present
0	R	1b	Stereo

#### Offset

#### Pin Capabilities (Payload = 0Ch)

Response: 0000 0010h

Bit	Attribute	Default	Description
31:17	R	0	Reserved
16	R	0	EAPD Capable
15:8	R	0	VRef Control
7	R	0	Reserved
6	R	0	Balanced I/O Pins
5	R	0	Input Capable
4	R	1b	Output Capable
3	R	0	Headphone Drive Capable
2	R	0	Presence Detect Capable
1	R	0	Trigger Required
0	R	0	Impedance Sense Capable

#### Offset

#### Connection List Length (Payload = 0Eh)

Response: 0000 0001h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Short Form
6:0	R	0000001b	1 Input Available

**Offset**

**Supported Power States (Payload = 0Fh)**

Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

**8.17.2 Connection List Entry Control Verbs (Verb ID = F02h)**

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

**Offset**

Response: 0000 0012h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Independent NID
6:0	R	0010010b	From DOW0 (NID = 12h)

**8.17.3 Power State Verbs (Verb ID = F05h & 705h)**

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

**Offset**

**PW9 Power-down Control**

Response: 0000 0400h

Bit	Attribute	Default	Description
31:11	R	0	Reserved
10	R	1b	PS-SettingsReset
9:8	R	0	Reserved
7:4	R	0	PS-Act Reports the actual power state of the widget.
3:0	RW	0	PS-Set

#### 8.17.4 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

#### Offset

##### PinCntl Format

Response: 0000 0000h

Bit	Attribute	Default	Description
7	R	0	Headphone Enable 0: Disabled
6	RW	0	Output Enable 0: Disabled                      1: Output enabled
5	R	0	Input Enable 0: Disabled
4:3	R	0	Reserved
2:0	R	0	VRef Enable

#### 8.17.5 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

#### Offset

##### Config Bits Format

Response: 0744 11F0h

Bit	Attribute	Default	Description
31:30	RW	0	Port Connectivity
29:24	RW	000111b	Location
23:20	RW	0100b	Default Device 0100b: SPDIF Out
19:16	RW	0100b	Connection Type
15:12	RW	0001b	Color
11:8	RW	0001b	Misc.
7:4	RW	1111b	Default Association
3:0	RW	0000b	Sequence



## 8.18 Pin Widget PW10 (Node ID = 21h ) HDMI Audio Output Pin

### 8.18.1 Get Parameter Verb (Verb ID = F00h)

#### Offset

#### Audio Widget Capabilities (Payload = 09h)

Response: 0040 0701h

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0100b	Pin Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R swap.
10	R	1b	Power Control Supported
9	R	1b	Digital Widget
8	R	1b	Connection List is Present
7	R	0	Does not Support Unsolicited Response
6	R	0	No Processing Control
5	R	0	Reserved
4	R	0	Contain no Format Information.
3	R	0	Contain no Amplifier Parameter.
2	R	0	Out amp not Presented
1	R	0	In amp not Present
0	R	1b	Stereo

#### Offset

#### Pin Capabilities (Payload = 0Ch)

Response: 0000 0010h

Bit	Attribute	Default	Description
31:17	R	0	Reserved
16	R	0	EAPD Capable
15:8	R	0	VRef Control
7	R	0	Reserved
6	R	0	Balanced I/O Pins
5	R	0	Input Capable
4	R	1b	Output Capable
3	R	0	Headphone Drive Capable
2	R	0	Presence Detect Capable
1	R	0	Trigger Required
0	R	0	Impedance Sense Capable

#### Offset

#### Connection List Length (Payload = 0Eh)

Response: 0000 0001h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Short Form
6:0	R	0000001b	1 Input Available

**Offset**

**Supported Power States (Payload = 0Fh)**

Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

**8.18.2 Connection List Entry Control Verbs (Verb ID = F02h)**

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

**Offset**

Response: 0000 0015h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Independent NID
6:0	R	0010101b	From DOW1, NID = 15h

**8.18.3 Power State Verbs (Verb ID = F05h & 705h)**

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

**Offset**

**PW10 Power-down Control**

Response: 0000 0400h

Bit	Attribute	Default	Description
31:11	R	0	Reserved
10	R	1b	PS-SettingsReset
9:8	R	0	Reserved
7:4	R	0	PS-Act. Reports the Actual Power State of the Widget.
3:0	RW	0	PS-Set

#### 8.18.4 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

##### Offset

##### PinCntl Format

Response: 0000 0000h

Bit	Attribute	Default	Description
7	R	0	Headphone Enable 0: Disabled
6	RW	0	Output Enable 0: Disabled 1: Output enabled
5	R	0	Input Enable 0: Disabled
4:3	R	0	Reserved
2:0	R	0	VRef Enable

#### 8.18.5 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

##### Offset

##### Config Bits Format

Response: 9856 01F0h

Bit	Attribute	Default	Description
31:30	RW	10b	Port Connectivity
29:24	RW	011000b	Location
23:20	RW	0101b	Default Device 0101b: SPDIF Out
19:16	RW	0110b	Connection Type
15:12	RW	0000b	Color
11:8	RW	0001b	Misc.
7:4	RW	1111b	Default Association
3:0	RW	0000b	Sequence

## 9 Functional Descriptions

### 9.1 Clock Control

One of the major differences between the High Definition Audio Specification and AC97 is the clock source. The High Definition Audio Controller provides a 24 MHz clock (BITCLK). An internal PLL (PLL1) in the codec uses BITCLK (24 MHz) as the reference clock and generates 49.152 MHz clocks for internal use. A second PLL (PLL2) also takes the 24 MHz BITCLK and generates 22.5792 MHz clock for 44.1 kHz base rates. The PLLs can be powered down by the Power Widget for power management. **Both PLL output clocks can be routed to Pin 48 by a vendor defined verb for testing.**

The interface signals between digital block and the 2 PLLs are listed below.

PLL1 (49.152 MHz)		
Pin Name	Direction (From PLL)	Pin Description
REFCLK	I	Connect to a 24-MHz clock input.
CLK49152	O	49.152-MHz clock output.
RST	I	When RST is high, the PLL enters a low power mode and all internal states are reset.
PWRPD	I	When PWRPD is high, the PLL enters a power-down mode.
VDD	IO	Digital power supply for PFD and Dividers. Nominally 3.3V.
GND	IO	Ground for PFD and Dividers.
VCOPWR	IO	Analog power supply for VCO. Nominally 3.3V.
VCOGND	IO	Ground for VCO.
CHGPPWR	IO	Analog power supply for Bias and Charge Pump. Nominally 3.3V.
CHGPGND	IO	Ground for Bias and Charge Pump.

22.5792 MHz		
Pin Name	Direction (From PLL)	Pin Description
REFCLK	I	Connect to a 24-MHz clock input.
CLK225792	O	22.5792-MHz clock output.
RST	I	When RST is high, the PLL enters a low power mode and all internal states are reset.
PWRPD	I	When PWRPD is high, the PLL enters a power-down mode.
VDD	IO	Digital power supply for PFD and Dividers. Nominally 3.3V.
GND	IO	Ground for PFD and Dividers.
VCOPWR	IO	Analog power supply for VCO. Nominally 3.3V.
VCOGND	IO	Ground for VCO.
CHGPPWR	IO	Analog power supply for Bias and Charge Pump. Nominally 3.3V.
CHGPGND	IO	Ground for Bias and Charge Pump.

### 9.2 Interpolation / Decimation

To take advantage of the high bandwidth provided by the new audio interface, the hardware only supports native 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, and 192 kHz sample rates, and the driver is responsible for converting the data to / from 192 kHz. This way the large area previously required for implementing the digital interpolation / decimation filters can be saved.

### 9.3 HPF for ADC DC Removal

The built-in high-pass filter for each ADC can remove the DC component in the ADC data.

### 9.4 Audio Jack Detection Circuits

Based on the jack detection circuit defined in the High Definition Audio Specification, the figure below summarizes the equivalent resistance values to the SENSE Pin in different scenario.

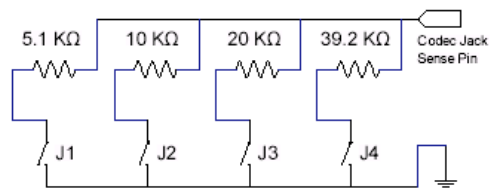


Figure 19 – Jack Detect Circuit

### 9.5 Internal Loop-back and Peak Detection for Low Cost Production Test

Internal loop-back paths can be used to test all DACs and ADCs functions. The output of each DAC can be routed back to the input of the ADC. The ADC output data is analyzed by a specially designed block to detect the zero-crossing point and the peak values. These information can be read back to decide whether the digital & analog functions are normal. Refer to the descriptions in the Vendor-Defined Verbs in the Audio Function Group.

### 9.6 GPIO Implementation

#### 9.6.1 GPIO Pinout

- Pin 47: EAPD
- Pin 48: SPDIF\_TX0
- Pin 2: GPIO0/ SPDIF\_TX1
- Pin 3: GPIO1

#### 9.6.2 Usage

- GPI:
  - Front Panel Sense
  - Others
- GPO:
  - EAPD-like Control
  - Others

	NB 1	NB 2	NB 3	Desk Top 1	Desk Top 2	I/O
GPO for EAPD0 (Line Out)	√	√	√	-	-	-
GPO for EAPD1 (Head Phone)	√	√	√	-	-	-
SPDIF_TX0	√	√	√	√	√	-
SPDIF_TX1	-	-	-	√	√	-
GPI (Front Panel Sense)	√	√	-	√	-	-
Pin 47: EAPD	GPO	GPO	GPO	-	-	O
Pin 48: SPDIF_TX0	SPDIF_TX0	SPDIF_TX0	SPDIF_TX0	SPDIF_TX0	SPDIF_TX0	O
Pin 2: SPDIF_TX1	GPO	GPO	GPO	SPDIF_TX1	SPDIF_TX1	IO
Pin 3: GPIO1	GPI	GPI	-	GPI	-	IO

## 10 Electrical Specification

### Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit	Note
T <sub>S</sub>	Storage Temperature	-55	125	°C	—
T <sub>A</sub>	Ambient Operating Temperature	0	85	°C	—
V <sub>ESD</sub>	Electrostatic Discharge (human body model)	—	2	kV	—

Note: Stress above conditions may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described.

### Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit	Note
AVDD	Analog Power Supplies (preferred)	—	5	—	V
AVDD	Analog Power Supplies (for low-power apps)	—	3.3	—	V

### Digital DC and AC Characteristics

#### DC Performance Characteristic

Symbol	Parameter	Min	Typ	Max	Unit
DVdd	Digital Power Supply	3.135	3.3	3.465	V
V <sub>IN</sub>	Input Voltage Range	-0.3		DVdd + 0.3	V
V <sub>IL</sub>	Low Level Input Voltage			0.35 x DVdd	V
V <sub>IH</sub>	High Level Input Voltage	0.65 x DVdd			V
V <sub>OH</sub>	High Level Output Voltage	0.9 x DVdd			V
V <sub>OL</sub>	Low Level Output Voltage			0.1 x DVdd	V
	Input Leakage Current (AC-Link inputs)	-10		10	μA
	Output Leakage Current (Hi-Z'd AC-Link outputs)	-10		10	μA
	Input / Output Pin Capacitance			7.5	pF

### Analog Performance Characteristics

Parameter	Min	Type	Max	Unit
<b>Analog Input</b>				
Full Scale Input Voltage				
Line Inputs		1.0		Vrms
Mic Inputs with 20 dB Gain		0.1		
Mic inputs with 0 dB Gain		1		
Input Impedance	10			kΩ
Input Capacitance		7.5		pF
Power Supply Rejection Ratio (10 kHz)		54.59		dB
Power Supply Rejection Ratio (1 kHz)		56.72		dB
<b>Analog Output</b>				
Full Scale Output Voltage				
Line Output		1.0		Vrms
Headphone Output			1.41	
Analog S/N				
Other to LINE_OUT		100		dB
Analog Frequency Response	20		20,000	Hz
Vrefout		2.25-2.75		V
Power Supply Rejection Ratio (10 kHz)		98.8		dB
Power Supply Rejection Ratio (1 kHz)		80.4		dB
<b>ADC Converters</b>				
Dynamic Range (-60 dB Full Scale, A-Weight)		93		dB
Total Harmonic Distortion			0.003	%
Frequency Response	20		21,600	Hz
Transition Band	21,600		28,800	Hz
Stop Band	28,800			Hz
Stop Band Rejection	-74			dB
Out-of-Band Rejection		-40		dB
Spurious Tone Reduction		-100		dB
Attenuation, Gain Step Size		1.5		dB
<b>DAC Converters</b>				
Dynamic Range (-60 dB Full Scale, A-Weight)		100		dB
Total Harmonic Distortion			0.003	%
Frequency Response	20		21,600	Hz
Transition Band	21,600		28,800	Hz
Stop Band	28800			Hz
Stop Band Rejection	-75			dB
Out-of-Band Rejection		-40		dB
Channel Separation		-90		dB
Spurious Tone Reduction		-100		dB
Attenuation, Gain Step Size		1.5		dB

Note: The frequency response, transition band and stop band specified in the table is based on  $f_s = 48$  kHz, and scale with  $f_s$ .





## 12 Application Circuit

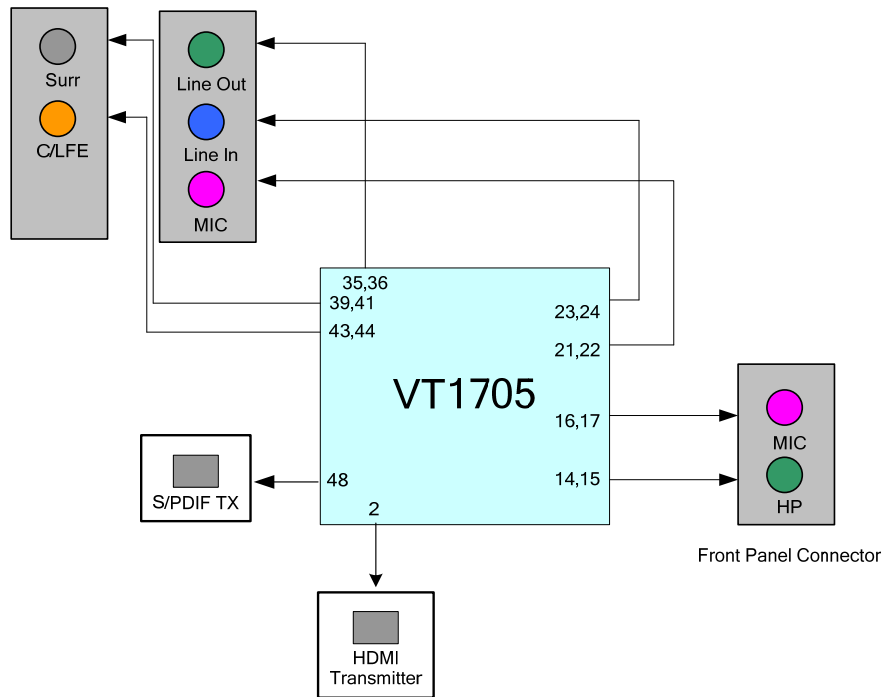


Figure 21 - The System with Front Panel Design

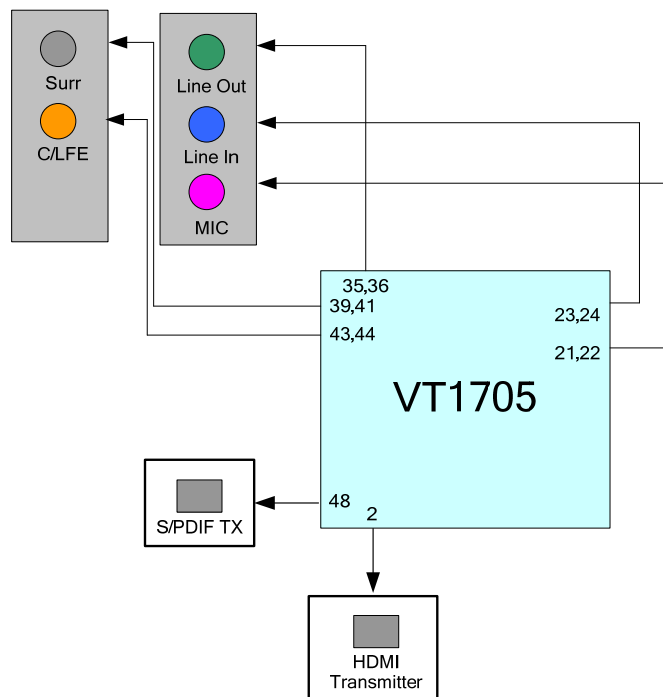


Figure 22 - The System without Front Panel Design

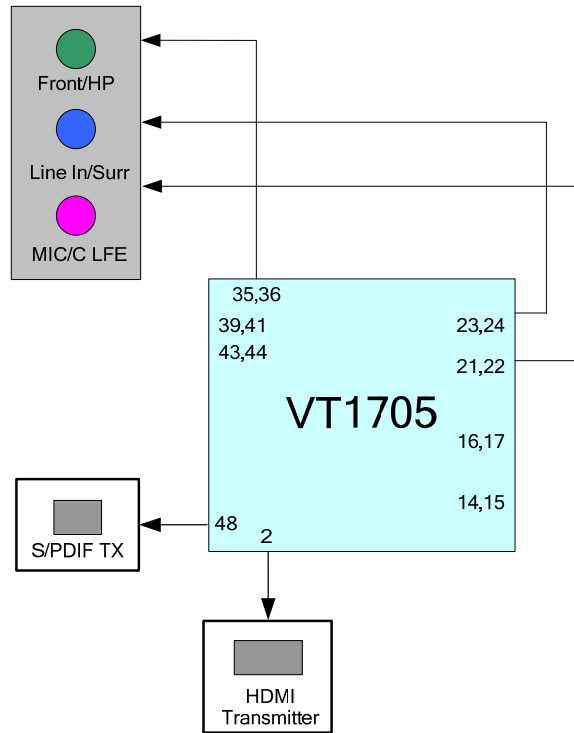


Figure 23 – The System with Only One Back Panel Connector Design

Copyright © 2008-2009 VIA Technologies Incorporated. All Rights Reserved. No part of this document may be reproduced, transmitted, transcribed, stored in a retrieval system, or translated into any language, in any form or by any means, electronic, mechanical, magnetic, optical, chemical, manual or otherwise without the prior written permission of VIA Technologies Incorporated. The material in this document is for information only and is subject to change without notice. VIA Technologies Incorporated reserves the right to make changes in the product design without reservation and without notice to its users.

All trademarks are the properties of their respective owners.

No license is granted, implied or otherwise, under any patent or patent rights of VIA Technologies, Inc. VIA Technologies makes no warranties, implied or otherwise, in regard to this document and to the products described in this document. The information provided by this document is believed to be accurate and reliable as of the publication date of this document. However, VIA Technologies assumes no responsibility for any errors in this document. Furthermore, VIA Technologies assumes no responsibility for the use or misuse of the information in this document and for any patent infringements that may arise from the use of this document. The information and product specifications within this document are subject to change at any time, without notice and without obligation to notify any person of such change.

VIA Technologies Incorporated  
Taiwan Office:  
1st Floor, No. 531  
Chung-Cheng Road, Hsin-Tien  
Taipei, Taiwan ROC  
Tel (886-2) 2218-5452  
Fax (886-2) 2218-5453  
URL <http://www.via.com.tw>

VIA Technologies Incorporated  
USA Office:  
940 Mission Court  
Fremont, CA 94539  
USA  
Tel (510) 683-3300  
Fax (510) 683-3301 or (510) 687-4654  
URL <http://www.viatech.com>