



VT82C595

APOLLO VP2

**Low-Power Single-Chip
Pentium / PCI North Bridge
with SDRAM / EDO / FPG and ECC
for Highly-Integrated Green PC Desktop
and Notebook Computers**

Preliminary Revision 0.4
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VIA TECHNOLOGIES, INC.

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Offices:

USA Office:

5020 Brandin Court
Fremont, CA 94538
USA

Tel: (510) 683-3300

Fax: (510) 683-3301

Taipei Office:

8th Floor, No. 533
Chung-Cheng Rd., Hsin-Tien
Taipei, Taiwan ROC

Tel: (886-2) 218-5452

Fax: (886-2) 218-5453

Online Services:

Home Page: <http://www.via.com.tw/>

FTP Server: <ftp.via.com.tw>

BBS: 886-2-2185208

REVISION HISTORY

Document Release	Date	Revision	Initials
Preliminary	4/15/96	Original release	
Version 0.2	7/19/96	<p>a. General Update:</p> <ol style="list-style-type: none"> 1. Add AC timing characteristics and BGA package info 2. Take out BEDO support (register 64,65,66 for VT82C595) 3. Pin number typo for signal MPD2 (J18) and AD28 (B3) of VT82C586 <p>b. VT82C595 with revision ID >= 01h</p> <ol style="list-style-type: none"> 1. Add multi-function capability to five pins (H6, P6, T11,N17,M17) to drive three DIMM modules (6 banks) of SDRAMs 2. Change pin N16 to MA13 to support 4 bank interleaving of 64Mbit SDRAMs 3. Move bit 3 of register 6E to bit 3 of register 65 4. Change partial bit definition of registers 51, 52, 58, 64, 65, 66, 67, 6B, 6C, 6D <p>c. VT82C586 with revision ID >= 20h</p> <ol style="list-style-type: none"> 1. Change pin 91 to DRDYB# and pin 92 to APICCS# 2. Change pin 137 to multifunction pin: MASTER#/IRQ12 3. Change register 43, 46-48 of PCI-ISA bridge (device ID=0586h) 4. Add register 50-53 of integrated enhanced IDE controller (ID=0571h) for supporting the Ultra DMA/33 mode operation 5. Add register for integrated USB controller (Function 2 of VT82C586) 	TL
Version 0.3	9/20/96	<ol style="list-style-type: none"> 1. Reformat document to conform to standard data sheet format 2. Clean up register definitions, add default values to all registers 3. Add register summary tables 4. Add legacy ISA I/O register definitions (DMA, IRQ, KBC, RTC) 5. Change "VT82C586" to "VT82C586A" (USB/UltraDMA33 enhanced) 6. Fix VT82C586A pinout documentation errors: <ul style="list-style-type: none"> Pin 89 change to DRDYB# (was MDRQ0) Pin 90 change to APICCS# (was MDACK0) Pin 91 change to MDRQ0 (was DRDYB#) Pin 92 change to MDACK0 (was APICCS#) RTCCS# on wrong pin in pin list (pin description was correct) (RTCCS# is an alternate function of pin 105 not pin 98) 	DH
Version 0.4	1/2/97	<ol style="list-style-type: none"> 1. Removed VT82C586A information to make this a North-Bridge-only document (separate data sheets now available for VT82C586A and 586B) 2. Removed references to parity (chip implements ECC only) 3. Removed references to UMA capability (not implemented) 4. Fixed pin definition errors: Rx50[4-3], Rx52[7-4, 1], Rx64-67, Rx6E-6F 	DH

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**VIA VT82C595 APOLLO VP2
LOW-POWER SINGLE-CHIP
PENTIUM / PCI NORTH BRIDGE
WITH SDRAM / EDO / FPG AND ECC
FOR HIGHLY-INTEGRATED GREEN PC DESKTOP
AND NOTEBOOK COMPUTERS**

- **PCI/ISA Green PC Ready**

- Supports 3.3V or 5V interface to CPU, system memory, and / or PCI bus
- Supports CPUs with internal voltages below 3.3V
- PC-97 compatible using VT82C586B South Bridge with ACPI Power Management

- **High Integration**

- Single chip implementation for 64-bit Pentium-CPU, 64-bit system memory, and 32-bit PCI interface
- VT82C590 Apollo VP2 Chipset: **VT82C595** system controller and **VT82C586B** PCI to ISA bridge
- Chipset includes UltraDMA-33 EIDE, USB, and Keyboard / PS2-Mouse Interfaces plus RTC / CMOS on chip
- Six TTLs for a complete main board implementation

- **Flexible CPU Interface**

- Supports 64-bit Pentium™, AMD 5_K86™, AMD 6_K86™ and Cyrix 6_X86™ CPUs
- CPU external bus speed up to 66 Mhz (internal 200Mhz and above)
- Supports CPU internal write-back cache
- System management interrupt, memory remap and STPCLK mechanism
- Cyrix 6_X86 linear burst support
- CPU NA# / Address pipeline capability

- **Advanced Cache Controller**

- Direct map write back or write through secondary cache
- Pipelined burst synchronous SRAM (PBSRAM) cache support (with global write enable feature)
- Flexible cache size: 0K/256K/512K/1M/2MB
- 32 byte line size to match the primary cache
- Integrated 10-bit tag comparator
- 3-1-1-1 read/write timing for PBSRAM access at 66 Mhz
- 3-1-1-1-1-1 back to back read timing for PBSRAM access at 66 Mhz
- Sustained 3 cycle write access for PBSRAM access or CPU to DRAM and PCI bus post write buffers at 66 Mhz
- Data streaming for simultaneous primary and secondary cache line fill
- System and video BIOS cacheable and write-protect
- Programmable cacheable region and cache timing

- **Fast DRAM Controller**

- Fast Page Mode/EDO/Synchronous-DRAM support in a mixed combination
- Mixed 1M/2M/4M/8M/16MxN DRAMs
- 6 banks up to 512MB DRAMs
- Flexible row and column addresses
- 64-bit or 32-bit data width in arbitrary mixed combination
- 3.3v and 5v DRAM without external buffers
- Optional bank-by-bank ECC (single-bit error correction and multi-bit error detection) for DRAM integrity
- Two-bank interleaving for 16Mbit SDRAM support
- Two-bank and four bank interleaving for 64Mbit SDRAM support (14 MA lines)
- Four cache lines (16 quadwords) of CPU/cache to DRAM write buffers
- Concurrent DRAM writeback
- Speculative DRAM access
- Read around write capability for non-stalled CPU read
- Burst read and write operation
- 4-2-2-2 on page, 7-2-2-2 start page and 9-2-2-2 off page timing for EDO DRAMs at 50/60 MHz
- 5-2-2-2 on page, 8-2-2-2 start page and 11-2-2-2 off page timing for EDO DRAMs at 66 MHz
- 6-1-1-1 on page, 8-1-1-1 start page and 10-1-1-1 off page for SDRAMs at 66 MHz
- 5-2-2-2-3-1-2-2 back-to-back access for EDO DRAM at 66 MHz
- 6-1-1-1-3-1-1-1 back-to-back access for SDRAM at 66 MHz
- BIOS shadow at 16KB increment
- Decoupled and burst DRAM refresh with staggered RAS timing
- Programmable refresh rate, CAS-before-RAS refresh and refresh on populated banks only

- **Intelligent PCI Bus Controller**

- 32 bit 3.3/5v PCI interface
- Synchronous divide-by-two PCI bus interface
- PCI master snoop ahead and snoop filtering
- PCI master peer concurrency
- Synchronous bus to CPU clock with divide-by-two from the CPU clock
- Automatic detection of data streaming burst cycles from CPU to the PCI bus
- Five levels (double-words) of CPU to PCI posted write buffers
- Byte merging in the write buffers to reduce the number of PCI cycles and to create further PCI bursting possibilities
- Zero wait state PCI master and slave burst transfer rate
- PCI to system memory data streaming up to 132Mbyte/sec
- Forty-eight levels (double-words) of post write buffers from PCI masters to DRAM
- Sixteen levels (double-words) of prefetch buffers from DRAM for access by PCI masters
- Enhanced PCI command optimization (MRL, MRM, MWI, etc.)
- Complete steerable PCI interrupts
- Supports L1 write-back forward to PCI master read to minimize PCI read latency
- Supports L1 write-back merged with PCI master post-write to minimize DRAM utilization
- Provides transaction timer to fairly arbitrate between PCI masters
- PCI-2.1 compliant

- **Built-in nand-tree pin scan test capability**

- **0.6um mixed voltage, high speed / low power CMOS process**

- **328 pin Low-Profile BGA Package**

OVERVIEW

The VT82C590 *Apollo-VP2* is a high performance, cost-effective and energy efficient chip set for the implementation of PCI/ISA desktop and notebook personal computer systems based on the 64-bit Pentium/AMD5_K86/AMD6_K86/Cyrix6_X86 super-scalar processors.

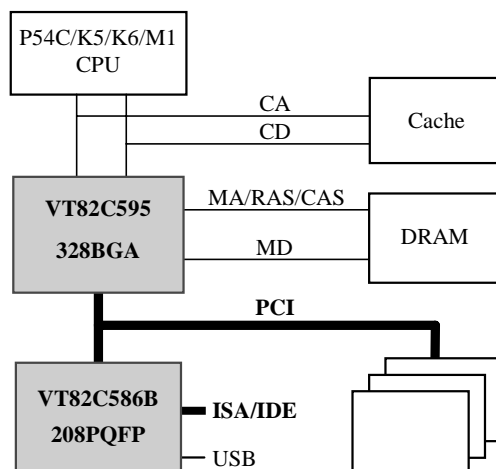


Figure 1. Apollo VP2 System Block Diagram

The Apollo-VP2 chip set consists of the VT82C595 system controller (328 pin BGA) and the VT82C586B PCI to ISA bridge (208 pin PQFP). The VT82C595 system controller provides superior performance between the CPU, optional synchronous cache, DRAM and the PCI bus with pipelined, burst and concurrent operation. For pipelined burst synchronous SRAMs, 3-1-1-1-1-1-1 timing can be achieved for both read and write transactions at 66 Mhz. Four cache lines (16 quadwords) of CPU/cache to DRAM write buffers with concurrent write-back capability are included in the chip to speed up the cache read and write miss cycles.

The VT82C595 supports six banks of DRAMs up to 512KB. The DRAM controller supports Standard Page Mode DRAM, EDO-DRAM and Synchronous DRAM in a flexible mix / match manner. The Synchronous DRAM interface allows zero wait state bursting between the DRAM and the data buffers at 66Mhz. The six banks of DRAM can be composed of an arbitrary mixture of 1M / 2M / 4M / 8M / 16MxN DRAMs. Each bank may be populated with either 32bit or 64bit data width. The DRAM controller also supports optional ECC (single-bit error correction and multi-bit detection) capability.

The VT82C595 supports 3.3 / 5V 32-bit PCI bus with 64-bit to 32-bit data conversion. Five levels (doublewords) of post write buffers are included to allow for concurrent CPU and PCI operation. Consecutive CPU addresses are converted into burst PCI cycles with byte merging capability for optimal CPU to PCI throughput. For PCI master operation, forty-eight levels (doublewords) of post write buffers and sixteen levels (doublewords) of prefetch buffers are included for concurrent PCI bus and DRAM/cache accesses. The chipset also supports enhanced PCI bus commands such as Memory-Read-Line, Memory-Read-Multiple and Memory-Write-Invalid commands to minimize snoop overhead. In addition, the chipset supports advanced features such as snoop ahead, snoop filtering, L1 write-back forward to PCI master and L1 write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. The VT82C586B PCI to ISA bridge supports four levels (doublewords) of line buffers, type F DMA transfers and delay transaction to allow efficient PCI bus utilization and (PCI-2.1 compliant). The VT82C586B also includes an integrated keyboard controller with PS2 mouse support, integrated DS12885 style real time clock with extended 256 byte CMOS RAM, integrated master mode enhanced IDE controller with full scatter and gather capability and extension to UltraDMA-33 / ATA-33 for 33MB/sec transfer rate, integrated USB interface with root hub and two function ports with built-in physical layer transceivers, Distributed DMA support, and OnNow / ACPI compliant advanced configuration and power management interface. A complete main board can be implemented with only six TTLs.

The VT82C590 chipset is ideal for high performance, high quality, high energy efficient and high integration desktop and notebook PCI/ISA computer systems.

PINOOTS

Figure 2. VT82C595 Ball Diagram (Top View)

Key	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	HD63	AD31	AD29	AD27	CBE3#	AD21	AD18	CBE2#	AD14	AD11	AD8	AD6	AD3	AD1	AD0	MD62	MD29	MD60	MD27	MD43
B	HD62	AD30	AD28	AD26	AD23	AD20	AD17	CBE1#	AD13	AD10	CBE0#	AD5	AD2	MD31	MD14	MD13	MD61	MD12	MD59	MD58
C	HD59	HD60	HD61	AD25	AD22	AD19	AD16	AD15	AD12	AD9	AD7	AD4	MD15	MD47	MD63	MD45	MD28	MD11	MD10	MD42
D	HD55	HD58	HD57	PREQ#	PGNT#	AD24	REQ0#	GNT0#	REQ1#	GNT1#	REQ2#	GNT2#	REQ3#	GNT3#	MD46	MD30	MD44	MD26	MD57	MD9
E	HD52	HD54	HD56	HD53	LOCK#	FRAME#	IRDY#	TRDY#	DEVSEL#	PCLK	STOP#	PAR	SERR#	VDD5	GND	RAS3#	MD25	MD41	MD24	MD56
F	HD48	HD47	HD51	HD50	VDD3	VDD3	MA12							VDD3	VDD3	RAS2#	RAS1#	MD8	MD40	MPD3
G	HD45	HD41	HD49	HD43	HLOCK#	VDD5									SWEB#	CAS6#	RAS0#	MPD7	MPD1	MPD5
H	HD39	HD40	HD46	HD44	M/IO#	SRASC#										CAS4#	CAS2#	MPD4	MPD0	MPD6
J	HD37	HD36	HD42	HD38	CACHE#				GND	GND	GND	GND				CAS5#	CAS0#	MPD2	MD55	MD23
K	HD34	BE0#	BE1#	BE2#	KEN#				GND	GND	GND	GND				HCLK	CAS1#	MD39	MD7	MD54
L	BE3#	BE4#	BE5#	BE6#	AHOLD				GND	GND	GND	GND				CAS7#	CAS3#	MD22	MD38	MD6
M	BE7#	HD33	HD32	HD35	BRDY#				GND	GND	GND	GND				SWEA#	RAS4#	MD53	MD21	MD37
N	HD27	HD30	HD29	HD31	NA#											MA13	RAS5#	MD5	MD52	MD20
P	HD23	HD26	HD25	HD28	BOFF#	SCASC#									VDD3	TA0	MD19	MD36	MD4	MD51
R	HD7	HD21	HD19	HD24	EADS#	VDD3	VDD3								VDD3	VDD3	MD35	MD18	MD50	MD3
T	HD12	HD22	HD17	HD20	ADS#	GND	D/C#	HITM#	W/R#	SMIACT#	SWEC#	MA1	MA6	TA4	RESET#	GND	MD1	MD49	MD2	MD34
U	HD8	HD18	HD14	HD16	HA20	HA16	HA12	HA5	HA23	HA22	HA29	SCASB#	MA5	MA8	COE#	TA1	TA2	MD16	MD33	MD17
V	HD6	HD15	HD10	HD13	HA19	HA14	HA9	HA8	HA21	HA26	HA3	MA0	MA4	MA11	CADV#	TAGWE#	TA3	TA5	MD32	MD48
W	HD4	HD5	HD9	HD11	HA18	HA15	HA11	HA31	HA25	HA24	HA30	SCASA#	MA3	MA7	CADS#	CE1#	SRASB#	TA6	TA8	MD0
Y	HD0	HD2	HD1	HD3	HA17	HA13	HA10	HA7	HA27	HA28	HA4	HA6	MA2	MA10	MA9	GWE#	BWE#	TA7	TA9	SRASA#

Figure 3. VT82C595 Pin List (Numerical Order)

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
A1	HD63	D7	REQ0#	H16	CAS4# / DQM4#	N16	MA13	U17	TA2
A2	AD31	D8	GNT0#	H17	CAS2# / DQM2#	N17	RAS5# / CS5#	U18	MD16
A3	AD29	D9	REQ1#	H18	MPD4	N18	MD5	U19	MD33
A4	AD27	D10	GNT1#	H19	MPD0	N19	MD52	U20	MD17
A5	CBE3#	D11	REQ2#	H20	MPD6	N20	MD20	V1	HD6
A6	AD21	D12	GNT2#	J1	HD37	P1	HD23	V2	HD15
A7	AD18	D13	REQ3#	J2	HD36	P2	HD26	V3	HD10
A8	CBE2#	D14	GNT3#	J3	HD42	P3	HD25	V4	HD13
A9	AD14	D15	MD46	J4	HD38	P4	HD28	V5	HA19
A10	AD11	D16	MD30	J5	CACHE#	P5	BOFF#	V6	HA14
A11	AD8	D17	MD44	J9	GND	P6	SCASC#	V7	HA9
A12	AD6	D18	MD26	J10	GND	P15	VDD3	V8	HA8
A13	AD3	D19	MD57	J11	GND	P16	TA0	V9	HA21
A14	AD1	D20	MD9	J12	GND	P17	MD19	V10	HA26
A15	AD0	E1	HD52	J16	CAS5# / DQM5#	P18	MD36	V11	HA3
A16	MD62	E2	HD54	J17	CAS0# / DQM0#	P19	MD4	V12	MA0
A17	MD29	E3	HD56	J18	MPD2	P20	MD51	V13	MA4
A18	MD60	E4	HD53	J19	MD55	R1	HD7	V14	MA11
A19	MD27	E5	LOCK#	J20	MD23	R2	HD21	V15	CADV#
A20	MD43	E6	FRAME#	K1	HD34	R3	HD19	V16	TAGWE#
B1	HD62	E7	IRDY#	K2	BE0#	R4	HD24	V17	TA3
B2	AD30	E8	TRDY#	K3	BE1#	R5	EADS#	V18	TA5
B3	AD28	E9	DEVSEL#	K4	BE2#	R6	VDD3	V19	MD32
B4	AD26	E10	PCLK	K5	KEN#/INV	R7	VDD3	V20	MD48
B5	AD23	E11	STOP#	K9	GND	R15	VDD3	W1	HD4
B6	AD20	E12	PAR	K10	GND	R16	VDD3	W2	HD5
B7	AD17	E13	SERR#	K11	GND	R17	MD35	W3	HD9
B8	CBE1#	E14	VDD5	K12	GND	R18	MD18	W4	HD11
B9	AD13	E15	GND	K16	HCLK	R19	MD50	W5	HA18
B10	AD10	E16	RAS3# / CS3#	K17	CAS1# / DQM1#	R20	MD3	W6	HA15
B11	CBE0#	E17	MD25	K18	MD39	T1	HD12	W7	HA11
B12	AD5	E18	MD41	K19	MD7	T2	HD22	W8	HA31
B13	AD2	E19	MD24	K20	MD54	T3	HD17	W9	HA25
B14	MD31	E20	MD56	L1	BE3#	T4	HD20	W10	HA24
B15	MD14	F1	HD48	L2	BE4#	T5	ADS#	W11	HA30
B16	MD13	F2	HD47	L3	BE5#	T6	GND	W12	SCASA#
B17	MD61	F3	HD51	L4	BE6#	T7	D/C#	W13	MA3
B18	MD12	F4	HD50	L5	AHOLD	T8	HITM#	W14	MA7
B19	MD59	F5	VDD3	L9	GND	T9	W/R#	W15	CADS#
B20	MD58	F6	VDD3	L10	GND	T10	SMIACT#	W16	CE1#
C1	HD59	F7	MA12	L11	GND	T11	SWEC# / MWE#	W17	SRASB#
C2	HD60	F14	VDD3	L12	GND	T12	MA1	W18	TA6
C3	HD61	F15	VDD3	L16	CAS7# / DQM7#	T13	MA6	W19	TA8
C4	AD25	F16	RAS2# / CS2#	L17	CAS3# / DQM3#	T14	TA4	W20	MD0
C5	AD22	F17	RAS1# / CS1#	L18	MD22	T15	RESET#	Y1	HD0
C6	AD19	F18	MD8	L19	MD38	T16	GND	Y2	HD2
C7	AD16	F19	MD40	L20	MD6	T17	MD1	Y3	HD1
C8	AD15	F20	MPD3	M1	BE7#	T18	MD49	Y4	HD3
C9	AD12	G1	HD45	M2	HD33	T19	MD2	Y5	HA17
C10	AD9	G2	HD41	M3	HD32	T20	MD34	Y6	HA13
C11	AD7	G3	HD49	M4	HD35	U1	HD8	Y7	HA10
C12	AD4	G4	HD43	M5	BRDY#	U2	HD18	Y8	HA7
C13	MD15	G5	HLOCK#	M9	GND	U3	HD14	Y9	HA27
C14	MD47	G6	VDD5	M10	GND	U4	HD16	Y10	HA28
C15	MD63	G15	SWEB#	M11	GND	U5	HA20	Y11	HA4
C16	MD45	G16	CAS6# / DQM6#	M12	GND	U6	HA16	Y12	HA6
C17	MD28	G17	RAS0# / CS0#	M16	SWEA#	U7	HA12	Y13	MA2
C18	MD11	G18	MPD7	M17	RAS4# / CS4#	U8	HA5	Y14	MA10
C19	MD10	G19	MPD1	M18	MD53	U9	HA23	Y15	MA9
C20	MD42	G20	MPD5	M19	MD21	U10	HA22	Y16	GWE#
D1	HD55	H1	HD39	M20	MD37	U11	HA29	Y17	BWE#
D2	HD58	H2	HD40	N1	HD27	U12	SCASB#	Y18	TA7
D3	HD57	H3	HD46	N2	HD30	U13	MA5	Y19	TA9
D4	PREQ#	H4	HD44	N3	HD29	U14	MA8	Y20	SRASA#
D5	PGNT#	H5	M/IO#	N4	HD31	U15	COE#		
D6	AD24	H6	SRASC#	N5	NA#	U16	TA1		

Figure 4. VT82C595 Pin List (Alphabetical Order)

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
A15	AD0	N17	CS5# / RAS5#	U1	HD8	U13	MA5	B20	MD58
A14	AD1	T7	D/C#	W3	HD9	T13	MA6	B19	MD59
B13	AD2	E9	DEVSEL#	V3	HD10	W14	MA7	A18	MD60
A13	AD3	R5	EADS#	W4	HD11	U14	MA8	B17	MD61
C12	AD4	E6	FRAME#	T1	HD12	Y15	MA9	A16	MD62
B12	AD5	E15	GND	V4	HD13	Y14	MA10	C15	MD63
A12	AD6	J9	GND	U3	HD14	V14	MA11	H19	MPD0
C11	AD7	J10	GND	V2	HD15	F7	MA12	G19	MPD1
A11	AD8	J11	GND	U4	HD16	N16	MA13	J18	MPD2
C10	AD9	J12	GND	T3	HD17	W20	MD0	F20	MPD3
B10	AD10	K9	GND	U2	HD18	T17	MD1	H18	MPD4
A10	AD11	K10	GND	R3	HD19	T19	MD2	G20	MPD5
C9	AD12	K11	GND	T4	HD20	R20	MD3	H20	MPD6
B9	AD13	K12	GND	R2	HD21	P19	MD4	G18	MPD7
A9	AD14	L9	GND	T2	HD22	N18	MD5	T11	MWE# / SWEC#
C8	AD15	L10	GND	P1	HD23	L20	MD6	N5	NA#
C7	AD16	L11	GND	R4	HD24	K19	MD7	E12	PAR
B7	AD17	L12	GND	P3	HD25	F18	MD8	E10	PCLK
A7	AD18	M9	GND	P2	HD26	D20	MD9	D5	PGNT#
C6	AD19	M10	GND	N1	HD27	C19	MD10	D4	PREQ#
B6	AD20	M11	GND	P4	HD28	C18	MD11	G17	RAS0# / CS0#
A6	AD21	M12	GND	N3	HD29	B18	MD12	F17	RAS1# / CS1#
C5	AD22	T6	GND	N2	HD30	B16	MD13	F16	RAS2# / CS2#
B5	AD23	T16	GND	N4	HD31	B15	MD14	E16	RAS3# / CS3#
D6	AD24	D8	GNT0#	M3	HD32	C13	MD15	M17	RAS4# / CS4#
C4	AD25	D10	GNT1#	M2	HD33	U18	MD16	N17	RAS5# / CS5#
B4	AD26	D12	GNT2#	K1	HD34	U20	MD17	D7	REQ0#
A4	AD27	D14	GNT3#	M4	HD35	R18	MD18	D9	REQ1#
B3	AD28	Y16	GWE#	J2	HD36	P17	MD19	D11	REQ2#
A3	AD29	V11	HA3	J1	HD37	N20	MD20	D13	REQ3#
B2	AD30	Y11	HA4	J4	HD38	M19	MD21	T15	RESET#
A2	AD31	U8	HA5	H1	HD39	L18	MD22	W12	SCASA#
T5	ADS#	Y12	HA6	H2	HD40	J20	MD23	U12	SCASB#
L5	AHOLD	Y8	HA7	G2	HD41	E19	MD24	P6	SCASC#
K2	BE0#	V8	HA8	J3	HD42	E17	MD25	E13	SERR#
K3	BE1#	V7	HA9	G4	HD43	D18	MD26	T10	SMACT#
K4	BE2#	Y7	HA10	H4	HD44	A19	MD27	Y20	SRASA#
L1	BE3#	W7	HA11	G1	HD45	C17	MD28	W17	SRASB#
L2	BE4#	U7	HA12	H3	HD46	A17	MD29	H6	SRASC#
L3	BE5#	Y6	HA13	F2	HD47	D16	MD30	E11	STOP#
L4	BE6#	V6	HA14	F1	HD48	B14	MD31	M16	SWEA#
M1	BE7#	W6	HA15	G3	HD49	V19	MD32	G15	SWEB#
P5	BOFF#	U6	HA16	F4	HD50	U19	MD33	T11	SWEC# / MWE#
M5	BRDY#	Y5	HA17	F3	HD51	T20	MD34	P16	TA0
Y17	BWE#	W5	HA18	E1	HD52	R17	MD35	U16	TA1
J5	CACHE#	V5	HA19	E4	HD53	P18	MD36	U17	TA2
W15	CADS#	U5	HA20	E2	HD54	M20	MD37	V17	TA3
V15	CADV#	V9	HA21	D1	HD55	L19	MD38	T14	TA4
J17	CAS0# / DQM0#	U10	HA22	E3	HD56	K18	MD39	V18	TA5
K17	CAS1# / DQM1#	U9	HA23	D3	HD57	F19	MD40	W18	TA6
H17	CAS2# / DQM2#	W10	HA24	D2	HD58	E18	MD41	Y18	TA7
L17	CAS3# / DQM3#	W9	HA25	C1	HD59	C20	MD42	W19	TA8
H16	CAS4# / DQM4#	V10	HA26	C2	HD60	A20	MD43	Y19	TA9
J16	CAS5# / DQM5#	Y9	HA27	C3	HD61	D17	MD44	V16	TAGWE#
G16	CAS6# / DQM6#	Y10	HA28	B1	HD62	C16	MD45	E8	TRDY#
L16	CAS7# / DQM7#	U11	HA29	A1	HD63	D15	MD46	F5	VDD3
B11	CBE0#	W11	HA30	T8	HITM#	C14	MD47	F6	VDD3
B8	CBE1#	W8	HA31	G5	HLOCK#	V20	MD48	F14	VDD3
A8	CBE2#	K16	HCLK	E7	IRDY#	T18	MD49	F15	VDD3
A5	CBE3#	Y1	HD0	K5	KEN#/INV	R19	MD50	P15	VDD3
W16	CE1#	Y3	HD1	E5	LOCK#	P20	MD51	R6	VDD3
U15	COE#	Y2	HD2	H5	M/IO#	N19	MD52	R7	VDD3
G17	CS0# / RAS0#	Y4	HD3	V12	MA0	M18	MD53	R15	VDD3
F17	CS1# / RAS1#	W1	HD4	T12	MA1	K20	MD54	R16	VDD3
F16	CS2# / RAS2#	W2	HD5	Y13	MA2	J19	MD55	E14	VDD5
E16	CS3# / RAS3#	V1	HD6	W13	MA3	E20	MD56	G6	VDD5
M17	CS4# / RAS4#	R1	HD7	V13	MA4	D19	MD57	T9	W/R#

Table 1. VT82C595 Pin Descriptions

Signal Name	Pin No.	I/O	Signal Description
Clock / Reset Control			
HCLK	K16	I	Host Clock. This pin receives a buffered host clock. This clock is used by all of the VT82C595 logic that is in the Host clock domain. This should be the same clock net that is delivered to the CPU.
PCLK	E10	I	PCI Clock. This pin receives a buffered divided-by-2 host clock. This clock is used by all of the VT82C595 logic that is in the PCI clock domain.
RESET#	T15	I	Reset. When asserted, this signal resets the VT82C595 and sets all register bits to the default value.

CPU Interface			
ADS#	T5	B	Address Strobe. The CPU asserts ADS# in T1 of the CPU bus cycle.
M/IO#	H5	B	Memory / IO Command Indicator
W/R#	T9	B	Write / Read Command Indicator
D/C#	T7	B	Data / Control Command Indicator
BE[7:0]#	M1, L4, L3, L2, L1, K4, K3, K2	B	Byte Enables. The CPU byte enables indicate which byte lane the current CPU cycle is accessing.
HA[31:3]	W8, W11, U11, Y10, Y9, V10, W9, W10, U9, U10, V9, U5, V5, W5, Y5, U6, W6, V6, Y6, U7, W7, Y7, V7, V8, Y8, Y12, U8, Y11, V11	B	Host Address Bus. HA[31:3] connect to the address bus of the host CPU. During CPU cycles HA[31:3] are inputs. These signals are driven by the VT82C595 during cache snooping operations.
BRDY#	M5	B	Bus Ready. The VT82C595 asserts BRDY# to indicate to the CPU that data is available on reads or has been received on writes.
EADS#	R5	O	External Address Strobe. Asserted by the VT82C595 to inquire the L1 cache when serving PCI master accesses to main memory.
KEN# / INV	K5	O	Cache Enable / Invalidate. KEN# / INV functions as both the KEN# signal during CPU read cycles and the INV signal during L1 cache snoop cycles.
HITM#	T8	I	Hit Modified. Asserted by the CPU to indicate that the address presented with the last assertion of EADS# is modified in the L1 cache and needs to be written back.
HLOCK#	G5	I	Host Lock. All CPU cycles sampled with the assertion of HLOCK# and ADS# until the negation of HLOCK# must be atomic.
CACHE#	J5	I	Cacheable Indicator. Asserted by the CPU during a read cycle to indicate the CPU can perform a burst line fill. Asserted by the CPU during a write cycle to indicate that the CPU will perform a burst write-back cycle.
AHOLD	L5	O	Address Hold. The VT82C586B asserts AHOLD when a PCI master is accessing main memory. AHOLD is held for the duration of the PCI burst transfer.
NA#	N5	O	Next Address Indicator.
BOFF#	P5	O	Back Off. Asserted by the VT82C595 when required to terminate a CPU cycle that was in progress.
SMIACK#	T10	I	System Management Interrupt Active. This is asserted by the CPU when it is in system management mode as a result of SMI.

HD[63:0]	A1, B1, C3, C2, C1, D2, D3, E3, D1, E2, E4, E1, F3, F4, G3, F1, F2, H3, G1, H4, G4, J3, G2, H2, H1, J4, J1, J2, M4, K1, M2, M3, N4, N2, N3, P4, N1, P2, P3, R4, P1, T2, R2, T4, R3, U2, T3, U4, V2, U3, V4, T1, W4, V3, W3, U1, R1, V1, W2, W1, Y4, Y2, Y3, Y1	B	Host CPU Data. These signals are connected to the CPU data bus.
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Cache Control			
CADS#	W15	O	Cache Address Strobe. Its assertion causes the burst SRAM load the BSRAM address register from BSRAM address pin.
CADV#	V15	O	Cache Advance. Its assertion causes the burst SRAM to advance to the next Qword in the cache line.
TA[9:0]	Y19, W19, Y18, W18, V18, T14, V17, U17, U16, P16	B	Tag Address. These are inputs during CPU accesses and outputs during L2 cache line fills and L2 line invalidates during inquire cycles.
GWE#	Y16	O	Global Write Enable
BWE#	Y17	O	Byte Write Enable
COE#	U15	O	Cache SRAM Output Enable
TAGWE#	V16	O	Tag Write Enable. When asserted, new state and tag addresses are written into the external tag.
CE1#	W16	O	Chip Enable 1. Chip select 1 for BSRAM.

DRAM Interface			
MD[63:0]	C15, A16, B17, A18, B19, B20, D19, E20, J19, K20, M18, N19, P20, R19, T18, V20, C14, D15, C16, D17, A20, C20, E18, F19, K18, L19, M20, P18, R17, T20, U19, V19, B14, D16, A17, C17, A19, D18, E17, E19, J20, L18, M19, N20, P17, R18, U20, U18, C13, B15, B16, B18, C18, C19, D20, F18, K19, L20, N18, P19, R20, T19, T17, W20	B	Memory Data. These signals are connected to the DRAM data bus.
MPD[7:0]	G18, H20, G20, H18, F20, J18, G19, H19	B	DRAM ECC Data
MA[13:0]	N16, F7, V14, Y14, Y15, U14, W14, T13, U13, V13, W13, Y13, T12, V12	O	Memory Address. DRAM address lines.
RAS#[5:0] / CS#[5:0]	N17, M17, E16, F16, F17, G17	O	Multifunction Pins 1. FPG/EDO DRAM: Row Address Strobe of each bank. 2. Synchronous DRAM: Chip select of each bank.
CAS#[7:0] / DQM#[7:0]	L16, G16, J16, H16, L17, H17, K17, J17	O	Multifunction Pins 1. FPG/EDO DRAM: Column Address Strobe of each byte lane. 2. Synchronous DRAM: Data mask of each byte lane.
SRASA-C#	Y20, W17, H6	O	Row Address Command Indicator. For Synchronous DRAM, three identical copies for better drive.
SCASA-C#	W12, U12, P6	O	Column Address Command Indicator. For Synchronous DRAM, three identical copies for better drive.
SWEA-B#, SWEC#/MWE#	M16, G15, T11	O	Write Enable Command Indicator. For Synchronous DRAM, three identical copies for better drive. SWEC# is a multifunction pin, used as MWE# in DRAM SIMM module applications.

PCI Bus Interface			
FRAME#	E6	B	Frame. Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
AD[31:0]	A2, B2, A3, B3, A4, B4, C4, D6, B5, C5, A6, B6, C6, A7, B7, C7, C8, A9, B9, C9, A10, B10, C10, A11, C11, A12, B12, C12, A13, B13, A14, A15	B	Address/Data Bus. The standard PCI address and data lines. The address is driven with FRAME# assertion and data is driven or received in following cycles.
CBE[3:0]#	A5, A8, B8, B11	B	Command/Byte Enable. The command is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
IRDY#	E7	B	Initiator Ready. Asserted when the initiator is ready for data transfer.
TRDY#	E8	B	Target Ready. Asserted when the target is ready for data transfer.
STOP#	E11	B	Stop. Asserted by the target to request the master to stop the current transaction.
DEVSEL#	E9	B	Device Select. This signal is driven by the VT82C595 when a PCI initiator is attempting to access main memory. It is an input when the VT82C595 is acting as a PCI initiator.
PAR	E12	B	Parity. A single parity bit is provided over AD[31:0] and C/BE[3:0].
SERR#	E13	B	System Error. VT82C595 will pulse this signal when it detect a system error condition.
LOCK#	E5	B	Lock. Used to establish, maintain, and release resource lock.
PREQ#	D4	I	PCI Request. This signal comes from the VT82C586A. PREQ# is the VT82C586A request for the PCI bus.
PGNT#	D5	O	PCI Grant. This signal driven by the VT82C595 to grant PCI access to the VT82C586A.
REQ[3:0]#	D13, D11, D9, D7	I	Request. PCI master requests for PCI.
GNT[3:0]#	D14, D12, D10, D8	O	Grant. Permission is given to the master to use PCI.

Power and Ground			
VDD5	E14, G6	I	Power for internal logic (5V).
VDD3	F5, F6, F14, F15, P15, R6, R7, R15, R16	I	Power for CPU interface (3.3V).
GND	E15, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12, T6, T16	I	Ground

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers of the VT82C595. These tables also document the power-on default value (“Default”) and access type (“Acc”) for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), “—” for reserved / used (essentially the same as RO), and RWC (or just WC) (Read / Write 1’s to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions for details).

Detailed register descriptions are provided in the following section of this document. All offset and default values are shown in hexadecimal unless otherwise indicated

Table 2. VT82C595 Registers

Configuration Space VT82C595 Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	0595	RO
5-4	Command	0007	RW
7-6	Status	02A0	WC
8	Revision ID	nn	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	06	RO
C	-reserved- (cache line size)	00	—
D	Latency Timer	00	RW
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
10-27	-reserved- (base address registers)	00	—
28-2F	-reserved- (unassigned)	00	—
30-33	-reserved- (expan ROM base addr)	00	—
34-3B	-reserved- (unassigned)	00	—
3C	-reserved- (interrupt line)	00	—
3D	-reserved- (interrupt pin)	00	—
3E	-reserved- (min gnt)	00	—
3F	-reserved- (max lat)	00	—

Configuration Space VT82C595-Specific Registers

Offset	Cache Control	Default	Acc
50	Cache Control 1	00	RW
51	Cache Control 2	00	RW
52	Non-Cacheable Control	02	RW
53	System Performance Control	00	RW
54	Non-Cacheable Region #1 High Byte	00	RW
55	Non-Cacheable Region #1 Low Byte	00	RW
56	Non-Cacheable Region #2 High Byte	00	RW
57	Non-Cacheable Region #2 Low Byte	00	RW

Offset	DRAM Control	Default	Acc
58	DRAM Configuration 1	40	RW
59	DRAM Configuration 2	05	RW
5A-5F	DRAM Row Ending Address:		
5A	Bank 0 Ending (HA[29:22])	01	RW
5B	Bank 1 Ending (HA[29:22])	01	RW
5C	Bank 2 Ending (HA[29:22])	01	RW
5D	Bank 3 Ending (HA[29:22])	01	RW
5E	Bank 4 Ending (HA[29:22])	01	RW
5F	Bank 5 Ending (HA[29:22])	01	RW
60	DRAM Type	00	RW
61	Shadow RAM Control C0000-CFFFF	00	RW
62	Shadow RAM Control D0000-DFFFF	00	RW
63	Shadow RAM Control E0000-FFFFFF	00	RW
64	DRAM Reference Timing	AB	RW
65	DRAM Timing Control 1	00	RW
66	DRAM Timing Control 2	00	RW
67	32-Bit DRAM Width	00	RW
68	-reserved- (do not program)	00	RW
69	-reserved- (do not program)	00	RW
6A	DRAM Refresh Counter	00	RW
6B	DRAM Refresh Control	00	RW
6C	SDRAM Control	00	RW
6D	DRAM Control Drive Strength	00	RW
6E	ECC Control	00	RW
6F	ECC Status	00	RO

Offset	PCI Bus Control	Default	Acc
70	PCI Buffer Control	00	RW
71	CPU to PCI Flow Control 1	00	RW
72	CPU to PCI Flow Control 2	00	WC
73	PCI Master Control 1	00	RW
74	PCI Master Control 2	00	RW
75	PCI Arbitration 1	00	RW
76	PCI Arbitration 2	00	RW
77	-reserved- (chip test - do not program)	00	RW
78-FF	-reserved-	00	—

Configuration Space I/O

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

Port CFB-CF8 - Configuration AddressRW

31 Configuration Space Enable

- 0 Disableddefault
- 1 Convert configuration data port writes to configuration cycles on the PCI bus

30-24 Reserved always reads 0

23-16 PCI Bus Number

Used to choose a specific PCI bus in the system

15-11 Device Number

Used to choose a specific device in the system

10-8 Function Number

Used to choose a specific function if the selected device supports multiple functions

7-2 Register Number

Used to select a specific DWORD in the device's configuration space

1-0 Fixed always reads 0

Port CFF-CFC - Configuration DataRW

Refer to PCI Bus Specification Version 2.1 for further details on operation of the above configuration registers.

Register Descriptions

PCI Configuration Space Header

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC.

Offset 1-0 - Vendor IDRO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Offset 3-2 - Device IDRO

15-0 ID Code (reads 0595h to identify the VT82C595)

Offset 5-4 - CommandRW

- 15-10 Reserved** always reads 0
- 9 Fast Back-to-Back Cycle Enable** RW
 - 0 Fast back-to-back transactions only allowed to the same agentdefault
 - 1 Fast back-to-back transactions allowed to different agents
- 8 SERR# Enable** RW
 - 0 SERR# driver disableddefault
 - 1 SERR# driver enabled
 (SERR# is used to report parity errors if bit-6 is set).
- 7 Address / Data Stepping** RO
 - 0 Device never does steppingdefault
 - 1 Device always does stepping
- 6 Parity Error Response** RW
 - 0 Ignore parity errors & continuedefault
 - 1 Take normal action on detected parity errors
- 5 VGA Palette Snoop** RO
 - 0 Treat palette accesses normallydefault
 - 1 Don't respond to palette accesses on PCI bus
- 4 Memory Write and Invalidate Command** RO
 - 0 Bus masters must use Mem Writedefault
 - 1 Bus masters may generate Mem Write & Inval
- 3 Special Cycle Monitoring** RO
 - 0 Does not monitor special cyclesdefault
 - 1 Monitors special cycles
- 2 Bus Master** RO
 - 0 Never behaves as a bus master
 - 1 Can behave as a bus masterdefault
- 1 Memory Space** RO
 - 0 Does not respond to memory space
 - 1 Responds to memory spacedefault
- 0 I/O Space** RO
 - 0 Does not respond to I/O space
 - 1 Responds to I/O spacedefault

Offset 7-6 - Status RWC

- 15 Detected Parity Error**
 - 0 No parity error detected default
 - 1 Error detected. May be set even if error response is disabled (command register bit-6)..
.....write one to clear
- 14 Signaled System Error** always reads 0
 - 1 SERR# asserted
- 13 Signaled Master Abort** always reads 0
 - 1 Transaction aborted by the master
- 12 Received Target Abort**
 - 0 No abort received default
 - 1 Transaction aborted by the target.....
..... write 1 to clear
- 11 Signaled Target Abort** always reads 0
 - 0 Target Abort never signaled
- 10-9 DEVSEL# Timing**
 - 00 Fast
 - 01 Medium..... always reads 01
 - 10 Slow
 - 11 Reserved
- 8 Data Parity Error Detected** always reads 0
- 7 Fast Back-to-Back Capable** always reads 1
- 6 Reserved** always reads 0
- 5 66MHz Capable** always reads 1
- 4-0 Reserved** always reads 0

Offset 8 - Revision ID RO

0-7 VT82C595 Chip Revision Code (00=First Silicon)

Offset 9 - Programming Interface RO

This register is defined in different ways for each Base/Sub-Class Code value and is undefined for this type of device.

0-7 Interface Identifier always reads 00

Offset A - Sub Class Code RO

0-7 Sub Class Code reads 00 to indicate Host Bridge

Offset B - Base Class Code RO

0-7 Base Class Code .. reads 06 to indicate Bridge Device

Offset D - Latency Timer RW

Specifies the latency timer value in PCI bus clocks. Bits 0-2 are fixed, resulting in a granularity of 8 clocks.

7-3 Guaranteed Time Slice for CPU default=0

2-0 Reserved always reads 0

Offset E - Header Type RO

0-7 Header Type Code reads 00: single function

Offset F - Built In Self Test (BIST) RO

7 BIST Supported reads 0: no supported functions

6 Start Test write 1 to start but writes ignored

5-4 Reserved always reads 0

3-0 Response Code 0 = test completed successfully

VT82C595-Specific Configuration Registers

Cache Control

Offset 50- Cache Control 1RW

- 7-6 Cache Enable**
 - 00 Cache disabledefault
 - 01 Cache Init - always does L2 fill
 - 10 Cache enable (normal operation)
 - 11 Cache flush - always does L2 write-back/fill
- 5 Linear Burst Enable** default=0
- 4-3 Tag Configuration**
 - 00 8+0 - 8 Tag bits, no alt (dirty) bitdefault
 - 01 7+1 - 7 Tag bits + alternate (dirty) bit
 - 10 10 - 10 Tag bits, no alt (dirty) bit
 - 11 9+1 - 9 Tag bits + alternate (dirty) bit
- 2 Reserved** RW, default=0
- 1-0 SRAM Type**
 - 00 No SRAM.....default
 - 01 Reserved
 - 10 Burst SRAM
 - 11 Pipeline Burst SRAM

Offset 51 - Cache Control 2 RW

- 7-6 Reserved**RW, default=0
- 5 Backoff CPU**

Used when register 52h bit-2 is set for “L2 fill when CACHE# is inactive”. This bit should normally be set to 0 for best performance, but performance differences are typically not significantly noticeable at a system level.

 - 0 Defer ready return until L2 is filled default
 - 1 Backoff CPU until L2 is filled
- 4 Reserved**RW, default=0
- 3 SRAM Banks**
 - 0 1 Bank..... default
 - 1 2 Banks
- 2 Reserved**RW, default=0
- 1-0 Cache Size**
 - 00 256K default
 - 01 512K
 - 10 1M
 - 11 2M

Offset 52 - Non-Cacheable Control.....RW

- 7 C0000-C7FFF Cacheable & Write-Protect ... def=0
- 6 D0000-DFFFF Cacheable & Write-Protect ... def=0
- 5 E0000-EFFFF Cacheable & Write-Protect ... def=0
- 4 F0000-FFFFF Cacheable & Write-Protect.... def=0
- 3 Reserved (no function)..... RW, default=0
- 2 L2 Fill
 - 0 Normal L2 cache fill.....default
 - 1 Force the requested data to be filled into the L2 cache (provided that L2 cache is enabled), even if the CPU does a read cycle with CACHE# de-asserted. Setting this bit significantly improves performance.
- 1 Reserved (no function)..... RW, default=0
- 0 L2 Write Thru/Write-Back
 - 0 Write-Backdefault
 - 1 Write-Thru

Offset 53 - System Performance Control.....RW

- 7 Read Around Write
 - 0 Disabledefault
 - 1 Enable
- 6 Cache Read Pipeline Cycle
 - 0 Disabledefault
 - 1 Enable
- 5 Cache Write Pipeline Cycle
 - 0 Disabledefault
 - 1 Enable
- 4 DRAM Pipeline Cycle
 - 0 Disabledefault
 - 1 Enable
- 3 PCI Master Peer Concurrency
 - 0 Disabledefault
 - 1 Enable
- 2-0 Reserved RW, default=0

Offset 54 - Non-Cacheable Region #1 High Byte RW

- 15-8 Base Address MSBs - A<28:21> default=0
As noted below, the base address must be a multiple of the region size.

Offset 55 - Non-Cacheable Region #1 Low Byte RW

- 7-3 Base Address LSBs - A<20:16> default=0
As noted below, the base address must be a multiple of the region size.
- 2-0 Range (Region Size)
 - 000 Disable default
 - 001 64K
 - 010 128K (Base Address A16 must be 0)
 - 011 256K (Base Address A16-17 must be 0)
 - 100 512K (Base Address A16-18 must be 0)
 - 101 1M (Base Address A16-19 must be 0)
 - 110 2M (Base Address A16-20 must be 0)
 - 111 4M (Base Address A16-21 must be 0)

Offset 56 - Non-Cacheable Region #2 High Byte RW

- 15-8 Base Address MSBs - A<28:21> default=0
As noted below, the base address must be a multiple of the region size.

Offset 57 - Non-Cacheable Region #2 Low Byte RW

- 7-3 Base Address LSBs - A<20:16> default=0
As noted below, the base address must be a multiple of the region size.
- 2-0 Range (Region Size)
 - 000 Disable default
 - 001 64K
 - 010 128K (Base Address A16 must be 0)
 - 011 256K (Base Address A16-17 must be 0)
 - 100 512K (Base Address A16-18 must be 0)
 - 101 1M (Base Address A16-19 must be 0)
 - 110 2M (Base Address A16-20 must be 0)
 - 111 4M (Base Address A16-21 must be 0)

DRAM Control

These registers are normally set at system initialization time and not accessed after that during normal system operation. Some of these registers, however, may need to be programmed using specific sequences during power-up initialization to properly detect the type and size of installed memory (refer to the VIA Technologies 82C590 BIOS porting guide for details).

Table 3. System Memory Map

Space	Start	Size	Address Range	Comment
DOS	0	640K	00000000-0009FFFF	Cacheable
VGA	640K	128K	000A0000-000BFFFF	Used for SMM
BIOS	768K	16K	000C0000-000C3FFF	Shadow Ctrl 1
BIOS	784K	16K	000C4000-000C7FFF	Shadow Ctrl 1
BIOS	800K	16K	000C8000-000CBFFF	Shadow Ctrl 1
BIOS	816K	16K	000CC000-000CFFFF	Shadow Ctrl 1
BIOS	832K	16K	000D0000-000D3FFF	Shadow Ctrl 2
BIOS	848K	16K	000D4000-000D7FFF	Shadow Ctrl 2
BIOS	864K	16K	000D8000-000DBFFF	Shadow Ctrl 2
BIOS	880K	16K	000DC000-000DFFFF	Shadow Ctrl 2
BIOS	896K	64K	000E0000-000EFFFF	Shadow Ctrl 3
BIOS	960K	64K	000F0000-000FFFFF	Shadow Ctrl 3
Sys Bus	1MB D Top	—	00100000-DRAM Top	Can have hole
Init	4G-64K	64K	FFFEFFFF-FFFFFFF	000Fxxxx alias

Offset 58 - DRAM Configuration 1RW

- 7-5 Bank 0/1 MA Map Type (EDO/FPG)**
 - 000 8-bit Column Address
 - 001 9-bit Column Address
 - 010 10-bit Column Addressdefault
 - 011 11-bit Column Address
 - 100 12-bit Column Address
 - 101 Reserved
 - 11x Reserved
- Bank 0/1 MA Map Type (SDRAM)**
 - 0xx 16Mbit SDRAM.....default
 - 1xx 64Mbit SDRAM
- 4 Reserved** RW, default=0
- 3-1 Bank 2/3 MA Map Type (EDO/FPG)**
 - 000 8-bit Column Addressdefault
 - 001 9-bit Column Address
 - 010 10-bit Column Address
 - 011 11-bit Column Address
 - 100 12-bit Column Address
 - 101 Reserved
 - 11x Reserved
- Bank 2/3 MA Map Type (SDRAM)**
 - 0xx 16Mbit SDRAM.....default
 - 1xx 64Mbit SDRAM
- 0 Reserved** RW, default=0

Offset 59 - DRAM Configuration 2..... RW

- 7-5 Bank 4/5 MA Map Type (EDO/FPG)**
 - 000 8-bit Column Address default
 - 001 9-bit Column Address
 - 010 10-bit Column Address
 - 011 11-bit Column Address
 - 100 12-bit Column Address
 - 101 Reserved
 - 11x Reserved
- Bank 4/5 MA Map Type (SDRAM)**
 - 0xx 16Mbit SDRAM default
 - 1xx 64Mbit SDRAM
- 4-3 Reserved**RW, default=0
- 2-0 Last Bank DRAM Populated**
 - 000 Bank 0
 - 001 Bank 1
 - 010 Bank 2
 - 011 Bank 3
 - 100 Bank 4
 - 101 Bank 5..... default
 - 11x Reserved

Offset 5A-5F - DRAM Row Ending Address:

All of the registers in this group default to 01h:

Offset 5A - Bank 0 Ending (HA[29:22]) RW

Offset 5B - Bank 1 Ending (HA[29:22])..... RW

Offset 5C - Bank 2 Ending (HA[29:22]) RW

Offset 5D - Bank 3 Ending (HA[29:22]) RW

Offset 5E - Bank 4 Ending (HA[29:22])..... RW

Offset 5F - Bank 5 Ending (HA[29:22])..... RW

Note : BIOS is required to fill the ending address registers for all banks even if no memory is populated. The endings have to be in incremental order.

Offset 60 - DRAM Type RW

- 7-6 Reserved** always reads 0
- 5-4 DRAM Type for Bank 4/5**
 - 00 Fast Page Mode DRAM (FPG)..... default
 - 01 EDO DRAM (EDO)
 - 10 Reserved
 - 11 Synchronous DRAM (SDRAM)
- 3-2 DRAM Type for Bank 2/3.....default=FPG**
- 1-0 DRAM Type for Bank 0/1.....default=FPG**

Offset 61 - Shadow RAM Control 1.....RW

- 7-6 CC000h-CFFFFh**
 - 00 Read/write disabledefault
 - 01 Write enable
 - 10 Read enable
 - 11 Read/write enable
- 5-4 C8000h-CBFFFh**
 - 00 Read/write disabledefault
 - 01 Write enable
 - 10 Read enable
 - 11 Read/write enable
- 3-2 C4000h-C7FFFh**
 - 00 Read/write disabledefault
 - 01 Write enable
 - 10 Read enable
 - 11 Read/write enable
- 1-0 C0000h-C3FFFh**
 - 00 Read/write disabledefault
 - 01 Write enable
 - 10 Read enable
 - 11 Read/write enable

Offset 62 - Shadow RAM Control 2.....RW

- 7-6 DC000h-DFFFFh**
 - 00 Read/write disabledefault
 - 01 Write enable
 - 10 Read enable
 - 11 Read/write enable
- 5-4 D8000h-DBFFFh**
 - 00 Read/write disabledefault
 - 01 Write enable
 - 10 Read enable
 - 11 Read/write enable
- 3-2 D4000h-D7FFFh**
 - 00 Read/write disabledefault
 - 01 Write enable
 - 10 Read enable
 - 11 Read/write enable
- 1-0 D0000h-D3FFFh**
 - 00 Read/write disabledefault
 - 01 Write enable
 - 10 Read enable
 - 11 Read/write enable

Offset 63 - Shadow RAM Control 3..... RW

- 7-6 E0000h-EFFFFh**
 - 00 Read/write disable default
 - 01 Write enable
 - 10 Read enable
 - 11 Read/write enable
- 5-4 F0000h-FFFFFh**
 - 00 Read/write disable default
 - 01 Write enable
 - 10 Read enable
 - 11 Read/write enable
- 3-2 Memory Hole**
 - 00 None default
 - 01 512K-640K
 - 10 15M-16M (1M)
 - 11 14M-16M (2M)
- 1 SMI Redirect to A0000h-BFFFFh**
 - 0 Disable Redirection default
 - 1 Enable Redirection
- 0 DRAM A0000h-BFFFFh Access**
 - 0 Disable read write to A0000-B0000 default
 - 1 Enable read write to A0000-B0000 in DRAM

Note: A0000-BFFFF is reserved for use by VGA controllers for system access to the VGA frame buffer. Setting this bit directs accesses to Axxxx-Bxxxx to corresponding memory addresses in system DRAM instead of directing those accesses to the PCI bus for VGA frame buffer access.

Offset 64 - DRAM Reference Timing (FPG Only)RW

Defines basic DRAM timing based on FPG (fast page mode) DRAMs. Timing for banks populated with EDO or SDRAM is adjusted according to the settings in Rx65 and Rx66.

- 7-6 RAS Precharge Time**
 - 00 2T
 - 01 3T
 - 10 4Tdefault
 - 11 6T
- 5-4 RAS Pulse Width**
 - 00 3T
 - 01 4T
 - 10 5Tdefault
 - 11 6T
- 3-2 CAS Read Pulse Width**
 - 00 1T
 - 01 2T (FPG), 1T (EDO)
 - 10 3T (FPG), 2T (EDO).....default
 - 11 4T (FPG), 3T (EDO)
- 1 CAS Write Pulse Width**
 - 0 1T
 - 1 2Tdefault
- 0 Column Address to CAS Delay (see also Rx67[7])**
 - 0 1T
 - 1 2Tdefault

Offset 65 - DRAM Timing Control 1 (EDO/SDRAM) ...RW

- 7-6 Page Mode Control**
 - 00 Page closes after access.....default
 - 01 Reserved
 - 10 Page stays open after access
 - 11 Page closes if CPU is idle
- 5 Fast DRAM Decoding Enable**
 - 0 End of Second T2.....default
 - 1 End of First T2 (recommended setting)

This bit determines the latch point for all DRAM-related decoding (bank, page-hit, MA address mux setup, etc). DRAM control signals (RAS#, CAS#, or SDRAM commands) are also activated at this point).
- 4 EDO DRAM Leadoff Cycle Reduction**
 - 0 Normal leadoff cycle (recommended)default
 - 1 Reduce leadoff cycle by 1T
- 3 DRAM Data Latch Delay .(recommended setting=0)**
 - 0 Latch DRAM data 1 cycle before CPU def
 - 1 Latch DRAM Data ½ cycle before the CPU
- 2-1 Reserved** RW, default=0
- 0 Relaxed DRAM Read Cycle Latency**
 - 0 No effect.....default
 - 1 Add 1 cycle delay if write-buffer is not empty

Used to relax the timing when Read-Around-Write (Rx53[7]) and Fast Decoding (Rx65[5]) are both enabled: if the write buffer is not empty, the DRAM decoding time is the end of T2 if this bit is 0 or the end of the second T2 if this bit is 1 (recommended).

Offset 66 - DRAM Timing Control 2 (EDO/SDRAM)... RW

- 7 EDO Test Mode Enable**
 - 0 Normal Mode..... default
 - 1 EDO Test Mode
- 6 Reserved**always reads 0
- 5 Reserved**RW, default=0
- 4 Reserved**always reads 0
- 3 Turbo EDO Mode Enable (recommended setting=0)**
 - 0 -2-2-2 Two-Cycle Burst..... def
 - 1 -1-1-1 One-Cycle Burst (only applicable to turbo EDO DRAMs)
- 2 MD to HD FIFO Control .(recommended setting=0)**
 - 0 -1-1-1 to pop the data from the DRAM-to-CPU FIFO to the CPU default
 - 1 -2-2-2 to pop data from the FIFO to the CPU
- 1 SDRAM RAS-Precharge Reduction**
 - (recommended setting=0)
 - 0 Use Rx64[7-6] for RAS-Precharge time def
 - 1 Reduce the above by 1T for SDRAM access
- 0 SDRAM RAS-to-CAS Delay Reduction**
 - (recommended setting=1)
 - 0 Use Rx64[0] for Column Address to CAS delay for SDRAM) default
 - 1 Column Address to CAS delay is fixed at 1T for SDRAM

Offset 67 - 32-Bit DRAM Width..... RW

- 7 RAS to Column Address Delay**

This bit determines the number of CPU clocks from RAS assertion to column address assertion.

 - 0 1T (recommended setting) default
 - 1 2T (only set this with heavily loaded DRAM)
- 6 NA# Delay**
 - 0 No NA# delay, 3-1-1-1-2-1-1-1 for L2 cache read hit (recommended setting) default
 - 1 Delay NA# 1T, 3-1-1-1-3-1-1-1

This bit only applies when 2 banks of PBSRAM is installed.
- 5 Bank 5 Width.** 1=32-bit, 0= 64 bit default=64
- 4 Bank 4 Width.** 1=32-bit, 0= 64 bit default=64
- 3 Bank 3 Width.** 1=32-bit, 0= 64 bit default=64
- 2 Bank 2 Width.** 1=32-bit, 0= 64 bit default=64
- 1 Bank 1 Width.** 1=32-bit, 0 =64 bit default=64
- 0 Bank 0 Width.** 1=32-bit, 0= 64 bit default=64

Offset 68 - Reserved (Do Not Program)RW

7-0 **Reserved** (do not program)..... RW, default = 0

Offset 69 - Reserved (Do Not Program)RW

7-0 **Reserved** (do not program)..... RW, default = 0

Offset 6A - Refresh CounterRW

7-0 **Refresh Counter** (in units of 16 CPUCLKs) def=0
note: When set to 00, DRAM refresh is disabled

Offset 6B - Refresh ControlRW

- 7 **CBR (CAS-before-RAS) Refresh**
 - 0 Disable CBR Refreshdefault
 - 1 Enable CBR Refresh
- 6 **Burst Refresh (Burst 4 Times)**
 - 0 Disable burst refresh.....default
 - 1 Enable burst refresh
- 5-2 **Reserved** RW, default=0
- 1-0 **Reserved**always read 0

Offset 6C - SDRAM Control..... RW

- 7 **64Mbit SDRAM Interleave**
 - 0 2-bank interleave for 64Mbit SDRAM.. default
 - 1 4-bank interleave for 64Mbit SDRAM

Note: This bit is a don't-care for 16Mbit SDRAM
- 6 **SDRAM Burst Write**
 - 0 Disabled..... default
 - 1 Enabled
- 5 **SDRAM Bank Interleave Enable**
 - 0 Disabled (bit-7 is a don't care) default
 - 1 Enabled

16Mbit is 2-way only
64Mbit is defined by bit-7 of this register
- 4 **Reserved**RW, default=0
- 3 **SDRAM CAS Latency**
 - 0 Cycle latency is 2..... default
 - 1 Cycle latency is 3
- 2-0 **SDRAM Operation Mode Select**
 - 000 Normal SDRAM Mode..... default
 - 001 NOP Command Enable
 - 010 All-Banks-Precharge Command Enable.
CPU-to-DRAM cycles are converted
to All-Banks-Precharge commands.
 - 011 CPU-to-DRAM cycles are converted to
commands and the commands are driven on
MA[11:0]. The BIOS selects an appropriate
host address for each row of memory such that
the right commands are generated on
MA[11:0].
 - 100 CBR Cycle Enable
 - 101 Reserved
 - 11x Reserved

Offset 6D - DRAM Control Drive Strength..... RW

- 7 **Bank Decoding Test**..... default=0
- 6 **MA[0:1] Drive**
 - 0 12mA default
 - 1 24mA
- 5 **Duplicate Copy of MA[0:1]**

	<u>Pin N17</u>	<u>Pin M17</u>	<u>Drive Control</u>
0	RAS5#	RAS4#	bit 0 default
1	MA1	MA0	bit 6
- 4 **Force SMM Mode** default=0
- 3 **SDRAM Command Drive (SRAS#, SCAS#, SWE#)**
 - 0 12mA default
 - 1 24mA
- 2 **MA[2:13] / WE# Drive**
 - 0 12mA default
 - 1 24mA
- 1 **CAS# Drive**
 - 0 8 mA default
 - 1 12 mA
- 0 **RAS# Drive**
 - 0 12mA default
 - 1 24mA

Offset 6E - ECC Control.....RW

- 7 ECC Mode Select** default = 0
This bit must be set to 1 if any of bits 0-2 are set to 1.
- 6 Reserved** RW, default= 0
- 5 Enable SERR# on ECC Multi-Bit Error**
 - 0 Don't assert SERR# for multi-bit errors..... def
 - 1 Assert SERR# for multi-bit errors
- 4 Enable SERR# on ECC Single-Bit Error**
 - 0 Don't assert SERR# for single-bit errors..... def
 - 1 Assert SERR# for single-bit errors
- 3 ECC Cycle Timing for CPU DRAM Reads**
 - 0 Normal CPU DRAM read cycles def
 - 1 Add 1T for CPU DRAM read cycles with ECC

This bit must be set to 1 if any of bits 0-2 are set to 1.
- 2 ECC Enable - Bank 5/4**
 - 0 Disabled def
 - 1 Enabled
- 1 ECC Enable - Bank 3/2**
 - 0 Disabled def
 - 1 Enabled
- 0 ECC Enable - Bank 1/0**
 - 0 Disabled def
 - 1 Enabled

Offset 6F - ECC Status..... RWC

- 7 Multi-bit Error Detected**..... write of '1' resets
- 6-4 Multi-Bit Error DRAM Bank** default=0
Encoded value of the bank with the multi-bit error.
- 3 Single-Bit Error Detected** write of '1' resets
- 2-0 Single-Bit Error DRAM Bank** default=0
Encoded value of the bank with the single-bit error.

PCI Bus Control

These registers are normally programmed once at system initialization time.

Offset 70 - PCI Buffer Control.....RW

- 7 CPU to PCI Post-Write**
 - 0 Disableddefault
 - 1 Enabled
- 6 PCI Master to DRAM Post-Write**
 - 0 Disableddefault
 - 1 Enabled
- 5 PCI Master to DRAM Prefetch**
 - 0 Disableddefault
 - 1 Enabled
- 4 Reserved**RW, default= 0
- 3-2 Reserved** always reads 0
- 1 PCI Retry for CPU QW Access**
 - 0 Disableddefault
 - 1 Enabled
- 0 PCI Master Does Not Flush CPU to PCI Buffer**
 - 0 Master flushes CPU-to-PCI bufferdefault
 - 1 Master does not flush CPU to PCI buffer

Offset 71 - CPU to PCI Flow Control 1.....RW

- 7 Dynamic Burst**
 - 0 Disableddefault
 - 1 Enabled (see note under bit-3 below)
- 6 Byte Merge**
 - 0 Disableddefault
 - 1 Enabled
- 5 Reserved** always reads 0
- 4 PCI I/O Cycle Post Write**
 - 0 Disableddefault
 - 1 Enabled
- 3 PCI Burst**
 - 0 Disableddefault
 - 1 Enabled (bit7=1 will override this option)
- bit-7 bit-3 Operation**
 - 0 0 Every write goes into the write buffer and no PCI burst operations occur.
 - 0 1 If the write transaction is a burst transaction, the information goes into the write buffer and burst transfers are later performed on the PCI bus. If the transaction is not a burst, PCI write occurs immediately (after a write buffer flush).
 - 1 x Every write transaction goes to the write buffer; burstable transactions will then burst on the PCI bus and non-burstable won't. This is the normal setting.
- 2 Enable PCI Fast Back-to-Back Write .. def=0 (disa)**
- 1 Enable Quick Frame Generation... def=0 (disabled)**
- 0 Enable 1 Wait State PCI Cycles def=0 (disabled)**

Offset 72 - CPU to PCI Flow Control 2..... RWC

- 7 Retry Status over 16 / 64 Times**
 - 0 No retry occurred..... default
 - 1 Retry occurred write 1 to clear
- 6 Retry Timeout Action**
 - 0 Retry Forever (record status only) default
 - 1 Flush buffer or return FFFFFFFF for read
- 5-4 Retry Count and Retry Backoff**
 - 00 Retry 2 times, back off CPU default
 - 01 Retry 16 times
 - 10 Retry 4 times, back off CPU
 - 11 Retry 64 times
- 3 Clear Failed Data and Continue Retry**
 - 0 Disabled..... default
 - 1 When data is posting and retry fails, pop the failed data if any, and keep posting
- 2 CPU Backoff on PCI Read Retry Failure**
 - 0 Disabled..... default
 - 1 Backoff CPU when reading data from PCI and retry fails
- 1 Reduce 1T for FRAME# Generation**
 - 0 Disabled..... default
 - 1 Enabled
- 0 Reduce 1T for CPU Read PCI Slave**
 - 0 Disabled..... default
 - 1 Enabled (bypass TRDY# to LRDY#)

Offset 73 - PCI Master Control 1.....RW

- 7 Local Memory Decoding**
 - 0 Fast (address phase)default
 - 1 Slow (first data phase)
- 6 PCI Master 1-Wait-State Write**
 - 0 Zero wait state TRDY# responsedefault
 - 1 One wait state TRDY# response
- 5 PCI Master 1-Wait-State Read**
 - 0 Zero wait state TRDY# responsedefault
 - 1 One wait state TRDY# response
- 4 Reserved** always reads 0
- 3 Assert STOP# after PCI Master Write Timeout**
 - 0 Disableddefault
 - 1 Enabled
- 2 Assert STOP# after PCI Master Read Timeout**
 - 0 Disableddefault
 - 1 Enabled
- 1 LOCK# Function**
 - 0 Disableddefault
 - 1 Enabled
- 0 PCI Master Broken Timer Enable**
 - 0 Disableddefault
 - 1 Enabled. Force into arbitration when there is no FRAME# 16 PCICLK's after the GRANT.

Offset 74 - PCI Master Control 2.....RW

- 7 PCI Enhance Command Support**
 - 0 Disableddefault
 - 1 Enabled
- 6 PCI Master Single Write Merge**
 - 0 Disableddefault
 - 1 Enabled
- 5-0 Reserved** always reads 0

Offset 75 - PCI Arbitration 1..... RW

- 7 Arbitration Mechanism**
 - 0 PCI has priority..... default
 - 1 Fair arbitration between PCI and CPU
- 6 Arbitration Mode**
 - 0 REQ-based (arbitrate at end of REQ#).. default
 - 1 Frame-based (arbitrate at end of each FRAME#)
- 5-4 Reserved**RW, default=0
- 3-0 PCI Master Bus Time-Out**
(force into arbitration after a period of time)
 - 0000 Disable..... default
 - 0001 1x32 PCICLKs
 - 0010 2x32 PCICLKs
 -
 - 1111 15x32 PCICLKs

Offset 76 - PCI Arbitration 2..... RW

- 7 Master Priority Rotation Enable**
 - 0 Disable (arbitration per Rx75 bit-7)..... default
 - 1 Enable (arbitration per bits 5-4 of this register)
(gives the CPU higher priority than either of the mechanisms defined by Rx75 bit-7)
- 6 Reserved**always reads 0
- 5-4 Master Priority Rotation Control**
 - 00 Disabled (arbitration per Rx75 bit-7)..... default
 - 01 Grant to CPU after every PCI master grant
 - 10 Grant to CPU after every 2 PCI master grants
 - 11 Grant to CPU after every 3 PCI master grants

With setting 01, the CPU will always be granted access after the current bus master completes, no matter how many PCI masters are requesting. With setting 10, if other PCI masters are requesting during the current PCI master grant, the highest priority master will get the bus after the current master completes, but the CPU will be guaranteed to get the bus after that master completes. With setting 11, if other PCI masters are requesting, the highest priority will get the bus next, then the next highest priority will get the bus, then the CPU will get the bus. In other words, with the above settings, even if multiple PCI masters are continuously requesting the bus, the CPU is guaranteed to get access after every master grant (01), after every other master grant (10) or after every third master grant (11).
- 3-1 Reserved**always reads 0
- 0 Reserved**RW, default=0

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Ambient operating temperature	0	70	°C
Storage temperature	-55	125	°C
Input voltage	-0.5	5.5	Volts
Output voltage ($V_{DD} = 3.1 - 3.6V$)	-0.5	$V_{DD} + 0.5$	Volts

Note: Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Characteristics

TA=0-70°C, $V_{DD}=5V \pm 5\%$, GND=0V

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input low voltage	-0.50	0.8	V	
V_{IH}	Input high voltage	2.0	$V_{DD}+0.5$	V	
V_{OL}	Output low voltage	-	0.45	V	$I_{OL}=4.0mA$
V_{OH}	Output high voltage	2.4	-	V	$I_{OH}=-1.0mA$
I_{IL}	Input leakage current	-	+/-10	uA	$0 < V_{IN} < V_{DD}$
I_{OZ}	Tristate leakage current	-	+/-20	uA	$0.45 < V_{OUT} < V_{DD}$
I_{CC}	Power supply current	-		mA	

AC Timing Specifications

AC timing specifications provided are based on external zero-pf capacitance load. Min/max cases are based on the following table:

Table 4. AC Timing Min / Max Conditions

	min	max
VDD3	3.6	3.135
VDD5	5.25	4.75
Temperature	0	70

Pad load derating curve specifications are listed from 0pf to 80pf with 5pf resolution; above 80 pf use 20 pf resolution up to 200 pf. The following pads are provided:

Table 5. PAD Load Derating Curve (I/V curve)

External pad name	Voltage	Remark
vpad000	3.3	
vpad 001	3.3	
vpad 002	3.3	
vpad 005	3.3	24mA
vpad 007	3.3	12mA
vpad 009	3.3	12mA
vpad 011	3.3	8mA
vpad 012	3.3	
vpad 013	3.3	
vpad 014	3.3	

Table 6. AC Characteristics - CPU Cycle Timing

	Parameter	Min	Max	Unit	Pad	Notes
T _S	ADS# Setup Time to CCLK Rising		5	ns		
T _S	W/R# Setup Time to CCLK Rising		5.5			
T _S	M/IO# Setup Time to CCLK Rising		6			
T _S	D/C# Setup Time to CCLK Rising		5			
T _S	SMIACK# Setup Time to CCLK Rising		5			
T _S	HITM# Setup Time to CCLK Rising		6			
T _S	HLOCK# Setup Time to CCLK Rising		5			
T _S	CACHE# Setup Time to CCLK Rising		5			
T _S	BE[7:0]# Setup Time to CCLK Rising		5			
T _S	HA[31:3] Setup Time to CCLK Rising		3			
T _S	HD[63:0] Setup Time to CCLK Rising		3			

T _H	ADS# Hold Time from CCLK Rising	1.5				
T _H	W/R#,M/IO#,D/C#,CACHE# Hold Time from CCLK Rising	1				
T _H	HITM#,HLOCK#,SMIACK# Hold Time from CCLK Rising	1				
T _H	HA[31:3], BE[7:0]# Hold Time from CCLK Rising	1				
T _H	HD[63:0] Hold Time from CCLK Rising	2				

T _{VD}	BRDY# Valid Delay From CCLK Rising	1.5	8		vpad000	0 pf
T _{VD}	NA# Valid Delay From CCLK Rising	1.5	8		vpad000	0 pf
T _{VD}	AHOLD Valid Delay From CCLK Rising	1.5	7		vpad000	0 pf
T _{VD}	BOFF# Valid Delay From CCLK Rising	1.5	7		vpad000	0 pf
T _{VD}	EADS# Valid Delay From CCLK Rising	1.5	7		vpad000	0 pf
T _{VD}	KEN#/INV Valid Delay from CCLK Rising	1.5	7		vpad000	0 pf
T _{VD}	HD[63:0] Valid Delay from CCLK Rising	1.5	7.5		vpad002	0 pf
T _{VD}	HA[31:3] Valid Delay from CCLK Rising	2	13		vpad002	0 pf

T _{FD}	HA[31:3] Float Delay from CCLK Rising	4	9			0 pf
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Table 7. AC Characteristics - L2 Cache Timing

	Parameter	Min	Max	Unit	Pad	Notes
T _S	TA[9:0] Setup time to CCLK Rising		6	ns		
T _H	TA[9:0] Hold Time from CCLK Rising	2		ns		

T _{VD}	TA[9:0] Valid Delay from CCLK Rising	2	9	ns	vpad001	0 pf
T _{VD}	TAGWE# Valid Delay from CCLK Rising	1.5	10	ns	vpad000	0 pf
T _{VD}	COE# Valid Delay from CCLK Rising	1.5	10	ns	vpad000	0 pf
T _{VD}	CWE[7:0]#/GWE#/BWE# Valid Delay from CCLK Rising	1.5	9	ns	vpad000	0 pf
T _{VD}	CADS#, CADV#, CE1# Valid Delay from CCLK Rising	1.5	7	ns	vpad000	0 pf

Table 8. AC Characteristics - FP / EDO Interface Timing

	Parameter	Min	Max	Unit	Pad	Notes
T _S	MD[63:0] Setup time to CCLK Rising (no ECC)		2	ns		0 pf
T _H	MD[63:0] Hold Time from CCLK Rising (no ECC)	4		ns		0 pf
T _{VD}	RAS[5:0]# Valid Delay from CCLK Rising	1.5	8		vpad005	0 pf
T _{VD}	CAS[7:0]# Valid Delay from CCLK Rising	1.5	8		vpad007	0 pf
T _{VD}	MA[1:0] Valid Delay from CCLK Rising (burst)	2	10		vpad005	0 pf
T _{VD}	MA[13:2] Valid Delay from CCLK Rising	2	10		vpad005	0 pf
T _{VD}	MD[63:0] Valid Delay from CCLK Rising	2	10		vpad005	0 pf
T _{VD}	MWE# Valid Delay from CCLK Rising	1.5	7		vpad005	0 pf
T _{FD}	MA[13:0] Float Delay from CCLK Rising	4	10		vpad005	0 pf

Table 9. AC Characteristics - SDRAM Interface Timing

	Parameter	Min	Max	Unit	Pad	Notes
T _S	MD[63:0] Setup time to CCLK Rising (no ECC)		2	ns		0 pf
T _H	MD[63:0] Hold Time from CCLK Rising (no ECC)	2.5		ns		0 pf
T _{VD}	RAS[5:0] Valid Delay from CCLK Rising	1.5	8		vpad005	0 pf
T _{VD}	DQM[7:0]# Valid Delay from CCLK Rising	1.5	7		vpad011	0 pf
T _{VD}	SRAS# Valid Delay from CCLK Rising	1.5	7		vpad005	0 pf
T _{VD}	SCAS# Valid Delay from CCLK Rising	1.5	7		vpad005	0 pf
T _{VD}	SWE# Valid Delay from CCLK Rising	1.5	7		vpad005	0 pf
T _{VD}	MA[1:0] Valid Delay from CCLK Rising (burst)	1.5	10		vpad005	0 pf
T _{VD}	MA[13:2] Valid Delay from CCLK Rising	1.5	10		vpad005	Leadoff, 0pf
T _{VD}	MD[63:0] Valid Delay from CCLK Rising	1.5	8		vpad005	0 pf
T _{FD}	MA[13:0] Float Delay from CCLK Rising	4	10		vpad005	0 pf

Table 10. AC Characteristics - PCI Cycle Timing

	Parameter	Min	Max	Unit	Notes
T _S	AD[31:0] Setup Time to PCLK Rising		7	ns	0pf on min, 50pf on max
T _S	FRAME#,TRDY#,IRDY# Setup Time to PCLK Rising		7	ns	0pf on min, 50pf on max
T _S	CBE[3:0]#, STOP#,DEVSEL# Setup Time to PCLK Rising		7	ns	0pf on min, 50pf on max
T _S	PREQ#, REQ[3:0]# Setup Time to PCLK Rising		12	ns	0pf on min, 50pf on max
T _H	AD[31:0] Hold Time from PCLK Rising	0		ns	0pf on min, 50pf on max
T _H	FRAME#,TRDY#,IRDY# Hold Time from PCLK Rising	0		ns	0pf on min, 50pf on max
T _H	CBE[3:0]#, STOP#,DEVSEL# Hold Time from PCLK Rising	0		ns	0pf on min, 50pf on max
T _H	PREQ#, REQ[3:0]# Hold Time from PCLK Rising	0		ns	0pf on min, 50pf on max
T _{VD}	AD[31:0] Valid Delay from PCLK Rising (address phase)	2	11	ns	0pf on min, 50pf on max
T _{VD}	AD[31:0] Valid Delay from PCLK Rising (data phase)	2	11	ns	0pf on min, 50pf on max
T _{VD}	FRAME#,TRDY#,IRDY# Valid Delay from PCLK Rising	2	11	ns	0pf on min, 50pf on max
T _{VD}	CBE[3:0]#, STOP#,DEVSEL# Valid Delay from PCLK Rising	2	11	ns	0pf on min, 50pf on max
T _{VD}	PREQ#, REQ[3:0]# Valid Delay from PCLK Rising	2	12	ns	0pf on min, 50pf on max
T _{FD}	FRAME#,TRDY#,IRDY# Float Delay from PCLK Rising		28	ns	0pf on min, 50pf on max
T _{FD}	CBE[3:0]#, STOP#,DEVSEL# Float Delay from PCLK Rising		28	ns	0pf on min, 50pf on max
T _{LAT}	REQ to GRANT Latency	2		clks	

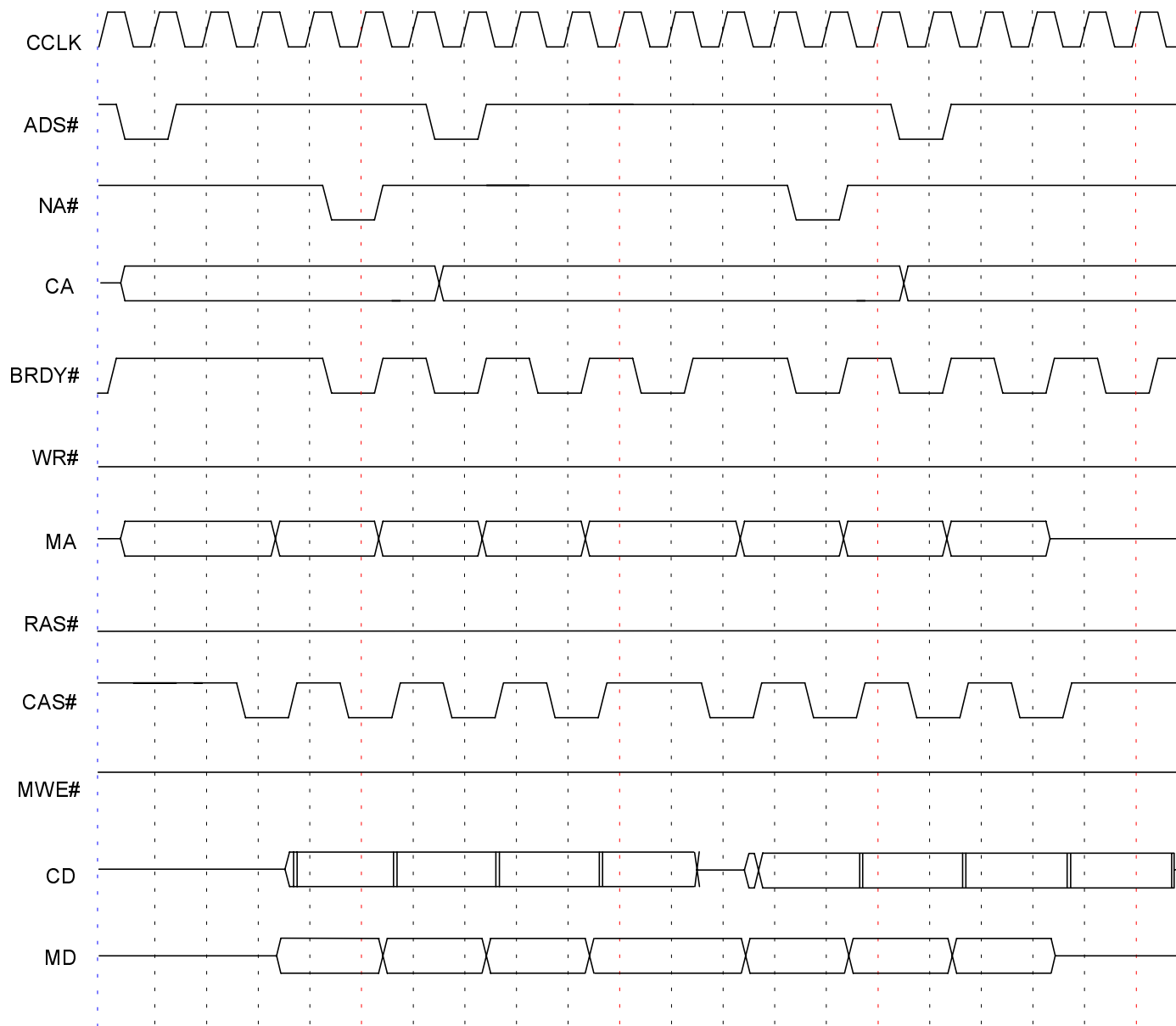


Figure 5. DRAM READ PIPE LINE EDO 5-2-2-2, 3-2-2-2

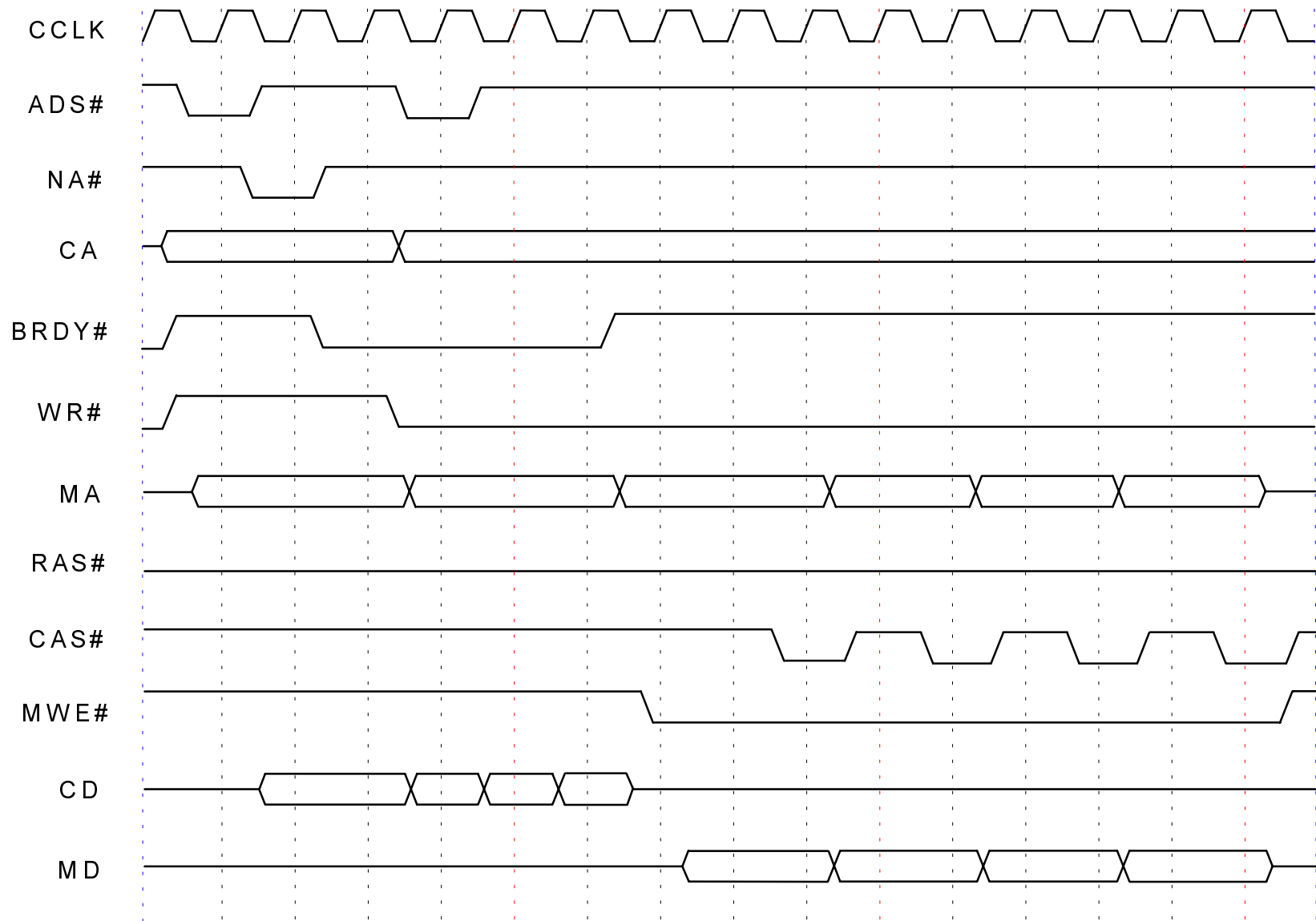


Figure 6. POST WRITE 3111, DRAM EDO 2222

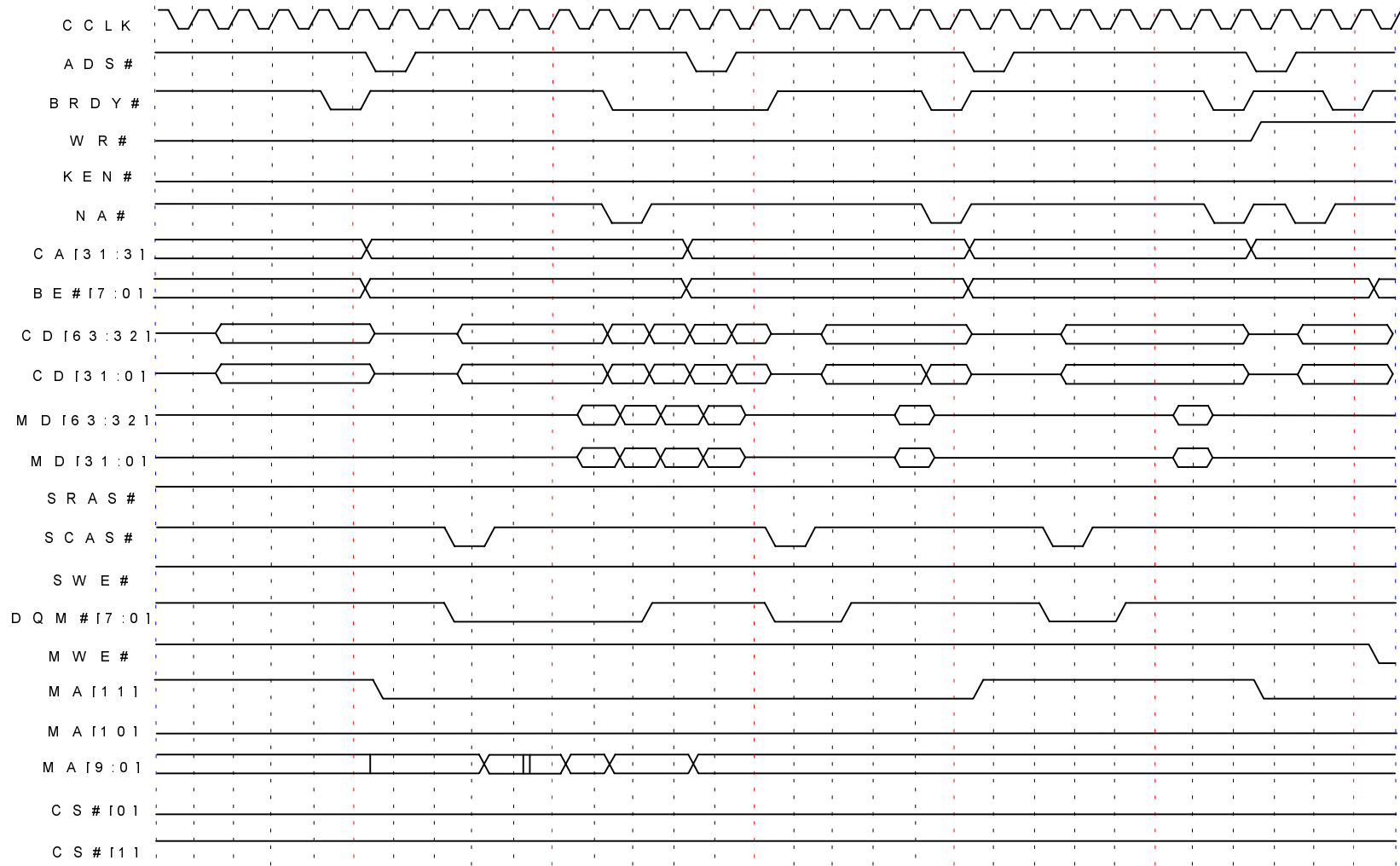


Figure 7. SDRAM READ CYCLE (BANK INTERLEAVE, CAS LATENCY=3)

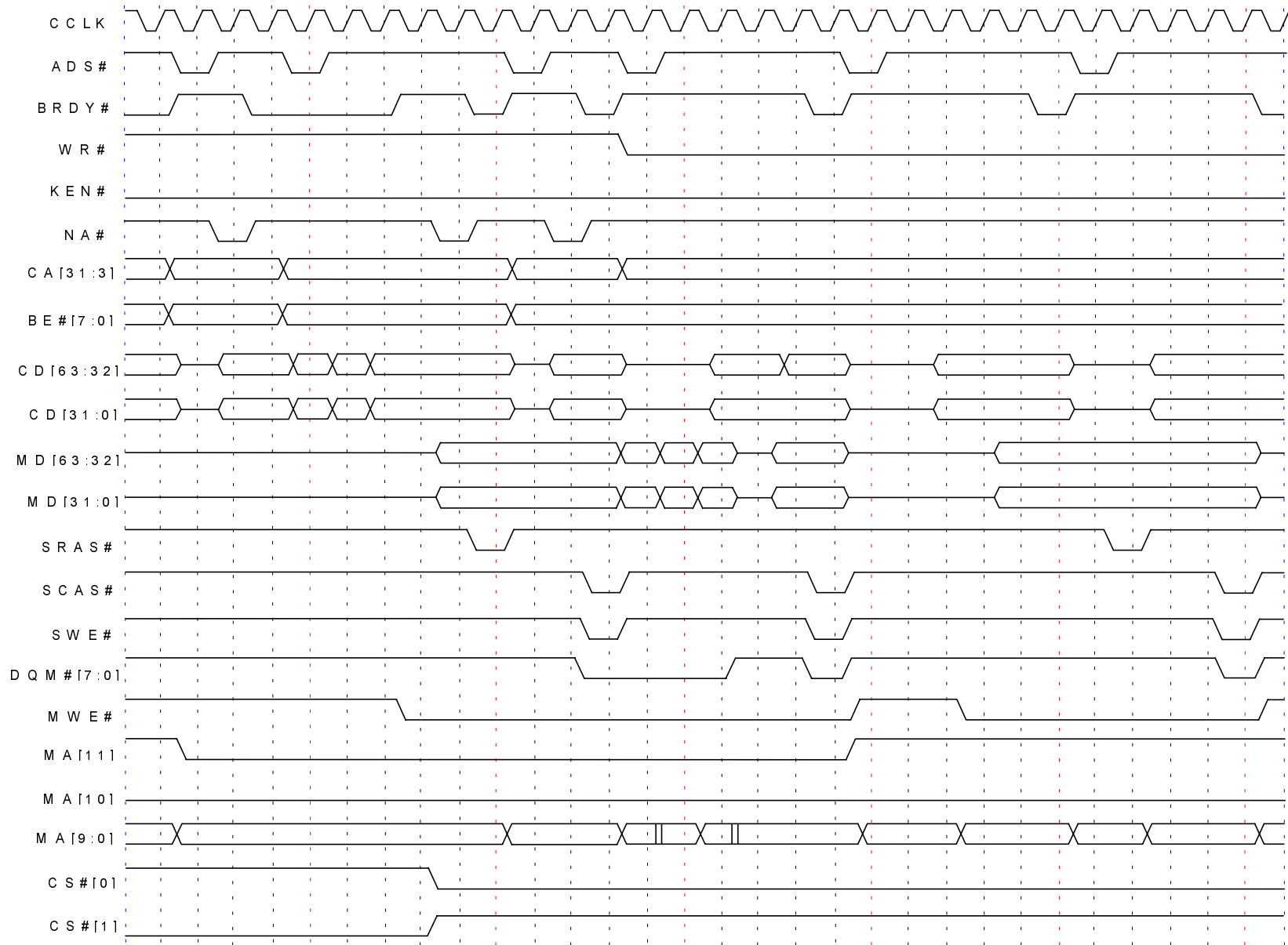


Figure 8. SDRAM WRITE CYCLE (BANK INTERLEAVE)

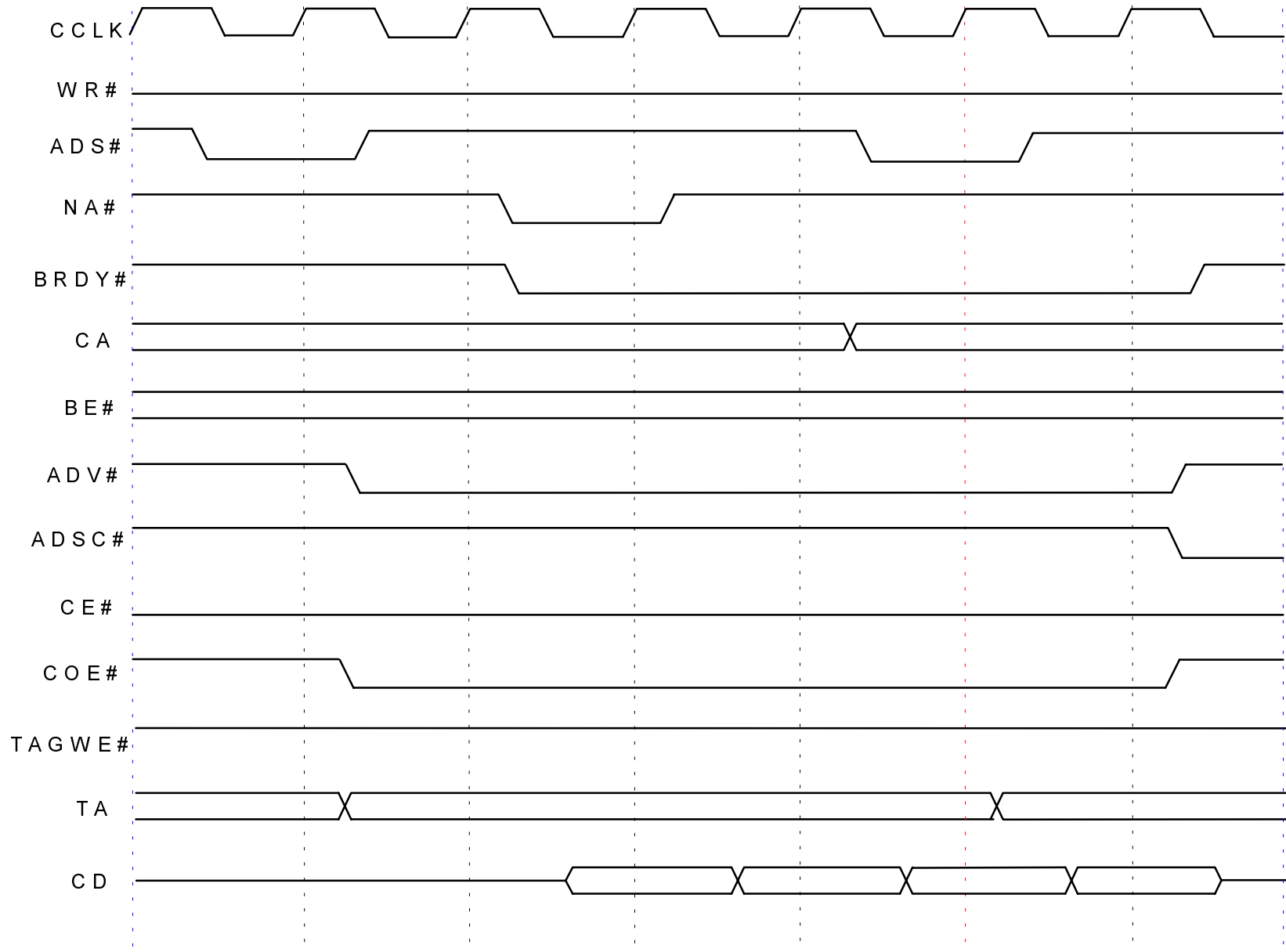


Figure 9. CPU READ HIT SYNCHRONOUS SRAM 3111

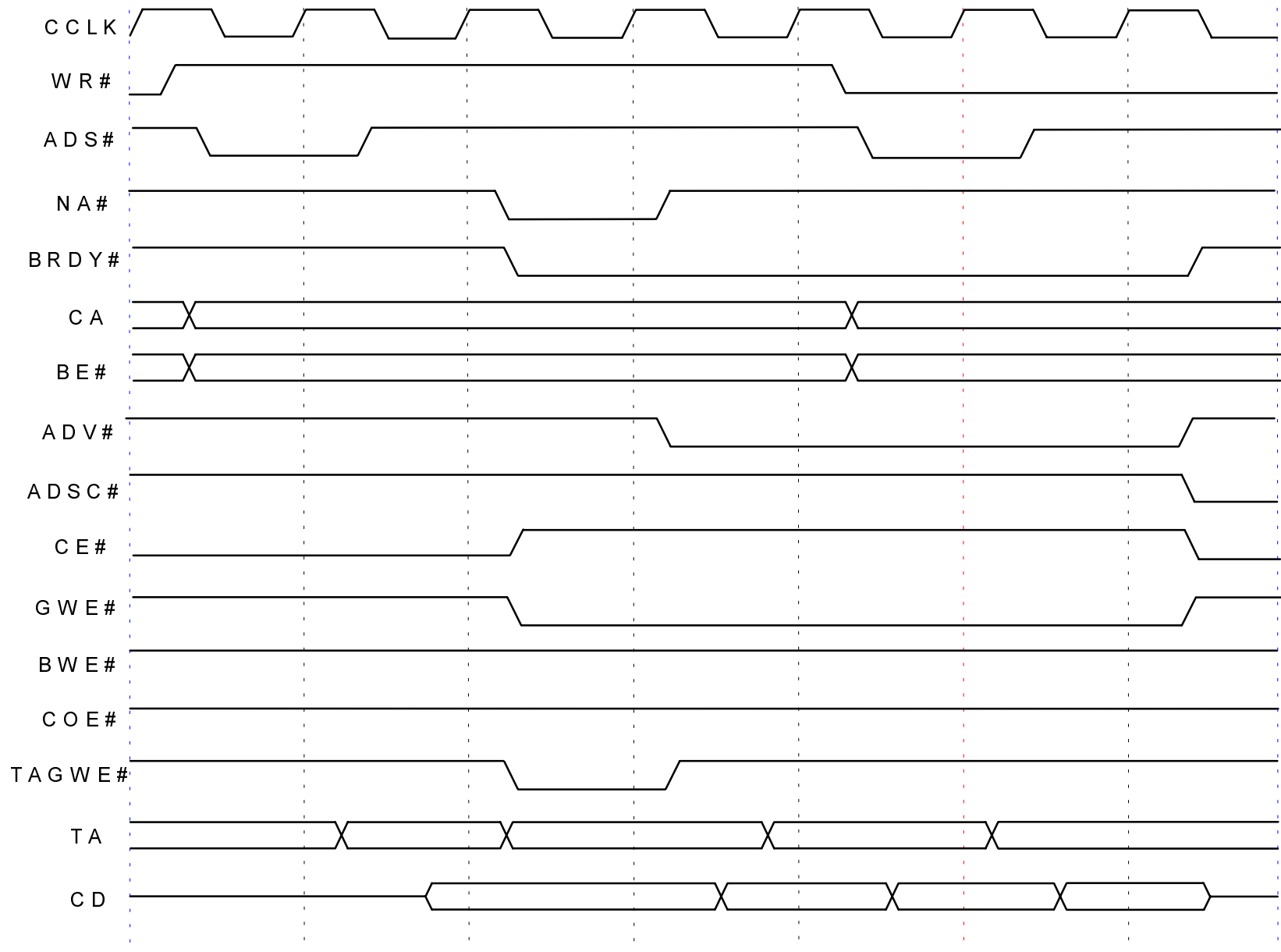


Figure 10. CPU WRITE HIT SYNCHRONOUS SRAM 3111

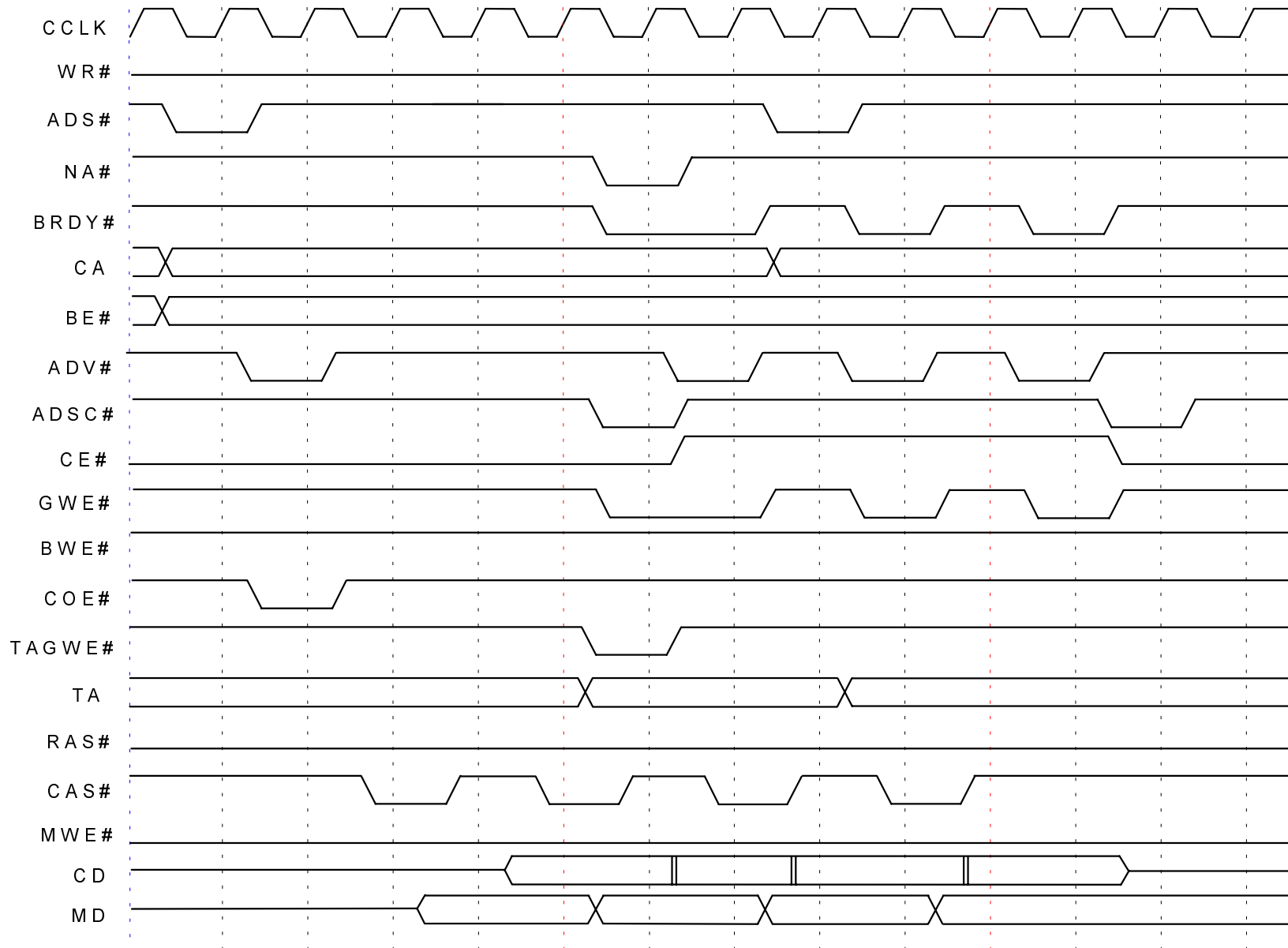


Figure 11. CPU READ MISS FILL SYNCHRONOUS SRAM

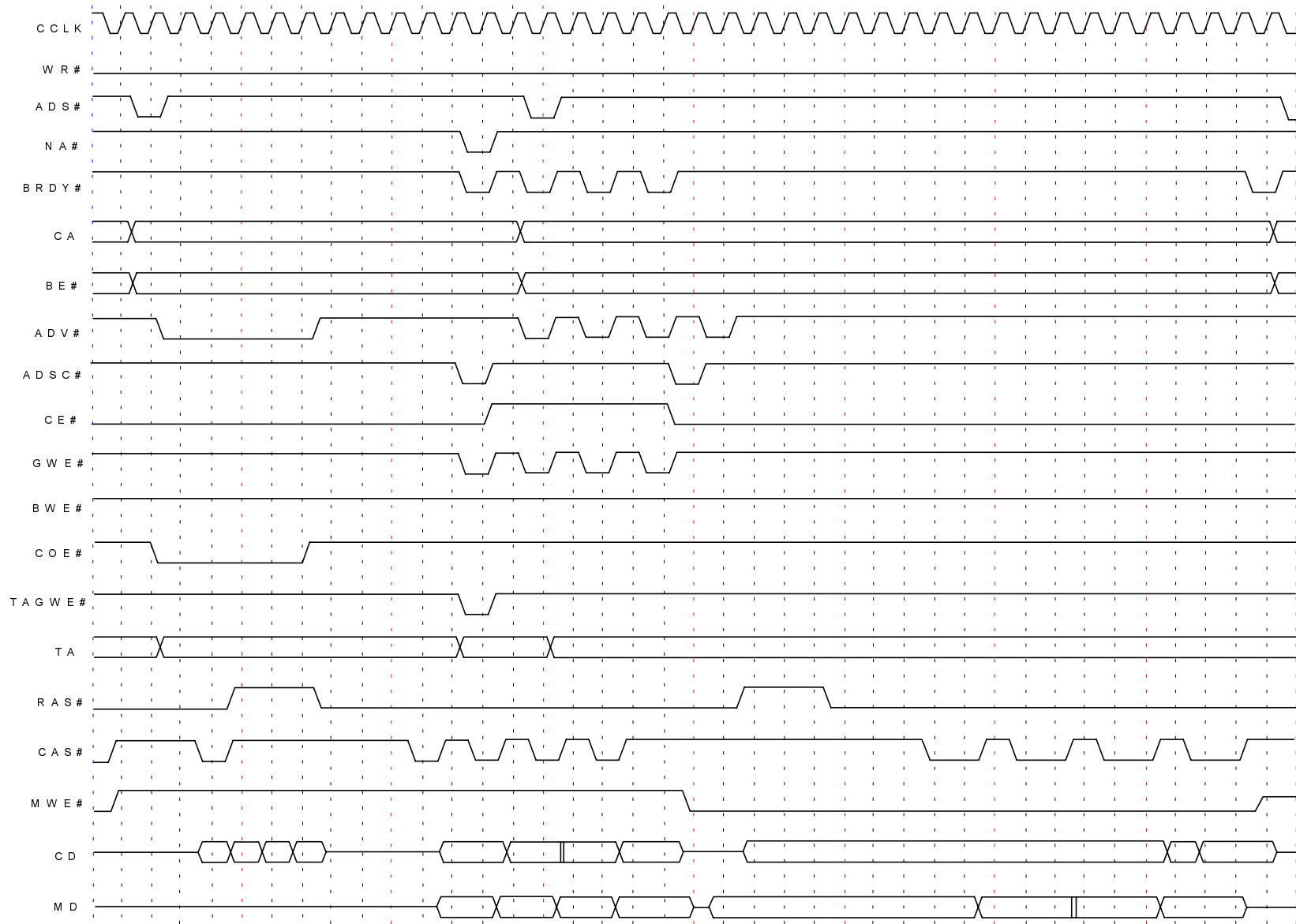


Figure 12. CPU READ MISS DIRTY L2 WRITE BACK FILL

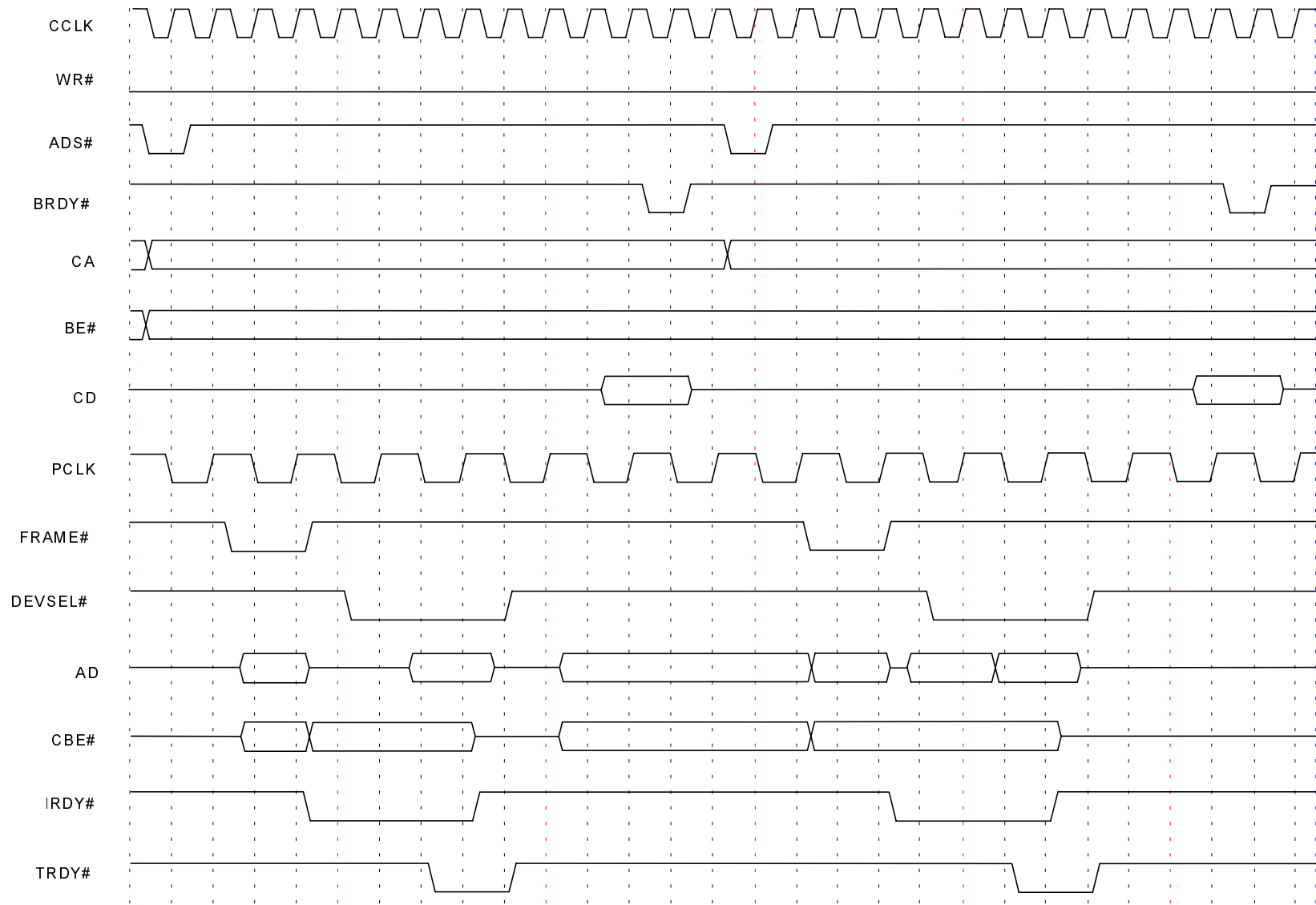


Figure 13. CPU READ PCI SLAVE

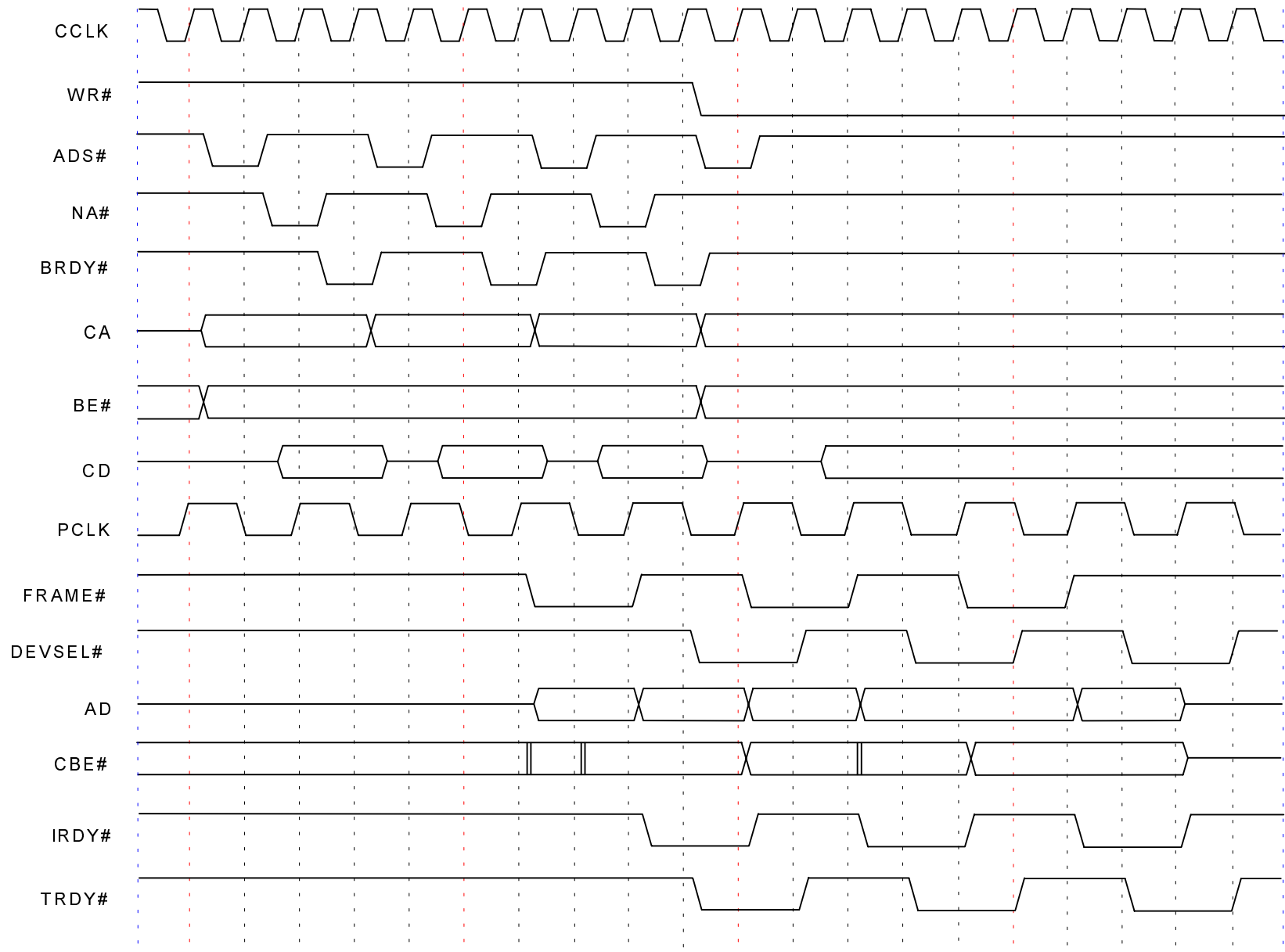


Figure 14. CPU WRITE PCI SLAVE WRITE BUFFER ON FAST BACK TO BACK

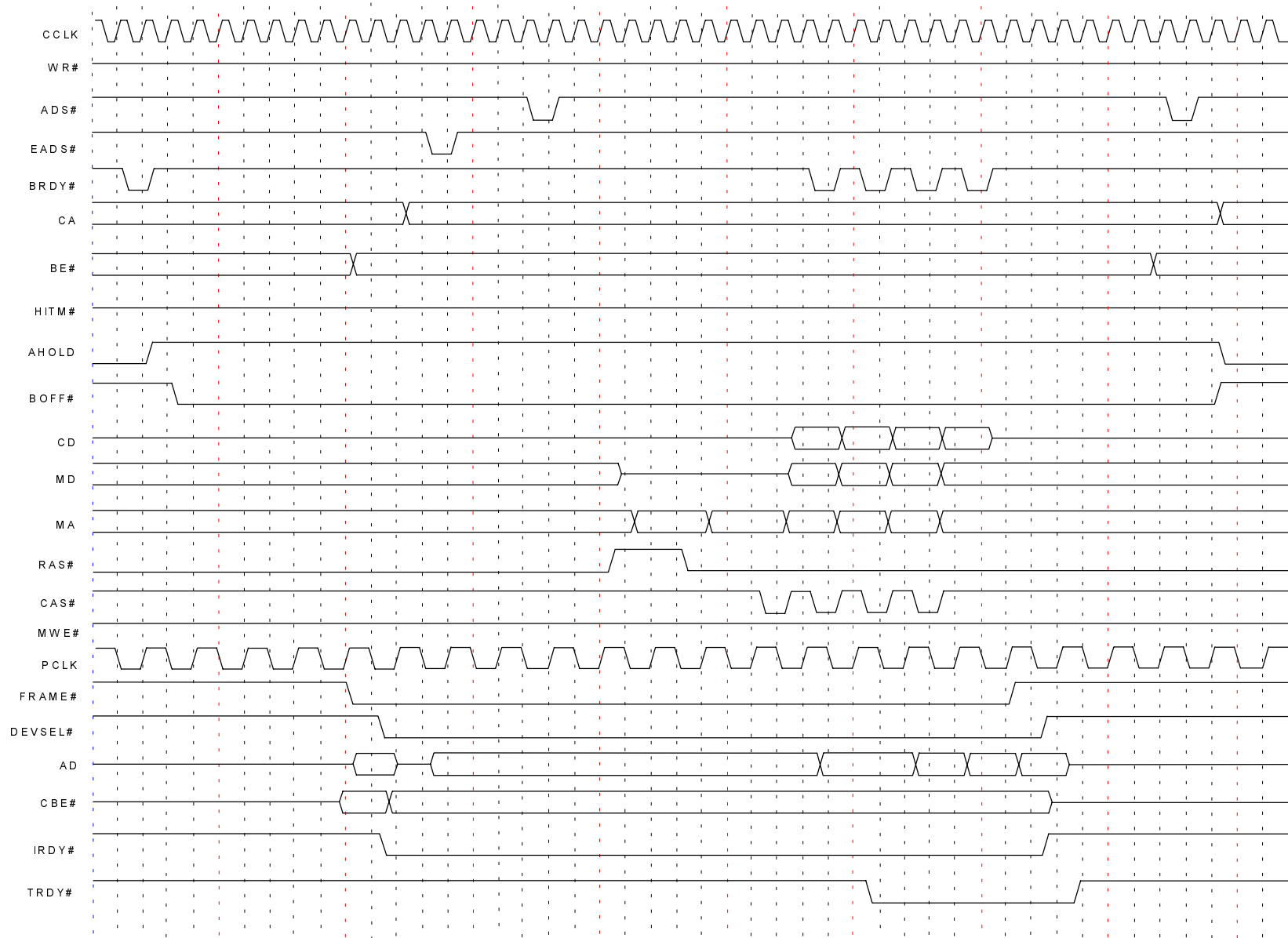


Figure 15. PCI MASTER READ HIT DRAM

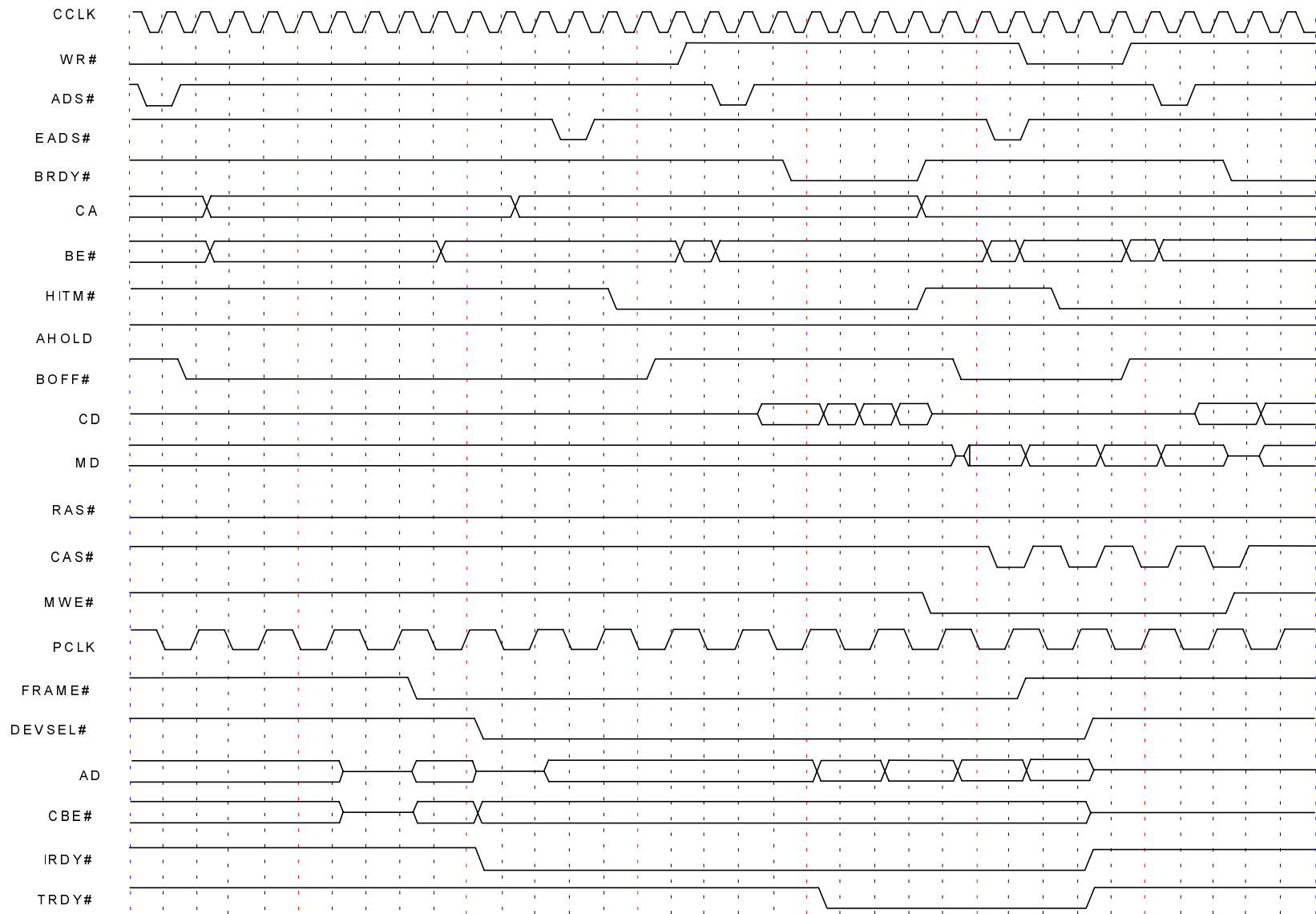


Figure 16. PCI MASTER READ L1 SNOOP TO DRAM

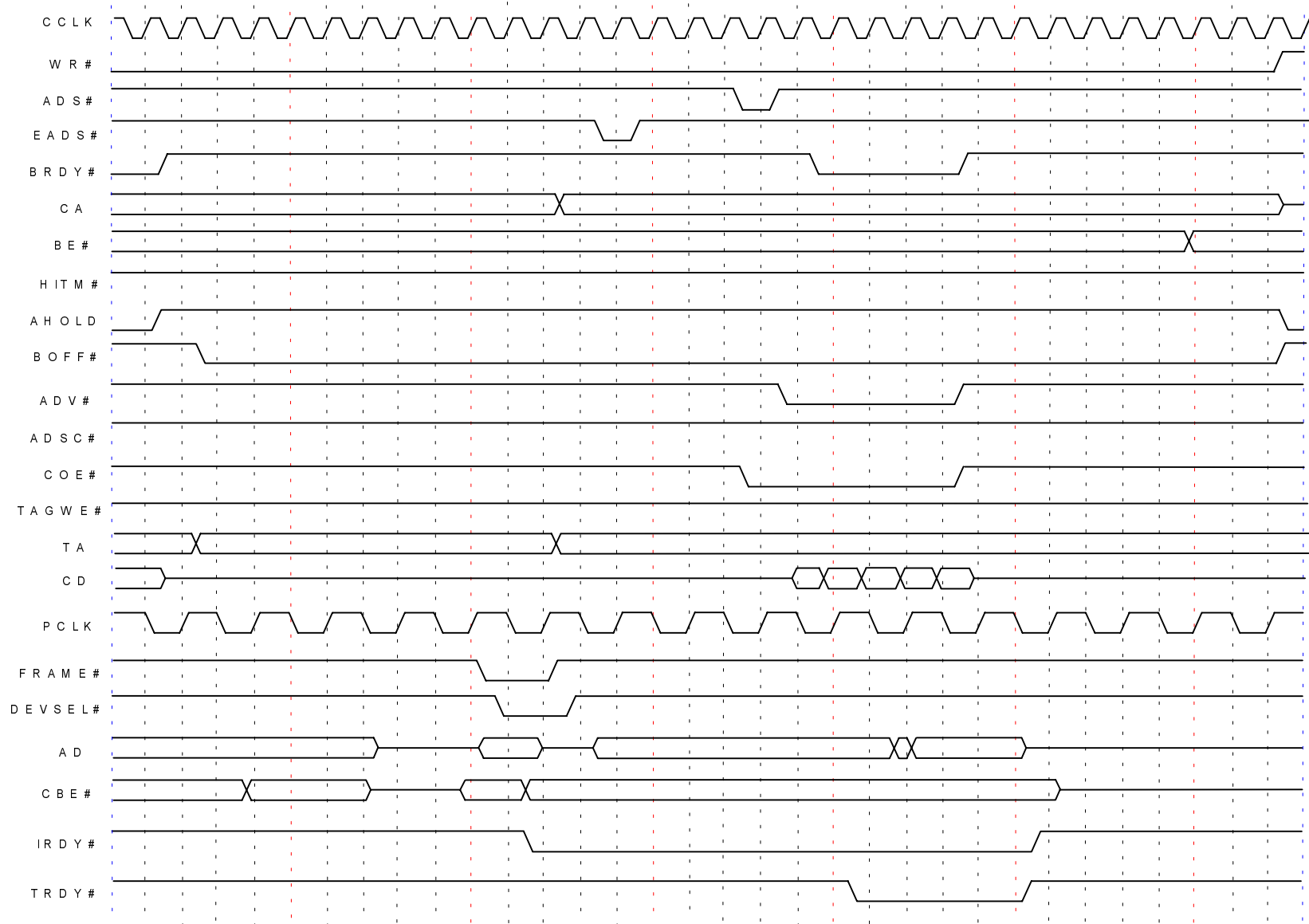


Figure 17. PCI MASTER READ HIT L2

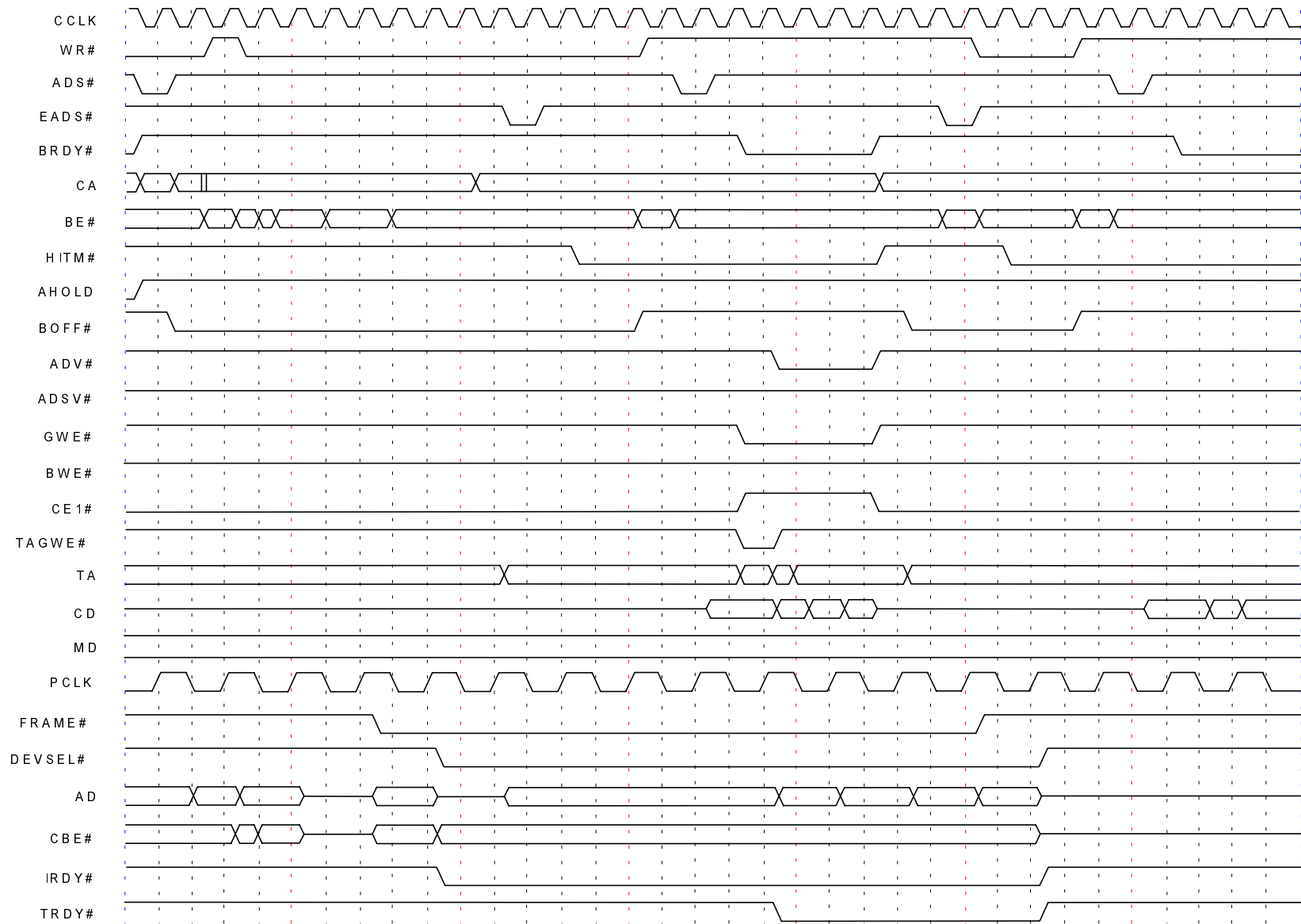


Figure 18. PCI MASTER READ L1 SNOOP TO L2

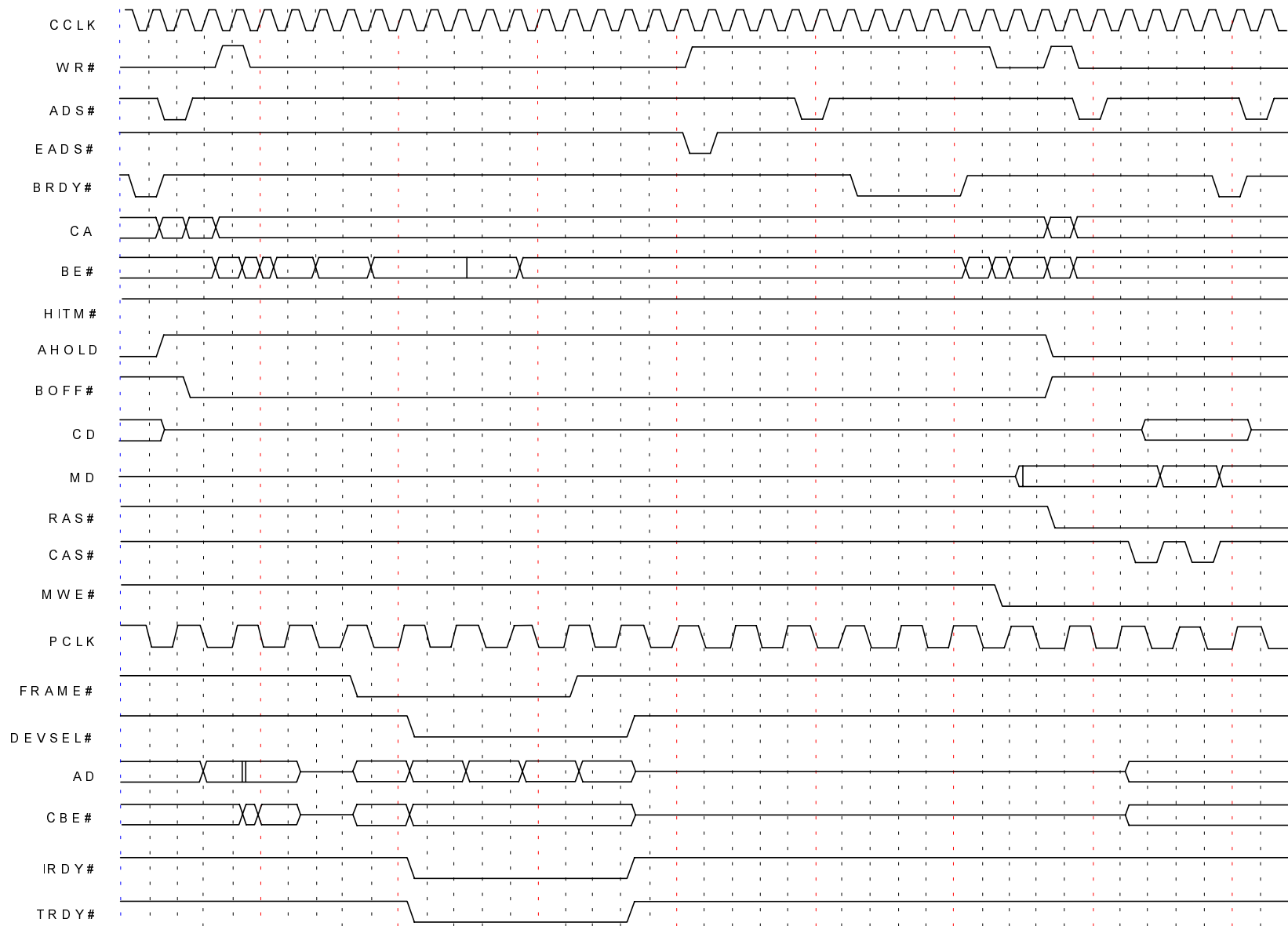


Figure 19. PCI MASTER WRITE DRAM

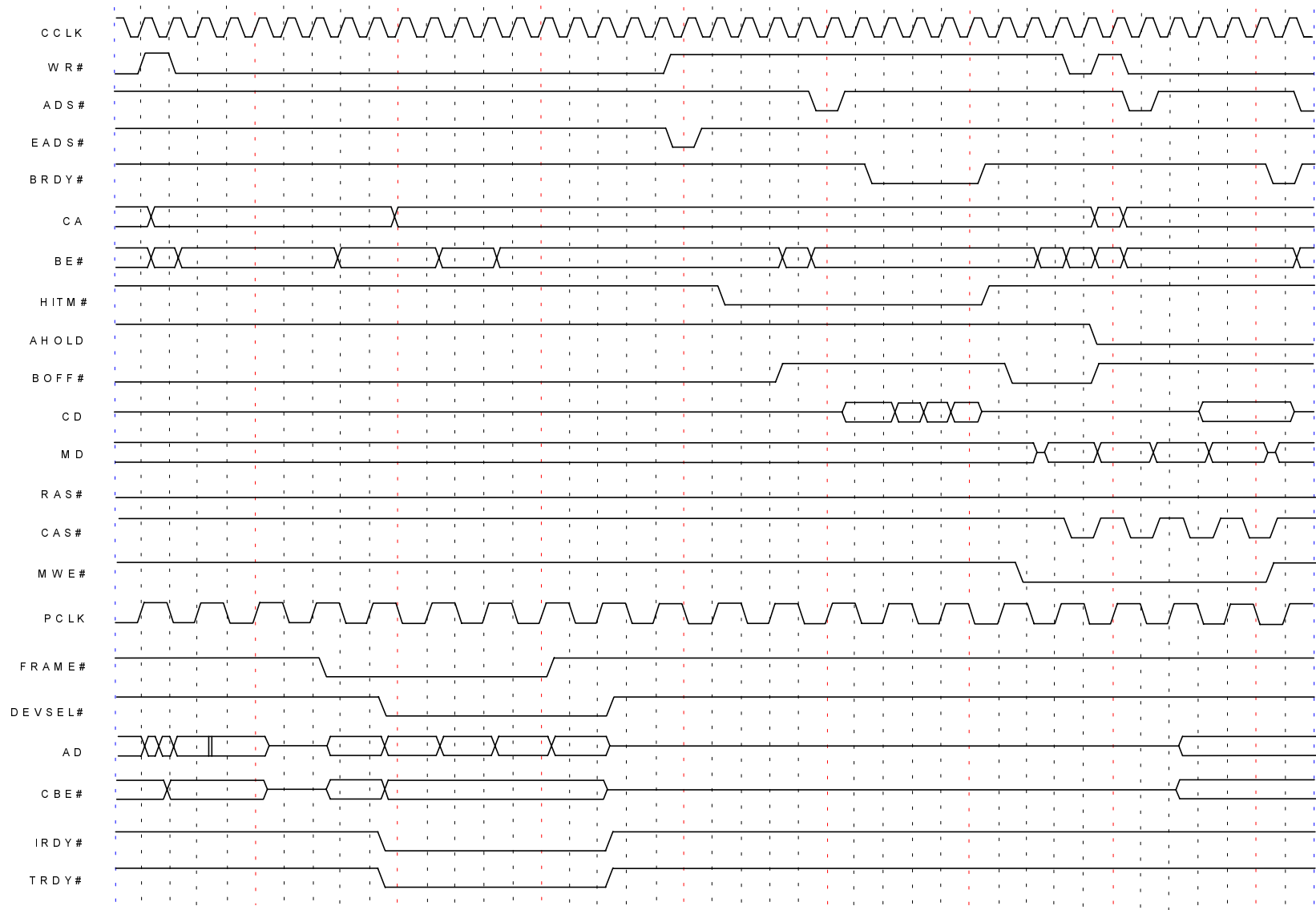


Figure 20. PCI MASTER WRITE HIT L1 SNOOP TO DRAM

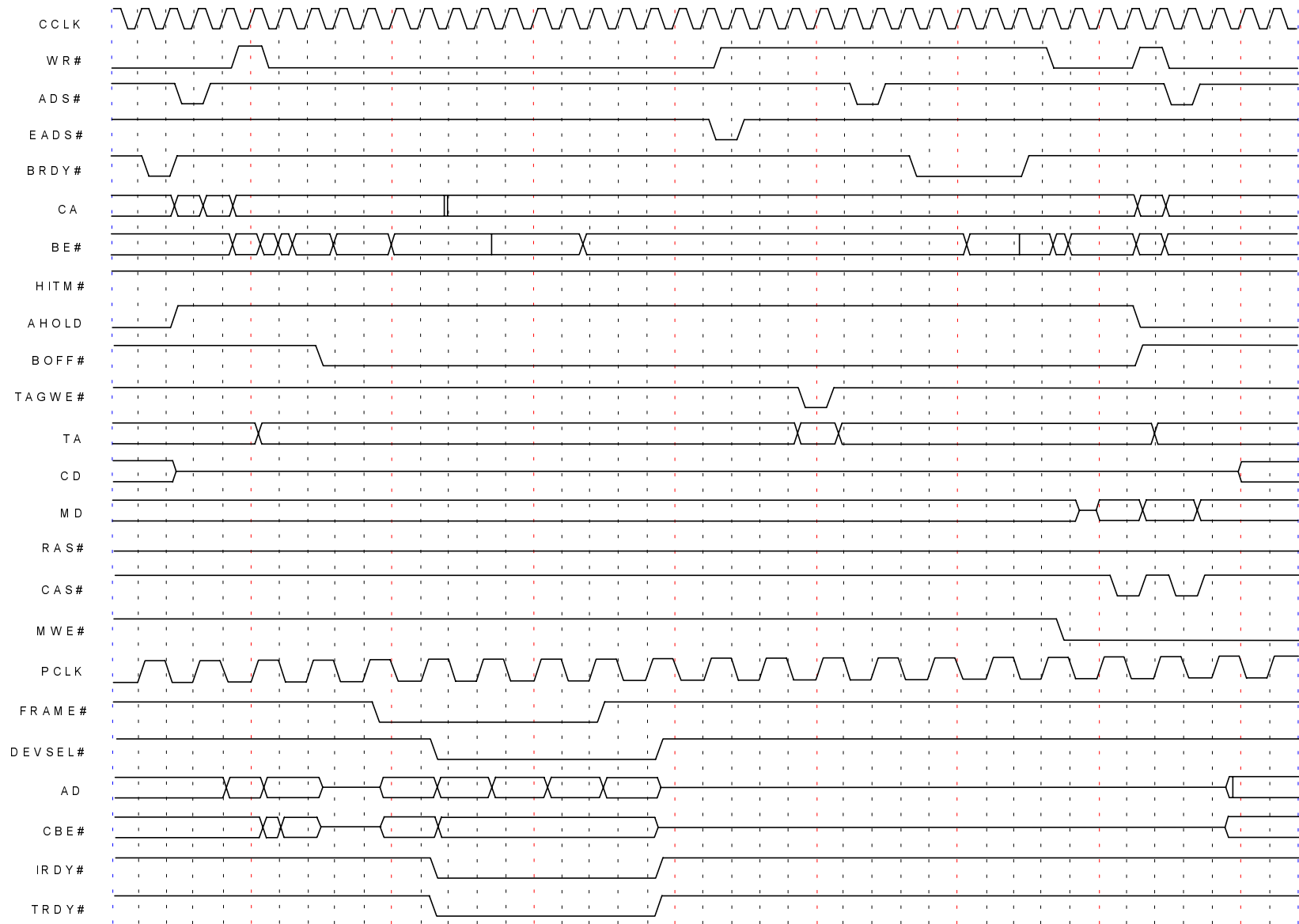


Figure 21. PCI MASTER WRITE HIT L2

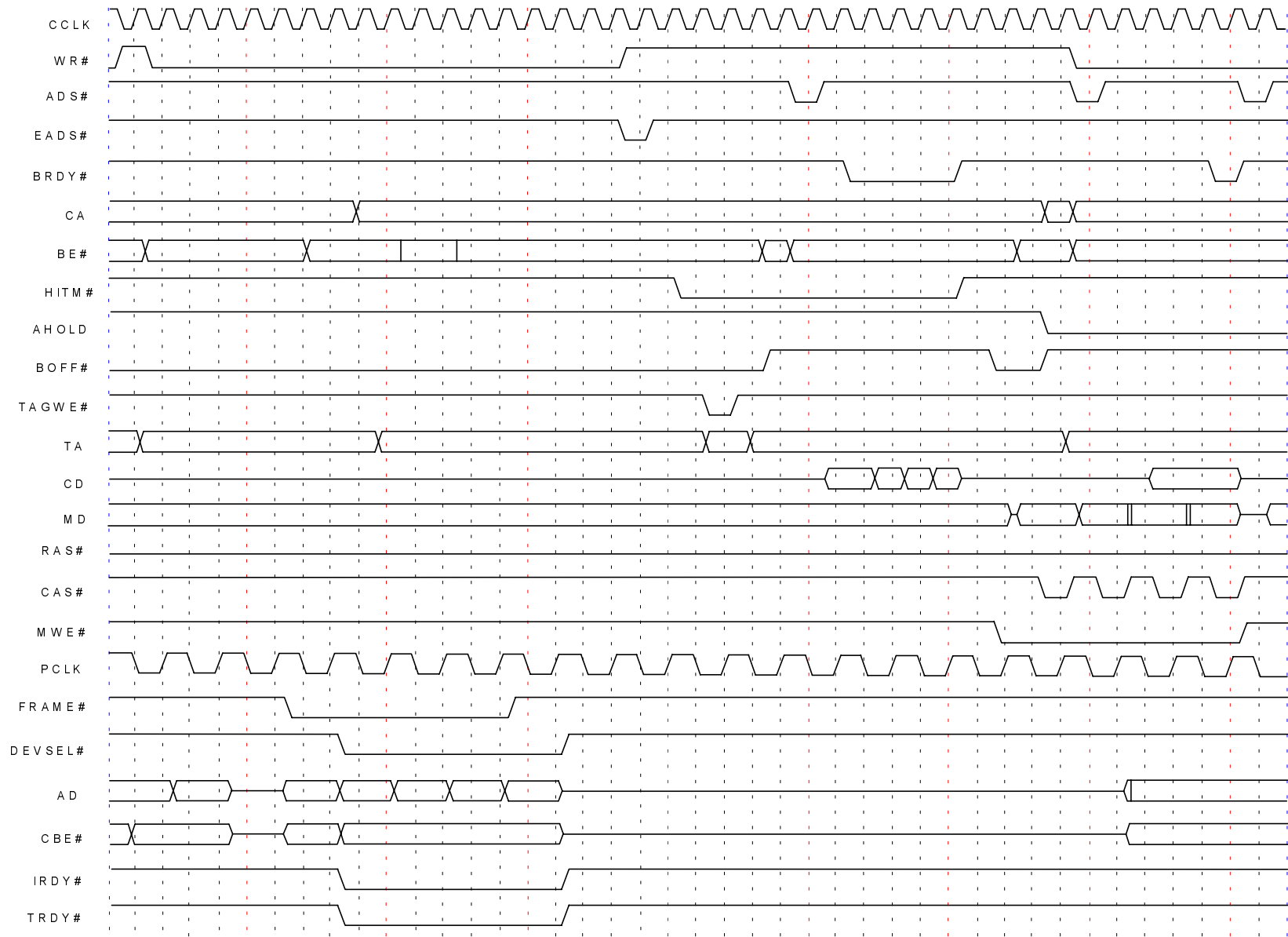


Figure 22. PCI MASTER WRITE HIT L2, L1 HITM

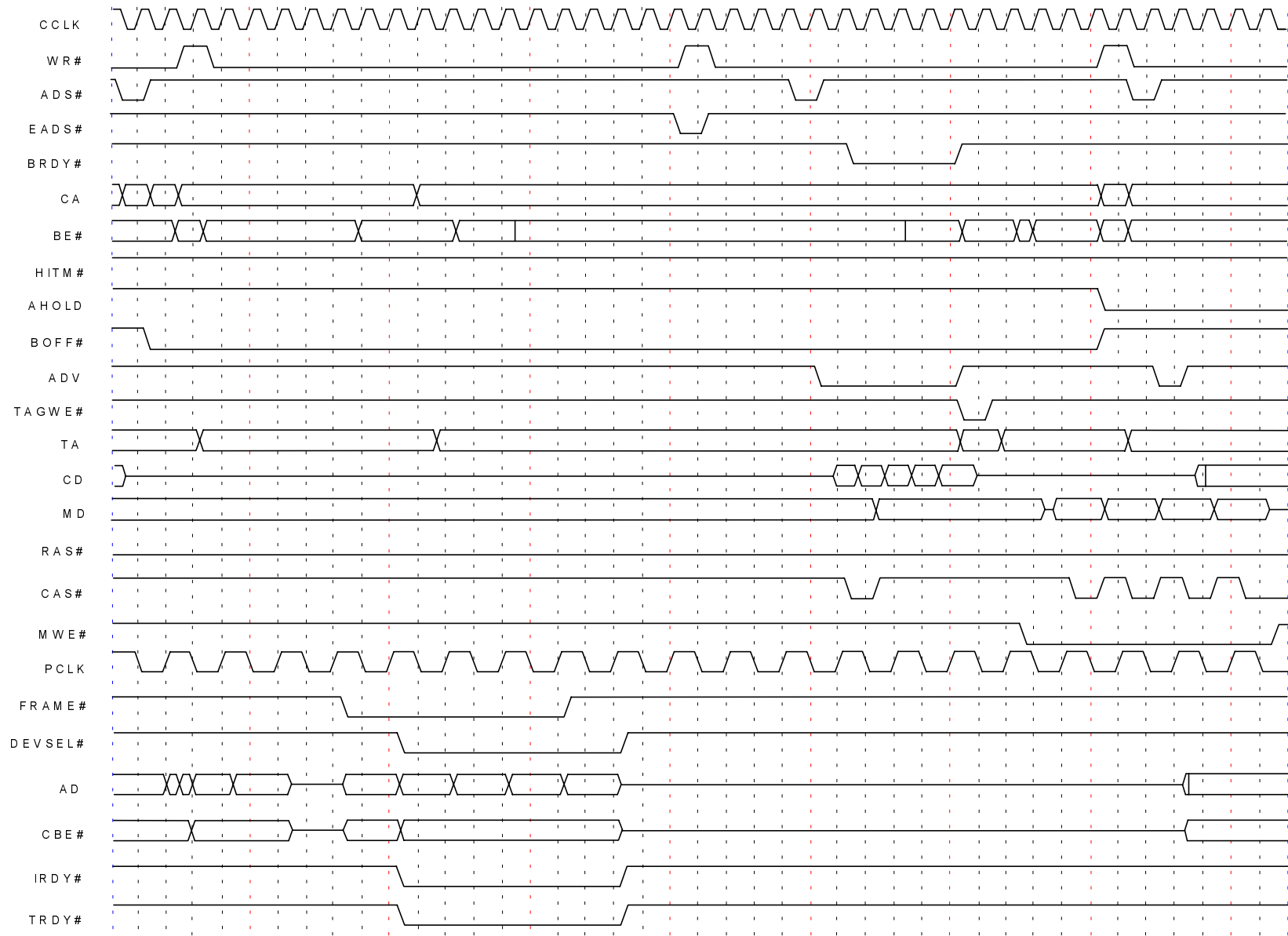


Figure 23. PCI MASTER WRITE HIT L2 & DIRTY

PACKAGE MECHANICAL SPECIFICATIONS

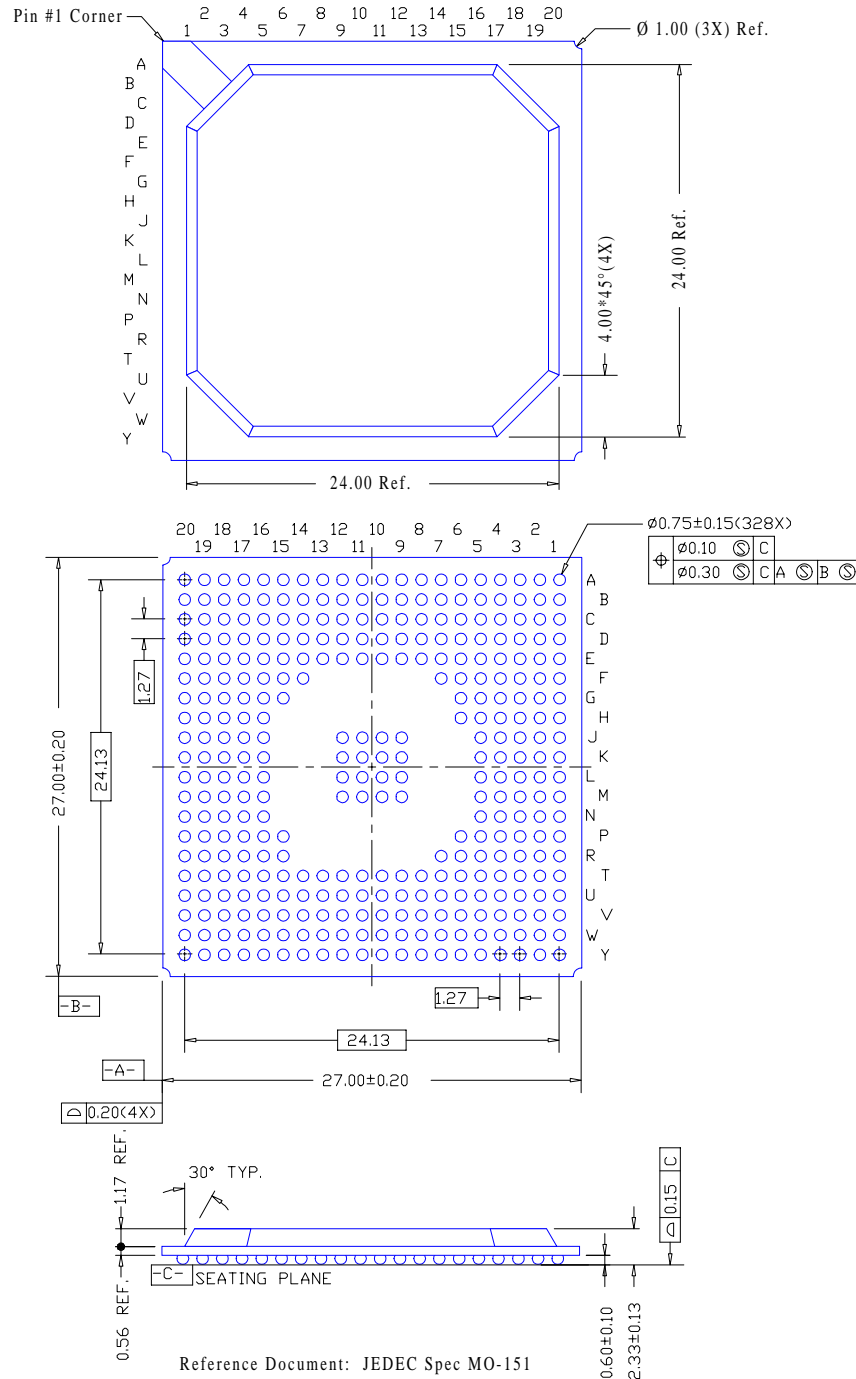


Figure 24. Mechanical Specifications - 328-Pin Ball Grid Array Package