



VT82C691

Apollo Pro

66 / 100 MHz

**Single-Chip Socket-8 / Slot-1 North Bridge
for Desktop and Mobile PC Systems
with AGP and PCI
plus Advanced ECC Memory Controller
supporting SDRAM, EDO, and FPG**

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VIA TECHNOLOGIES, INC.

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REVISION HISTORY

Document Release	Date	Revision	Initials
0.1	11/11/97	Initial internal release based on Apollo MVP3 Data Sheet Revision 0.5 Replaced CPU interface pin descriptions from Apollo P6 Data Sheet	DH
0.2	12/15/97	Incorporated changes based on internal document review Added preliminary pinouts Updated mechanical specification to reflect 492-ball BGA	DH
0.3	12/18/97	Updated pinouts to proposed pinout	DH
0.4	1/30/98	Updated pinouts to final pinout Fixed CPU/DRAM Frequency strapping options (moved to MECC0 and 2)	DH
0.5	2/13/98	Updated feature bullets Fixed GTLREF pin number in pin descriptions Moved strapping options from HA to MECC (PCLK description, Rx68-69) Updated register and bit definitions: Added Rx2C Subsystem Vendor ID and Rx2E Subsystem ID Added clarifying note on Rx50[7] Redefined Rx51 all bits Added Rx52[7] (strap MECC4) GTL pullup enable Added Rx6B[3-1] suspend refresh rate Changed Rx6C[7] to reserved / do not program Added Rx6D[7] MAB output disable Removed Rx70[5] (no function) and added new bits Rx70[3,0], Rx73[4] Swapped 0/1 bit definition for Rx78[5] Added RxF0-F7 BIOS Scratch Registers	DH
0.6	2/17/98	Removed internal CPU frequency comment in feature bullets Added BIOS scratch registers to register summary tables Fixed typos in Rx51[5] and Rx70[0]	DH
1.0	7/16/98	Changed 586B to 596 in Apollo Pro Chipset Removed DDR, Virtual Channel, and ESDRAM feature bullets Fixed feature bullet / overview errors regarding writeback & EDO timing Changed Device 0 Rx78[4] to "Reserved, Do Not Program" Updated AGP spec support from 1.0 to 2.0	DH

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VIA VT82C691 APOLLO PRO

66 / 100 MHz

Single-Chip Socket-8 / Slot-1 North Bridge
for Desktop and Mobile PC Systems
with AGP and PCI
plus Advanced ECC Memory Controller
supporting SDRAM, EDO, and FPG

- **AGP / PCI / ISA Mobile and Deep Green PC Ready**

- Supports 3.3V and sub-3.3V interface to CPU
- Supports separately powered 3.3V (5V tolerant) interface to system memory, AGP, and PCI bus
- PC-98 compatible using VIA south bridge chips VT82C586B (208-pin PQFP) or VT82C596 (324-contact BGA) with ACPI Power Management for cost-efficient desktop applications
- Modular power management and clock control for mobile system applications
- Combine with VIA VT82C596 (Intel PIIx4 pin compatible 324-pin BGA) “Mobile South” south bridge chip for state-of-the-art mobile applications

- **High Integration**

- Single chip implementation for 64-bit Socket-8 / Slot-1-CPU, 64-bit system memory, 32-bit PCI and 32-bit AGP interfaces
- **Apollo Pro** Chipset: **VT82C691** system controller and **VT82C596** PCI to ISA bridge
- Chipset includes UltraDMA-33 EIDE, USB, and Keyboard / PS2-Mouse Interfaces plus RTC / CMOS on chip

- **High Performance CPU Interface**

- Supports Socket-8 (Intel Pentium Pro™) and Slot-1 (Intel Pentium II™) processors
- 66 / 100 MHz CPU external bus speed
- Built-in deskew DLL (Delay Lock Loop) circuitry for optimal skew control within and between clocking regions
- Five outstanding transactions (four In-Order Queue (IOQ) plus one input latch)
- Supports WC (Write Combining) cycles
- Dynamic deferred transaction support
- Sleep mode support
- System management interrupt, memory remap and STPCLK mechanism

• Full Featured Accelerated Graphics Port (AGP) Controller

- Synchronous and pseudo-synchronous with the host CPU bus with optimal skew control

<u>PCI</u>	<u>AGP</u>	<u>CPU</u>	<u>Mode</u>
33 MHz	66 MHz	100 MHz	3x synchronous
33 MHz	66 MHz	66 MHz	2x synchronous
- AGP v2.0 compliant (1x and 2x transfer modes)
- Supports SideBand Addressing (SBA) mode (non-multiplexed address / data)
- Supports 133MHz 2X mode for AD and SBA signalling
- Pipelined split-transaction long-burst transfers up to 533 MB/sec
- Eight level read request queue
- Four level posted-write request queue
- Thirty-two level (quadwords) read data FIFO (128 bytes)
- Sixteen level (quadwords) write data FIFO (64 bytes)
- Intelligent request reordering for maximum AGP bus utilization
- Supports Flush/Fence commands
- Graphics Address Relocation Table (GART)
 - One level TLB structure
 - Sixteen entry fully associative page table
 - LRU replacement scheme
 - Independent GART lookup control for host / AGP / PCI master accesses
- Windows 95 OSR-2 VXD and integrated Windows 98 / NT5 miniport driver support

• Concurrent PCI Bus Controller

- PCI buses are synchronous / pseudo-synchronous to host CPU bus
- 33 MHz operation on the primary PCI bus
- 66 MHz PCI operation on the AGP bus
- PCI-to-PCI bridge configuration on the 66MHz PCI bus
- Supports up to five PCI masters
- Peer concurrency
- Concurrent multiple PCI master transactions; i.e., allow PCI masters from both PCI buses active at the same time
- Zero wait state PCI master and slave burst transfer rate
- PCI to system memory data streaming up to 132Mbyte/sec
- PCI master snoop ahead and snoop filtering
- Five levels (double-words) of CPU to PCI posted write buffers
- Byte merging in the write buffers to reduce the number of PCI cycles and to create further PCI bursting possibilities
- Enhanced PCI command optimization (MRL, MRM, MWI, etc.)
- Forty-eight levels (double-words) of post write buffers from PCI masters to DRAM
- Sixteen levels (double-words) of prefetch buffers from DRAM for access by PCI masters
- Delay transaction from PCI master accessing DRAM
- Read caching for PCI master reading DRAM
- Transaction timer for fair arbitration between PCI masters (granularity of two PCI clocks)
- Symmetric arbitration between Host/PCI bus for optimized system performance
- Complete steerable PCI interrupts
- PCI-2.1 compliant, 32 bit 3.3V PCI interface with 5V tolerant inputs

- **Advanced High-Performance DRAM Controller**

- DRAM interface synchronous with host CPU (66/100 MHz) or AGP (66MHz) for most flexible configuration
- Concurrent CPU, AGP, and PCI access
- FP, EDO, and SDRAM (standard speed and PC100)
- Different DRAM types may be used in mixed combinations
- Different DRAM timing for each bank
- Dynamic Clock Enable (CKE) control for SDRAM power reduction in mobile and desktop systems
- Mixed 1M / 2M / 4M / 8M / 16MxN DRAMs
- 8 banks up to 1GB DRAMs
- Flexible row and column addresses
- 64-bit data width only
- 3.3V DRAM interface with 5V-tolerant inputs
- Programmable I/O drive capability for MA, command, and MD signals
- Dual copies of MA signals for improved drive
- Optional bank-by-bank ECC (single-bit error correction and multi-bit error detection) or EC (error checking only) for DRAM integrity
- Two-bank interleaving for 16Mbit SDRAM support
- Two-bank and four bank interleaving for 64Mbit SDRAM support
- Supports maximum 16-bank interleave (i.e., 16 pages open simultaneously); banks are allocated based on LRU
- Independent SDRAM control for each bank
- Seamless DRAM command scheduling for maximum DRAM bus utilization (e.g., precharge other banks while accessing the current bank)
- Four cache lines (16 quadwords) of CPU to DRAM write buffers
- Four quadwords of CPU to DRAM read prefetch buffers
- Read around write capability for non-stalled CPU read
- Speculative DRAM read before snoop result
- Burst read and write operation
- x-2-2-2-2-2-2 back-to-back accesses for EDO DRAM
- x-1-1-1-2-1-1-1 back-to-back accesses for SDRAM
- BIOS shadow at 16KB increment
- Decoupled and burst DRAM refresh with staggered RAS timing
- Programmable refresh rate and refresh on populated banks only
- CAS before RAS or self refresh

- **Mobile System Support**

- Independent clock stop controls for CPU / SDRAM, AGP, and PCI bus
- PCI and AGP bus clock run and clock generator control
- VTT suspend power plane preserves memory data
- Suspend-to-DRAM and Self-Refresh operation
- Dynamic clock gating for internal functional blocks for power reduction during normal operation
- Low-leakage I/O pads

- **Built-in NAND-tree pin scan test capability**

- **3.3V, 0.35um, high speed / low power CMOS process**

- **35 x 35 mm, 492 pin BGA Package**

OVERVIEW

The *Apollo Pro* is a high performance, cost-effective and energy efficient chip set for the implementation of AGP / PCI / ISA desktop and notebook personal computer systems from 66 MHz to 100 MHz based on 64-bit Socket-8 (Intel Pentium Pro) and Slot-1 (Intel Pentium-II) super-scalar processors.

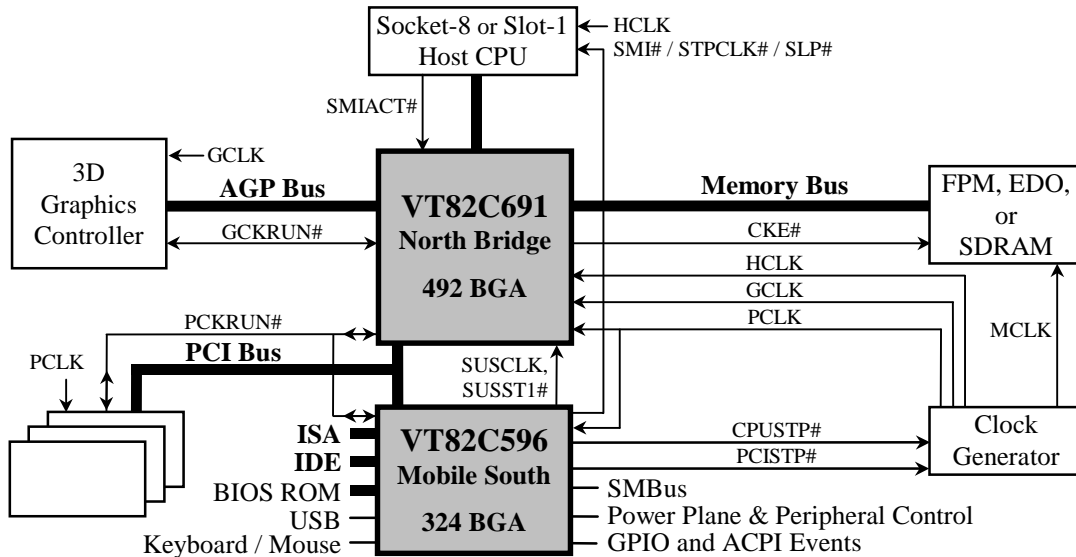


Figure 1. Apollo Pro System Block Diagram Using the VT82C596 Mobile South Bridge

The Apollo-Pro chip set consists of the VT82C691 system controller (492 pin BGA) and the VT82C596 PCI to ISA bridge (324 pin BGA). The system controller provides superior performance between the CPU, DRAM, AGP bus, and PCI bus with pipelined, burst, and concurrent operation. Four cache lines (16 quadwords) of CPU to DRAM write buffers are included on chip to speed up write cycle performance.

The VT82C691 supports eight banks of DRAMs up to 1GB. The DRAM controller supports standard Fast Page Mode (FPM) DRAM, EDO-DRAM, and Synchronous DRAM (SDRAM) in a flexible mix / match manner. The Synchronous DRAM interface allows zero wait state bursting between the DRAM and the data buffers at 100 MHz. The eight banks of DRAM can be composed of an arbitrary mixture of 1M / 2M / 4M / 8M / 16MxN DRAMs. The DRAM controller also supports optional ECC (single-bit error correction and multi-bit detection) or EC (error checking) capability separately selectable on a bank-by-bank basis. The DRAM Controller can run at either the host CPU bus frequency (66 /100 MHz) or at the AGP bus frequency (66 MHz) with built-in deskew DLL timing control. Coupled with PC100 SDRAM, the VT82C691 allows implementation of the most flexible, reliable, and high-performance DRAM interface with data transfers at 66 or 100 MHz.

The VT82C691 also supports full AGP v2.0 capability for maximum bus utilization including 2x mode transfers, SBA (SideBand Addressing), Flush/Fence commands, and pipelined grants. An eight level request queue plus a four level post-write request queue with thirty-two and sixteen quadwords of read and write data FIFO's respectively are included for deep pipelined and split AGP transactions. A single-level GART TLB with 16 full associative entries and flexible CPU / AGP / PCI remapping control is also provided for operation under protected mode operating environments. Both Windows-95 VXD and Windows-98 / NT5 miniport drivers are supported for interoperability with major AGP-based 3D and DVD-capable multimedia accelerators.

The VT82C691 supports two 32-bit 3.3 / 5V system buses (one AGP and one PCI) that are synchronous / pseudo-synchronous to the CPU bus. The chip also contains a built-in bus-to-bus bridge to allow simultaneous concurrent operations on each bus. Five levels (doublewords) of post write buffers are included to allow for concurrent CPU and PCI operation. For PCI master operation, forty-eight levels (doublewords) of post write buffers and sixteen levels (doublewords) of prefetch buffers are included for concurrent PCI bus and DRAM/cache accesses. The chip also supports enhanced PCI bus commands such as Memory-Read-Line, Memory-Read-Multiple and Memory-Write-Invalid commands to minimize snoop overhead. In addition, advanced features are supported such as snoop ahead, snoop filtering, L1 write-back forward to PCI master, and L1 write-back merged with PCI post

write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

The 324-pin Ball Grid Array VT82C596 PCI to ISA bridge supports four levels (doublewords) of line buffers, type F DMA transfers and delay transaction to allow efficient PCI bus utilization and (PCI-2.1 compliant). The VT82C596 also includes an integrated keyboard controller with PS2 mouse support, integrated DS12885 style real time clock with extended 256 byte CMOS RAM, integrated master mode enhanced IDE controller with full scatter and gather capability and extension to UltraDMA-33 / ATA-33 for 33MB/sec transfer rate, integrated USB interface with root hub and two function ports with built-in physical layer transceivers, Distributed DMA support, and OnNow / ACPI compliant advanced configuration and power management interface.

For sophisticated notebook implementations, the VT82C691 provides independent clock stop control for the CPU / SDRAM, PCI, and AGP buses and Dynamic CKE control for powering down of the SDRAM. A separate suspend-well plane is implemented for the SDRAM control signals for Suspend-to-DRAM operation. Coupled with the VT82C596 "Mobile South" chip, a complete notebook PC main board can be implemented with no external TTLs.

The Apollo Pro chipset is ideal for high performance, high quality, high energy efficient and high integration desktop and notebook AGP / PCI / ISA computer systems.

PINOUPS – VT82C691 APOLLO PRO

Figure 2. VT82C691 Ball Diagram (Top View)

Key	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26		
A	GND	GD29	SBA6	SBA5	SBA3	SBA0	INIT#	HD58#	HD53#	HD63#	HD54#	HD57#	GND	HD47#	HD45#	HD34#	HD33#	HD29#	HD24#	HD23#	HD20#	HD10#	HD6#	HD5#	HD1#	GND		
B	GD27	GD30	SBA7	SBA4	SBA2	GRBF#	GREQ#	HD61#	HD50#	HD56#	HD60#	HD52#	HD51#	HD42#	HD39#	HD37#	HD28#	HD30#	HD22#	HD18#	HD13#	HD12#	HD8#	HD0#	HA30	HA29		
C	GD28	GD31	GND	SBS#	SBA1	GPIPE#	GGNT#	VCC3	HD48#	HD62#	HD55#	HD59#	HD46#	GND	HD36#	HD38#	HD31#	HD25#	VCC3	HD16#	HD15#	HD14#	HD4#	GND	HA26	HA31		
D	GD25	GD24	GD26	GVREF	GD23	GDS1#	ST2	HD49#	HD44#	HD43#	HD32#	GTL REF	HD35#	MCLKO	HD26#	MCLKI	HD27#	HD19#	HD11#	HD9#	HD3#	CPURST#	GTL REF	HA28	HA22	HA20		
E	GD18	GD19	GD21	GD22	GND	ST0	ST1	HD41#	HD40#	GCLK	AGND	VTT	GND	GND	AVCC	HCLK	AGND	HD21#	HD17#	HD7#	HD2#	GND	BREQ0#	HA23	HA25	HA19		
F	GTRDY#	GFRM#	GD17	GD16	GBE3#	GND	VCC3	VCC3	VCC3	AVCC	11	12	13	14	15	16	VTT	VCC3	VCC3	VCC3	GND	HA24	HA27	HA15	HA18	HA11		
G	GD13	GPAR	GSTP#	GD20	GBE2#	GND	G7	8	9	10							17	18	19	G20	GND	HA17	HA21	HA13	HA12	HA14		
H	GD10	GD11	VCC3	GSERR#	GIRDY#	VCC3	H	9												H	VCC3	HA16	HA7	VCC3	HA5	HA3		
J	GD7	GD8	GD9	GD15	GDSSEL#	VCC3	J	AGP Pins														J	VCC3	HA10	HA8	HA9	HA4	BNR#
K	GD6	GD5	GDS0#	GD14	GBE1#	GD12	K																					
L	GD3	GD2	GD4	GD1	GBE0#	L					L	GND	VCC3	GND	GND	VCC3	GND	L			L	HTRDY#	DRDY#	DEFER#	HLOCK#	HREQ2#		
M	REQ3#	GNT2#	REQ2#	LOCK#	GD0	M					M	VCC3	GND	GND	GND	GND	VCC3	M			M	HREQ3#	RS2#	RS0#	HITM#	HIT#		
N	GNT1#	REQ1#	GND	GNT3#	GND	N					N	GND	GND	GND	GND	GND	GND	N			N	GND	ADS#	DBSY#	RS1#	GND		
P	GND	REQ0#	AD31	GNT0#	GND	P					P	GND	GND	GND	GND	GND	GND	P			P	GND	MD0	GND	MD2	MD34		
R	AD30	AD29	AD28	REQ4#	GNT4#	R					R	VCC3	GND	GND	GND	GND	VCC3	R			R	MD1	MD32	MD3	MD35	MD4		
T	AD27	AD25	AD24	AD26	PCLK	T					T	GND	VCC3	GND	GND	VCC3	GND	T			T	MD6	MD33	MD36	MD5	MD37		
U	CBE3#	AD21	AD20	AD23	AD22	5VREF	U	PCI Pins														U	VSUS	MD7	MD38	MD8	MD40	MD9
V	AD19	AD16	CBE2#	AD18	AD17	VCC3	V																					
W	FRM#	IRDY#	VCC3	TRDY#	PAR	VCC3	W														W	VCC3	MD13	MD43	VCC3	MD12	MD44	
Y	DSEL#	STOP#	SERR#	AD13	CBE1#	GND	Y7	8	9	10											Y20	GND	MD47	MD45	MD14	MD46	MD15	
AA	AD15	AD14	AD11	AD12	AD8	GND	VCC3	VCC3	VCC3	MD22	11	12	13	14	15	16	5VREF	VCC3	VCC3	VCC3	GND	MECC0	MECC4	MECC5	SWEC#	RAS0#		
AB	AD10	AD9	AD7	CBE0#	GND	SUST#	MD58	VSUS	MD23	MD51	MD19	MD18	GND	GND	DS3#	CAS2#	CAS6#	RAS5#	SCASD#	MAA13	MAB0	GND	MECC1	SWEA#	SCASA#	CAS4#		
AC	AD6	AD5	RESET#	CRSTI#	MD30	MD27	MD26	MD55	MD21	MD54	MD50	MVREF	DS7#	DS6#	MAA2	DS2#	CAS3#	CAS7#	MAB10	MAB7	MAA11	MAA3	DS1#	RAS1#	SCASC#	DS0#		
AD	AD3	AD0	GND	MD63	MD60	SUCLK	MD56	VCC3	MD49	MD16	MECC2	MECC3	GND	MAA9	MAB5	SWED#	RAS4#	MAB8	VCC3	MAA7	MAA0	MVREF	MAA4	GND	DS5#	DS4#		
AE	AD4	AD1	PGNT#	MD62	MD29	MD59	MD25	MD53	MD20	MD48	MECC6	MAB12	SRASD#	MAA10	MAA12	MAB9	RAS3#	RAS6#	MAB3	MAA8	MAA1	RAS2#	CAS0#	MAA6	SRASC#	SRASB#		
AF	GND	AD2	PREQ#	MD31	MD61	MD28	MD57	MD24	MD52	MD17	MECC7	MAB13	MAB11	GND	MAA5	MAB4	SWEB#	RAS7#	MAB6	MAB2	SRASA#	CAS5#	CAS1#	SCASB#	MAB1	GND		

Figure 3. VT82C691 Pin List (Numerical Order)

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
A01	P GND	D05	IO GD23	H03	P VCC3	P01	P GND	W25	IO MD12	AC23	O DS1#
A02	IO GD29	D06	IO GDS1#	H04	IO GSERR# / PCKR#	P02	I REQ0#	W26	IO MD44	AC24	O RAS1# / CS1#
A03	I SBA6	D07	O ST2	H05	IO GIRDY#	P03	IO AD31	Y01	IO DEVSEL#	AC25	O SCASC#
A04	I SBA5	D08	IO HD49#	H06	P VCC3	P04	O GNT0#	Y02	IO STOP#	AC26	O DS0#
A05	I SBA3	D09	IO HD44#	H21	P VCC3	P05	P GND	Y03	IO SERR#	AD01	IO AD03
A06	I SBA0	D10	IO HD43#	H22	IO HA16	P11	P GND	Y04	IO AD13	AD02	IO AD00
A07	O INIT#	D11	IO HD32#	H23	IO HA07	P12	P GND	Y05	IO CBE1#	AD03	P GND
A08	IO HD58#	D12	I GTLREF	H24	P VCC3	P13	P GND	Y06	P GND	AD04	IO MD63
A09	IO HD53#	D13	IO HD35#	H25	IO HA05	P14	P GND	Y21	P GND	AD05	IO MD60
A10	IO HD63#	D14	O MCLKO	H26	IO HA03	P15	P GND	Y22	IO MD47	AD06	I SUCLK
A11	IO HD54#	D15	IO HD27#	J01	IO GD07	P16	P GND	Y23	IO MD45	AD07	IO MD56
A12	IO HD57#	D16	I MCLKI	J02	IO GD08	P22	P GND	Y24	IO MD14	AD08	P VCC3
A13	P GND	D17	IO HD19#	J03	IO GD09	P23	IO MD00	Y25	IO MD46	AD09	IO MD49
A14	IO HD47#	D18	IO HD11#	J04	IO GD15	P24	P GND	Y26	IO MD15	AD10	IO MD16
A15	IO HD45#	D19	IO HD09#	J05	IO GDSEL#	P25	IO MD02	AA01	IO AD15	AD11	IO MECC2 / CKE2#
A16	IO HD34#	D20	IO HD03#	J06	P VCC3	P26	IO MD34	AA02	IO AD14	AD12	IO MECC3 / CKE3#
A17	IO HD33#	D21	O CPURST#	J21	P VCC3	R01	IO AD30	AA03	IO AD11	AD13	P GND
A18	IO HD29#	D22	O CPURST#	J22	IO HA10	R02	IO AD29	AA04	IO AD12	AD14	O MAA9
A19	IO HD24#	D23	I GTLREF	J23	IO HA08	R03	IO AD28	AA05	IO AD08	AD15	O MAB5
A20	IO HD23#	D24	IO HA28	J24	IO HA09	R04	I REQ4#	AA06	P GND	AD16	O SWED# / MWED#
A21	IO HD20#	D25	IO HA22	J25	IO HA04	R05	O GNT4#	AA07	P VCC3	AD17	O RAS4# / CS4#
A22	IO HD10#	D26	IO HA20	J26	IO BNR#	R11	P VCC3	AA08	P VCC3	AD18	O MAB8
A23	IO HD06#	E01	IO GD18	K01	IO GD06	R12	P GND	AA09	P VCC3	AD19	P VCC3
A24	IO HD05#	E02	IO GD19	K02	IO GD05	R13	P GND	AA10	IO MD22	AD20	O MAA7
A25	IO HD01#	E03	IO GD21	K03	IO GDS0#	R14	P GND	AA17	P SVREF	AD21	O MAA0
A26	P GND	E04	IO GD22	K04	IO GD14	R15	P GND	AA18	P VCC3	AD22	P MVREF
B01	IO GD27	E05	P GND	K05	IO GBE1#	R16	P VCC3	AA19	P VCC3	AD23	O MAA4
B02	IO GD30	E06	O ST0	K06	IO GD12	R22	IO MD01	AA20	P VCC3	AD24	P GND
B03	I SBA7	E07	O ST1	K21	P VTT	R23	IO MD32	AA21	P GND	AD25	O DS5#
B04	I SBA4	E08	IO HD41#	K22	IO HA06	R24	IO MD03	AA22	IO MECC0 / CKE0#	AD26	O DS4#
B05	I SBA2	E09	IO HD40#	K23	IO HREQ1#	R25	IO MD35	AA23	IO MECC4 / CKE4#	AE01	IO AD04
B06	I GRBF#	E10	I GCLK	K24	IO HREQ0#	R26	IO MD04	AA24	IO MECC5 / CKE5#	AE02	IO AD01
B07	I GREQ#	E11	P AGND	K25	IO BPR1#	T01	IO AD27	AA25	O SWEC# / MWEC#	AE03	O PGNT#
B08	IO HD61#	E12	P VTT	K26	IO HREQ4#	T02	IO AD25	AA26	O RAS0# / CS0#	AE04	IO MD62
B09	IO HD50#	E13	P GND	L01	IO GD03	T03	IO AD24	AB01	IO AD10	AE05	IO MD29
B10	IO HD56#	E14	P GND	L02	IO GD02	T04	IO AD26	AB02	IO AD09	AE06	IO MD59
B11	IO HD60#	E15	P AVCC	L03	IO GD04	T05	I PCLK	AB03	IO AD07	AE07	IO MD25
B12	IO HD52#	E16	I HCLK	L04	IO GD01	T11	P GND	AB04	IO CBE0#	AE08	IO MD53
B13	IO HD51#	E17	P AGND	L05	IO GBE0#	T12	P VCC3	AB05	P GND	AE09	IO MD20
B14	IO HD42#	E18	IO HD21#	L11	P GND	T13	P GND	AB06	I SUST#	AE10	IO MD48
B15	IO HD39#	E19	IO HD17#	L12	P VCC3	T14	P GND	AB07	IO MD58	AE11	IO MECC6 / CKE6#
B16	IO HD37#	E20	IO HD07#	L13	P GND	T15	P VCC3	AB08	P VSUS	AE12	O MAB12
B17	IO HD28#	E21	IO HD02#	L14	P GND	T16	P GND	AB09	IO MD23	AE13	O SRASD#
B18	IO HD30#	E22	P GND	L15	P VCC3	T22	IO MD06	AB10	IO MD51	AE14	O MAA10
B19	IO HD22#	E23	O BREQ0#	L16	P GND	T23	IO MD33	AB11	IO MD19	AE15	O MAA12
B20	IO HD18#	E24	IO HA23	L22	IO HTRDY#	T24	IO MD36	AB12	IO MD18	AE16	O MAB9
B21	IO HD13#	E25	IO HA25	L23	IO DRDY#	T25	IO MD05	AB13	P GND	AE17	O RAS3# / CS3#
B22	IO HD12#	E26	IO HA19	L24	IO DEFER#	T26	IO MD37	AB14	P GND	AE18	O RAS6# / CS6#
B23	IO HD08#	F01	IO GTRDY#	L25	I HLOCK#	U01	IO CBE3#	AB15	O DS3#	AE19	O MAB3
B24	IO HD00#	F02	IO GFRM#	L26	IO HREQ2#	U02	IO AD21	AB16	O CAS2# / DQM2#	AE20	O MAA8
B25	IO HA30	F03	IO GD17	M01	I REQ3#	U03	IO AD20	AB17	O CAS6# / DQM6#	AE21	O MAA1
B26	IO HA29	F04	IO GD16	M02	O GNT2#	U04	IO AD23	AB18	O RAS5# / CS5#	AE22	O RAS2# / CS2#
C01	IO GD28	F05	IO GBE3#	M03	I REQ2#	U05	IO AD22	AB19	O SCASD#	AE23	O CAS0# / DQM0#
C02	IO GD31	F06	P GND	M04	IO LOCK#	U06	P SVREF	AB20	O MAA13	AE24	O MAA6
C03	P GND	F07	P VCC3	M05	IO GD00	U21	P VSUS	AB21	O MAB0	AE25	O SRASC#
C04	I SBS#	F08	P VCC3	M11	P VCC3	U22	IO MD07	AB22	P GND	AE26	O SRASB#
C05	I SBA1	F09	P VCC3	M12	P GND	U23	IO MD38	AB23	IO MECC1 / CKE1#	AF01	P GND
C06	I GPIPE#	F10	P AVCC	M13	P GND	U24	IO MD08	AB24	O SWEA# / MWEA#	AF02	IO AD02
C07	O GGNT#	F17	P VTT	M14	P GND	U25	IO MD40	AB25	O SCASA#	AF03	I PREQ#
C08	P VCC3	F18	P VCC3	M15	P GND	U26	IO MD09	AB26	O CAS4# / DQM4#	AF04	IO MD31
C09	IO HD48#	F19	P VCC3	M16	P VCC3	V01	IO AD19	AC01	IO AD06	AF05	IO MD61
C10	IO HD62#	F20	P VCC3	M22	IO HREQ3#	V02	IO AD16	AC02	IO AD05	AF06	IO MD28
C11	IO HD55#	F21	P GND	M23	IO RS2#	V03	IO CBE2#	AC03	I RESET#	AF07	IO MD57
C12	IO HD59#	F22	IO HA24	M24	IO RS0#	V04	IO AD18	AC04	I CRSTI#	AF08	IO MD24
C13	IO HD46#	F23	IO HA27	M25	I HITM#	V05	IO AD17	AC05	IO MD30	AF09	IO MD52
C14	P GND	F24	IO HA15	M26	IO HIT#	V06	P VCC3	AC06	IO MD27	AF10	IO MD17
C15	IO HD36#	F25	IO HA18	N01	O GNT1#	V21	P VCC3	AC07	IO MD26	AF11	IO MECC7 / CKE7#
C16	IO HD38#	F26	IO HA11	N02	I REQ1#	V22	IO MD11	AC08	IO MD55	AF12	O MAB13
C17	IO HD31#	G01	IO GD13	N03	P GND	V23	IO MD39	AC09	IO MD21	AF13	O MAB11
C18	IO HD25#	G02	IO GPAR / GCKR#	N04	O GNT3#	V24	IO MD41	AC10	IO MD54	AF14	P GND
C19	P VCC3	G03	IO GSTOP#	N05	P GND	V25	IO MD10	AC11	IO MD50	AF15	O MAA5
C20	IO HD16#	G04	IO GD20	N11	P GND	V26	IO MD42	AC12	P MVREF	AF16	O MAB4
C21	IO HD15#	G05	IO GBE2#	N12	P GND	W01	IO FRAME#	AC13	O DS7#	AF17	O SWEB# / MWEB#
C22	IO HD14#	G06	P GND	N13	P GND	W02	IO IRDY#	AC14	O DS6#	AF18	O RAS7# / CS7#
C23	IO HD04#	G21	P GND	N14	P GND	W03	P VCC3	AC15	O MAA2	AF19	O MAB6
C24	P GND	G22	IO HA17	N15	P GND	W04	IO TRDY#	AC16	O DS2#	AF20	O MAB2
C25	IO HA26	G23	IO HA21	N16	P GND	W05	IO PAR	AC17	O CAS3# / DQM3#	AF21	O SRASA#
C26	IO HA31	G24	IO HA13	N22	P GND	W06	P VCC3	AC18	O CAS7# / DQM7#	AF22	O CAS5# / DQM5#
D01	IO GD25	G25	IO HA12	N23	IO ADS#	W21	P VCC3	AC19	O MAB10	AF23	O CAS1# / DOM1#
D02	IO GD24	G26	IO HA14	N24	IO DBSY#	W22	IO MD13	AC20	O MAB7	AF24	O SCASB#
D03	IO GD26	H01	IO GD10	N25	IO RS1#	W23	IO MD43	AC21	O MAA11	AF25	O MAB1
D04	P GVREF	H02	IO GD11	N26	P GND	W24	P VCC3	AC22	O MAA3	AF26	P GND

Figure 4. VT82C691 Pin List (Alphabetical Order)

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
U06	P 5VREF	J02	IO GD08	AA06	P GND	C18	IO HD25#	R22	IO MD01	AB18	O RAS5# / CS5#
AA17	P 5VREF	J03	IO GD09	AA21	P GND	D15	IO HD26#	P25	IO MD02	AE18	O RAS6# / CS6#
AD02	IO AD00	H01	IO GD10	AB05	P GND	D17	IO HD27#	R24	IO MD03	AF18	O RAS7# / CS7#
AE02	IO AD01	H02	IO GD11	AB13	P GND	B17	IO HD28#	R26	IO MD04	P02	I REQ0#
AF02	IO AD02	K06	IO GD12	AB14	P GND	A18	IO HD29#	T25	IO MD05	N02	I REQ1#
AD01	IO AD03	G01	IO GD13	AB22	P GND	B18	IO HD30#	T22	IO MD06	M03	I REQ2#
AE01	IO AD04	K04	IO GD14	AD03	P GND	C17	IO HD31#	U22	IO MD07	M01	I REQ3#
AC02	IO AD05	J04	IO GD15	AD13	P GND	D11	IO HD32#	U24	IO MD08	R04	I REQ4#
AC01	IO AD06	F04	IO GD16	AD24	P GND	A17	IO HD33#	U26	IO MD09	AC03	I RESET#
AB03	IO AD07	F03	IO GD17	AF01	P GND	A16	IO HD34#	V25	IO MD10	M24	IO RS0#
AA05	IO AD08	E01	IO GD18	AF14	P GND	D13	IO HD35#	V22	IO MD11	N25	IO RS1#
AB02	IO AD09	E02	IO GD19	AF26	P GND	C15	IO HD36#	W25	IO MD12	M23	IO RS2#
AB01	IO AD10	G04	IO GD20	P04	O GNT0#	B16	IO HD37#	W22	IO MD13	A06	I SBA0
AA03	IO AD11	E03	IO GD21	N01	O GNT1#	C16	IO HD38#	Y24	IO MD14	C05	I SBA1
AA04	IO AD12	E04	IO GD22	M02	O GNT2#	B15	IO HD39#	Y26	IO MD15	B05	I SBA2
Y04	IO AD13	D05	IO GD23	N04	O GNT3#	E09	IO HD40#	AD10	IO MD16	A05	I SBA3
AA02	IO AD14	D02	IO GD24	R05	O GNT4#	E08	IO HD41#	AF10	IO MD17	B04	I SBA4
AA01	IO AD15	D01	IO GD25	G02	IO GPAR/GCKR#	B14	IO HD42#	AB12	IO MD18	A04	I SBA5
V02	IO AD16	D03	IO GD26	C06	I GPIPE#	D10	IO HD43#	AB11	IO MD19	A03	I SBA6
V05	IO AD17	B01	IO GD27	B06	I GRBF#	D09	IO HD44#	AE09	IO MD20	B03	I SBA7
V04	IO AD18	C01	IO GD28	B07	I GREO#	A15	IO HD45#	AC09	IO MD21	C04	I SBS#
V01	IO AD19	A02	IO GD29	H04	IO GSERR#/PCKR#	C13	IO HD46#	AA10	IO MD22	AB25	O SCASA#
U03	IO AD20	B02	IO GD30	G03	IO GSTOP#	A14	IO HD47#	AB09	IO MD23	AF24	O SCASB#
U02	IO AD21	K02	IO GD31	D12	I GTLREF	C09	IO HD48#	AF08	IO MD24	AC25	O SCASC#
U05	IO AD22	C03	IO GDS0#	D23	I GTLREF	D08	IO HD49#	AE07	IO MD25	AB19	O SCASD#
U04	IO AD23	D06	IO GDS1#	F01	IO GTRDY#	B09	IO HD50#	AC07	IO MD26	Y03	IO SFERR#
T03	IO AD24	J05	IO GDSEL#	D04	P GVREF	B13	IO HD51#	AC06	IO MD27	AF21	O SRASA#
T02	IO AD25	F02	IO GFRM#	H26	IO HA03	B12	IO HD52#	AF06	IO MD28	AE26	O SRASB#
T04	IO AD26	C07	IO GGNT#	J25	IO HA04	A09	IO HD53#	AE05	IO MD29	AE25	O SRASC#
T01	IO AD27	H05	IO GIRDY#	H25	IO HA05	A11	IO HD54#	AC05	IO MD30	AE13	O SRASD#
R03	IO AD28	A01	P GND	K22	IO HA06	C11	IO HD55#	AF04	IO MD31	E06	O ST0
R02	IO AD29	A13	P GND	H23	IO HA07	B10	IO HD56#	R23	IO MD32	E07	O ST1
R01	IO AD30	A26	P GND	J23	IO HA08	A12	IO HD57#	T23	IO MD33	D07	O ST2
P03	IO AD31	C03	P GND	J24	IO HA09	A08	IO HD58#	P26	IO MD34	Y02	IO STOP#
N23	IO ADS#	C14	P GND	J22	IO HA10	C12	IO HD59#	R25	IO MD35	AB06	I SUST#
E11	P AGND	C24	P GND	F26	IO HA11	B11	IO HD60#	T24	IO MD36	AD06	I SUCLK
E17	P AGND	E05	P GND	G25	IO HA12	B08	IO HD61#	T26	IO MD37	AB24	O SWEA# / MWEA#
E15	P AVCC	E13	P GND	G24	IO HA13	C10	IO HD62#	U23	IO MD38	AF17	O SWEB# / MWEB#
F10	P AVCC	E14	P GND	G26	IO HA14	A10	IO HD63#	V23	IO MD39	AA25	O SWEC# / MWEC#
J26	IO BNR#	E22	P GND	F24	IO HA15	M26	IO HIT#	U25	IO MD40	AD16	O SWED# / MWED#
K25	IO BPRI#	F06	P GND	H22	IO HA16	M25	I HITM#	V24	IO MD41	W04	IO TRDY#
E23	O BREQ0#	F21	P GND	G22	IO HA17	L25	I HLOCK#	V26	IO MD42	C08	P VCC3
AE23	O CAS0# / DQM0#	G06	P GND	F25	IO HA18	K24	IO HREQ0#	W23	IO MD43	C19	P VCC3
AF23	O CAS1# / DQM1#	G21	P GND	E26	IO HA19	K23	IO HREQ1#	W26	IO MD44	F07	P VCC3
AB16	O CAS2# / DQM2#	L11	P GND	D26	IO HA20	L26	IO HREQ2#	Y23	IO MD45	F08	P VCC3
AC17	O CAS3# / DQM3#	L13	P GND	G23	IO HA21	M22	IO HREQ3#	Y25	IO MD46	F09	P VCC3
AB26	O CAS4# / DQM4#	L14	P GND	D25	IO HA22	K26	IO HREQ4#	Y22	IO MD47	F18	P VCC3
AF22	O CAS5# / DQM5#	L16	P GND	E24	IO HA23	L22	IO HTRDY#	AE10	IO MD48	F19	P VCC3
AB17	O CAS6# / DQM6#	M12	P GND	F22	IO HA24	A07	O INIT#	AD09	IO MD49	F20	P VCC3
AC18	O CAS7# / DQM7#	M13	P GND	E25	IO HA25	W02	IO IRDY#	AC11	IO MD50	H03	P VCC3
AB04	IO CBE0#	M14	P GND	C25	IO HA26	M04	IO LOCK#	AB10	IO MD51	H06	P VCC3
Y05	IO CBE1#	M15	P GND	F23	IO HA27	AD21	O MAA0	AF09	IO MD52	H21	P VCC3
V03	IO CBE2#	N03	P GND	D24	IO HA28	AE21	O MAA1	AE08	IO MD53	H24	P VCC3
U01	IO CBE3#	N05	P GND	B26	IO HA29	AC15	O MAA2	AC10	IO MD54	J06	P VCC3
D22	O CPURST#	N11	P GND	B25	IO HA30	AC22	O MAA3	AC08	IO MD55	J21	P VCC3
AC04	I CRSTI#	N12	P GND	C26	IO HA31	AD23	O MAA4	AD07	IO MD56	L12	P VCC3
N24	IO DBSY#	N13	P GND	E16	I HCLK	AF15	O MAA5	AF07	IO MD57	L15	P VCC3
L24	IO DEFER#	N14	P GND	B24	IO HD00#	AE24	O MAA6	AB07	IO MD58	M11	P VCC3
Y01	IO DEVSEL#	N15	P GND	A25	IO HD01#	AD20	O MAA7	AE06	IO MD59	M16	P VCC3
L23	IO DRDY#	N16	P GND	E21	IO HD02#	AE20	O MAA8	AD05	IO MD60	R11	P VCC3
AC26	O DS0#	N22	P GND	D21	IO HD03#	AD14	O MAA9	AF05	IO MD61	R16	P VCC3
AC23	O DS1#	N26	P GND	C23	IO HD04#	AE14	O MAA10	AE04	IO MD62	T12	P VCC3
AC16	O DS2#	P01	P GND	A24	IO HD05#	AC21	O MAA11	AD04	IO MD63	T15	P VCC3
AB15	O DS3#	P05	P GND	A23	IO HD06#	AE15	O MAA12	AA22	IO MECC0/CKE0#	V06	P VCC3
AD26	O DS4#	P11	P GND	E20	IO HD07#	AB20	O MAA13	AB23	IO MECC1/CKE1#	V21	P VCC3
AD25	O DS5#	P12	P GND	B23	IO HD08#	AB21	O MAB0	AD11	IO MECC2/CKE2#	W03	P VCC3
AC14	O DS6#	P13	P GND	D20	IO HD09#	AF25	O MAB1	AD12	IO MECC3/CKE3#	W06	P VCC3
AC13	O DS7#	P14	P GND	A22	IO HD10#	AF20	O MAB2	AA23	IO MECC4/CKE4#	W21	P VCC3
W01	IO FRAME#	P15	P GND	D19	IO HD11#	AE19	O MAB3	AA24	IO MECC5/CKE5#	W24	P VCC3
L05	IO GBE0#	P16	P GND	B22	IO HD12#	AF16	O MAB4	AE11	IO MECC6/CKE6#	AA07	P VCC3
K05	IO GBE1#	P22	P GND	B21	IO HD13#	AD15	O MAB5	AF11	IO MECC7/CKE7#	AA08	P VCC3
G05	IO GBE2#	P24	P GND	C22	IO HD14#	AF19	O MAB6	AC12	P MVREF	AA09	P VCC3
F05	IO GBE3#	R12	P GND	C21	IO HD15#	AC20	O MAB7	AD22	P MVREF	AA18	P VCC3
E10	I GCLK	R13	P GND	C20	IO HD16#	AD18	O MAB8	W05	IO PAR	AA19	P VCC3
M05	IO GD00	R14	P GND	E19	IO HD17#	AE16	O MAB9	T05	I PCLK	AA20	P VCC3
L04	IO GD01	R15	P GND	B20	IO HD18#	AC19	O MAB10	AE03	O PGNT#	AD08	P VCC3
L02	IO GD02	T11	P GND	D18	IO HD19#	AF13	O MAB11	AF03	I PREQ#	AD19	P VCC3
L01	IO GD03	T13	P GND	A21	IO HD20#	AE12	O MAB12	AA26	O RAS0# / CS0#	U21	P VSUS
L03	IO GD04	T14	P GND	E18	IO HD21#	AF12	O MAB13	AC24	O RAS1# / CS1#	AB08	P VSUS
K02	IO GD05	T16	P GND	B19	IO HD22#	D16	I MCLKI	AE22	O RAS2# / CS2#	E12	P VTT
K01	IO GD06	Y06	P GND	A20	IO HD23#	D14	O MCLKO	AE17	O RAS3# / CS3#	F17	P VTT
J01	IO GD07	Y21	P GND	A19	IO HD24#	P23	IO MD00	AD17	O RAS4# / CS4#	K21	P VTT

PIN DESCRIPTIONS

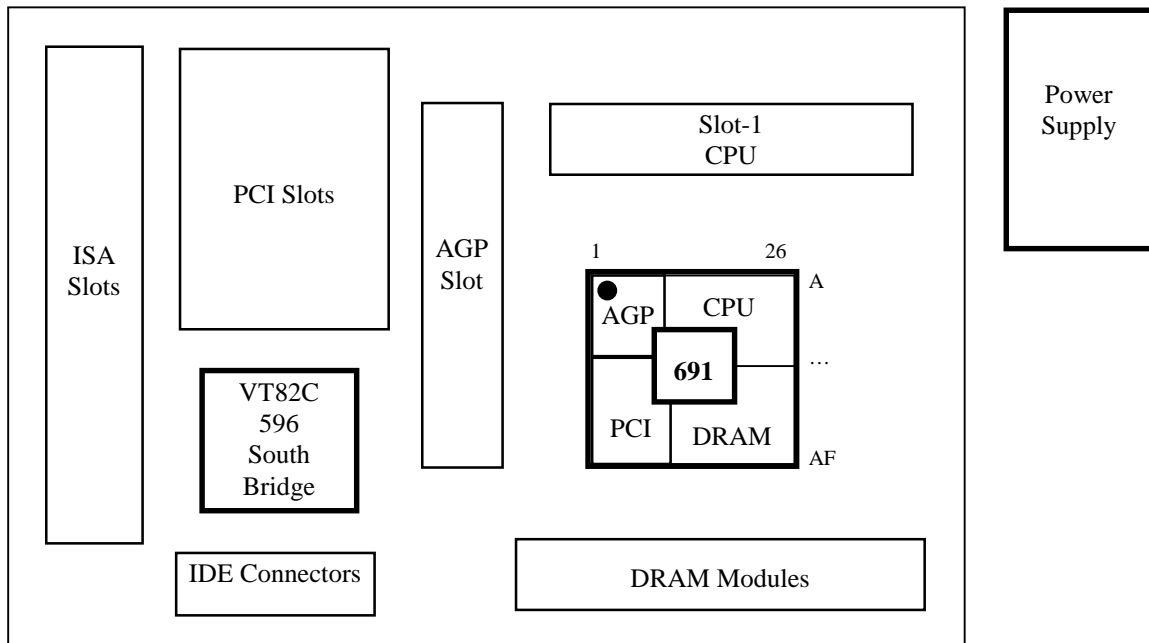
Table 1. VT82C691 Pin Descriptions

CPU Interface																					
Signal Name	Pin #	I/O	Signal Description																		
ADS#	N23	B	Address Strobe. The CPU asserts ADS# in T1 of the CPU bus cycle.																		
BNR#	J26	B	Block Next Request. Used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.																		
BPRI#	K25	B	Priority Agent Bus Request. The owner of this signal will always be the next bus owner. This signal has priority over symmetric bus requests and causes the current symmetric owner to stop issuing new transactions unless the HLOCK# signal is asserted. The VT82C691 drives this signal to gain control of the processor bus.																		
DBSY#	N24	B	Data Bus Busy. Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.																		
DEFER#	L24	B	Defer. The VT82C691 uses a dynamic deferring policy to optimize system performance. The VT82C691 also uses the DEFER# signal to indicate a processor retry response.																		
DRDY#	L23	B	Data Ready. Asserted for each cycle that data is transferred.																		
HIT#	M26	B	Hit. Indicates that a cacheing agent holds an unmodified version of the requested line. Also driven in conjunction with HITM# by the target to extend the snoop window.																		
HITM#	M25	I	Hit Modified. Asserted by the CPU to indicate that the address presented with the last assertion of EADS# is modified in the L1 cache and needs to be written back.																		
HLOCK#	L25	I	Host Lock. All CPU cycles sampled with the assertion of HLOCK# and ADS# until the negation of HLOCK# must be atomic.																		
HREQ[4:0]#	K26, M22, L26, K23, K24	B	Request Command. Asserted during both clocks of the request phase. In the first clock, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type.																		
HTRDY#	L22	B	Host Target Ready. Indicates that the target of the processor transaction is able to enter the data transfer phase.																		
RS[2:0]#	M23, N25, M24	B	Response Signals. Indicates the type of response per the table below: <table style="margin-left: 20px; border: none;"> <tr> <td style="text-align: right;">RS[2:0]#</td> <td>Response type</td> </tr> <tr> <td>000</td> <td>Idle State</td> </tr> <tr> <td>001</td> <td>Retry Response</td> </tr> <tr> <td>010</td> <td>Defer Response</td> </tr> <tr> <td>011</td> <td>Reserved</td> </tr> <tr> <td>100</td> <td>Hard Failure</td> </tr> <tr> <td>101</td> <td>Normal Without Data</td> </tr> <tr> <td>110</td> <td>Implicit Writeback</td> </tr> <tr> <td>111</td> <td>Normal With Data</td> </tr> </table>	RS[2:0]#	Response type	000	Idle State	001	Retry Response	010	Defer Response	011	Reserved	100	Hard Failure	101	Normal Without Data	110	Implicit Writeback	111	Normal With Data
RS[2:0]#	Response type																				
000	Idle State																				
001	Retry Response																				
010	Defer Response																				
011	Reserved																				
100	Hard Failure																				
101	Normal Without Data																				
110	Implicit Writeback																				
111	Normal With Data																				
CPURST#	D22	O	CPU Reset. Reset output to CPU																		
INIT#	A7	O	Init. Init output to CPU.																		
BREQ0#	E23	O	Bus Request 0. Bus request output to CPU.																		

CPU Interface (Continued)			
Signal Name	Pin #	I/O	Signal Description
HA[31:3]	(see pinout tables)	B	Host Address Bus. HA[31:3] connect to the address bus of the host CPU. During CPU cycles HA[31:3] are inputs. These signals are driven by the VT82C691 during cache snooping operations.
HD[63:0]#	(see pinout tables)	B	Host CPU Data. These signals are connected to the CPU data bus.
GTLREF	D12, D23	P	GTL⁺ Reference Voltage. This is the reference voltage derived from the termination voltage to the pullup resistors and determines the noise margin for the signals. This signal goes to the reference input of the GTL ⁺ sense amp on each GTL ⁺ input or I/O pin.

Note: Clocking of the CPU and cache interfaces is performed with HCLK. See the clock pin group at the end of the pin descriptions section for descriptions of the clock input pins.

Note: The VT82C691 pinouts were defined assuming the ATX PCB layout model shown below (and general pin layout shown) as a guide for PCB component placement. Other PCB layouts (AT, LPX, and NLX) were also considered and can typically follow the same general component placement.



DRAM Interface			
Signal Name	Pin #	I/O	Signal Description
MD[63:0]	(see pinout tables)	B	Memory Data. These signals are connected to the DRAM data bus. Note: MD0 is internally pulled up for use in EDO memory type detection.
MECC[7:0] / CKE[7:0]	AF11, AE11, AA24, AA23, AD12, AD11, AB23, AA22	B	Multifunction Pins 1. DRAM ECC or EC Data (Rx78[0]=0) 2. Clock Enables. Clock enables for each DRAM bank (Rx78[0]=1) for powering down the SDRAMs in notebook applications. 3. Strap Options: (strap pin low for 0 or high for 1 using 4.7K ohm) MECC0 Rx68[0] CPU Frequency (0 = 66 MHz, 100 MHz) MECC2 Rx69[2] DRAM Frequency (0 = CPU, 1 = AGP)
MAA[13:0]	AB20, AE15, AC21, AE14, AD14, AE20, AD20, AE24, AF15, AD23, AC22, AC15, AE21, AD21	O	Memory Address A. DRAM address lines (two sets for better drive)
MAB[13:0]	AF12, AE12, AF13, AC19, AE16, AD18, AC20, AF19, AD15, AF16, AE19, AF20, AF25, AB21	O	Memory Address B. DRAM address lines (two sets for better drive)
RAS[7:0]# / CS[7:0]#	AF18, AE18, AB18, AD17, AE17, AE22, AC24, AA26	O	Multifunction Pins 1. FPG/EDO DRAM: Row Address Strobe of each bank. 2. Synchronous DRAM: Chip select of each bank..
CAS[7:0]# / DQM[7:0]#	AC18, AB17, AF22, AB26, AC17, AB16, AF23, AE23	O	Multifunction Pins 1. FPG/EDO DRAM: Column Address Strobe of each byte lane. 2. Synchronous DRAM: Data mask of each byte lane.
SRASA#, SRASB#, SRASC#, SRASD#	AF21 AE26 AE25 AE13	O	Row Address Command Indicator. For support of up to four Synchronous DRAM DIMM slots (these are not copies as each DIMM slot may have separate timing). "A" controls banks 0-1 (module 0), "B" controls banks 2-3 (module 1), "C" controls banks 4-5 (module 2), and "D" controls banks 6-7 (module 3).
SCASA#, SCASB#, SCASC#, SCASD#	AB25 AF24 AC25 AB19	O	Column Address Command Indicator. For support of up to three Synchronous DRAM DIMM slots (these are not copies as each DIMM slot may have separate timing). "A" controls banks 0-1 (module 0), "B" controls banks 2-3 (module 1), "C" controls banks 4-5 (module 2), and "D" controls banks 6-7 (module 3).
SWEA# / MWEA#, SWEB# / MWEB#, SWEC# / MWEC#, SWED# / MWED#	AB24 AF17 AA25 AD16	O	Write Enable Command Indicator. For support of up to three Synchronous DRAM DIMM slots (these are not copies as each DIMM slot may have separate timing). Multifunction pins, used as MWE# pins for FPG/EDO memory. "A" controls banks 0-1 (module 0), "B" controls banks 2-3 (module 1), "C" controls banks 4-5 (module 2), and "D" controls banks 6-7 (module 3).
DS[7:0]#	AC13, AC14, AD25, AD26, AB15, AC16, AC23, AC26	O	DDR SDRAM Data Strobes. Every 8 data bits share one common data strobe. I.e., DS0# corresponds to MD[7:0], DS1# corresponds to MD[15:0], etc..

PCI Bus Interface			
Signal Name	Pin #	I/O	Signal Description
FRAME#	W1	B	Frame. Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
AD[31:0]	(see pinout tables)	B	Address/Data Bus. The standard PCI address and data lines. The address is driven with FRAME# assertion and data is driven or received in following cycles.
CBE[3:0]#	U1, V3, Y5, AB4	B	Command/Byte Enable. Commands are driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
IRDY#	W2	B	Initiator Ready. Asserted when the initiator is ready for data transfer.
TRDY#	W4	B	Target Ready. Asserted when the target is ready for data transfer.
STOP#	Y2	B	Stop. Asserted by the target to request the master to stop the current transaction.
DEVSEL#	Y1	B	Device Select. This signal is driven by the VT82C691 when a PCI initiator is attempting to access main memory. It is an input when the VT82C691 is acting as a PCI initiator.
PAR	W5	B	Parity. A single parity bit is provided over AD[31:0] and C/BE[3:0].
SERR#	Y3	B	System Error. VT82C691 will pulse this signal when it detects a system error condition.
LOCK#	M4	B	Lock. Used to establish, maintain, and release resource lock.
PREQ#	AF3	I	South Bridge Request. This signal comes from the South Bridge. PREQ# is the South Bridge request for the PCI bus.
PGNT#	AE3	O	South Bridge Grant. This signal driven by the VT82C691 to grant PCI access to the South Bridge.
REQ[4:0]#	R4, M1, M3, N2, P2	I	PCI Master Request. PCI master requests for PCI.
GNT[4:0]#	R5, N4, M2, N1, P4	O	PCI Master Grant. Permission is given to the master to use PCI.

Note: Clocking of the PCI interface is performed with PCLK; see the clock pin group at the end of the pin descriptions section for descriptions of the clock input pins.

AGP Bus Interface			
Signal Name	Pin #	I/O	Signal Description
GFRM#	F2	B	Frame (PCI transactions only). Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
GDS0#	K3	B	Bus Strobe 0 (AGP transactions only). Provides timing for 2x data transfer mode on AD[15:0]. The agent that is providing the data drives this signal.
GDS1#	D6	B	Bus Strobe 1 (AGP transactions only). Provides timing for 2x data transfer mode on AD[31:16]. The agent that is providing the data drives this signal.
GD[31:0]	(see pinout tables)	B	Address/Data Bus. The standard AGP/PCI address and data lines. The address is driven with GDS0# and GDS1# assertion for AGP transfers and is driven with GFRM# assertion for PCI transfers.
GBE[3:0]#	F5, G5, K5, L5	B	Command/Byte Enable. AGP: These pins provide command information (different commands than for PCI) driven by the master (graphics controller) when requests are being enqueued using PIPE#. These pins provide valid byte information during AGP write transactions and are driven by the master. The target (this chip) drives these lines to "0000" during the return of AGP read data, but the state of these pins is ignored by the AGP master. PCI: Commands are driven with GFRM# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
GIRDY#	H5	B	Initiator Ready AGP: For write operations, the assertion of this pin indicates that the master is ready to provide <i>all</i> write data for the current transaction. Once this pin is asserted, the master is not allowed to insert wait states. For read operations, the assertion of this pin indicates that the master is ready to transfer a subsequent block of read data. The master is <i>never</i> allowed to insert a wait state during the initial block of a read transaction. However, it may insert wait states after each block transfers. PCI: Asserted when the initiator is ready for data transfer.
GTRDY#	F1	B	Target Ready: AGP: Indicates that the target is ready to provide read data for the entire transaction (when the transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfers on both read and write transactions. PCI: Asserted when the target is ready for data transfer.
GSTOP#	G3	B	Stop (PCI transactions only). Asserted by the target to request the master to stop the current transaction.
GDSEL#	J5	B	Device Select (PCI transactions only). This signal is driven by the VT82C691 when a PCI initiator is attempting to access main memory. It is an input when the VT82C691 is acting as PCI initiator. Not used for AGP cycles.

Note: Clocking of the AGP interface is performed with GCLK; see the clock pin group for descriptions of the clock input pins.

Note: PCB Layout Guidelines (reference from AGP specification)

- Total motherboard trace length 10" max, trace impedance = 65 ohms \pm 15 ohms, minimize signal crosstalk
- Trace lengths within groups matched to within 2 inches or better
 Groups are:
 - GDS0#, GD15-0, GBE1-0#
 - GDS1#, GD31-16, GBE3-2#
 - SBS#, SBA7-0
- Ground isolation should be provided around GDS0# and GDS1# to prevent crosstalk with GD[31:0]. Ideally ground traces should be provided adjacent to GDSn# on the same signal layer, but at a minimum wider spaces should be provided on either side (e.g., 16 mil spaces on either side of GDSn# if GDSn# signal traces are 8 mil).

AGP Bus Interface (continued)			
Signal Name	Pin #	IO	Signal Description
GPIPE#	C6	I	Pipelined Request. Asserted by the master (graphics controller) to indicate that a full-width request is to be enqueued by the target VT82C691. The master enqueues one request each rising edge of GCLK while PIPE# is asserted. When PIPE# is deasserted no new requests are enqueued across the AD bus.
GRBF#	B6	I	Read Buffer Full. Indicates if the master (graphics controller) is ready to accept previously requested low priority read data. When RBF# is asserted, the VT82C691 will not return low priority read data to the master.
SBA[7:0]	B3, A3, A4, B4, A5, B5, C5, A6	I	SideBand Address. Provides an additional bus to pass address and command information from the master (graphics controller) to the target (the VT82C691). These pins are ignored until enabled.
SBS#	C4	I	Sideband Strobe. Provides timing for SBA[7:0] (driven by the master)
ST[2:0]	D7, E7, E6	O	Status (AGP only). Provides information from the arbiter to a master to indicate what it may do. Only valid while GGNT# is asserted. 000 Indicates that previously requested low priority read or flush data is being returned to the master (graphics controller). 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously enqueued write command. 011 Indicates that the master is to provide high priority write data for a previously enqueued write command. 100 Reserved. (arbiter must not issue, may be defined in the future). 101 Reserved. (arbiter must not issue, may be defined in the future). 110 Reserved. (arbiter must not issue, may be defined in the future). 111 Indicates that the master (graphics controller) has been given permission to start a bus transaction. The master may enqueue AGP requests by asserting PIPE# or start a PCI transaction by asserting GFRM#. ST[2:0] are always outputs from the VT82C691 and inputs to the master.
GREQ#	B7	I	Request. Master request for AGP.
GGNT#	C7	O	Grant. Permission is given to the master to use AGP.
GPAR / GCKRUN#	G2	IO O	Rx78[1]=0: AGP Parity. A single parity bit is provided over GD[31:0] and GBE[3:0]. Rx78[1]=1: AGP Clock Run. Used to stop the AGP bus clock to reduce bus power usage.
GSERR# / PCKRUN#	H4	IO O	Rx78[1]=0: AGP System Error. The VT82C691 will pulse this signal when it detects a system error condition. Rx78[1]=1: PCI Clock Run. Used to stop the PCI bus clock to reduce bus power usage.

Note: For PCI operation on the AGP bus, the following pins are not required:

- PERR# (parity and error reporting not required on transient data devices such as graphics controllers)
- LOCK# (no lock requirement on AGP)
- IDSEL (internally connected to AD16 on AGP-compliant masters)

Note: Separate system interrupts are not provided for AGP. The AGP connector provides interrupts via PCI bus INTA-B#.

Note: The AGP bus supports only one master directly (REQ[3:0]# and GNT[3:0]# are not provided). External logic is required to implement additional master capability. Note that the arbitration mechanism on the AGP bus is different from the PCI bus.

Note: A separate reset is not required for the AGP bus (RESET# resets both PCI and AGP buses)

Note: Two mechanisms are provided by the AGP bus to enqueue master requests: PIPE# (to send addresses multiplexed on the AD lines) and the SBA port (to send addresses unmultiplexed). AGP masters implement one or the other or select one at initialization time (they are not allowed to change during runtime). Therefore only one of the two will be used and the signals associated with the other will not be used. Therefore the 691 has an internal pullup on RBF# to maintain it in the de-asserted state in case it is not implemented on the master device.

Clock / Reset Control																		
Signal Name	Pin #	I/O	Signal Description															
HCLK	E16	I	Host Clock. This pin receives the host CPU clock. This clock is used by all VT82C691 logic that is in the host CPU domain. The memory interface logic will also use this clock if selected (memory system timing can alternately be selected to use the AGP bus clock). The CPU clock must lead the AGP clock by 0.2 ± 0.5 nsec.															
MCLKI	D16	I	Memory Clock In.															
MCLKO	D14	O	Memory Clock Out.															
GCLK	E10	I	AGP Clock. This pin receives the AGP bus clock. This clock is used by all VT82C691 logic that is in the AGP clock domain. The AGP clock must be synchronous / pseudo-synchronous to the host CPU clock (selectable as shown in the table below). The CPU clock must lead the AGP clock by 0.2 ± 0.5 nsec.															
PCLK	T5	I	<p>PCI Clock. This pin receives a buffered host clock divided-by-2 or 3. See strapping option on MECC0 (strapping options can be read back in configuration register 68). This clock is used by all of the VT82C691 logic that is in the PCI clock domain. This clock input must be 33 MHz maximum to comply with PCI specification requirements and must be synchronous with the host CPU clock, HCLK, with an HCLK:PCLK frequency ratio of 2:1 or 3:1 as shown in the table below. The host CPU clock must lead the PCI clock by 1.5 ± 0.5 nsec.</p> <p><u>Typical Clock Frequency Combinations</u></p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th><u>Rx68[0]</u></th> <th><u>Mode</u></th> <th><u>Host Clock</u></th> <th><u>AGP Clock</u></th> <th><u>PCI Clock</u></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>2x</td> <td>66 MHz</td> <td>66 MHz</td> <td>33 MHz</td> </tr> <tr> <td>1</td> <td>3x</td> <td>100 MHz</td> <td>66 MHz</td> <td>33 MHz</td> </tr> </tbody> </table>	<u>Rx68[0]</u>	<u>Mode</u>	<u>Host Clock</u>	<u>AGP Clock</u>	<u>PCI Clock</u>	0	2x	66 MHz	66 MHz	33 MHz	1	3x	100 MHz	66 MHz	33 MHz
<u>Rx68[0]</u>	<u>Mode</u>	<u>Host Clock</u>	<u>AGP Clock</u>	<u>PCI Clock</u>														
0	2x	66 MHz	66 MHz	33 MHz														
1	3x	100 MHz	66 MHz	33 MHz														
RESET#	AC3	I	Reset. Input from south bridge chip. When asserted, this signal resets the VT82C691 and sets all register bits to the default value. The same signal that connects to this pin may also be used (connected through an external inverter) to reset the ISA bus (if implemented). The rising edge of this signal is used to sample all power-up strap options (see HA25-27).															
CRSTI#	AC4	I	CPU Reset In. CPU Reset input from south bridge chip.															
CPURST#	D22	O	CPU Reset. CPU Reset output to CPU.															
INIT#	A7	O	CPU Init. Init output to CPU															
SUSCLK	AD6	I	Suspend Clock. For implementation of the Suspend-to-DRAM feature. Ground this pin to disable.															
SUSTAT#	AB6	I	Suspend Status. For implementation of the Suspend-to-DRAM feature. Connect to an external pullup to disable.															
GCKRUN# / GPAR	G2	O IO	AGP Clock Run (Rx78[1]=1). For implementation of AGP bus clock control for very low-power AGP bus operation. Refer to the AGP Specification for additional information.															
PCKRUN# / GSERR#	H4	O IO	PCI Clock Run (Rx78[1]=1). For implementation of PCI bus clock control for very low-power PCI bus operation. Refer to the PCI Mobile Design Guidelines document for additional information.															

Power and Ground			
Signal Name	Pin #	I/O	Signal Description
VCC3	C8, C19, F7-9, F18-F20, H3, H6, H21, H24, J6, J21, L12, L15, M11, M16, R11, R16, T12, T15, V6, V21, W3, W6, W21, W24, AA7-AA9, AA18-AA20, AD8, AD19	P	Power for Internal Logic (3.3V ±5%).
VSUS	U21, AB8	P	Suspend Power (3.3V ±5%). Power for SWEA-D#, RAS[7-0]#, CAS[7-0]#, SUSTAT#, SUSCLK, CKE[7:0]#.
GND	A1, A13, A26, C3, C14, C24, E5, E13-E14, E22, F6, F21, G6, G21, L11, L13-L14, L16, M12-M15, N3, N5, N11-N16, N22, N26, P1, P5, P11-16, P22, P24, R12-R15, T11, T13-T14, T16, Y6, Y21, AA6, AA21, AB5, AB13-AB14, AB22, AD3, AD13, AD24, AF1, AF14, AF26	P	Ground
AVCC	E15, F10	P	Analog Power (3.3V ±5%). For internal clock logic.
AGND	E11, E17	P	Analog Ground. For internal clock logic. Connect to main ground plane.
VTT	E12, F17, K21	P	CPU Interface Termination Voltage (1.5V ±10%).
GTLREF	D12, D23	P	CPU Interface GTL+ Voltage Reference. 2/3 VTT ±2%
5VREF	U6, AA17	P	5V Reference (5V ±5%). Used to provide 5V input tolerance.
MVREF	AC12, AD22	P	DRAM Voltage Reference. 1.5V for SDR SDRAM, 1.0V for DDR SDRAM (±5%)
GVREF	D4	P	AGP Voltage Reference. 0.39 GVCC to 0.41 GVCC. Typical value is 1.32V (0.40 times 3.3V). This can be provided with a resistive divider on GVCC using 270 ohm and 180 ohm (2%) resistors.

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers of the VT82C691. These tables also document the power-on default value (“Default”) and access type (“Acc”) for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), “—” for reserved / used (essentially the same as RO), and RWC (or just WC) (Read / Write 1’s to Clear individual bits). Registers indicated as RW may have some read-only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions following these tables for details). All offset and default values are shown in hexadecimal unless otherwise indicated.

Table 2. VT82C691 Registers

VT82C691 I/O Ports

Port #	I/O Port	Default	Acc
22	PCI / AGP Arbiter Disable	00	RW
CFB-8	Configuration Address	0000 0000	RW
CFF-C	Configuration Data	0000 0000	RW

VT82C691 Device 0 Registers - Host Bridge
Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	0691	RO
5-4	Command	0006	RW
7-6	Status	0290	WC
8	Revision ID	nn	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	06	RO
C	-reserved- (cache line size)	00	—
D	Latency Timer	00	RW
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
13-10	Graphics Aperture Base	0000 0008	RW
14-27	-reserved- (base address registers)	00	—
28-2B	-reserved- (unassigned)	00	—
2D-2C	Subsystem Vendor ID	0000	W1
2F-2E	Subsystem ID	0000	W1
33-30	-reserved- (expan ROM base addr)	00	—
37-34	Capability Pointer	0000 00A0	RO
34-3B	-reserved- (unassigned)	00	—
3C-3D	-reserved- (interrupt line & pin)	00	—
3E-3F	-reserved- (min gnt and max latency)	00	—

Device-Specific Registers

Offset	Host CPU Protocol Control	Default	Acc
50	Host CPU Protocol Control 1	00	RW
51	Host CPU Protocol Control 2	00	RW
52	Dynamic Defer Timer	00	RW
53-55	-reserved- (unassigned)	00	—

Offset	DRAM Control	Default	Acc
59-58	MA Map Type	0000	RW
5A-5F	DRAM Row Ending Address:		
5A	Bank 0 Ending (HA[29:22])	01	RW
5B	Bank 1 Ending (HA[29:22])	01	RW
5C	Bank 2 Ending (HA[29:22])	01	RW
5D	Bank 3 Ending (HA[29:22])	01	RW
5E	Bank 4 Ending (HA[29:22])	01	RW
5F	Bank 5 Ending (HA[29:22])	01	RW
56	Bank 6 Ending (HA[29:22])	01	RW
57	Bank 7 Ending (HA[29:22])	01	RW
60	DRAM Type	00	RW
61	ROM Shadow Control C0000-CFFFF	00	RW
62	ROM Shadow Control D0000-DFFFF	00	RW
63	ROM Shadow Control E0000-FFFFF	00	RW
64	DRAM Timing for Banks 0,1	EC	RW
65	DRAM Timing for Banks 2,3	EC	RW
66	DRAM Timing for Banks 4,5	EC	RW
67	DRAM Timing for Banks 6,7	EC	RW
68	DRAM Control	00	RW
69	DRAM Clock Select	00	RW
6A	DRAM Refresh Counter	00	RW
6B	DRAM Arbitration Control	01	RW
6C	SDRAM Control	00	RW
6D	DRAM Control Drive Strength	00	RW
6E	ECC Control	00	RW
6F	ECC Status	00	RO

Device-Specific Registers (continued)

Offset	PCI Bus Control	Default	Acc
70	PCI Buffer Control	00	RW
71	CPU to PCI Flow Control 1	00	RW
72	CPU to PCI Flow Control 2	00	RW
73	PCI Master Control 1	00	RW
74	PCI Master Control 2	00	RW
75	PCI Arbitration 1	00	RW
76	PCI Arbitration 2	00	RW
77	Chip Test (do not program)	00	RW
78	PMU Control	00	RW
79-7D	-reserved-	00	—
7E-7F	DLL Test Mode (do not program)	00	RW
80-FF	-reserved-	00	—

Offset	GART/TLB Control	Default	Acc
83-80	GART/TLB Control	0000 0000	RW
84	Graphics Aperture Size	00	RW
85-87	-reserved- (unassigned)	00	—
8B-88	Gr. Aperture Translation Table Base	0000 0000	RW
8C-8F	-reserved- (unassigned)	00	—

Offset	AGP Control	Default	Acc
A0	AGP ID	02	RO
A1	AGP Next Item Pointer	00	RO
A2	AGP Specification Revision	10	RO
A3	-reserved- (unassigned)	00	—
A7-A4	AGP Status	0700 0203	RO
AB-A8	AGP Command	0000 0000	RW
AC	AGP Control	00	RW
AD-AF	-reserved- (unassigned)	00	—

Offset	Miscellaneous Control	Default	Acc
B0-EF	-reserved- (unassigned)	00	—
F0-F7	BIOS Scratch Registers	00	RW
F8-FB	-reserved- (unassigned)	00	—
FD-FF	Reserved (do not program)	0000 0000	RW

VT82C691 Device 1 - PCI-to-PCI Bridge
Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	8691	RO
5-4	Command	0007	RW
7-6	Status	0220	WC
8	Revision ID	nn	RO
9	Program Interface	00	RO
A	Sub Class Code	04	RO
B	Base Class Code	06	RO
C	-reserved- (cache line size)	00	—
D	Latency Timer	00	RW
E	Header Type	01	RO
F	Built In Self Test (BIST)	00	RO
10-17	-reserved- (base address registers)	00	—
18	Primary Bus Number	00	RW
19	Secondary Bus Number	00	RW
1A	Subordinate Bus Number	00	RW
1B	-reserved- (secondary latency timer)	00	—
1C	I/O Base	F0	RW
1D	I/O Limit	00	RW
1F-1E	Secondary Status	0000	RO
21-20	Memory Base	FFF0	RW
23-22	Memory Limit (Inclusive)	0000	RW
25-24	Prefetchable Memory Base	FFF0	RW
27-26	Prefetchable Memory Limit	0000	RW
28-3D	-reserved- (unassigned)	00	—
3F-3E	PCI-to-PCI Bridge Control	00	RW

Device-Specific Registers

Offset	PCI Bus #2 Control	Default	Acc
40	CPU-to-PCI Flow Control 1	00	RW
41	CPU-to-PCI Flow Control 2	00	RW
42	PCI Master Control	00	RW
43-4F	-reserved- (unassigned)	00	—

Miscellaneous I/O

One I/O port is defined in the VT82C691: Port 22.

Port 22 – PCI Arbiter Disable.....RW

- 7-2 **Reserved** always reads 0
- 1 **PCI #2 (AGP) Arbiter Disable**
 - 0 Respond to GREQ# signaldefault
 - 1 Do not respond to GREQ# signal
- 0 **PCI #1 Arbiter Disable**
 - 0 Respond to all REQ# signals.....default
 - 1 Do not respond to any REQ# signals, including PREQ#

This port can be enabled for read/write access by setting bit-7 of Device 0 Configuration Register 78.

Configuration Space I/O

All registers in the VT82C691 (listed above) are addressed via the following configuration mechanism:

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

Port CFB-CF8 - Configuration Address..... RW

- 31 **Configuration Space Enable**
 - 0 Disabled..... default
 - 1 Convert configuration data port writes to configuration cycles on the PCI bus

30-24 **Reserved** always reads 0

23-16 PCI Bus Number

Used to choose a specific PCI bus in the system

15-11 Device Number

Used to choose a specific device in the system (devices 0 and 1 are defined for the VT82C691)

10-8 Function Number

Used to choose a specific function if the selected device supports multiple functions (only function 0 is defined for the VT82C691).

7-2 Register Number (also called the "Offset")

Used to select a specific DWORD in the VT82C691 configuration space

1-0 **Fixed** always reads 0

Port CFF-CFC - Configuration Data..... RW

Refer to PCI Bus Specification Version 2.1 for further details on operation of the above configuration registers.

Register Descriptions

Device 0 Header Registers - Host Bridge

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number, function number, and device number equal to zero.

Device 0 Offset 1-0 - Vendor ID.....RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 0 Offset 3-2 - Device ID.....RO

15-0 ID Code (reads 0691h to identify the VT82C691)

Device 0 Offset 5-4 - Command.....RW

- 15-10 Reserved** always reads 0
- 9 Fast Back-to-Back Cycle Enable** RO
 - 0 Fast back-to-back transactions only allowed to the same agentdefault
 - 1 Fast back-to-back transactions allowed to different agents
- 8 SERR# Enable**..... RO
 - 0 SERR# driver disableddefault
 - 1 SERR# driver enabled
 (SERR# is used to report parity errors if bit-6 is set).
- 7 Address / Data Stepping** RO
 - 0 Device never does steppingdefault
 - 1 Device always does stepping
- 6 Parity Error Response**.....RW
 - 0 Ignore parity errors & continuedefault
 - 1 Take normal action on detected parity errors
- 5 VGA Palette Snoop** RO
 - 0 Treat palette accesses normallydefault
 - 1 Don't respond to palette accesses on PCI bus
- 4 Memory Write and Invalidate Command**..... RO
 - 0 Bus masters must use Mem Writedefault
 - 1 Bus masters may generate Mem Write & Inval
- 3 Special Cycle Monitoring** RO
 - 0 Does not monitor special cyclesdefault
 - 1 Monitors special cycles
- 2 Bus Master** RO
 - 0 Never behaves as a bus master
 - 1 Can behave as a bus masterdefault
- 1 Memory Space**..... RO
 - 0 Does not respond to memory space
 - 1 Responds to memory spacedefault
- 0 I/O Space** RO
 - 0 Does not respond to I/O spacedefault
 - 1 Responds to I/O space

Device 0 Offset 7-6 - Status RWC

- 15 Detected Parity Error**
 - 0 No parity error detected default
 - 1 Error detected in either address or data phase. This bit is set even if error response is disabled (command register bit-6).write one to clear
- 14 Signaled System Error (SERR# Asserted)** always reads 0
- 13 Signaled Master Abort**
 - 0 No abort received default
 - 1 Transaction aborted by the master write one to clear
- 12 Received Target Abort**
 - 0 No abort received default
 - 1 Transaction aborted by the target..... write 1 to clear
- 11 Signaled Target Abort**..... always reads 0
 - 0 Target Abort never signaled
- 10-9 DEVSEL# Timing**
 - 00 Fast
 - 01 Medium..... always reads 01
 - 10 Slow
 - 11 Reserved
- 8 Data Parity Error Detected**
 - 0 No data parity error detected default
 - 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and VT82C691 was initiator of the operation in which the error occurred.write one to clear
- 7 Fast Back-to-Back Capable** always reads 1
- 6 Reserved** always reads 0
- 5 66MHz Capable**..... always reads 0
- 4 Supports New Capability list** always reads 1
- 3-0 Reserved** always reads 0

Device 0 Offset 8 - Revision ID RO

7-0 VT82C691 Chip Revision Code

Device 0 Offset 9 - Programming Interface RO

7-0 Interface Identifier always reads 00

Device 0 Offset A - Sub Class Code..... RO

7-0 Sub Class Codereads 00 to indicate Host Bridge

Device 0 Offset B - Base Class Code..... RO

7-0 Base Class Code .. reads 06 to indicate Bridge Device

Device 0 Offset D - Latency Timer RW

Specifies the latency timer value in PCI bus clocks.

- 7-3 Guaranteed Time Slice for CPU**..... default=0
- 2-0 Reserved** (fixed granularity of 8 clks) .. always read 0
Bits 2-1 are writeable but read 0 for PCI specification compatibility. The programmed value may be read back in Offset 75 bits 5-4 (PCI Arbitration 1).

Device 0 Host Bridge Header Registers (continued)

Device 0 Offset E - Header Type.....RO

7-0 Header Type Codereads 00: single function

Device 0 Offset F - Built In Self Test (BIST).....RO

7 BIST Supportedreads 0: no supported functions

6-0 Reserved always reads 0

Device 0 Offset 13-10 - Graphics Aperture Base.....RW

31-28 Upper Programmable Base Address Bits..... def=0

27-20 Lower Programmable Base Address Bits def=0

These bits behave as if hardwired to 0 if the corresponding Graphics Aperture Size register bit (Device 1 Offset 84h) is 0.

27	26	25	24	23	22	21	20	(This Register)
<u>7</u>	<u>6</u>	<u>5</u>	<u>4</u>	<u>3</u>	<u>2</u>	<u>1</u>	<u>0</u>	(Gr Aper Size)
RW	RW	RW	RW	RW	RW	RW	RW	1M
RW	RW	RW	RW	RW	RW	RW	0	2M
RW	RW	RW	RW	RW	RW	0	0	4M
RW	RW	RW	RW	RW	0	0	0	8M
RW	RW	RW	RW	0	0	0	0	16M
RW	RW	RW	0	0	0	0	0	32M
RW	RW	0	0	0	0	0	0	64M
RW	0	0	0	0	0	0	0	128M
0	0	0	0	0	0	0	0	256M

19-0 Reserved always reads 00008

Note: The locations in the address range defined by this register are prefetchable.

Device 0 Offset 2D-2C – Subsystem Vendor ID R/W1

15-0 Subsystem Vendor ID..... default = 0
This register may be written once and is then read only.

Device 0 Offset 2F-2E – Subsystem ID..... R/W1

15-0 Subsystem ID default = 0
This register may be written once and is then read only.

Device 0 Offset 37-34 - Capability Pointer RO

Contains an offset from the start of configuration space.

31-0 AGP Capability List Pointer always reads A0h

Device 0 Configuration Registers - Host Bridge

These registers are normally programmed once at system initialization time.

Host CPU Control

Device 0 Offset 50 – Host CPU Protocol Control 1RW

- 7 CPU Hardwired IOQ (In Order Queue) Size**
Default per strap on pin MECC3 / CKE3. During reset, HA7 is driven low if MECC3 is sampled low. This register can be written 0 to restrict the chip to one level of IOQ.
0 1-Level
1 4-Level
- 6 Read-Around-Write**
0 Disabledefault
1 Enable
- 5 I/O Write Deferable**
0 Disabledefault
1 Enable
- 4 Defer Retry When HLOCK Active**
0 Disabledefault
1 Enable
- 3 CPU Read PCI Retry**
0 Disabledefault
1 Enable
- 2 CPU Read PCI Deferred**
0 Disabledefault
1 Enable
- 1 CPU Read DRAM Timing**
0 Start DRAM access after snoop phase complete.....default
1 Start DRAM access before snoop phase complete
- 0 PCI Master Read DRAM Timing**
0 Start DRAM access after snoop phase complete.....default
1 Start DRAM access before snoop phase complete

Device 0 Offset 51 – Host CPU Protocol Control 2..... RW

- 7 CPU Read DRAM 0ws for Back-to-Back Read Transactions**
0 Disable..... default
1 Enable
Setting this bit enables maximum read performance by allowing continuous 0 wait state reads for pipelined line reads. If this bit is not set, there will be at least 1T idle time between read transactions.
- 6 CPU Write DRAM 0ws for Back-to-Back Write Transactions**
0 Disable..... default
1 Enable
Setting this bit enables maximum write performance by allowing continuous 0 wait state writes for pipelined line writes and sustained 3T single writes. If this bit is not set, there will be at least 1T idle time between write transactions.
- 5 DRAM Read Request Rate**
0 3T default
1 2T
- 4 Reserved (Do Not Program) default = 0**
- 3 Reserved (Do Not Program) default = 0**
- 2 CPU Read DRAM Prefetch Buffer Depth**
0 1-level prefetch buffer default
1 4-level prefetch buffer
- 1 CPU-to-DRAM Post-Write Buffer Depth**
0 1-level post-write buffer default
1 4-level post-write buffer
- 0 Concurrent PCI Master / Host Operation**
0 Disable (CPU bus will be occupied (BPRI asserted) during the entire PCI operation period) default
1 Enable (CPU bus is only requested before ADS# assertion)

Device 0 Offset 52 – Dynamic Defer Time RW

- 7 GTL I/O Buffer Pullup default = MECC4 Strap**
0 Disable
1 Enable
The default value of this bit is determined by a strap on the MECC4 pin during reset.
- 6-5 Reserved always reads 0**
- 4-0 Snoop Stall Count**
00 Disable dynamic defer default
1-1F Snoop stall count

DRAM Control

These registers are normally set at system initialization time and not accessed after that during normal system operation. Some of these registers, however, may need to be programmed using specific sequences during power-up initialization to properly detect the type and size of installed memory (refer to the VIA Technologies 82C691 BIOS porting guide for details).

Table 3. System Memory Map

Space	Start	Size	Address Range	Comment
DOS	0	640K	00000000-0009FFFF	Cacheable
VGA	640K	128K	000A0000-000BFFFF	Used for SMM
BIOS	768K	16K	000C0000-000C3FFF	Shadow Ctrl 1
BIOS	784K	16K	000C4000-000C7FFF	Shadow Ctrl 1
BIOS	800K	16K	000C8000-000CBFFF	Shadow Ctrl 1
BIOS	816K	16K	000CC000-000CFFFF	Shadow Ctrl 1
BIOS	832K	16K	000D0000-000D3FFF	Shadow Ctrl 2
BIOS	848K	16K	000D4000-000D7FFF	Shadow Ctrl 2
BIOS	864K	16K	000D8000-000DBFFF	Shadow Ctrl 2
BIOS	880K	16K	000DC000-000DFFFF	Shadow Ctrl 2
BIOS	896K	64K	000E0000-000EFFFF	Shadow Ctrl 3
BIOS	960K	64K	000F0000-000FFFFF	Shadow Ctrl 3
Sys	1MB	—	00100000-DRAM Top	Can have hole
Bus	D Top		DRAM Top-FFFEFFFF	
Init	4G-64K	64K	FFFEFFFF-FFFFFFFF	000Fxxxx alias

Device 0 Offset 59-58 - DRAM MA Map Type.....RW

- 15-13 Bank 5/4 MA Map Type (EDO/FPG)**
 - 000 8-bit Column Address
 - 001 9-bit Column Address
 - 010 10-bit Column Addressdefault
 - 011 11-bit Column Address
 - 100 12-bit Column Address (64Mb)
 - 101 Reserved
 - 11x Reserved
- Bank 5/4 MA Map Type (SDRAM)**
 - 0xx 16Mbit SDRAM.....default
 - 100 64Mbit SDRAM (x4, x8, x16, 4-bank x32)
 - 101 Reserved
 - 11x Reserved
- 12 Bank 5/4 Virtual Channel Enable..... default=0**
- 11-9 Bank 7/6 MA Map Type (see above)**
- 8 Bank 7/6 Virtual Channel Enable..... default=0**
- 7-5 Bank 1/0 MA Map Type (see above)**
- 4 Bank 1/0 Virtual Channel Enable..... default=0**
- 3-1 Bank 3/2 MA Map Type (see above)**
- 0 Bank 3/2 Virtual Channel Enable..... default=0**

Device 0 Offset 5A-5F – DRAM Row Ending Address:

All of the registers in this group default to 01h:

- Offset 5A – Bank 0 Ending (HA[30:23])..... RW**
- Offset 5B – Bank 1 Ending (HA[30:23])..... RW**
- Offset 5C – Bank 2 Ending (HA[30:23])..... RW**
- Offset 5D – Bank 3 Ending (HA[30:23])..... RW**
- Offset 5E – Bank 4 Ending (HA[30:23])..... RW**
- Offset 5F – Bank 5 Ending (HA[30:23])..... RW**
- Offset 56 – Bank 6 Ending (HA[30:23])..... RW**
- Offset 57 – Bank 7 Ending (HA[30:23])..... RW**

Note : BIOS is required to fill the ending address registers for all banks even if no memory is populated. The endings have to be in incremental order.

Device 0 Offset 60 – DRAM Type RW

- 7-6 DRAM Type for Bank 7/6**
 - 00 Fast Page Mode DRAM (FPG)..... default
 - 01 EDO DRAM (EDO)
 - 10 SDRAM Double Data Rate (DDR SDRAM-II)
 - 11 SDRAM Single Data Rate (SDR SDRAM)
- 5-4 DRAM Type for Bank 5/4.....default=FPG**
- 3-2 DRAM Type for Bank 3/2.....default=FPG**
- 1-0 DRAM Type for Bank 1/0.....default=FPG**

Table 4. Memory Address Mapping Table

EDO/FP DRAM

MA:	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
8-bit Col (000)		23	22	21	11	20	19	18	17	16	15	14	13	12	Row Bits Col Bits
9-bit Col (001)		24	23	22	21	20	19	18	17	16	15	14	13	12	Row Bits Col Bits
10-bit Col (010)		25	24	23	21	20	19	18	17	16	15	14	13	12	Row Bits Col Bits
11-bit Col (011)		26	25	23	21	20	19	18	17	16	15	14	13	12	Row Bits Col Bits
12-bit Col (100)		27	25	23	21	20	19	18	17	16	15	14	13	12	Row Bits Col Bits

SDRAM

MA:	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
16Mb (0xx)			11	11	PC	24	23	10	9	8	7	6	5	4	3	Row Bits Col Bits
64Mb (100) 2/4 bank x4, x8, x16; 4-bank x32	24	13	12	22	21	20	19	18	17	16	15	14	11	23	x4: 10 col x8: 9 col x16: 8 col x32: 8 col	

"PC" = "Precharge Control" (refer to SDRAM specifications)

16Mb 11x10, 11x9, and 11x8 configurations supported

64Mb x4: 12x10 4bank, 13x10 2bank
x8: 12x9 4bank, 13x9 2bank
x16: 12x8 4bank, 13x8 2bank
x32: 11x8 4bank

Device 0 Offset 61 - Shadow RAM Control 1RW

- 7-6 CC000h-CFFFFh**
 - 00 Read/write disabledefault
 - 01 Write enable
 - 10 Read enable
 - 11 Read/write enable
- 5-4 C8000h-CBFFFh**
 - 00 Read/write disabledefault
 - 01 Write enable
 - 10 Read enable
 - 11 Read/write enable
- 3-2 C4000h-C7FFFh**
 - 00 Read/write disabledefault
 - 01 Write enable
 - 10 Read enable
 - 11 Read/write enable
- 1-0 C0000h-C3FFFh**
 - 00 Read/write disabledefault
 - 01 Write enable
 - 10 Read enable
 - 11 Read/write enable

Device 0 Offset 62 - Shadow RAM Control 2RW

- 7-6 DC000h-DFFFFh**
 - 00 Read/write disabledefault
 - 01 Write enable
 - 10 Read enable
 - 11 Read/write enable
- 5-4 D8000h-DBFFFh**
 - 00 Read/write disabledefault
 - 01 Write enable
 - 10 Read enable
 - 11 Read/write enable
- 3-2 D4000h-D7FFFh**
 - 00 Read/write disabledefault
 - 01 Write enable
 - 10 Read enable
 - 11 Read/write enable
- 1-0 D0000h-D3FFFh**
 - 00 Read/write disabledefault
 - 01 Write enable
 - 10 Read enable
 - 11 Read/write enable

Device 0 Offset 63 - Shadow RAM Control 3..... RW

- 7-6 E0000h-EFFFFh**
 - 00 Read/write disable default
 - 01 Write enable
 - 10 Read enable
 - 11 Read/write enable
- 5-4 F0000h-FFFFFFh**
 - 00 Read/write disable default
 - 01 Write enable
 - 10 Read enable
 - 11 Read/write enable
- 3-2 Memory Hole**
 - 00 None default
 - 01 512K-640K
 - 10 15M-16M (1M)
 - 11 14M-16M (2M)
- 1-0 SMI Mapping Control**

	<u>SMM</u>		<u>Non-SMM</u>	
	<u>Code</u>	<u>Data</u>	<u>Code</u>	<u>Data</u>
00	DRAM	DRAM	PCI	PCI
01	DRAM	DRAM	DRAM	DRAM
10	Invalid	Invalid	DRAM	PCI
11	DRAM	DRAM	Invalid	Invalid

Device 0 Offset 64 - DRAM Timing for Banks 0,1RW

Device 0 Offset 65 - DRAM Timing for Banks 2,3RW

Device 0 Offset 66 - DRAM Timing for Banks 4,5RW

Device 0 Offset 67 - DRAM Timing for Banks 6,7RW

FPG / EDO Settings for Registers 64-67

- 7 RAS Precharge Time**
 - 0 3T
 - 1 4Tdefault
- 6 RAS Pulse Width**
 - 0 4T
 - 1 5Tdefault
- 5-4 CAS Read Pulse Width**
 - 00 1T
 - 01 2T
 - 10 3Tdefault
 - 11 4T

Note: EDO will not automatically reduce the CAS pulse width. For EDO type DRAMs, use 00 if CAS width = 1 is to be used.
- 3 CAS Write Pulse Width**
 - 0 1T
 - 1 2Tdefault
- 2 MA-to-CAS Delay**
 - 0 1T
 - 1 2Tdefault
- 1 RAS to MA Delay**
 - 0 1Tdefault
 - 1 2T
- 0 Reserved** always reads 0

SDRAM Settings for Registers 64-67

- 7 Precharge Command to Active Command Period**
 - 0 TRP = 2T
 - 1 TRP = 3T default
- 6 Active Command to Precharge Command Period**
 - 0 TRAS = 5T
 - 1 TRAS = 6T default
- 5-4 CAS Latency**

	<u>SDRAM</u>	<u>SDRAM-II</u>
00	1T	n/a
01	2T	n/a
10	3T	2T, 2.5T default
11	n/a	3T
- 3 DDR Write Enable (SDRAM-II Only)**
 - 0 Disable
 - 1 Enable default
- 2 ACTIVE Command to CMD Command Period**
 - 0 2T
 - 1 3T default
- 1-0 Bank Interleave**
 - 00 No Interleave default
 - 01 2-way
 - 10 4-way
 - 11 Reserved

Device 0 Offset 68 - DRAM Control.....RW

- 7 SDRAM Open Page Control**
 - 0 Always precharge SDRAM banks when accessing EDO/FPG DRAMs.....default
 - 1 SDRAM banks remain active when accessing EDO/FPG banks
- 6 Bank Page Control**
 - 0 Allow only pages of the same bank active... def
 - 1 Allow pages of different banks to be active
- 5 EDO Pipeline Burst Rate**
 - 0 X-2-2-2-2-2-2-2.....default
 - 1 X-2-2-2-3-2-2-2
- 4 Reserved (do not program)..... default = 0**
- 3 EDO Test Mode**
 - 0 Disabledefault
 - 1 Enable
- 2 Burst Refresh**
 - 0 Disabledefault
 - 1 Enable (burst 4 times)
- 1 Reserved always reads 0**
- 0 System Frequency Divider RO**
 - 0 CPU/PCI Frequency Ratio = 2x (66 MHz)
 - 1 CPU/PCI Frequency Ratio = 3x (100 MHz)

This bit is latched from MECC0 at the rising edge of RESET#.

Note: MD0 is internally pulled up for EDO detection.

Device 0 Offset 69 – DRAM Clock Select.....RW

- 7 DRAM Operating Frequency RO**
 - 0 Same as CPU Frequency (66/100 MHz)
 - 1 Same as AGP Frequency (66 MHz)

This bit is latched from MECC2 at the rising edge of RESET#.
- 6-0 Reserved always reads 0**

Device 0 Offset 6A - Refresh Counter RW

- 7-0 Refresh Counter (in units of 16 CPUCLKs)**
 - 00 DRAM Refresh Disabled..... default
 - 01 32 CPUCLKs
 - 02 48 CPUCLKs
 - 03 64 CPUCLKs
 - 04 80 CPUCLKs
 - 05 96 CPUCLKs
 -

The programmed value is the desired number of 16-CPUCLK units minus one.

Device 0 Offset 6B - DRAM Arbitration Control..... RW

- 7-6 Arbitration Parking Policy**
 - 00 Park at last bus owner default
 - 01 Park at CPU side
 - 10 Park at AGP side
 - 11 Reserved
- 5-4 Reserved always reads 0**
- 3-1 Suspend Refresh Rate**
 - 000 Refresh disable
 - 001 15.6 usec
 - 010 31.2 usec
 - 011 64.4 usec
 - 100 125 usec
 - 101 256 usec
 - 110 Reserved
 - 111 Reserved

- 0 Multi-Page Open**
 - 0 Disable (page registers marked invalid and no page register update which causes non page-mode operation)
 - 1 Enable default

Device 0 Offset 6C - SDRAM Control.....RW

- 7 **Reserved (Do Not Program)**..... must be 0
- 6 **DRAM Start Cycle**
 - 0 Concurrent with cache hit detection
(for 66MHz operation)default
 - 1 After cache hit detection
(for 100MHz operation)
- 5 **MD-to-HD Pop**
 - 0 Normaldefault
 - 1 Add 1T latency to improve MD setup time at
100 MHz
- 4 **DDR Write-to-Read Turnaround**
 - 0 1T Turnaround (i.e., 3T from Write command
to Read command)default
 - 1 2T Turnaround
- 3 **Single RW Burst Stop Command**
 - 0 Disabledefault
 - 1 Enable BST command to SDRAM to allow
fast single-cycle pipeline
- 2-0 **SDRAM Operation Mode Select**
 - 000 Normal SDRAM Modedefault
 - 001 NOP Command Enable
 - 010 All-Banks-Precharge Command Enable
(CPU-to-DRAM cycles are converted
to All-Banks-Precharge commands).
 - 011 MSR Enable
CPU-to-DRAM cycles are converted to
commands and the commands are driven on
MA[13:0]. The BIOS selects an appropriate
host address for each row of memory such that
the right commands are generated on
MA[13:0].
 - 100 CBR Cycle Enable (if this code is selected,
CAS-before-RAS refresh is used; if it is not
selected, RAS-Only refresh is used)
 - 101 Reserved
 - 11x Reserved

Device 0 Offset 6D - DRAM Drive Strength..... RW

- 7 **MAB Output Disable**
 - 0 Banks 0-3 use MAA; banks 4-7 use MAB... def
 - 1 Disable MAB (all memory banks use MAA)
- 6-5 **Delay DRAM Read Latch**
 - 00 Disable default
 - 01 0.5 ns
 - 10 1.0 ns
 - 11 2.0 ns
- 4 **MD Drive**
 - 0 8 mA default
 - 1 6 mA
- 3 **SDRAM Command Drive (SRAS#, SCAS#, SWE#)**
 - 0 16mA default
 - 1 24mA
- 2 **MA[2:13] / WE# Drive**
 - 0 16mA default
 - 1 24mA
- 1 **CAS# Drive**
 - 0 8 mA default
 - 1 12 mA
- 0 **RAS# Drive**
 - 0 16mA default
 - 1 24mA

Device 0 Offset 6E - ECC ControlRW

- 7 ECC / ECMode Select**
 - 0 ECC Checking and Reportingdefault
 - 1 ECC Checking, Reporting, and Correcting
- 6 Reserved** always reads 0
- 5 Enable SERR# on ECC / EC Multi-Bit Error**
 - 0 Don't assert SERR# for multi-bit errors..... def
 - 1 Assert SERR# for multi-bit errors
- 4 Enable SERR# on ECC / EC Single-Bit Error**
 - 0 Don't assert SERR# for single-bit errors..... def
 - 1 Assert SERR# for single-bit errors
- 3 Reserved** always reads 0
- 2 ECC / EC Enable - Bank 5/4 (DIMM 2)**
 - 0 Disable (no ECC or EC for banks 5/4)...default
 - 1 Enable (ECC or EC per bit-7)
- 1 ECC / EC Enable - Bank 3/2 (DIMM 1)**
 - 0 Disable (no ECC or EC for banks 3/2)...default
 - 1 Enable (ECC or EC per bit-7)
- 0 ECC / EC Enable - Bank 1/0 (DIMM 0)**
 - 0 Disable (no ECC or EC for banks 1/0)...default
 - 1 Enable (ECC or EC per bit-7)

Device 0 Offset 6F - ECC Status..... RWC

- 7 Multi-bit Error Detected.....** write of '1' resets
- 6-4 Multi-bit Error DRAM Bank.....** default=0
Encoded value of the bank with the multi-bit error.
- 3 Single-bit Error Detected.....** write of '1' resets
- 2-0 Single-bit Error DRAM Bank** default=0
Encoded value of the bank with the single-bit error.

Error checking / correction may be enabled bank-pair by bank-pair (DIMM by DIMM) by using bits 0-2 above. Bank pairs must be populated with 72-bit memory to enable for EC or ECC since the additional data bits must be present in either case. For this reason, if 64-bit memory is populated in a particular bank pair, the corresponding bit 0-2 should be set to 0 to disable both EC and ECC for that bank pair. For those bank pairs that have 72-bit memory available (and have the corresponding bit 0-2 set), either EC or ECC may be selected via bit-7 above (i.e., all enabled bank pairs will use EC or all will use ECC).

If error checking / reporting only (EC) is selected, all read and write cycles will use normal timing. Partial writes (with EC or ECC enabled) will use read-modify-write cycles to maintain correct error correction codes in the additional 8 data bits. If EC and ECC are disabled for a particular bank pair, partial writes to that bank pair will use the byte enables to write only the selected bytes (using normal write cycles and cycle timing). If error correction (ECC) is selected, the first read of a transaction will always have one additional cycle of latency.

<u>Bit-7</u>	<u>Bits 2-0</u>	<u>RMW</u>	<u>Error Checking</u>	<u>Error Correction</u>
0/1	0	No	No	No
0	1	Yes	Yes	No
1	1	Yes	Yes	Yes

PCI Bus #1 Control

These registers are normally programmed once at system initialization time.

Device 0 Offset 70 - PCI Buffer ControlRW

- 7 CPU to PCI Post-Write**
 - 0 Disabledefault
 - 1 Enable
- 6 PCI Master to DRAM Post-Write**
 - 0 Disabledefault
 - 1 Enable
- 5 Reserved (No Function) default = 0**
- 4 PCI Master to DRAM Prefetch**
 - 0 Disabledefault
 - 1 Enable
- 3 CPU-to-PCI Buffer Available Cycle Reduction**
 - 0 Normal operationdefault
 - 1 Reduce 1 cycle when the CPU-to-PCI buffer becomes available after being full (PCI and AGP buses)
- 2 PCI Master Read Caching**
 - 0 Disabledefault
 - 1 Enable
- 1 Delay Transaction**
 - 0 Disabledefault
 - 1 Enable
- 0 Slave Device Stopped Idle Cycle Reduction**
 - 0 Normal Operation.....default
 - 1 Reduce 1 PCI idle cycle when stopped by a slave device (PCI and AGP buses)

Device 0 Offset 71 - CPU to PCI Flow Control 1..... RW

- 7 Dynamic Burst**
 - 0 Disable..... default
 - 1 Enable (see note under bit-3 below)
- 6 Byte Merge**
 - 0 Disable..... default
 - 1 Enable
- 5 Reserved (do not program) default = 0**
- 4 PCI I/O Cycle Post Write**
 - 0 Disable..... default
 - 1 Enable
- 3 PCI Burst**
 - 0 Disable..... default
 - 1 Enable (bit7=1 will override this option)
- bit-7 bit-3 Operation**
 - 0 0 Every write goes into the write buffer and no PCI burst operations occur.
 - 0 1 If the write transaction is a burst transaction, the information goes into the write buffer and burst transfers are later performed on the PCI bus. If the transaction is not a burst, PCI write occurs immediately (after a write buffer flush).
 - 1 x Every write transaction goes to the write buffer; burstable transactions will then burst on the PCI bus and non-burstable won't. This is the normal setting.
- 2 PCI Fast Back-to-Back Write**
 - 0 Disable..... default
 - 1 Enable
- 1 Quick Frame Generation**
 - 0 Disable..... default
 - 1 Enable
- 0 1 Wait State PCI Cycles**
 - 0 Disable..... default
 - 1 Enable

Device 0 Offset 72 - CPU to PCI Flow Control 2.....RWC

- 7 Retry Status**
 - 0 Retry occurred less than retry limitdefault
 - 1 Retry occurred more than x times (where x is defined by bits 5-4) **write 1 to clear**
- 6 Retry Timeout Action**
 - 0 Retry Forever (record status only).....default
 - 1 Flush buffer for write or return all 1s for read
- 5-4 Retry Limit**
 - 00 Retry 2 timesdefault
 - 01 Retry 16 times
 - 10 Retry 4 times
 - 11 Retry 64 times
- 3 Clear Failed Data and Continue Retry**
 - 0 Flush the entire post-write bufferdefault
 - 1 When data is posting and master (or target) abort fails, pop the failed data if any, and keep posting
- 2 CPU Backoff on PCI Read Retry Failure**
 - 0 Disabledefault
 - 1 Backoff CPU when reading data from PCI and retry fails
- 1 Reduce 1T for FRAME# Generation**
 - 0 Disabledefault
 - 1 Enable
- 0 Reserved** (do not program)..... default = 0

Device 0 Offset 73 - PCI Master Control 1..... RW

- 7 Reserved** always reads 0
- 6 PCI Master 1-Wait-State Write**
 - 0 Zero wait state TRDY# response default
 - 1 One wait state TRDY# response
- 5 PCI Master 1-Wait-State Read**
 - 0 Zero wait state TRDY# response default
 - 1 One wait state TRDY# response
- 4 Reserved (Do Not Program)** default = 0
- 3 Assert STOP# after PCI Master Write Timeout**
 - 0 Disable default
 - 1 Enable
- 2 Assert STOP# after PCI Master Read Timeout**
 - 0 Disable default
 - 1 Enable
- 1 LOCK# Function**
 - 0 Disable default
 - 1 Enable
- 0 PCI Master Broken Timer Enable**
 - 0 Disable default
 - 1 Enable. Force into arbitration when there is no FRAME# 16 PCICLK's after the grant.

Device 0 Offset 74 - PCI Master Control 2..... RW

- 7 PCI Master Read Prefetch by Enhance Command**
 - 0 Always Prefetch default
 - 1 Prefetch only if Enhance command
- 6 PCI Master Write Merge**
 - 0 Disable default
 - 1 Enable
- 5-0 Reserved** always reads 0

Device 0 Offset 75 - PCI Arbitration 1RW

- 7 Arbitration Mechanism**
 - 0 PCI has prioritydefault
 - 1 Fair arbitration between PCI and CPU
- 6 Arbitration Mode**
 - 0 REQ-based (arbitrate at end of REQ#)...default
 - 1 Frame-based (arbitrate at FRAME# assertion)
- 5-4 Latency Timer** read only, reads Rx0D bits 2:1
- 3-0 PCI Master Bus Time-Out**
(force into arbitration after a period of time)
 - 0000 Disabledefault
 - 0001 1x32 PCICLKs
 - 0010 2x32 PCICLKs
 - 0011 3x32 PCICLKs
 - 0100 4x32 PCICLKs
 -
 - 1111 15x32 PCICLKs

Device 0 Offset 76 - PCI Arbitration 2RW

- 7 PCI #2 Master Access PCI #1 Retry Disconnect**
 - 0 Disable (PCI #2 will not be disconnected until access finishes).....default
 - 1 Enable (PCI #2 will be disconnected if max retries are attempted without success)
- 6 CPU Latency Timer Bit-0**..... RO
 - 0 CPU has at least 1 PCLK time slot when CPU has PCI bus
 - 1 CPU has no time slot
- 5-4 Master Priority Rotation Control**
 - 00 Disabled (arbitration per Rx75 bit-7)default
 - 01 Grant to CPU after every PCI master grant
 - 10 Grant to CPU after every 2 PCI master grants
 - 11 Grant to CPU after every 3 PCI master grants

With setting 01, the CPU will always be granted access after the current bus master completes, no matter how many PCI masters are requesting. With setting 10, if other PCI masters are requesting during the current PCI master grant, the highest priority master will get the bus after the current master completes, but the CPU will be guaranteed to get the bus after that master completes. With setting 11, if other PCI masters are requesting, the highest priority will get the bus next, then the next highest priority will get the bus, then the CPU will get the bus. In other words, with the above settings, even if multiple PCI masters are continuously requesting the bus, the CPU is guaranteed to get access after every master grant (01), after every other master grant (10) or after every third master grant (11).
- 3-0 Reserved** always reads 0

Device 0 Offset 77 - Chip Test ModeRW

- 7-6 Reserved (no function)**..... always reads 0
- 5-0 Reserved (do not use)**..... default=0

Device 0 Offset 78 - PMU Control..... RW

- 7 I/O Port 22 Access**
 - 0 CPU access to I/O address 22h is passed on to the PCI bus default
 - 1 CPU access to I/O address 22h is processed internally
- 6 Suspend Refresh Type**
 - 0 CBR Refresh..... default
 - 1 Self Refresh
- 5 Normal Refresh**
 - 0 Normal refresh using HCLK..... default
 - 1 Suspend refresh using SUSCLK
- 4 Dynamic Clock Control**
 - 0 Normal (clock is always running) default
 - 1 Clock to various internal functional blocks is disabled when those blocks are not being used
- 3 GCKRUN# De-assertion**
 - 0 GCKRUN# always low..... default
 - 1 GCKRUN# could be high due to PCKRUN#
- 2 Reserved**always reads 0
- 1 PCKRUN# / GCKRUN# Pin Control**
 - 0 Disable (pins are GPAR & GSERR#) ... default
 - 1 Enable (pins are GCKRUN# and PCKRUN#)
- 0 Memory Clock Enable (CKE) Function**
 - 0 CKE Disable (pins used for MECC)..... default
 - 1 CKE Enable (pins used for CKE# signals)

Device 0 Offset 7E – DLL Test Mode..... RW

- 7-6 Reserved (status)**RO
- 5-0 Reserved (do not use)** default=0

Device 0 Offset 7F – DLL Test Mode..... RW

- 7-0 Reserved (do not use)** default=0

GART / Graphics Aperture Control

The function of the Graphics Address Relocation Table (GART) is to translate virtual 32-bit addresses issued by an AGP device into 4K-page based physical addresses for system memory access. In this translation, the upper 20 bits (A31-A12) are remapped, while the lower 12 address bits (A11-A0) are used unchanged.

A one-level fully associative lookup scheme is used to implement the address translation. In this scheme, the upper 20 bits of the virtual address are used to point to an entry in a page table located in system memory. Each page table entry contains the upper 20 bits of a physical address (a "physical page" address). For simplicity, each page table entry is 4 bytes. The total size of the page table depends on the GART range (called the "aperture size") which is programmable in the VT82C691.

This scheme is shown in the figure below.

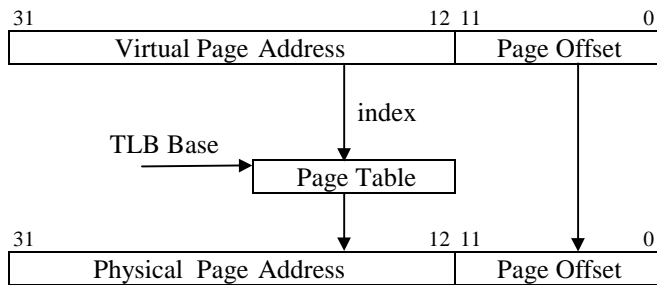


Figure 5. Graphics Aperture Address Translation

Since address translation using the above scheme requires an access to system memory, an on-chip cache (called a "Translation Lookaside Buffer" or TLB) is utilized to enhance performance. The TLB in the 82C691 contains 16 entries. Address "misses" in the TLB require an access of system memory to retrieve translation data. Entries in the TLB are replaced using an LRU (Least Recently Used) algorithm.

Addresses are translated only for accesses within the "Graphics Aperture" (GA). The Graphics Aperture can be any power of two in size from 1MB to 256MB (i.e., 1MB, 2MB, 4MB, 8MB, etc). The base of the Graphics Aperture can be anywhere in the system virtual address space on an address boundary determined by the aperture size (e.g., if the aperture size is 4MB, the base must be on a 4MB address boundary). The Graphics Aperture Base is defined in register offset 10 of device 0. The Graphics Aperture Size and TLB Table Base are defined in the following register group (offsets 84 and 88 respectively) along with various control bits.

Device 0 Offset 83-80 - GART/TLB Control.....RW

- 31-16 Reserved always reads 0
- 15-8 Reserved (test mode status)..... RO
- 7 **Flush Page TLB**
 - 0 Disabledefault
 - 1 Enable
- 6-4 **Reserved (always program to 0) RW**
- 3 **PCI#1 Master Address Translation for GA Access**
 - 0 Addresses generated by PCI #1 Master accesses of the Graphics Aperture will not be translateddefault
 - 1 PCI #1 Master GA addresses will be translated
- 2 **PCI#2 Master Address Translation for GA Access**
 - 0 Addresses generated by PCI #2 Master accesses of the Graphics Aperture will not be translateddefault
 - 1 PCI #2 Master GA addresses will be translated
- 1 **CPU Address Translation for GA Access**
 - 0 Addresses generated by CPU accesses of the Graphics Aperture will not be translated..... def
 - 1 CPU GA addresses will be translated
- 0 **AGP Address Translation for GA Access**
 - 0 Addresses generated by AGP accesses of the Graphics Aperture will not be translated..... def
 - 1 AGP GA addresses will be translated

Note: For any master access to the Graphics Aperture range, snoop will not be performed.

Device 0 Offset 84 - Graphics Aperture Size..... RW

- 7-0 **Graphics Aperture Size**
 - 11111111 1M
 - 11111110 2M
 - 11111100 4M
 - 11111000 8M
 - 11110000 16M
 - 11100000 32M
 - 11000000 64M
 - 10000000 128M
 - 00000000 256M
- 3-0 **Reserved** always reads 0

Offset 8B-88 - GA Translation Table Base..... RW

- 31-12 **Graphics Aperture Translation Table Base.**
Pointer to the base of the translation table in system memory used to map addresses in the aperture range (the pointer to the base of the "Directory" table).
- 11-3 **Reserved** always reads 0
- 2 **PCI Master Directly Accesses DRAM if in GART Range**
 - 0 Disable..... default
 - 1 Enable
- 1 **Graphics Aperture Enable**
 - 0 Disable..... default
 - 1 Enable

Note: To disable the Graphics Aperture, set this bit to 0 and set all bits of the Graphics Aperture Size to 0. To enable the Graphics Aperture, set this bit to 1 and program the Graphics Aperture Size to the desired aperture size.

- 0 **Translation Table Noncachable**
 - 0 Cachable default
 - 1 Non-cachable

Note: Setting this bit will make the address range programmed in bits 31-12 of this register non-cachable to L1/L2 with the following bits masked per the Graphics Aperture Size (offset 84 described above):

- Address bit 17 masked if Size bit-7 = 0
- Address bit 16 masked if Size bit-6 = 0
- Address bit 15 masked if Size bit-5 = 0
- Address bit 14 masked if Size bit-4 = 0
- Address bit 13 masked if Size bit-3 = 0
- Address bit 12 masked if Size bit-2 = 0
- Address bit 11 masked if Size bit-1 = 0
- Address bit 10 masked if Size bit-0 = 0

Note: If TLB miss, the TLB table is fetched by the address:

Gr Ap Trans Table Base [31:12] + A[27:22], A[21:12], 2'b00

AGP Control

Device 0 Offset A3-A0 - AGP Capability IdentifierRO

- 31-24 Reserved** always reads 00
- 23-20 Major Specification Revision** always reads 0001
Major revision # of AGP spec device conforms to
- 19-16 Minor Specification Revision** always reads 0000
Minor revision # of AGP spec device conforms to
- 15-8 Pointer to Next Item**..... always reads 00 (last item)
- 7-0 AGP ID** .. (always reads 02 to indicate it is AGP)

Device 0 Offset A7-A4 - AGP Status.....RO

- 31-24 Maximum AGP Requests** always reads 07
Max # of AGP requests the device can manage (8)
- 23-10 Reserved**always reads 0s
- 9 Supports SideBand Addressing** always reads 1
- 8-2 Reserved**always reads 0s
- 1 2X Rate Supported**
Value returned can be programmed by writing to RxAC[3]
- 0 1X Rate Supported**..... always reads 1

Device 0 Offset AB-A8 - AGP Command RW

- 31-24 Request Depth** (reserved for target).. always reads 0s
- 23-10 Reserved** always reads 0s
- 9 SideBand Addressing Enable**
0 Disable..... default
1 Enable
- 8 AGP Enable**
0 Disable..... default
1 Enable
- 7-2 Reserved** always reads 0s
- 1 2X Mode Enable**
0 Disable..... default
1 Enable
- 0 1X Mode Enable**
0 Disable..... default
1 Enable

Device 0 Offset AC - AGP ControlRW

- 7-4 **Reserved**always reads 0s
- 3 **2X Rate Supported** (read also at RxA4[1])
 - 0 Not supporteddefault
 - 1 Supported
- 2 **LPR In-Order Access (Force Fence)**
 - 0 Fence/Flush functions not guaranteed. AGP read requests (low/normal priority and high priority) may be executed before previously issued write requests.....default
 - 1 Force all requests to be executed in order (automatically enables Fence/Flush functions). Low (i.e., normal) priority AGP read requests will never be executed before previously issued writes. High priority AGP read requests may still be executed prior to previously issued write requests as required.
- 1 **AGP Arbitration Parking**
 - 0 Disabledefault
 - 1 Enable (GGNT# remains asserted until either GREQ# de-asserts or data phase ready)
- 0 **Arbitration Priority Between CPU-to-PCI Post Write and PCI Master Request After PCI Master Access**
 - 0 CPU-to-PCI write buffer has prioritydefault
 - 1 PCI master has priority

Device 0 Offset F0-F7 – BIOS Scratch Registers RW

- 7-0 **No hardware function**default = 0

Device 0 Offset FD-FC – Reserved RW

- 15-1 **Reserved** always reads 0s
- 0 **Reserved (Do Not Program)** default = 0

Device 0 Offset FF-FE – Reserved RW

- 15-0 **Reserved**default = 00

Device 1 Header Registers - PCI-to-PCI Bridge

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number of 0 and function number equal to 0 and device number equal to one.

Device 1 Offset 1-0 - Vendor ID.....RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 1 Offset 3-2 - Device ID.....RO

15-0 ID Code (reads 8691h to identify the VT82C691 PCI-to-PCI Bridge device)

Device 1 Offset 5-4 - Command.....RW

- 15-10 Reserved** always reads 0
- 9 Fast Back-to-Back Cycle Enable** RO
 - 0 Fast back-to-back transactions only allowed to the same agentdefault
 - 1 Fast back-to-back transactions allowed to different agents
- 8 SERR# Enable**..... RO
 - 0 SERR# driver disableddefault
 - 1 SERR# driver enabled
 (SERR# is used to report parity errors if bit-6 is set).
- 7 Address / Data Stepping** RO
 - 0 Device never does steppingdefault
 - 1 Device always does stepping
- 6 Parity Error Response**.....RW
 - 0 Ignore parity errors & continuedefault
 - 1 Take normal action on detected parity errors
- 5 VGA Palette Snoop** RO
 - 0 Treat palette accesses normallydefault
 - 1 Don't respond to palette writes on PCI bus (10-bit decode of I/O addresses 3C6-3C9 hex)
- 4 Memory Write and Invalidate Command**..... RO
 - 0 Bus masters must use Mem Writedefault
 - 1 Bus masters may generate Mem Write & Inval
- 3 Special Cycle Monitoring** RO
 - 0 Does not monitor special cyclesdefault
 - 1 Monitors special cycles
- 2 Bus Master**RW
 - 0 Never behaves as a bus master
 - 1 Enable to operate as a bus master on the primary interface on behalf of a master on the secondary interfacedefault
- 1 Memory Space**.....RW
 - 0 Does not respond to memory space
 - 1 Enable memory space accessdefault
- 0 I/O Space**RW
 - 0 Does not respond to I/O space
 - 1 Enable I/O space accessdefault

Device 1 Offset 7-6 - Status (Primary Bus)..... RWC

- 15 Detected Parity Error** always reads 0
- 14 Signaled System Error (SERR#)** always reads 0
- 13 Signaled Master Abort**
 - 0 No abort received default
 - 1 Transaction aborted by the master with Master-Abort (except Special Cycles)..... write 1 to clear
- 12 Received Target Abort**
 - 0 No abort received default
 - 1 Transaction aborted by the target with Target-Abort write 1 to clear
- 11 Signaled Target Abort**..... always reads 0
- 10-9 DEVSEL# Timing**
 - 00 Fast
 - 01 Medium..... always reads 01
 - 10 Slow
 - 11 Reserved
- 8 Data Parity Error Detected** always reads 0
- 7 Fast Back-to-Back Capable** always reads 0
- 6 User Definable Features**..... always reads 0
- 5 66MHz Capable**..... always reads 1
- 4 Supports New Capability list**..... always reads 0
- 3-0 Reserved** always reads 0

Device 1 Offset 8 - Revision ID..... RO

7-0 VT82C691 Chip Revision Code (00=First Silicon)

Device 1 Offset 9 - Programming Interface..... RO

This register is defined in different ways for each Base/Sub-Class Code value and is undefined for this type of device.

7-0 Interface Identifier always reads 00

Device 1 Offset A - Sub Class Code..... RO

7-0 Sub Class Code .reads 04 to indicate PCI-PCI Bridge

Device 1 Offset B - Base Class Code..... RO

7-0 Base Class Code.. reads 06 to indicate Bridge Device

Device 1 Offset D - Latency Timer RO

7-0 Reserved always reads 0

Device 1 Offset E - Header Type RO

7-0 Header Type Code..... reads 01: PCI-PCI Bridge

Device 1 Offset F - Built In Self Test (BIST) RO

- 7 BIST Supported** reads 0: no supported functions
- 6 Start Test** write 1 to start but writes ignored
- 5-4 Reserved** always reads 0
- 3-0 Response Code**.....0 = test completed successfully

Device 1 Offset 18 - Primary Bus NumberRW
7-0 Primary Bus Number..... default = 0

This register is read write, but internally the chip always uses bus 0 as the primary.

Device 1 Offset 19 - Secondary Bus NumberRW
7-0 Secondary Bus Number..... default = 0

Note: PCI#2 must use these bits to convert Type 1 to Type 0.

Device 1 Offset 1A - Subordinate Bus NumberRW
7-0 Primary Bus Number..... default = 0

Note: PCI#2 must use these bits to decide if Type 1 to Type 1 command passing is allowed.

Device 1 Offset 1C - I/O BaseRW
7-4 I/O Base AD[15:12]..... default = 1111b

3-0 I/O Addressing Capability..... default = 0

Device 1 Offset 1D - I/O Limit.....RW
7-4 I/O Limit AD[15:12]..... default = 0

3-0 I/O Addressing Capability..... default = 0

Device 1 Offset 1F-1E - Secondary Status RO
15-0 Reserved always reads 0000

Device 1 Offset 21-20 - Memory Base RW
15-4 Memory Base AD[31:20] default = 0FFFh

3-0 Reserved always reads 0

Device 1 Offset 23-22 - Memory Limit (Inclusive)..... RW
15-4 Memory Limit AD[31:20] default = 0

3-0 Reserved always reads 0

Device 1 Offset 25-24 - Prefetchable Memory Base..... RW
15-4 Prefetchable Memory Base AD[31:20] def = 0FFFh

3-0 Reserved always reads 0

Device 1 Offset 27-26 - Prefetchable Memory Limit RW
15-4 Prefetchable Memory Limit AD[31:20].....

..... default = 0

3-0 Reserved always reads 0

Device 1 Offset 3F-3E – PCI-to-PCI Bridge ControlRW

15-4 Reserved always reads 0

3 VGA-Present on AGP

- 0 Forward VGA accesses to PCI Bus #1 ...default
- 1 Forward VGA accesses to PCI Bus #2 / AGP

Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.

2 Block / Forward ISA I/O Addresses

- 0 Forward all I/O accesses to the AGP bus if they are in the range defined by the I/O Base and I/O Limit registers (device 1 offset 1C-1D)default
- 1 Do not forward I/O accesses to the AGP bus that are in the 100-3FFh address range even if they are in the range defined by the I/O Base and I/O Limit registers.

1-0 Reserved always reads 0

Device 1 Configuration Registers - PCI-to-PCI Bridge

PCI Bus #2 Control

Device 1 Offset 40 - CPU-to-PCI #2 Flow Control 1..RW

- 7 CPU-PCI #2 Post Write**
0 Disabledefault
1 Enable
- 6 CPU-PCI #2 Dynamic Burst**
0 Disabledefault
1 Enable
- 5 CPU-PCI #2 One Wait State Burst Write**
0 Disabledefault
1 Enable
- 4 PCI #2 to DRAM Prefetch**
0 Disabledefault
1 Enable
- 3 PCI Master Allowed Before CPU-to-PCI Post Write Buffer is not Flushed**
0 Disabledefault
1 Enable
This option is always enabled for PCI #1
- 2 MDA Present on PCI #2**
0 Forward MDA accesses to AGP.....default
1 Forward MDA accesses to PCI #1
Note: Forward despite IO / Memory Base / Limit
Note: MDA (Monochrome Display Adapter) addresses are memory addresses B0000h-B7FFFh and I/O addresses 3B4-3B5h, 3B8-3BAh, and 3BFh (10-bit decode). 3BC-3BE are reserved for printers.
Note: If Rx3E bit-3 is 0, this bit is a don't care (MDA accesses are forwarded to the PCI bus).
- 1 PCI #2 Master Read Caching**
0 Disabledefault
1 Enable
- 0 PCI #2 Delay Transaction**
0 Disabledefault
1 Enable

Table 5. VGA/MDA Memory/IO Redirection

3E[3]	40[2]	VGA	MDA	Axxxx,	B0000	3Cx,	
VGA	MDA	is	is	B8xxx	-B7FFF	3Dx	3Bx
Pres.	Pres.	on	on	Access	Access	I/O	I/O
0	-	PCI	PCI	PCI	PCI	PCI	PCI
1	0	AGP	AGP	AGP	AGP	AGP	AGP
1	1	AGP	PCI	AGP	PCI	AGP	PCI

Device 1 Offset 41 - CPU-to-PCI #2 Flow Control 2 .. RWC

- 7 Retry Status**
0 No retry occurred..... default
1 Retry Occurredwrite 1 to clear
- 6 Retry Timeout Action**
0 No action taken except to record status def
1 Flush buffer for write or return all 1s for read
- 5-4 Retry Count**
00 Retry 2, backoff CPU default
01 Retry 4, backoff CPU
10 Retry 16, backoff CPU
11 Retry 64, backoff CPU
- 3 Post Write Data on Abort**
0 Flush entire post-write buffer on target-abort or master abort..... default
1 Pop one data output on target-abort or master-abort
- 2 CPU Backoff on PCI #2 Read Retry Timeout**
0 Disable..... default
1 Enable
- 1 CPU to PCI #2 I/O Write Posting**
0 Disable..... default
1 Enable
- 0 Reserved**always reads 0

Device 1 Offset 42 - PCI #2 Master Control..... RW

- 7 Read Prefetch for Enhance Command**
0 Always Perform Prefetch..... default
1 Prefetch only if Enhance Command
- 6 PCI #2 Master One Wait State Write**
0 Disable..... default
1 Enable
- 5 PCI #2 Master One Wait State Read**
0 Disable..... default
1 Enable
- 4 Extend PCI #2 Internal Master for Efficient Handling of Dummy Request Cycles**
0 Disable..... default
1 Enable
This bit is normally set to 1.
- 3 Reserved**always reads 0
- 2 Fast Response / Read Caching Prefetch Disable**
0 Normal operation..... default
1 Disable prefetch when doing fast response to the previous delay transaction or doing read caching
- 1-0 Reserved**always reads 0

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Ambient operating temperature	0	70	°C
Storage temperature	-55	125	°C
Input voltage	-0.5	5.5	Volts
Output voltage ($V_{CC} = 3.1 - 3.6V$)	-0.5	$V_{CC} + 0.5$	Volts

Note: Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Characteristics

TA=0-70°C, $V_{CC}=5V \pm 5\%$, GND=0V

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input low voltage	-0.50	0.8	V	
V_{IH}	Input high voltage	2.0	$V_{CC}+0.5$	V	
V_{OL}	Output low voltage	-	0.45	V	$I_{OL}=4.0mA$
V_{OH}	Output high voltage	2.4	-	V	$I_{OH}=-1.0mA$
I_{IL}	Input leakage current	-	+/-10	uA	$0 < V_{IN} < V_{CC}$
I_{OZ}	Tristate leakage current	-	+/-20	uA	$0.45 < V_{OUT} < V_{CC}$
I_{CC}	Power supply current	-		mA	

AC Timing Specifications

AC timing specifications provided are based on external zero-pf capacitance load. Min/max cases are based on the following table:

Table 6. AC Timing Min / Max Conditions

Parameter	Min	Max	Unit
3.3V Power (V_{CC} , V_{CCI} , V_{TT} , AV_{CC} , HV_{CC})	3.135	3.465	Volts
5V Reference (5VREF)	4.75	5.25	Volts
Temperature	0	70	°C

Drive strength for each output pin is programmable. See Rx6D for details.

Table 8. AC Characteristics - DRAM Interface Timing

Parameter	Min	Max	Unit	Notes
RAS[5:0]# Valid Delay from HCLK Rising (EDO)			ns	0pf
CS[5:0]# Valid Delay from HCLK Rising (SDRAM)			ns	
CAS[7:0]# Valid Delay from HCLK Rising (EDO)			ns	
DQM[7:0]# Valid Delay from HCLK Rising (SDRAM)			ns	
SRAS[A,B,C]# Valid Delay from HCLK Rising (SDRAM)			ns	
SCAS[A,B,C]# Valid Delay from HCLK Rising (SDRAM)			ns	
SWE[A,B,C]# Valid Delay from HCLK Rising (SDRAM)			ns	
MA[11:2] Valid Delay from HCLK Rising on first Clock after RAS# asserts			ns	
MA[1:0] Valid Delay from HCLK Rising (burst)			ns	
MA[11:0] Flow Through Delay from HA for first read cycle			ns	
SWE[A,B,C]# Valid Delay from HCLK Rising (EDO)			ns	

Table 9. AC Characteristics - Data Timing

Parameter	Min	Max	Unit	Notes
HD Valid Delay from HCLK Rising			ns	0pf
HD Setup Time to HCLK Rising			ns	
HD Hold Time from HCLK Rising			ns	
MD Valid Delay from HCLK Rising			ns	
MD Setup Time to HCLK Rising (SDRAM)			ns	
MD Setup Time to HCLK Falling (EDO)			ns	
MD Hold Time from HCLK Rising (SDRAM)			ns	
MD Hold Time from HCLK Falling (EDO)			ns	

Table 10. AC Characteristics - PCI Cycle Timing

Parameter	Min	Max	Unit	Notes
AD[31:0] Valid Delay from PCLK Rising (address phase)	5.0	11	ns	50pf
AD[31:0] Valid Delay from PCLK Rising (data phase)	5.0	11	ns	
AD[31:0] Setup Time to HCLK Rising	1.5		ns	
AD[31:0] Hold Time to HCLK Rising	0.8		ns	
CBE[3:0]# Setup Time to HCLK Rising	1.0		ns	
FRAME# Setup Time to HCLK Rising	5.8		ns	
TRDY# Setup Time to HCLK Rising	5.5		ns	
IRDY# Setup Time to HCLK Rising	5.0		ns	
STOP# Setup Time to HCLK Rising	3.8		ns	
DEVSEL# Setup Time to HCLK Rising	4.8		ns	
REQ[3:0]# Setup Time to HCLK Rising	8.7		ns	
CBE[3:0]# Hold Time to HCLK Rising	0.2		ns	
FRAME# Hold Time to HCLK Rising	0.3		ns	
TRDY# Hold Time to HCLK Rising	0.4		ns	
IRDY# Hold Time to HCLK Rising	0.3		ns	
STOP# Hold Time to HCLK Rising	0.8		ns	
DEVSEL# Hold Time to HCLK Rising	0.3		ns	
REQ[3:0]# Hold Time to HCLK Rising	0.8		ns	
CBE[3:0]# Valid Delay from PCLK Rising	2.9	7.5	ns	
FRAME# Valid Delay from PCLK Rising	2.8	7.3	ns	
TRDY# Valid Delay from PCLK Rising	5.8	15.0	ns	
IRDY# Valid Delay from PCLK Rising	2.9	7.5	ns	
STOP# Valid Delay from PCLK Rising	2.9	7.5	ns	
DEVSEL# Valid Delay from PCLK Rising	2.8	7.3	ns	
GNT[3:0]#, Valid Delay from PCLK Rising	2.3	6.0	ns	
CBE[3:0]# ,Float Delay from HCLK Rising	3.4	8.7	ns	
FRAME# ,Float Delay from HCLK Rising	3.4	9.8	ns	
TRDY# ,Float Delay from HCLK Rising	3.8	10.0	ns	
IRDY# ,Float Delay from HCLK Rising	3.9	10.0	ns	
STOP# ,Float Delay from HCLK Rising	3.4	9.8	ns	
DEVSEL# ,Float Delay from HCLK Rising	3.8	9.9	ns	

Table 11. AC Characteristics – PCI-66 Cycle Timing

Parameter	Min	Max	Unit	Notes
AD[31:0] Valid Delay from HCLK Rising (address phase)	3.1	5.4	ns	0pf
AD[31:0] Valid Delay from HCLK Rising (data phase)	3.1	5.4	ns	
AD[31:0] Setup Time to HCLK Rising	1.4		ns	
AD[31:0] Hold Time to HCLK Rising	0.3		ns	
CBE[3:0]# Setup Time to HCLK Rising	0.9		ns	
FRAME# Setup Time to HCLK Rising	4.0		ns	
TRDY# Setup Time to HCLK Rising	2.0		ns	
IRDY# Setup Time to HCLK Rising	4.5		ns	
STOP# Setup Time to HCLK Rising	2.7		ns	
DEVSEL# Setup Time to HCLK Rising	4.4		ns	
CBE[3:0]# Hold Time to HCLK Rising	0.4		ns	
FRAME# Hold Time to HCLK Rising	0.6		ns	
TRDY# Hold Time to HCLK Rising	0.4		ns	
IRDY# Hold Time to HCLK Rising	0.2		ns	
STOP# Hold Time to HCLK Rising	0.7		ns	
DEVSEL# Hold Time to HCLK Rising	0.4		ns	
CBE[3:0]# Valid Delay from HCLK Rising	2.1	5.3	ns	
FRAME# Valid Delay from HCLK Rising	2.1	5.2	ns	
TRDY# Valid Delay from HCLK Rising	2.1	5.3	ns	
IRDY# Valid Delay from HCLK Rising	2.1	5.4	ns	
STOP# Valid Delay from HCLK Rising	2.1	5.2	ns	
DEVSEL# Valid Delay from HCLK Rising	2.1	5.6	ns	
GNT#, Valid Delay from HCLK Rising	2.5	5.2	ns	
CBE[3:0]# ,Float Delay from HCLK Rising	3.3	11	ns	
FRAME# ,Float Delay from HCLK Rising	1.7	7	ns	
TRDY# ,Float Delay from HCLK Rising	1.7	7	ns	
IRDY# ,Float Delay from HCLK Rising	3.3	11	ns	
STOP# ,Float Delay from HCLK Rising	1.7	7	ns	
DEVSEL# ,Float Delay from HCLK Rising	2.1	8	ns	

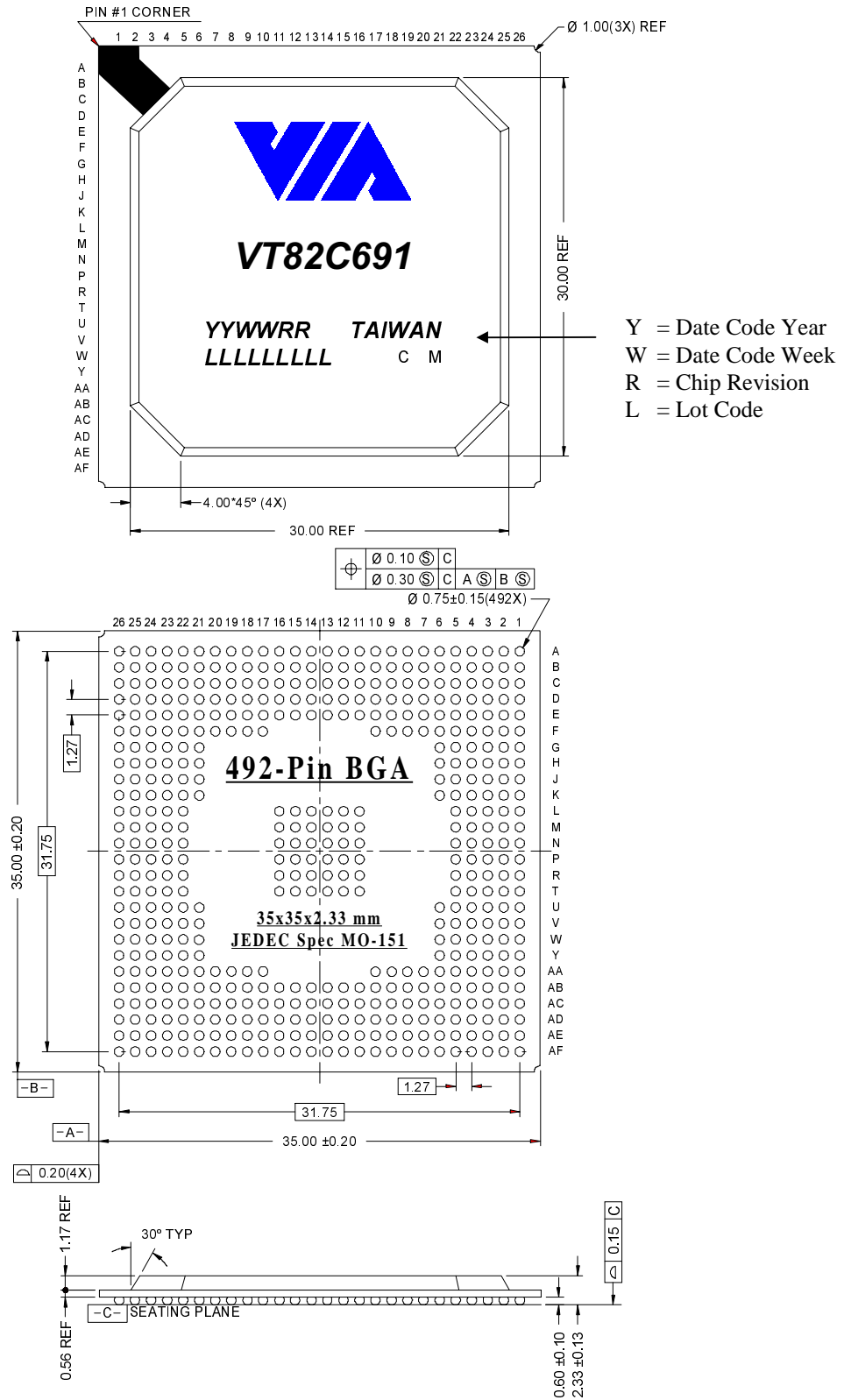
Table 12. AC Characteristics - AGP (1X) Cycle Timing

Parameter	Min	Max	Unit	Notes
GD[31:0] Valid delay from HCLK Rising (request phase)	1.1	5.2	ns	0 pf
GD[31:0] Valid delay from HCLK Rising (data phase)	0.2		ns	
GD[31:0] Valid delay from HCLK Rising (data phase)	2.0	5.0	ns	
GD[31:0] Hold Time to HCLK Rising	0.6		ns	
GBE[3:0]#, Setup Time to HCLK Rising	5.0		ns	
GPIPE#, Setup Time to HCLK Rising	3.6		ns	
SBA[7:0], Setup Time to HCLK Rising	4.7		ns	
GIRDY#, Setup Time to HCLK Rising	4.7		ns	
GRBF#, Setup Time to HCLK Rising	4.7		ns	
GBE[3:0]#, Hold Time from HCLK Rising	0.8		ns	
GPIPE, Hold Time from HCLK Rising	0.3		ns	
SBA[7:0], Hold Time from HCLK Rising	0.2		ns	
GIRDY#, Hold Time from HCLK Rising	0.3		ns	
GRBF#, Hold Time from HCLK Rising	0.1		ns	
ST[2:0], valid Delay from HCLK Rising	2.4	5.5	ns	
GTRDY#, Valid Delay from HCLK Rising	2.6	5.7	ns	
GREQ# Setup Time to HCLK Rising	3.5		ns	
GREQ# Hold Time to HCLK Rising	0.3		ns	
GGNT# Valid Delay from HCLK Rising	1.5	5.5	ns	

Table 13. AC Characteristics - AGP (2X) Cycle Timing

Parameter	Min	Max	Unit	Notes
GD[31:0] Setup Time to GDS[1:0]#	0.4		ns	0 pf
GBE[3:0]# Setup Time to GDS[1:0]#	0.4		ns	
SBA[7:0] Setup Time to SBS#	0.7		ns	
GDS[1:0]# to HCLK Rising (T2) Setup Time	0.7		ns	
SBS# to HCLK Rising Setup Time	0.7		ns	
GD[31:0] Hold Time from to GDS[1:0]# falling	0.7		ns	
GBE[3:0]# Hold Time from to GDS[1:0]# falling	0.7		ns	
SBA[7:0] Hold Time from to SBS# falling	0.4		ns	
GDS[1:0]# to HCLK Rising (T2) Hold Time	1.5		ns	
SBS# to HCLK Rising Hold Time	1.5		ns	
GD[31:0] Valid Delay before GDS[1:0]#	1.8	3.7	ns	
GD[31:0] Valid Delay after GDS[1:0]#	1.8	3.8	ns	
GD[31:0] Float to Active Delay	2.0	5.2	ns	
GD[31:0] Active to Float Delay	1.7	4.4	ns	
GDS[1:0]# Falling Delay from HCLK Rising	3.4	8.9	ns	
GDS[1:0]# Rising Delay from HCLK Rising	6.0	15.6	ns	

MECHANICAL SPECIFICATIONS



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Figure 8. Mechanical Specifications - 492-Pin Ball Grid Array Package