
# Apollo Pro133T Chipset

## VT82C694T
## Single-Chip North Bridge
## with 133 / 100 / 66 MHz Front Side Bus
## for VIA C3 and Intel Celeron,
## Pentium III and Pentium III-M (Tualatin) CPUs
## with AGP 4x and PCI
## plus Advanced ECC Memory Controller
## supporting PC133 / PC100 SDRAM
## for Desktop and Mobile PC Systems

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**VIA TECHNOLOGIES, INC.**

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**PRODUCT FEATURES**

- **AGP / PCI / ISA Mobile and Deep Green PC Ready**
  - GTL+ compliant host bus supports write-combine cycles
  - Supports separately powered 3.3V (5V tolerant) interface to system memory, AGP, and PCI bus
  - Modular power management and clock control for mobile system applications
  - Combine with VIA VT82C686B south bridge chip for state-of-the-art system power management
- **High Integration**
  - Single chip implementation for 64-bit CPU, 64-bit system memory, 32-bit PCI and 32-bit AGP interfaces
  - **Apollo Pro133T** Chipset: **VT82C694T** system controller and **VT82C686B** PCI to ISA bridge
  - Chipset includes UltraDMA-33/66/100 EIDE, 4 USB ports, Integrated Super-I/O, AC97 / MC97 link (for Audio and Modem support), Hardware Monitoring, Power Management, and Keyboard / PS2-Mouse Interfaces plus RTC / CMOS on chip
- **High Performance CPU Interface**
  - Supports Socket-370 VIA C3™ and Intel Celeron™, Pentium III™ & Pentium III-M™ (Tualatin) processors
  - 133 / 100 / 66 MHz CPU Front Side Bus (FSB)
  - Built-in PLL (Phase Lock Loop) circuitry for optimal skew control within and between clocking regions
  - Five outstanding transactions (four In-Order Queue (IOQ) plus one input latch)
  - Supports WC (Write Combining) cycles
  - Dynamic deferred transaction support
  - Sleep mode support
  - System management interrupt, memory remap and STPCLK mechanism

- **Full Featured Accelerated Graphics Port (AGP) Controller**
  - Synchronous and pseudo-synchronous with the host CPU bus with optimal skew control

| PCI | AGP | CPU | Mode |
|---|---|---|---|
| 33 MHz | 66 MHz | 133 MHz | 4x synchronous |
| 33 MHz | 66 MHz | 100 MHz | 3x synchronous |
| 33 MHz | 66 MHz | 66 MHz | 2x synchronous |

  - AGP v2.0 compliant
  - Supports SideBand Addressing (SBA) mode (non-multiplexed address / data)
  - Supports 266 MHz 4x mode for AD and SBA signaling
  - Pipelined split-transaction long-burst transfers up to 1GB/sec
  - Eight level read request queue
  - Four level posted-write request queue
  - Thirty-two level (quadwords) read data FIFO (256 bytes)
  - Sixteen level (quadwords) write data FIFO (128 bytes)
  - Intelligent request reordering for maximum AGP bus utilization
  - Supports Flush/Fence commands
  - Graphics Address Relocation Table (GART)
    - One level TLB structure
    - Sixteen entry fully associative page table
    - LRU replacement scheme
    - Independent GART lookup control for host / AGP / PCI master accesses
  - Windows 95 OSR-2 VXD and integrated Windows 98 / NT5 miniport driver support

- **Concurrent PCI Bus Controller**
  - PCI buses are synchronous / pseudo-synchronous to host CPU bus
  - 33 MHz operation on the primary PCI bus
  - 66 MHz PCI operation on the AGP bus
  - PCI-to-PCI bridge configuration on the 66MHz PCI bus
  - Supports up to five PCI masters
  - Peer concurrency
  - Concurrent multiple PCI master transactions; i.e., allow PCI masters from both PCI buses active at the same time
  - Zero wait state PCI master and slave burst transfer rate
  - PCI to system memory data streaming up to 132Mbyte/sec
  - PCI master snoop ahead and snoop filtering
  - Two lines of CPU to PCI posted write buffers
  - Byte merging in the write buffers to reduce the number of PCI cycles and to create further PCI bursting possibilities
  - Enhanced PCI command optimization (MRL, MRM, MWI, etc.)
  - Forty-eight levels (double-words) of post write buffers from PCI masters to DRAM
  - Sixteen levels (double-words) of prefetch buffers from DRAM for access by PCI masters
  - Delay transaction from PCI master accessing DRAM
  - Read caching for PCI master reading DRAM
  - Transaction timer for fair arbitration between PCI masters (granularity of two PCI clocks)
  - Symmetric arbitration between Host/PCI bus for optimized system performance
  - Complete steerable PCI interrupts
  - PCI-2.2 compliant, 32 bit 3.3V PCI interface with 5V tolerant inputs

- **Advanced High-Performance DRAM Controller**
  - DRAM interface synchronous with host CPU (66/100/133 MHz) or AGP (66MHz) for most flexible configuration
  - DRAM interface may be faster than CPU by 33 MHz to allow use of PC100 memory modules with 66MHz Celeron or use of PC133 with 100MHz Pentium II or Pentium III
  - DRAM interface may be slower than CPU by 33 MHz to allow use of older memory modules with newer CPUs (e.g., PC66 memory modules with 100 MHz Pentium II or Pentium III)
  - Concurrent CPU, AGP, and PCI access
  - Different DRAM types may be used in mixed combinations
  - Different DRAM timing for each bank
  - Dynamic Clock Enable (CKE) control for SDRAM power reduction in high speed systems
  - Mixed 1M / 2M / 4M / 8M / 16M / 32MxN DRAMs
  - Pinouts support 8 banks up to 2 GB DRAMs (256Mb DRAM technology) at 100 MHz (PC133 specifications, however, recommend a limit of 3 DIMMs or 6 banks at 133 MHz for 1.5 GB max memory)
  - Flexible row and column addresses
  - 64-bit data width only
  - 3.3V DRAM interface with 5V-tolerant inputs
  - Programmable I/O drive capability for MA, command, and MD signals
  - Dual copies of MA signals for improved drive
  - Optional bank-by-bank ECC (single-bit error correction and multi-bit error detection) or EC (error checking only) for DRAM integrity
  - Two-bank interleaving for 16Mbit SDRAM support
  - Two-bank and four bank interleaving for 64Mbit SDRAM support
  - Supports maximum 8-bank interleave (i.e., 8 pages open simultaneously); banks are allocated based on LRU
  - Independent SDRAM control for each bank
  - Seamless DRAM command scheduling for maximum DRAM bus utilization (e.g., precharge other banks while accessing the current bank)
  - Four cache lines (16 quadwords) of CPU to DRAM write buffers
  - Four cache lines of CPU to DRAM read prefetch buffers
  - Read around write capability for non-stalled CPU read
  - Speculative DRAM read before snoop result
  - Burst read and write operation
  - x-2-2-2-2-2-2-2 back-to-back accesses for EDO DRAM from CPU or from DRAM controller
  - x-1-1-1-1-1-1-1 back-to-back accesses for SDRAM
  - BIOS shadow at 16KB increment
  - Decoupled and burst DRAM refresh with staggered RAS timing
  - CAS before RAS or self refresh
- **Advanced System Power Management Support**
  - Dynamic power down of SDRAM (CKE)
  - Independent clock stop controls for CPU / SDRAM, AGP, and PCI bus
  - PCI and AGP bus clock run and clock generator control
  - VTT suspend power plane preserves memory data
  - Suspend-to-DRAM and Self-Refresh operation
  - SDRAM self-refresh power down
  - 8 bytes of BIOS scratch registers
  - Low-leakage I/O pads
- **Built-in NAND-tree pin scan test capability**
- **3.3V, 0.35um, high speed / low power CMOS process**
- **35 x 35 mm, 520 pin BGA Package**

# OVERVIEW

The ***Apollo Pro133T*** is a high performance, cost-effective and energy efficient chip set for the implementation of AGP / PCI / ISA desktop personal computer systems with 133 MHz, 100 MHz and 66 MHz front side bus (FSB) frequencies based on 64-bit Socket-370 VIA C3 and Intel Celeron, Pentium III, and Pentium III-M (Tualatin) super-scalar processors.

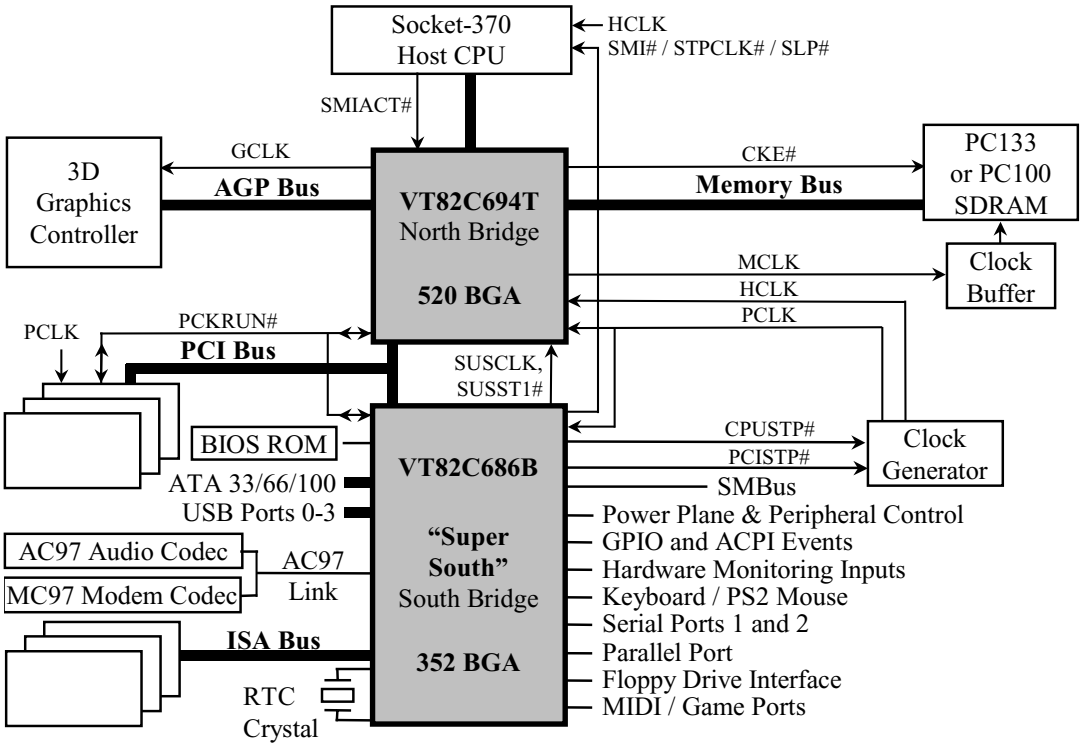



**Figure 1. Apollo Pro133T Chipset System Block Diagram**

The **Apollo Pro133T** chip set consists of the **VT82C694T** system controller (520 pin BGA) and the **VT82C686B** PCI to ISA bridge (352 pin BGA). The system controller provides superior performance between the CPU, DRAM, AGP bus, and PCI bus with pipelined, burst, and concurrent operation.

The VT82C694T supports eight banks of DRAMs up to 1.5GB. The DRAM controller supports standard Fast Page Mode (FPM) DRAM, EDO-DRAM, Synchronous DRAM (SDRAM) and Virtual Channel SDRAM (VC SDRAM), in a flexible mix / match manner. The Synchronous DRAM interface allows zero wait state bursting between the DRAM and the data buffers at 66/100/133 MHz. The eight banks of DRAM can be composed of an arbitrary mixture of 1M / 2M / 4M / 8M / 16M / 32MxN DRAMs. The DRAM controller also supports optional ECC (single-bit error correction and multi-bit detection) or EC (error checking) capability separately selectable on a bank-by-bank basis. The DRAM controller can run at either the host CPU bus frequency (66 /100 /133 MHz) or at the AGP bus frequency (66 MHz) with built-in PLL timing control.

The VT82C694T system controller also supports full AGP v2.0 capability for maximum bus utilization including 2x and 4x mode transfers, SBA (SideBand Addressing), Flush/Fence commands, and pipelined grants. An eight level request queue plus a four level post-write request queue with thirty-two and sixteen quadwords of read and write data FIFO's respectively are included for deep pipelined and split AGP transactions. A single-level GART TLB with 16 full associative entries and flexible CPU / AGP / PCI remapping control is also provided for operation under protected mode operating environments. Both Windows-95 VXD and Windows-98 / NT5 miniport drivers are supported for interoperability with major AGP-based 3D and DVD-capable multimedia accelerators.

The VT82C694T supports two 32-bit 3.3 / 5V system buses (one AGP and one PCI) that are synchronous / pseudo-synchronous to the CPU bus. The chip also contains a built-in bus-to-bus bridge to allow simultaneous concurrent operations on each bus. Five

levels (doublewords) of post write buffers are included to allow for concurrent CPU and PCI operation. For PCI master operation, forty-eight levels (doublewords) of post write buffers and sixteen levels (doublewords) of prefetch buffers are included for concurrent PCI bus and DRAM/cache accesses. The chip also supports enhanced PCI bus commands such as Memory-Read-Line, Memory-Read-Multiple and Memory-Write-Invalid commands to minimize snoop overhead. In addition, advanced features are supported such as snoop ahead, snoop filtering, L1 write-back forward to PCI master, and L1 write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

The 352-pin Ball Grid Array VT82C686B PCI to ISA bridge supports four levels (doublewords) of line buffers, type F DMA transfers and delay transaction to allow efficient PCI bus utilization and (PCI-2.1 compliant). The VT82C686B also includes an integrated keyboard controller with PS2 mouse support, integrated DS12885 style real time clock with extended 256 byte CMOS RAM, integrated master mode enhanced IDE controller with full scatter / gather capability and extension to UltraDMA-33/66/100 for 33/66/100 MB/sec transfer rate, integrated USB interface with root hub and four function ports with built-in physical layer transceivers, Distributed DMA support, and OnNow / ACPI compliant advanced configuration and power management interface. The VT82C686B also includes an AC97 / MC97 link for interface to external audio and modem codecs, and all “Super-I/O” functions (serial ports, parallel port, and floppy drive interface and game port).

For sophisticated power management, the Apollo Pro133T provides independent clock stop control for the CPU / SDRAM, PCI, and AGP buses and Dynamic CKE control for powering down of the SDRAM. A separate suspend-well plane is implemented for the SDRAM control signals for Suspend-to-DRAM operation. Coupled with the VT82C686B south bridge chip, a complete power conscious PC main board can be implemented with no external TTLs.

The Apollo Pro133T chipset is ideal for high performance, high quality, high energy efficient and high integration desktop and notebook AGP / PCI / ISA computer systems.

**PINOUTS**

## Figure 2. VT82C694T Ball Diagram (Top View)

| Key | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | GND | AD20 | REQ0# | AD25 | AD29 | RESET# | HD56# | HD62# | HD55# | HD54# | HD49# | HD47# | HD40# | GND | HD33# | HD31# | HD27# | HD19# | HD20# | HD10# | HD6# | HD3# | HA29# | HA24# | HA22# | GND |
| B | VCC | PCLK | AD22 | AD27 | AD28 | PREQ# | HD50# | HD61# | HD63# | HD53# | HD48# | HD42# | HD36# | HD43# | HD32# | HD29# | HD25# | HD21# | HD18# | HD12# | HD8# | HD0# | CPU RST# | HA27# | HA20# | BREQ 0# |
| C | AD19 | VCC | AD21 | CBE3# | GND | AD31 | REQ1# | HD52# | GND | HD60# | HD59# | HD51# | HD44# | HD37# | HD28# | HD26# | HD22# | GND | HD17# | HD7# | HD5# | GND | HA26# | HA28# | HA23# | HA21# |
| D | AD16 | AD18 | AD17 | AD23 | AD26 | PGNT# | GNT1# | REQ3# | HD58# | REQ4# | HD46# | HD41# | HD39# | HD34# | HD35# | HD30# | HD24# | HD16# | HD15# | HD14# | HD4# | HD1# | HA31# | HA25# | HA18# | HA19# |
| E | FRM# | IRDY# | GND | CBE2# | AD24 | AD30 | GNT0# | GNT3# | GNT4# | GNT2# | HD57# | GND | HD45# | HD38# | GND | GTL REF | HD23# | HD13# | HD11# | HD9# | HD2# | HA30# | HA15# | GND | HA17# | HA16# |
| F | SERR# | LOCK# | DEV SEL# | STOP# | TRDY# | GND | VCC | GND | VCC | REQ2# | VTT | VTT | VCC | VCC | VTT | VTT | VTT | VCC | GND | VCC | GND | HA11# | HA12# | HA13# | HA14# | HA8# |
| G | AD13 | AD14 | CBE1# | AD15 | PAR | VCC | G7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | G20 | VCC | HA10# | HA5# | HA7# | HA3# | HA9# |
| H | AD8 | AD7 | AD10 | AD12 | AD11 | GND | H | | | | | | | | CPU Pins | | | | | H | GND | HA4# | HA6# | BNR# | H TRDY# | BPRI# |
| J | AD5 | AD6 | GND | CBE0# | AD9 | VCC | J | | PCI | | | | | | | | | VTT | | J | VCC | HREQ 0# | HREQ 1# | GND | HREQ 4# | DEFER # |
| K | GND | AD1 | AD3 | AD2 | AD4 | AD0 | GND | K | Pins | K10 | 11 | 12 | 13 | 14 | 15 | 16 | K17 | VTT | | K | ADS# | HLOCK # | DRDY# | HREQ 2# | HREQ 3# | RS0# |
| L | ST1 | SBA0 | GGNT# | ST0 | GREQ# | VCCQ | VCCQ | L | | L | VCC | GND | VCC | VCC | GND | VCC | L | VTT | | L | VTT | HITM# | DBSY# | HIT# | RS2# | RS1# |
| M | SBA2 | SBA1 | GPIPE# | ST2 | SBS# | GWBF# | M | | | M | GND | VCC | GND | GND | VCC | GND | M | | | M | GND | GNDA | GTL REF | VTT | TEST IN# | CPU RSTD# |
| N | AGP REF | SBA3 | SBS | GCLKO | GCLK | GRBF# | GND | N | | N | VCC | GND | GND | GND | GND | VCC | N | | | N | VCC | VCCA | HCLK | GND | MD63 | VCC |
| P | SBA7 | SBA6 | GND | SBA4 | SBA5 | GD30 | GND | P | | P | VCC | GND | GND | GND | GND | VCC | P | | | | P | GND | MD62 | MD30 | MD31 | GND |
| R | GD31 | GD29 | VCCQ | GD27 | GD24 | VCCQ | VCCQ | R | | R | GND | VCC | GND | GND | VCC | GND | R | | | | R | GND | MD28 | MD60 | MD61 | MD29 |
| T | GD26 | GD23 | GBE3# | GD20 | GDS1# | GDS1 | T | | | T | VCC | GND | VCC | VCC | GND | VCC | T | | | | T | MD57 | MD58 | MD25 | MD26 | MD59 |
| U | GD22 | GD25 | GD19 | GD18 | GDS0# | GND | GNDA | U | AGP | U10 | 11 | 12 | 13 | 14 | 15 | 16 | U17 | | DRAM | U | MD27 | MD22 | MD56 | MD55 | MD23 | MD24 |
| V | GD17 | GD16 | GD28 | G STOP# | GBE2# | VCCA | V | | Pins | | | | | | | | | | Pins | V | VCC | MD19 | MD20 | GND | MD21 | MD54 |
| W | GD21 | G FRM# | GI RDY# | GD15 | GDEV SEL# | VCCQ | W7 | 8 | | | | | | | | | | | | W | GNDA | MD18 | MD50 | MD51 | MD53 | MD52 |
| Y | GPAR | GT RDY# | GND | GBE1# | GDS0 | GND | GND | GND | 9 | 10 | 11 | 12 | | | | | 17 | 18 | 19 | Y20 | VCCA | MECC3 | MD16 | MD48 | MD49 | MD17 |
| AA | GD13 | GD12 | VCCQ | GD11 | GD9 | GND | VCCQ | GND | VCC | MECC5 | VSUS | SUST# | 13 | 14 | 15 | 16 | SRAS R# | VCC | GND | VCC | GND | DQM A?# | MECC6 | DQM A?# | MECC2 | MECC7 |
| AB | GD8 | GD10 | GBE0# | GD7 | GD0 | MD2 | MD37 | MD40 | MD41 | MD44 | MD14 | GND | SCAS R# | CS A0# | GND | MA A1 | MA B?# | MA B6# | MA B7# | MA B10 | DCLK O | DCKR/ MAA14 | CS B5# | GND | GND | DQM A7# |
| AC | GD6 | GD4 | GD5 | GND | MD0 | MD3 | MD38 | MD7 | MD42 | MD45 | MD15 | SWEB# | DQM A5# | DQM A1# | CS A3# | MA B1# | MA A3 | MA A7 | MA A8 | MA B9# | MA A12 | CKE0 | CKE4 | CS B3# | DQM A6# | CS B4# |
| AD | GD14 | GD3 | GD2 | VCC QQ | GND QQ | MD35 | MD5 | MD8 | GND | MD12 | MD47 | MECC1 | DQM A?# | DQM B1# | CS A?# | MA B0# | MA B?# | GND | MA B5# | MA A10 | MA B12# | GND | CKE3 | CS B1# | DCLK WR | CS B?# |
| AE | GD1 | VCCQ | WSC# | MD33 | MD1 | MD36 | MD6 | MD10 | MD43 | MD13 | MECC4 | SWEA# | DQM B5# | DQM A0# | CS A?# | CS A5# | MA A? | MA B4# | MA A5 | MA A9 | MA B11# | MA B14# | GND | CKE2 | CS B0# | VCC |
| AF | GND | PCOMP | PWR OK | MD32 | MD34 | MD4 | MD39 | MD9 | MD11 | MD46 | MECC0 | SCAS A# | GND | VCC | CS A1# | SRAS A# | MA A0 | MA A4 | MA A6 | MA B8# | MA A11 | MA B13# | CKE1 | CKE5 | MA A13 | GND |

**Table 1. VT82C694T Pin List (Numerical Order)**

| Pin # | | Pin Name | Pin # | | Pin Name | Pin # | | Pin Name | Pin # | | Pin Name | Pin # | | Pin Names | Pin # | | Pin Name |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **A01** | **P** | **GND** | D04 | IO | AD23 | **G21** | **P** | **VCC** | **N24** | **P** | **GND** | **Y07** | **P** | **GND** | AC26 | O | CSB4# / RASB4# |
| A02 | IO | AD20 | D05 | IO | AD26 | G22 | IO | HA10# | N25 | IO | MD63 | **Y08** | **P** | **GND** | AD01 | IO | GD14 |
| A03 | I | REQ0# | D06 | O | PGNT# | G23 | IO | HA05# | **N26** | **P** | **VCC** | **Y21** | **P** | **VCCA** | AD02 | IO | GD03 |
| A04 | IO | AD25 | D07 | O | GNT1# | G24 | IO | HA07# | P01 | I | SBA7 | Y22 | IO | MECC3 | AD03 | IO | GD02 |
| A05 | IO | AD29 | D08 | I | REQ3# | G25 | IO | HA03# | P02 | I | SBA6 | Y23 | IO | MD16 | **AD04** | **P** | **VCCQQ** |
| A06 | I | RESET# | D09 | IO | HD58# | G26 | IO | HA09# | **P03** | **P** | **GND** | Y24 | IO | MD48 | **AD05** | **P** | **GNDQQ** |
| A07 | IO | HD56# | D10 | I | REQ4# | H01 | IO | AD08 | P04 | I | SBA4 | Y25 | IO | MD49 | AD06 | IO | MD35 |
| A08 | IO | HD62# | D11 | IO | HD46# | H02 | IO | AD07 | P05 | I | SBA5 | Y26 | IO | MD17 | AD07 | IO | MD05 |
| A09 | IO | HD55# | D12 | IO | HD41# | H03 | IO | AD10 | P06 | IO | GD30 | AA01 | IO | GD13 | AD08 | IO | MD08 |
| A10 | IO | HD54# | D13 | IO | HD39# | H04 | IO | AD12 | **P07** | **P** | **GND** | AA02 | IO | GD12 | **AD09** | **P** | **GND** |
| A11 | IO | HD49# | D14 | IO | HD34# | H05 | IO | AD11 | **P22** | **P** | **GND** | **AA03** | **I** | **VCCQ** | AD10 | IO | MD12 |
| A12 | IO | HD47# | D15 | IO | HD35# | **H06** | **P** | **GND** | P23 | IO | MD62 | AA04 | IO | GD11 | AD11 | IO | MD47 |
| A13 | IO | HD40# | D16 | IO | HD30# | **H21** | **P** | **GND** | P24 | IO | MD30 | AA05 | IO | GD09 | AD12 | IO | MECC1 |
| **A14** | **P** | **GND** | D17 | IO | HD24# | H22 | IO | HA04# | P25 | IO | MD31 | **AA06** | **P** | **GND** | AD13 | O | DQMA4 / CASA4# |
| A15 | IO | HD33# | D18 | IO | HD16# | H23 | IO | HA06# | **P26** | **P** | **GND** | **AA07** | **I** | **VCCQ** | AD14 | O | DQMB1 / CASB1# |
| A16 | IO | HD31# | D19 | IO | HD15# | H24 | IO | BNR# | R01 | IO | GD31 | **AA08** | **P** | **GND** | AD15 | O | CSA4# / RASA4# |
| A17 | IO | HD27# | D20 | IO | HD14# | H25 | IO | HTRDY# | R02 | IO | GD29 | **AA09** | **P** | **VCC** | AD16 | O | MAB0# |
| A18 | IO | HD19# | D21 | IO | HD04# | H26 | IO | BPRI# | **R03** | **P** | **VCCQ** | AA10 | IO | MECC5 | AD17 | O | MAB2# |
| A19 | IO | HD20# | D22 | IO | HD01# | J01 | IO | AD05 | R04 | IO | GD27 | **AA11** | **P** | **VSUS** | **AD18** | **P** | **GND** |
| A20 | IO | HD10# | D23 | IO | HA31# | J02 | IO | AD06 | R05 | IO | GD24 | **AA12** | **I** | **SUST#** | AD19 | O | MAB5# / strap |
| A21 | IO | HD06# | D24 | IO | HA25# | **J03** | **P** | **GND** | **R06** | **P** | **VCCQ** | AA17 | O | SRASB# | AD20 | O | MAA10 |
| A22 | IO | HD03# | D25 | IO | HA18# | J04 | IO | CBE0# | **R07** | **P** | **VCCQ** | **AA18** | **P** | **VCC** | AD21 | O | MAB12# / strap |
| A23 | IO | HA29# | D26 | IO | HA19# | J05 | IO | AD09 | **R22** | **P** | **GND** | **AA19** | **P** | **GND** | **AD22** | **P** | **GND** |
| A24 | IO | HA24# | E01 | IO | FRAME# | **J06** | **P** | **VCC** | R23 | IO | MD28 | **AA20** | **P** | **VCC** | AD23 | O | CKE3 / CSB7# |
| A25 | IO | HA22# | E02 | IO | IRDY# | **J18** | **P** | **VTT** | R24 | IO | MD60 | **AA21** | **P** | **GND** | AD24 | O | CSB1# / RASB1# |
| **A26** | **P** | **GND** | **E03** | **P** | **GND** | **J21** | **P** | **VCC** | R25 | IO | MD61 | AA22 | O | DQMA2 / CASA2# | AD25 | I | DCLKWR |
| **B01** | **P** | **VCC** | E04 | IO | CBE2# | J22 | IO | HREQ0# | R26 | IO | MD29 | AA23 | IO | MECC6 | AD26 | O | CSB2# / RASB2# |
| B02 | I | PCLK | E05 | IO | AD24 | J23 | IO | HREQ1# | T01 | IO | GD26 | AA24 | O | DQMA3 / CASA3# | AE01 | IO | GD01 |
| B03 | IO | AD22 | E06 | IO | AD30 | **J24** | **P** | **GND** | T02 | IO | GD23 | AA25 | IO | MECC2 | **AE02** | **P** | **VCCQ** |
| B04 | IO | AD27 | E07 | O | GNT0# | J25 | IO | HREQ4# | T03 | IO | GBE3# | AA26 | IO | MECC7 | AE03 | O | WSC# |
| B05 | IO | AD28 | E08 | O | GNT3# | J26 | IO | DEFER# | T04 | IO | GD20 | AB01 | IO | GD08 | AE04 | IO | MD33 |
| B06 | I | PREQ# | E09 | O | GNT4# | **K01** | **P** | **GND** | T05 | IO | GDS1# | AB02 | IO | GD10 | AE05 | IO | MD01 |
| B07 | IO | HD50# | E10 | O | GNT2# | K02 | IO | AD01 | T06 | IO | GDS1 | AB03 | IO | GBE0# | AE06 | IO | MD36 |
| B08 | IO | HD61# | E11 | IO | HD57# | K03 | IO | AD03 | T22 | IO | MD57 | AB04 | IO | GD07 | AE07 | IO | MD06 |
| B09 | IO | HD63# | **E12** | **P** | **GND** | K04 | IO | AD02 | T23 | IO | MD58 | AB05 | IO | GD00 | AE08 | IO | MD10 |
| B10 | IO | HD53# | E13 | IO | HD45# | K05 | IO | AD04 | T24 | IO | MD25 | AB06 | IO | MD02 | AE09 | IO | MD43 |
| B11 | IO | HD48# | E14 | IO | HD38# | K06 | IO | AD00 | T25 | IO | MD26 | AB07 | IO | MD37 | AE10 | IO | MD13 |
| B12 | IO | HD42# | **E15** | **P** | **GND** | **K07** | **P** | **GND** | T26 | IO | MD59 | AB08 | IO | MD40 | AE11 | IO | MECC4 |
| B13 | IO | HD36# | **E16** | **I** | **GTLREF** | **K18** | **P** | **VTT** | U01 | IO | GD22 | AB09 | IO | MD41 | AE12 | O | SWEA# / MWEA# |
| B14 | IO | HD43# | E17 | IO | HD23# | K21 | IO | ADS# | U02 | IO | GD25 | AB10 | IO | MD44 | AE13 | O | DQMB5 / CASB5# |
| B15 | IO | HD32# | E18 | IO | HD13# | K22 | I | HLOCK# | U03 | IO | GD19 | AB11 | IO | MD14 | AE14 | O | DQMA0 / CASA0# |
| B16 | IO | HD29# | E19 | IO | HD11# | K23 | IO | DRDY# | U04 | IO | GD18 | **AB12** | **P** | **GND** | AE15 | O | CSA2# / RASA2# |
| B17 | IO | HD25# | E20 | IO | HD09# | K24 | IO | HREQ2# | U05 | IO | GDS0# | AB13 | O | SCASB# | AE16 | O | CSA5# / RASA5# |
| B18 | IO | HD21# | E21 | IO | HD02# | K25 | IO | HREQ3# | **U06** | **P** | **GND** | AB14 | O | CSA0# / RASA0# | AE17 | O | MAA2 |
| B19 | IO | HD18# | E22 | IO | HA30# | K26 | IO | RS0# | **U07** | **P** | **GNDA** | **AB15** | **P** | **GND** | AE18 | O | MAB4# |
| B20 | IO | HD12# | E23 | IO | HA15# | L01 | O | ST1 | U21 | IO | MD27 | AB16 | O | MAA1 | AE19 | O | MAA5 |
| B21 | IO | HD08# | **E24** | **P** | **GND** | L02 | I | SBA0 | U22 | IO | MD22 | AB17 | O | MAB3# | AE20 | O | MAA9 |
| B22 | IO | HD00# | E25 | IO | HA17# | L03 | O | GGNT# | U23 | IO | MD56 | AB18 | O | MAB6# / strap | AE21 | O | MAB11# / strap |
| B23 | O | CPURST# | E26 | IO | HA16# | L04 | O | ST0 | U24 | IO | MD55 | AB19 | O | MAB7# / strap | AE22 | O | MAB14# |
| B24 | IO | HA27# | F01 | IO | SERR# | L05 | I | GREQ# | U25 | IO | MD23 | AB20 | O | MAB10 / strap | **AE23** | **P** | **GND** |
| B25 | IO | HA20# | F02 | IO | LOCK# | **L06** | **I** | **VCCQ** | U26 | IO | MD24 | AB21 | O | DCLKO | AE24 | O | CKE2 / CSB6# |
| B26 | O | BREQ0# | F03 | IO | DEVSEL# | **L07** | **P** | **VCCQ** | V01 | IO | GD17 | AB22 | O | MAA14/DCLKRD | AE25 | O | CSB0# / RASB0# |
| C01 | IO | AD19 | F04 | IO | STOP# | **L18** | **P** | **VTT** | V02 | IO | GD16 | AB23 | O | CSB5# / RASB5# | **AE26** | **P** | **VCC** |
| **C02** | **P** | **VCC** | F05 | IO | TRDY# | **L21** | **P** | **VTT** | V03 | IO | GD28 | **AB24** | **P** | **GND** | **AF01** | **P** | **GND** |
| C03 | IO | AD21 | **F06** | **P** | **GND** | L22 | I | HITM# | V04 | IO | GSTOP# | **AB25** | **P** | **GND** | AF02 | I | PCOMP |
| C04 | IO | CBE3# | **F07** | **P** | **VCC** | L23 | IO | DBSY# | V05 | IO | GBE2# | AB26 | O | DQMA7 / CASA7# | AF03 | I | PWROK |
| **C05** | **P** | **GND** | **F08** | **P** | **GND** | L24 | IO | HIT# | **V06** | **P** | **VCCA** | AC01 | IO | GD06 | AF04 | IO | MD32 |
| C06 | IO | AD31 | **F09** | **P** | **VCC** | L25 | IO | RS2# | **V21** | **P** | **VCC** | AC02 | IO | GD04 | AF05 | IO | MD34 |
| C07 | I | REQ1# | F10 | I | REQ2# | L26 | IO | RS1# | V22 | IO | MD19 | AC03 | IO | GD05 | AF06 | IO | MD04 |
| C08 | IO | HD52# | **F11** | **P** | **VTT** | M01 | I | SBA2 | V23 | IO | MD20 | **AC04** | **P** | **GND** | AF07 | IO | MD39 |
| **C09** | **P** | **GND** | **F12** | **P** | **VTT** | M02 | I | SBA1 | **V24** | **P** | **GND** | AC05 | IO | MD00 | AF08 | IO | MD09 |
| C10 | IO | HD60# | **F13** | **P** | **VCC** | M03 | I | GPIPE# | V25 | IO | MD21 | AC06 | IO | MD03 | AF09 | IO | MD11 |
| C11 | IO | HD59# | **F14** | **P** | **VCC** | M04 | O | ST2 | V26 | IO | MD54 | AC07 | IO | MD38 | AF10 | IO | MD46 |
| C12 | IO | HD51# | **F15** | **P** | **VTT** | M05 | I | SBS# | W01 | IO | GD21 | AC08 | IO | MD07 | AF11 | IO | MECC0 |
| C13 | IO | HD44# | **F16** | **P** | **VTT** | M06 | I | GWBF# | W02 | IO | GFRM# | AC09 | IO | MD42 | AF12 | O | SCASA# |
| C14 | IO | HD37# | **F17** | **P** | **VTT** | **M21** | **P** | **GND** | W03 | IO | GIRDY# | AC10 | IO | MD45 | **AF13** | **P** | **GND** |
| C15 | IO | HD28# | **F18** | **P** | **VCC** | **M22** | **P** | **GNDA** | W04 | IO | GD15 | AC11 | IO | MD15 | **AF14** | **P** | **VCC** |
| C16 | IO | HD26# | **F19** | **P** | **GND** | **M23** | **I** | **GTLREF** | W05 | IO | GDSEL# | AC12 | O | SWEB# / MWEB# | AF15 | O | CSA1# / RASA1# |
| C17 | IO | HD22# | **F20** | **P** | **VCC** | **M24** | **P** | **VTT** | **W06** | **P** | **VCCQ** | AC13 | O | DQMA5 / CASA5# | AF16 | O | SRASA# |
| **C18** | **P** | **GND** | **F21** | **P** | **GND** | M25 | I | TESTIN# | **W21** | **P** | **GNDA** | AC14 | O | DQMA1 / CASA1# | AF17 | O | MAA0 |
| C19 | IO | HD17# | F22 | IO | HA11# | M26 | O | CPURSTD# | W22 | IO | MD18 | AC15 | O | CSA3# / RASA3# | AF18 | O | MAA4 |
| C20 | IO | HD07# | F23 | IO | HA12# | **N01** | **P** | **AGPREF** | W23 | IO | MD50 | AC16 | O | MAB1# | AF19 | O | MAA6 |
| C21 | IO | HD05# | F24 | IO | HA13# | N02 | I | SBA3 | W24 | IO | MD51 | AC17 | O | MAA3 | AF20 | O | MAB8# / strap |
| **C22** | **P** | **GND** | F25 | IO | HA14# | N03 | I | SBS | W25 | IO | MD53 | AC18 | O | MAA7 | AF21 | O | MAA11 |
| C23 | IO | HA26# | F26 | IO | HA08# | N04 | O | GCLKO | W26 | IO | MD52 | AC19 | O | MAA8 | AF22 | O | MAB13# |
| C24 | IO | HA28# | G01 | IO | AD13 | N05 | I | GCLK | Y01 | IO | GPAR | AC20 | O | MAB9# / strap | AF23 | O | CKE1 / GCKE |
| C25 | IO | HA23# | G02 | IO | AD14 | N06 | I | GRBF# | Y02 | IO | GTRDY# | AC21 | O | MAA12 | AF24 | O | CKE5 / CSA7# |
| C26 | IO | HA21# | G03 | IO | CBE1# | **N07** | **P** | **GND** | **Y03** | **P** | **GND** | AC22 | O | CKE0 / FENA | AF25 | O | MAA13 |
| D01 | IO | AD16 | G04 | IO | AD15 | **N21** | **P** | **VCC** | Y04 | IO | GBE1# | AC23 | O | CKE4 / CSA6# | **AF26** | **P** | **GND** |
| D02 | IO | AD18 | G05 | IO | PAR | **N22** | **P** | **VCCA** | Y05 | IO | GDS0 | AC24 | O | CSB3# / RASB3# | | | |
| D03 | IO | AD17 | **G06** | **P** | **VCC** | N23 | I | HCLK | **Y06** | **P** | **GND** | AC25 | O | DQMA6 / CASA6# | | | |

Center **VCC** Pins (16 pins): **L11, L13-14, L16, M12, M15, N11, N16, P11, P16, R12, R15, T11, T13-14, T16**
Center **GND** Pins (20 pins): **L12, L15, M11, M13-14, M16, N12-15, P12-15, R11, R13-14, R16, T12, T15**

**Table 2. VT82C694T Pin List (Alphabetical Order)**

| Pin # | | Pin Name | Pin # | | Pin Name | Pin # | | Pin Name | Pin # | | Pin Name | Pin # | | Pin Names | Pin # | | Pin Name |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| K06 | IO | AD00 | T03 | IO | GBE3# | **AA21** | **P** | **GND** | A19 | IO | HD20# | AE21 | O | MAB11# / strap | AF03 | I | PWROK |
| K02 | IO | AD01 | N05 | I | GCLK | **AB12** | **P** | **GND** | B18 | IO | HD21# | AD21 | O | MAB12# / strap | A03 | I | REQ0# |
| K04 | IO | AD02 | N04 | O | GCLKO | **AB15** | **P** | **GND** | C17 | IO | HD22# | AF22 | O | MAB13# | C07 | I | REQ1# |
| K03 | IO | AD03 | AB05 | IO | GD00 | **AB24** | **P** | **GND** | E17 | IO | HD23# | AE22 | O | MAB14# | F10 | I | REQ2# |
| K05 | IO | AD04 | AE01 | IO | GD01 | **AB25** | **P** | **GND** | D17 | IO | HD24# | AC05 | IO | MD00 | D08 | I | REQ3# |
| J01 | IO | AD05 | AD03 | IO | GD02 | **AC04** | **P** | **GND** | B17 | IO | HD25# | AE05 | IO | MD01 | D10 | I | REQ4# |
| J02 | IO | AD06 | AD02 | IO | GD03 | **AD09** | **P** | **GND** | C16 | IO | HD26# | AB06 | IO | MD02 | A06 | I | RESET# |
| H02 | IO | AD07 | AC02 | IO | GD04 | **AD18** | **P** | **GND** | A17 | IO | HD27# | AC06 | IO | MD03 | K26 | IO | RS0# |
| H01 | IO | AD08 | AC03 | IO | GD05 | **AD22** | **P** | **GND** | C15 | IO | HD28# | AF06 | IO | MD04 | L26 | IO | RS1# |
| J05 | IO | AD09 | AC01 | IO | GD06 | **AE23** | **P** | **GND** | B16 | IO | HD29# | AD07 | IO | MD05 | L25 | IO | RS2# |
| H03 | IO | AD10 | AB04 | IO | GD07 | **AF01** | **P** | **GND** | D16 | IO | HD30# | AE07 | IO | MD06 | L02 | I | SBA0 |
| H05 | IO | AD11 | AB01 | IO | GD08 | **AF13** | **P** | **GND** | A16 | IO | HD31# | AC08 | IO | MD07 | M02 | I | SBA1 |
| H04 | IO | AD12 | AA05 | IO | GD09 | **AF26** | **P** | **GND** | B15 | IO | HD32# | AD08 | IO | MD08 | M01 | I | SBA2 |
| G01 | IO | AD13 | AB02 | IO | GD10 | **M22** | **P** | **GNDA** | A15 | IO | HD33# | AF08 | IO | MD09 | N02 | I | SBA3 |
| G02 | IO | AD14 | AA04 | IO | GD11 | **U07** | **P** | **GNDA** | D14 | IO | HD34# | AE08 | IO | MD10 | P04 | I | SBA4 |
| G04 | IO | AD15 | AA02 | IO | GD12 | **W21** | **P** | **GNDA** | D15 | IO | HD35# | AF09 | IO | MD11 | P05 | I | SBA5 |
| D01 | IO | AD16 | AA01 | IO | GD13 | **AD05** | **P** | **GNDQQ** | B13 | IO | HD36# | AD10 | IO | MD12 | P02 | I | SBA6 |
| D03 | IO | AD17 | AD01 | IO | GD14 | E07 | O | GNT0# | C14 | IO | HD37# | AE10 | IO | MD13 | P01 | I | SBA7 |
| D02 | IO | AD18 | W04 | IO | GD15 | D07 | O | GNT1# | E14 | IO | HD38# | AB11 | IO | MD14 | N03 | I | SBS |
| C01 | IO | AD19 | V02 | IO | GD16 | E10 | O | GNT2# | D13 | IO | HD39# | AC11 | IO | MD15 | M05 | I | SBS# |
| A02 | IO | AD20 | V01 | IO | GD17 | E08 | O | GNT3# | A13 | IO | HD40# | Y23 | IO | MD16 | AF12 | O | SCASA# |
| C03 | IO | AD21 | U04 | IO | GD18 | E09 | O | GNT4# | D12 | IO | HD41# | Y26 | IO | MD17 | AB13 | O | SCASB# |
| B03 | IO | AD22 | U03 | IO | GD19 | Y01 | IO | GPAR | B12 | IO | HD42# | W22 | IO | MD18 | F01 | IO | SERR# |
| D04 | IO | AD23 | T04 | IO | GD20 | M03 | I | GPIPE# | B14 | IO | HD43# | V22 | IO | MD19 | AF16 | O | SRASA# |
| E05 | IO | AD24 | W01 | IO | GD21 | N06 | I | GRBF# | C13 | IO | HD44# | V23 | IO | MD20 | AA17 | O | SRASB# |
| A04 | IO | AD25 | U01 | IO | GD22 | L05 | I | GREQ# | E13 | IO | HD45# | V25 | IO | MD21 | L04 | O | ST0 |
| D05 | IO | AD26 | T02 | IO | GD23 | V04 | IO | GSTOP# | D11 | IO | HD46# | U22 | IO | MD22 | L01 | O | ST1 |
| B04 | IO | AD27 | R05 | IO | GD24 | **E16** | **I** | **GTLREF** | A12 | IO | HD47# | U25 | IO | MD23 | M04 | O | ST2 |
| B05 | IO | AD28 | U02 | IO | GD25 | **M23** | **I** | **GTLREF** | B11 | IO | HD48# | U26 | IO | MD24 | F04 | IO | STOP# |
| A05 | IO | AD29 | T01 | IO | GD26 | Y02 | IO | GTRDY# | A11 | IO | HD49# | T24 | IO | MD25 | AA12 | I | SUST# |
| E06 | IO | AD30 | R04 | IO | GD27 | M06 | I | GWBF# | B07 | IO | HD50# | T25 | IO | MD26 | AE12 | O | SWEA# / |
| C06 | IO | AD31 | V03 | IO | GD28 | G25 | IO | HA03# | C12 | IO | HD51# | U21 | IO | MD27 | AC12 | O | SWEB# / MWEB# |
| K21 | IO | ADS# | R02 | IO | GD29 | H22 | IO | HA04# | C08 | IO | HD52# | R23 | IO | MD28 | M25 | I | TESTIN# |
| **N01** | **P** | **AGPREF** | P06 | IO | GD30 | G23 | IO | HA05# | B10 | IO | HD53# | R26 | IO | MD29 | F05 | IO | TRDY# |
| H24 | IO | BNR# | R01 | IO | GD31 | H23 | IO | HA06# | A10 | IO | HD54# | P24 | IO | MD30 | **B01** | **P** | **VCC** |
| H26 | IO | BPRI# | Y05 | IO | GDS0 | G24 | IO | HA07# | A09 | IO | HD55# | P25 | IO | MD31 | **C02** | **P** | **VCC** |
| B26 | O | BREQ0# | U05 | IO | GDS0# | F26 | IO | HA08# | A07 | IO | HD56# | AF04 | IO | MD32 | **F07** | **P** | **VCC** |
| J04 | IO | CBE0# | T06 | IO | GDS1 | G26 | IO | HA09# | E11 | IO | HD57# | AE04 | IO | MD33 | **F09** | **P** | **VCC** |
| G03 | IO | CBE1# | T05 | IO | GDS1# | G22 | IO | HA10# | D09 | IO | HD58# | AF05 | IO | MD34 | **F13** | **P** | **VCC** |
| E04 | IO | CBE2# | W05 | IO | GDSEL# | F22 | IO | HA11# | C11 | IO | HD59# | AD06 | IO | MD35 | **F14** | **P** | **VCC** |
| C04 | IO | CBE3# | W02 | IO | GFRM# | F23 | IO | HA12# | C10 | IO | HD60# | AE06 | IO | MD36 | **F18** | **P** | **VCC** |
| AC22 | O | CKE0 / FENA | L03 | O | GGNT# | F24 | IO | HA13# | B08 | IO | HD61# | AB07 | IO | MD37 | **F20** | **P** | **VCC** |
| AF23 | O | CKE1 / GCKE | W03 | IO | GIRDY# | F25 | IO | HA14# | A08 | IO | HD62# | AC07 | IO | MD38 | **G06** | **P** | **VCC** |
| AE24 | O | CKE2 / CSB6# | **A01** | **P** | **GND** | E23 | IO | HA15# | B09 | IO | HD63# | AF07 | IO | MD39 | **G21** | **P** | **VCC** |
| AD23 | O | CKE3 / CSB7# | **A14** | **P** | **GND** | E26 | IO | HA16# | L24 | IO | HIT# | AB08 | IO | MD40 | **J06** | **P** | **VCC** |
| AC23 | O | CKE4 / CSA6# | **A26** | **P** | **GND** | E25 | IO | HA17# | L22 | I | HITM# | AB09 | IO | MD41 | **J21** | **P** | **VCC** |
| AF24 | O | CKE5 / CSA7# | **C05** | **P** | **GND** | D25 | IO | HA18# | K22 | I | HLOCK# | AC09 | IO | MD42 | **N21** | **P** | **VCC** |
| B23 | O | CPURST# | **C09** | **P** | **GND** | D26 | IO | HA19# | J22 | IO | HREQ0# | AE09 | IO | MD43 | **N26** | **P** | **VCC** |
| M26 | O | CPURSTD# | **C18** | **P** | **GND** | B25 | IO | HA20# | J23 | IO | HREQ1# | AB10 | IO | MD44 | **V21** | **P** | **VCC** |
| AB14 | O | CSA0# / RASA0# | **C22** | **P** | **GND** | C26 | IO | HA21# | K24 | IO | HREQ2# | AC10 | IO | MD45 | **AA09** | **P** | **VCC** |
| AF15 | O | CSA1# / RASA1# | **E03** | **P** | **GND** | A25 | IO | HA22# | K25 | IO | HREQ3# | AF10 | IO | MD46 | **AA18** | **P** | **VCC** |
| AE15 | O | CSA2# / RASA2# | **E12** | **P** | **GND** | C25 | IO | HA23# | J25 | IO | HREQ4# | AD11 | IO | MD47 | **AA20** | **P** | **VCC** |
| AC15 | O | CSA3# / RASA3# | **E15** | **P** | **GND** | A24 | IO | HA24# | H25 | IO | HTRDY# | Y24 | IO | MD48 | **AE26** | **P** | **VCC** |
| AD15 | O | CSA4# / RASA4# | **E24** | **P** | **GND** | D24 | IO | HA25# | E02 | IO | IRDY# | Y25 | IO | MD49 | **AF14** | **P** | **VCC** |
| AE16 | O | CSA5# / RASA5# | **F06** | **P** | **GND** | C23 | IO | HA26# | F02 | IO | LOCK# | W23 | IO | MD50 | **N22** | **P** | **VCCA** |
| AE25 | O | CSB0# / RASB0# | **F08** | **P** | **GND** | B24 | IO | HA27# | AF17 | O | MAA0 | W24 | IO | MD51 | **V06** | **P** | **VCCA** |
| AD24 | O | CSB1# / RASB1# | **F19** | **P** | **GND** | C24 | IO | HA28# | AB16 | O | MAA1 | W26 | IO | MD52 | **Y21** | **P** | **VCCA** |
| AD26 | O | CSB2# / RASB2# | **F21** | **P** | **GND** | A23 | IO | HA29# | AE17 | O | MAA2 | W25 | IO | MD53 | **L06** | **P** | **VCCO** |
| AC24 | O | CSB3# / RASB3# | **H06** | **P** | **GND** | E22 | IO | HA30# | AC17 | O | MAA3 | V26 | IO | MD54 | **L07** | **P** | **VCCQ** |
| AC26 | O | CSB4# / RASB4# | **H21** | **P** | **GND** | D23 | IO | HA31# | AF18 | O | MAA4 | U24 | IO | MD55 | **R03** | **P** | **VCCQ** |
| AB23 | O | CSB5# / RASB5# | **J03** | **P** | **GND** | N23 | I | HCLK | AE19 | O | MAA5 | U23 | IO | MD56 | **R06** | **P** | **VCCQ** |
| L23 | IO | DBSY# | **J24** | **P** | **GND** | B22 | IO | HD00# | AF19 | O | MAA6 | T22 | IO | MD57 | **R07** | **P** | **VCCQ** |
| AB21 | O | DCLKO | **K01** | **P** | **GND** | D22 | IO | HD01# | AC18 | O | MAA7 | T23 | IO | MD58 | **W06** | **P** | **VCCQ** |
| AD25 | I | DCLKWR | **K07** | **P** | **GND** | E21 | IO | HD02# | AC19 | O | MAA8 | T26 | IO | MD59 | **AA03** | **P** | **VCCQ** |
| J26 | IO | DEFER# | **M21** | **P** | **GND** | A22 | IO | HD03# | AE20 | O | MAA9 | R24 | IO | MD60 | **AA07** | **P** | **VCCQ** |
| F03 | IO | DEVSEL# | **N07** | **P** | **GND** | D21 | IO | HD04# | AD20 | O | MAA10 | R25 | IO | MD61 | **AE02** | **P** | **VCCQ** |
| AE14 | O | DQMA0# / CASA0 | **N24** | **P** | **GND** | C21 | IO | HD05# | AF21 | O | MAA11 | P23 | IO | MD62 | **AD04** | **P** | **VCCQQ** |
| AC14 | O | DQMA1# / CASA1 | **P03** | **P** | **GND** | A21 | IO | HD06# | AC21 | O | MAA12 | N25 | IO | MD63 | **AA11** | **P** | **VSUS** |
| AA22 | O | DQMA2# / CASA2 | **P07** | **P** | **GND** | C20 | IO | HD07# | AF25 | O | MAA13 | AF11 | IO | MECC0 | **F11** | **P** | **VTT** |
| AA24 | O | DQMA3# / CASA3 | **P22** | **P** | **GND** | B21 | IO | HD08# | AB22 | O | MAA14/DCLKR | AD12 | IO | MECC1 | **F12** | **P** | **VTT** |
| AD13 | O | DQMA4# / CASA4 | **P26** | **P** | **GND** | E20 | IO | HD09# | AD16 | O | MAB0# | AA25 | IO | MECC2 | **F15** | **P** | **VTT** |
| AC13 | O | DQMA5# / CASA5 | **R22** | **P** | **GND** | A20 | IO | HD10# | AC16 | O | MAB1# | Y22 | IO | MECC3 | **V16** | **P** | **VTT** |
| AC25 | O | DQMA6# / CASA6 | **U06** | **P** | **GND** | E19 | IO | HD11# | AD17 | O | MAB2# | AE11 | IO | MECC4 | **F17** | **P** | **VTT** |
| AB26 | O | DQMA7# / CASA7 | **V24** | **P** | **GND** | B20 | IO | HD12# | AB17 | O | MAB3# | AA10 | IO | MECC5 | **J18** | **P** | **VTT** |
| AD14 | O | DQMB1# / CASB1 | **Y03** | **P** | **GND** | E18 | IO | HD13# | AE18 | O | MAB4# | AA23 | IO | MECC6 | **K18** | **P** | **VTT** |
| AE13 | O | DQMB5# / CASB5 | **Y06** | **P** | **GND** | D20 | IO | HD14# | AD19 | O | MAB5# / strap | AA26 | IO | MECC7 | **L18** | **P** | **VTT** |
| K23 | IO | DRDY# | **Y07** | **P** | **GND** | D19 | IO | HD15# | AB18 | O | MAB6# / strap | G05 | IO | PAR | **L21** | **P** | **VTT** |
| E01 | IO | FRAME# | **Y08** | **P** | **GND** | D18 | IO | HD16# | AB19 | O | MAB7# / strap | B02 | I | PCLK | **M24** | **P** | **VTT** |
| AB03 | IO | GBE0# | **AA06** | **P** | **GND** | C19 | IO | HD17# | AF20 | O | MAB8# / strap | AF02 | I | PCOMP | AE03 | O | WSC# |
| Y04 | IO | GBE1# | **AA08** | **P** | **GND** | B19 | IO | HD18# | AC20 | O | MAB9# / strap | D06 | O | PGNT# | | | |
| V05 | IO | GBE2# | **AA19** | **P** | **GND** | A18 | IO | HD19# | AB20 | O | MAB10 / strap | B06 | I | PREQ# | | | |

Center **VCC** Pins (16 pins): **L11, L13-14, L16, M12, M15, N11, N16, P11, P16, R12, R15, T11, T13-14, T16**
Center **GND** Pins (20 pins): **L12, L15, M11, M13-14, M16, N12-15, P12-15, R11, R13-14, R16, T12, T15**

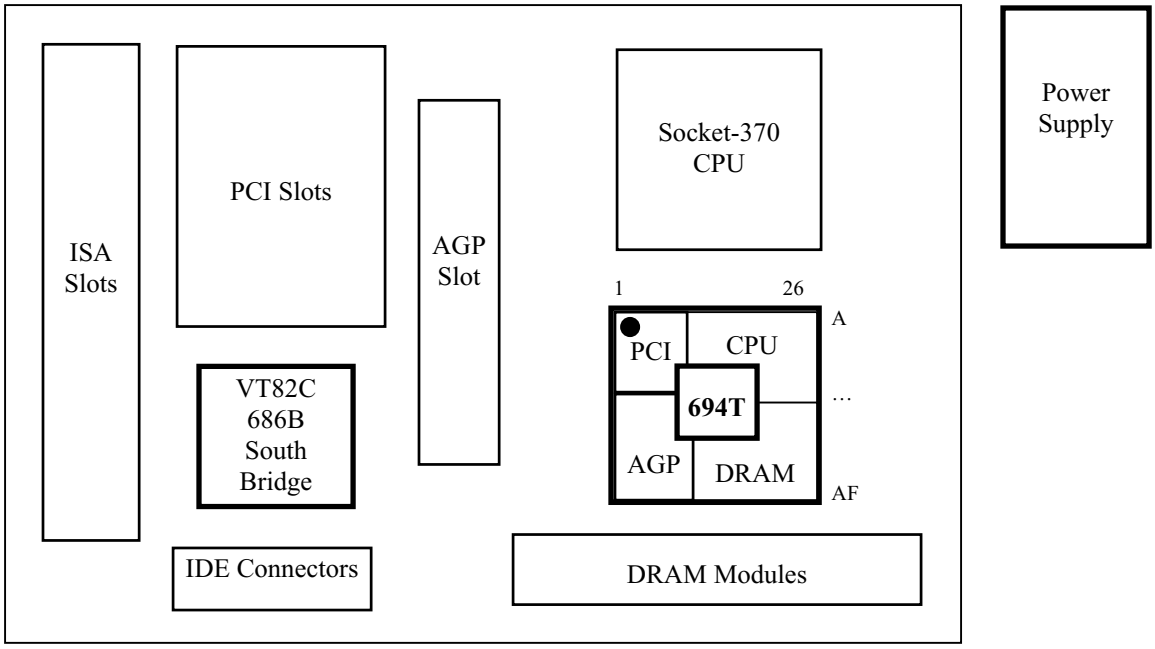
# PIN DESCRIPTIONS

**Table 3. VT82C694T Pin Descriptions**

| CPU Interface | | | |
|---|---|---|---|
| **Signal Name** | **Pin #** | **I/O** | **Signal Description** |
| **HA[31:3]#** | (see pinout tables) | IO | **Host Address Bus.** HA[31:3] connect to the address bus of the host CPU. During CPU cycles HA[31:3] are inputs. These signals are driven by the VT82C694T during cache snooping operations. |
| **HD[63:0]#** | (see pinout tables) | IO | **Host CPU Data.** These signals are connected to the CPU data bus. |
| **ADS#** | K21 | IO | **Address Strobe**. The CPU asserts ADS# in T1 of the CPU bus cycle. |
| **BNR#** | H24 | IO | **Block Next Request**. Used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth. |
| **BPRI#** | H26 | IO | **Priority Agent Bus Request**. The owner of this signal will always be the next bus owner. This signal has priority over symmetric bus requests and causes the current symmetric owner to stop issuing new transactions unless the HLOCK# signal is asserted. The VT82C694T drives this signal to gain control of the processor bus. |
| **DBSY#** | L23 | IO | **Data Bus Busy**. Used by the data bus owner to hold the data bus for transfers requiring more than one cycle. |
| **DEFER#** | J26 | IO | **Defer**. The VT82C694T uses a dynamic deferring policy to optimize system performance. The VT82C694T also uses the DEFER# signal to indicate a processor retry response. |
| **DRDY#** | K23 | IO | **Data Ready**. Asserted for each cycle that data is transferred. |
| **HIT#** | L24 | IO | **Hit**. Indicates that a cacheing agent holds an unmodified version of the requested line. Also driven in conjunction with HITM# by the target to extend the snoop window. |
| **HITM#** | L22 | I | **Hit Modified**. Asserted by the CPU to indicate that the address presented with the last snoop cycle is modified in the L1 cache and needs to be written back. |
| **HLOCK#** | K22 | I | **Host Lock**. All CPU cycles sampled with the assertion of HLOCK# and ADS# until the negation of HLOCK# must be atomic. |
| **HREQ[4:0]#** | J25, K25, K24, J23, J22 | IO | **Request Command**. Asserted during both clocks of the request phase. In the first clock, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type. |
| **HTRDY#** | H25 | IO | **Host Target Ready**. Indicates that the target of the processor transaction is able to enter the data transfer phase. |
| **RS[2:0]#** | L25, L26, K26 | IO | **Response Signals**. Indicates the type of response per the table below:<br>**RS[2:0]#** — **Response type**<br>000 — Idle State<br>001 — Retry Response<br>010 — Defer Response<br>011 — Reserved<br>100 — Hard Failure<br>101 — Normal Without Data<br>110 — Implicit Writeback<br>111 — Normal With Data |
| **CPURST#** | B23 | O | **CPU Reset.** Reset output to CPU |
| **CPURSTD#** | M26 | O | **CPU Reset Delayed.** Reset output delayed 2T from CPURST#. Used to enable an external LV244 buffer for fraction / ratio selection. |
| **BREQ0#** | B26 | O | **Bus Request 0.** Bus request output to CPU. |

Note: Clocking of the CPU interface is performed with HCLK. See the clock pin group at the end of the pin descriptions section for descriptions of the clock pins.

The VT82C694T pinouts were defined assuming the ATX PCB layout model shown below (and general pin layout shown) as a guide for PCB component placement. Other PCB layouts (AT, LPX, and NLX) were also considered and can typically follow the same general component placement.



## DRAM Interface

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **MD[63:0]** | (see pinout tables) | IO | **Memory Data.** These signals are connected to the DRAM data bus.<br><br>Note: MD0 is internally pulled up for use in EDO memory type detection. |
| **MECC[7:0]** | AA26, AA23, AA10, AE11, Y22, AA25, AD12, AF11 | IO | **DRAM ECC or EC Data** (see Rx6E) |
| **MAA14 / DCLKRD**<br>**MAA[13:0]** | (see pinout tables) | O / I<br>O | **Memory Address A.** DRAM address lines (two sets for better drive) |
| **MAB[14]#,**<br>**MAB[13]#,**<br>**MAB[12]#** / strap,<br>**MAB[11]#** / strap,<br>**MAB[10]** / strap,<br>**MAB[9]#** / strap,<br>**MAB[8]#** / strap,<br>**MAB[7]#** / strap,<br>**MAB[6]#** / strap,<br>**MAB[5]#** / strap,<br>**MAB[4:0]#** | AE22,<br>AF22,<br>AD21,<br>AE21,<br>AB20,<br>AC20,<br>AF20,<br>AB19,<br>AB18,<br>AD19,<br>AE18, AB17, AD17,<br>AC16, AD16 | O | **Memory Address B.** DRAM address lines (two sets for better drive). Note that this set of memory address pins is opposite polarity from the "A" set (except for MAB10 which must be positive polarity because it is used for the SDRAM Precharge command). Selected pins are also used for strap options:<br>MAB12# CPU Bus Frequency Select 0 — Bit Rx68[0] — Internal PD<br>MAB11# In-Order Queue Depth Enable — Rx50[7] — PU<br>MAB10 Quick Start Select — Rx52[5] — PD<br>MAB9# AGP Disable — RxAC[7] — PD<br>MAB8# CPU Bus Frequency Select 1 — Rx68[1] — PD<br>MAB7# Memory Module Configuration — Rx6B[4] — PD<br>MAB6# GTL I/O Buffer Pullup — Rx52[7] — PD<br>MAB5# PCI 33 / 66 MHz Select — Rx7B[0] — none |
| **CSA[5:0]#** /<br>RASA[5:0]# | AE16, AD15, AC15,<br>AE15, AF15, AB14 | O | **Multifunction Pins** (two sets for better drive)<br>1. Synchronous DRAM: Chip select of each bank..<br>2. FPG/EDO DRAM: Row Address Strobe of each bank. |
| **CSB[5:0]#** /<br>RASB[5:0]# | AB23, AC26, AC24,<br>AD26, AD24, AE25 | O | **Multifunction Pins** (two sets for better drive)<br>1. Synchronous DRAM: Chip select of each bank..<br>2. FPG/EDO DRAM: Row Address Strobe of each bank. |
| **DQMA[7:0]** /<br>CASA[7:0]# | AB26, AC25, AC13,<br>AD13, AA24, AA22,<br>AC14, AE14 | O | **Multifunction Pins**<br>1. Synchronous DRAM: Data mask of each byte.<br>2. FPG/EDO DRAM: Column Address Strobe of each byte lane. |
| **DQMB5** / CASB5#,<br>**DQMB1** / CASB1# | AE13<br>AD14 | O | **Multifunction Pins**<br>1. Synchronous DRAM: Data mask of bytes 5 and 1<br>2. FPG/EDO DRAM: Column Address Strobe of bytes 5 and 1 |
| **SRASA#,**<br>**SRASB#** | AF16,<br>AA17 | O | **Row Address Command Indicator.** (two sets for better drive) |
| **SCASA#,**<br>**SCASB#** | AF12,<br>AB13 | O | **Column Address Command Indicator.** (two sets for better drive) |
| **SWEA#** / MWEA#,<br>**SWEB#** / MWEB# | AE12,<br>AC12 | O | **Write Enable Command Indicator.** (two sets for better drive) |
| **CKE0** / FENA,<br>**CKE1** / GCKE,<br>**CKE2** / CSB6#,<br>**CKE3** / CSB7#,<br>**CKE4** / CSA6#,<br>**CKE5** / CSA7# | AC22,<br>AF23,<br>AE24,<br>AD23,<br>AC23,<br>AF24 | O | **Clock Enables.** Clock enables for each DRAM bank (Rx78[0]=1) for powering down the SDRAMs in notebook applications. Also used in desktop systems for clock control for reducing power usage and for reducing heat/temperature in high-speed memory systems. Alternate functions: FENA = FET Enable, GCKE = Global CKE. |

| PCI Bus Interface | | | |
|---|---|---|---|
| **Signal Name** | **Pin #** | **I/O** | **Signal Description** |
| **AD[31:0]** | (see pinout tables) | IO | **Address/Data Bus.** The standard PCI address and data lines. The address is driven with FRAME# assertion and data is driven or received in following cycles. |
| **CBE[3:0]#** | C4, E4, G3, J4 | IO | **Command/Byte Enable.** Commands are driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks. |
| **FRAME#** | E1 | IO | **Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator. |
| **IRDY#** | E2 | IO | **Initiator Ready.** Asserted when the initiator is ready for data transfer. |
| **TRDY#** | F5 | IO | **Target Ready.** Asserted when the target is ready for data transfer. |
| **STOP#** | F4 | IO | **Stop.** Asserted by the target to request the master to stop the current transaction. |
| **DEVSEL#** | F3 | IO | **Device Select.** This signal is driven by the VT82C694T when a PCI initiator is attempting to access main memory. It is an input when the VT82C694T is acting as a PCI initiator. |
| **PAR** | G5 | IO | **Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0]. |
| **SERR#** | F1 | IO | **System Error.** VT82C694T will pulse this signal when it detects a system error condition. |
| **LOCK#** | F2 | IO | **Lock.** Used to establish, maintain, and release resource lock. |
| **PREQ#** | B6 | I | **South Bridge Request.** This signal comes from the South Bridge. PREQ# is the South Bridge request for the PCI bus. It should be connected to PREQ# of the VT82C686A or to PREQL# of the VT8231. |
| **PGNT#** | D6 | O | **South Bridge Grant.** This signal driven by the VT82C694T to grant PCI access to the South Bridge. It should be connected to PGNT# of the VT82C686A or to PGNTL# of the VT8231. |
| **REQ[4:0]#** | D10, D8, F10, C7, A3 | I | **PCI Master Request.** PCI master requests for PCI. Device 0 Rx76[0] may be used to enable REQ4# as a high priority request for use with on-board high-bandwidth PCI controllers or for connection to PREQH# of the VT8231 South Bridge. These inputs thus allow support for either 5 PCI slots or 4 slots plus one high-priority on-board master (6 slots plus 2 high-priority masters with the VT8231). |
| **GNT[4:0]#** | E9, E8, E10, D7, E7 | O | **PCI Master Grant.** Permission is given to the master to use PCI. GNT4# may be used for connection to the grant input of an on-board high priority device or for connection to PGNTH# of the VT8231. These inputs thus allow support for either 5 PCI slots or 4 slots plus one high-priority on-board master (6 slots plus 2 high-priority masters with the VT8231). |
| **WSC#** | AE3 | O | **Write Snoop Complete.** Sideband PCI signal (used on the planar only in multiprocessor configurations) asserted to indicate that all snoop activity on the CPU bus initiated by the last PCI-to-DRAM write is complete and that it is safe to send an APIC interrupt message. Basically this signal is always active except when PCI master write data is not flushed. |

Note: Clocking of the PCI interface is performed with PCLK; see the clock pin group at the end of the pin descriptions section for descriptions of the clock pins.

| AGP Bus Interface | | | |
|---|---|---|---|
| **Signal Name** | **Pin #** | **I/O** | **Signal Description** |
| **GD[31:0]** | (see pinout tables) | IO | **Address/Data Bus.** The standard AGP/PCI address and data lines. The address is driven with GDS0# and GDS1# assertion for AGP transfers and is driven with GFRM# assertion for PCI transfers. |
| **GDS0** | Y5 | IO | **Bus Strobe 0 (AGP transactions only).** Provides timing for 2x data transfer mode on AD[15:0]. The agent that is providing the data drives this signal. |
| **GDS0#** | U5 | IO | **Bus Strobe 0 complement and Bus Strobe 0 (AGP transactions only).** Provides timing for 4x data transfer mode on AD[15:0]. The agent that is providing the data drives this signal. |
| **GDS1** | T6 | IO | **Bus Strobe 1 (AGP transactions only).** Provides timing for 2x data transfer mode on AD[31:16]. The agent that is providing the data drives this signal. |
| **GDS1#** | T5 | IO | **Bus Strobe 1 complement and Bus Strobe 1 (AGP transactions only).** Provides timing for 4x data transfer mode on AD[31:16]. The agent that is providing the data drives this signal. |
| **GBE[3:0]#** | T3, V5, Y4, AB3 | IO | **Command/Byte Enable.**<br>**AGP:** These pins provide command information (different commands than for PCI) driven by the master (graphics controller) when requests are being enqueued using PIPE#. These pins provide valid byte information during AGP write transactions and are driven by the master. The target (this chip) drives these lines to "0000" during the return of AGP read data, but the state of these pins is ignored by the AGP master.<br>**PCI:** Commands are driven with GFRM# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks. |
| **GFRM#** | W2 | IO | **Frame (PCI transactions only).** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator. |
| **GIRDY#** | W3 | IO | **Initiator Ready**<br>**AGP:** For write operations, the assertion of this pin indicates that the master is ready to provide *all* write data for the current transaction. Once this pin is asserted, the master is not allowed to insert wait states. For read operations, the assertion of this pin indicates that the master is ready to transfer a subsequent block of read data. The master is *never* allowed to insert a wait state during the initial block of a read transaction. However, it may insert wait states after each block transfers.<br>**PCI:** Asserted when the initiator is ready for data transfer. |
| **GTRDY#** | Y2 | IO | **Target Ready:**<br>**AGP:** Indicates that the target is ready to provide read data for the entire transaction (when the transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfers on both read and write transactions.<br>**PCI:** Asserted when the target is ready for data transfer. |
| **GSTOP#** | V4 | IO | **Stop (PCI transactions only).** Asserted by the target to request the master to stop the current transaction. |
| **GDSEL#** | W5 | IO | **Device Select (PCI transactions only).** This signal is driven by the VT82C694T when a PCI initiator is attempting to access main memory. It is an input when the VT82C694T is acting as PCI initiator. Not used for AGP cycles. |

Note: Clocking of the AGP interface is performed with GCLK; see the clock pin group for descriptions of the clock pins.

Note: PCB Layout Guidelines (reference from AGP specification)

1. Total motherboard trace length 10" max, trace impedance = 65 ohms ± 15 ohms, minimize signal crosstalk
2. Trace lengths within groups matched to within 2 inches or better

   Groups are:
   a. GDS0#, GDS0, GD15-0, GBE1-0#
   b. GDS1#, GDS1, GD31-16, GBE3-2#
   c. SBS#, SBS, SBA7-0

3. Ground isolation should be provided around GDS0#, GDS0, GDS1# and GDS1 to prevent crosstalk with GD[31:0]. Ideally ground traces should be provided adjacent to GDSn# on the same signal layer, but at a minimum wider spaces should be provided on either side (e.g., 16 mil spaces on either side of GDSn# if GDSn# signal traces are 8 mil).

| AGP Bus Interface (continued) | | | |
|---|---|---|---|
| **Signal Name** | **Pin #** | **IO** | **Signal Description** |
| **GPIPE#** | M3 | I | **Pipelined Request.** Asserted by the master (graphics controller) to indicate that a full-width request is to be enqueued by the target VT82C694T. The master enqueues one request each rising edge of GCLK while GPIPE# is asserted. When GPIPE# is deasserted no new requests are enqueued across the AD bus. |
| **GRBF#** | N6 | I | **Read Buffer Full.** Indicates if the master (graphics controller) is ready to accept previously requested low priority read data. When GRBF# is asserted, the VT82C694T will not return low priority read data to the master. |
| **GWBF#** | M6 | I | **Write Buffer Full.** |
| **SBA[7:0]** | P1, P2, P5, P4, N2, M1, M2, L2 | I | **SideBand Address.** Provides an additional bus to pass address and command information from the master (graphics controller) to the target (the VT82C694T). These pins are ignored until enabled. |
| **SBS** | N3 | I | **Sideband Strobe.** Provides timing for SBA[7:0] (driven by the master) |
| **SBS#** | M5 | I | **Sideband Strobe complement and SBS .** Provides timing for SBA[7:0] (driven by the master) when 4x timing is supported. |
| **ST[2:0]** | M4, L1, L4 | O | **Status (AGP only).** Provides information from the arbiter to a master to indicate what it may do. Only valid while GGNT# is asserted.<br>000 Indicates that previously requested low priority read or flush data is being returned to the master (graphics controller).<br>001 Indicates that previously requested high priority read data is being returned to the master.<br>010 Indicates that the master is to provide low priority write data for a previously enqueued write command.<br>011 Indicates that the master is to provide high priority write data for a previously enqueued write command.<br>100 Reserved. (arbiter must not issue, may be defined in the future).<br>101 Reserved. (arbiter must not issue, may be defined in the future).<br>110 Reserved. (arbiter must not issue, may be defined in the future).<br>111 Indicates that the master (graphics controller) has been given permission to start a bus transaction. The master may enqueue AGP requests by asserting PIPE# or start a PCI transaction by asserting GFRM#. ST[2:0] are always outputs from the VT82C694T and inputs to the master. |
| **GREQ#** | L5 | I | **Request.** Master request for AGP. |
| **GGNT#** | L3 | O | **Grant.** Permission is given to the master to use AGP. |
| **GPAR** | Y1 | IO | **AGP Parity.** A single parity bit is provided over GD[31:0] and GBE[3:0]. |

Note: For PCI operation on the AGP bus, the following pins are not required:
- PERR# (parity and error reporting not required on transient data devices such as graphics controllers)
- LOCK# (no lock requirement on AGP)
- IDSEL (internally connected to AD16 on AGP-compliant masters)

Note: Separate system interrupts are not provided for AGP. The AGP connector provides interrupts via PCI bus INTA-B#.

Note: The AGP bus supports only one master directly (REQ[3:0]# and GNT[3:0]# are not provided). External logic is required to implement additional master capability. Note that the arbitration mechanism on the AGP bus is different from the PCI bus.

Note: A separate reset is not required for the AGP bus (RESET# resets both PCI and AGP buses)

Note: Two mechanisms are provided by the AGP bus to enqueue master requests: GPIPE# (to send addresses multiplexed on the AD lines) and the SBA port (to send addresses unmultiplexed). AGP masters implement one or the other or select one at initialization time (they are not allowed to change during runtime). Therefore only one of the two will be used and the signals associated with the other will not be used. Therefore the VT82C694T has an internal pullup on GRBF# to maintain it in the de-asserted state in case it is not implemented on the master device.

## Clock / Reset Control

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **HCLK** | N23 | I | **Host Clock.** This pin receives the host CPU clock (66 / 100 / 133 MHz). This clock is used by all VT82C694T logic that is in the host CPU domain. |
| **PCLK** | B2 | I | **PCI Clock.** This pin receives a buffered host clock divided-by-2, 3, or 4 to create 33 MHz. This clock is used by all of the VT82C694T logic that is in the PCI clock domain. This clock input must be 33 MHz maximum to comply with PCI specification requirements and must be synchronous with the host CPU clock, HCLK, with an HCLK:PCLK frequency ratio of 2:1, 3:1, or 4:1 as shown in the table below. The host CPU clock must lead the PCI clock by 2.0 ± 1.0 nsec.<br>Typical Clock Frequency Combinations<br>Rx68[1:0] / Mode / Host Clock / AGP Clock / PCI Clock<br>00 / 2x / 66 MHz / 66 MHz / 33 MHz<br>01 / 3x / 100 MHz / 66 MHz / 33 MHz<br>10 / 4x / 133 MHz / 66 MHz / 33 MHz<br>11 / Reserved |
| **GCLK** | N5 | I | **AGP Clock.** This pin receives the AGP bus clock (66 MHz). This clock is used by all VT82C694T logic that is in the AGP clock domain. The AGP clock must be synchronous / pseudo-synchronous to the host CPU clock (selectable as shown in the table above). |
| **GCLKO** | N4 | O | **AGP Clock Feedback.** |
| **DCLKO** | AB21 | O | **DRAM Clock.** Output from internal clock generator to the external clock buffer. |
| **DCLKWR** | AD25 | I | **DRAM Clock Input.** Input from the external clock buffer. |
| **DCLKRD / MAA14** | AB22 | I / O | **DRAM Clock Input.** No function (used for chip test). MAA14 if Rx69[5]=1. |
| **RESET#** | A6 | I | **Reset.** Input from south bridge chip. When asserted, this signal resets the VT82C694T and sets all register bits to the default value. The same signal that connects to this pin may also be used (connected through an external inverter) to reset the ISA bus (if implemented). The rising edge of this signal is used to sample all power-up strap options (see HA25-27). |
| **PWROK** | AF3 | I | **Power OK.** |
| **CPURST#** | B23 | O | **CPU Reset.** CPU Reset output to the CPU. |
| **CPURSTD#** | M26 | O | **CPU Reset Delayed.** Reset output delayed 2T from CPURST#. Used to enable an external LV244 buffer for fraction / ratio selection. |
| **SUST#** | AA12 | I | **Suspend Status.** For implementation of the Suspend-to-DRAM feature. Connect to an external pullup to disable. |

| Power, Ground, and Test | | | |
|---|---|---|---|
| **Signal Name** | **Pin #** | **I/O** | **Signal Description** |
| **VCC** | (see pin list) | P | **Power** for **Internal Logic** (3.3V ±5%). |
| **GND** | (see pin list) | P | **Ground** |
| **VSUS** | AA11 | P | **Suspend Power** (3.3V ±5%). |
| **VCCA** | N22, V6, Y21 | P | **Analog Power** (3.3V ±5%). For internal clock logic. |
| **GNDA** | M22, U7, W21 | P | **Analog Ground.** For internal clock logic. Connect to main ground plane. |
| **VCCQ** | L6-L7, R3, R6-R7, W6, AA3, AA7, AE2 | P | **AGP 1.5V or 3.3V Power.** 1.5V is used for AGP 4x transfer mode. 3.3V is used for AGP 2x mode. |
| **VCCQQ** | AD4 | P | **AGP Quiet Power.** |
| **GNDQQ** | AD5 | | **AGP Quiet Ground.** |
| **VTT** | F11-F12, F15-F17, J18, K18, L18, L21, M24 | P | **CPU Interface Termination Voltage** (1.5V ±10%). |
| **GTLREF** | E16, M23 | P | **CPU Interface GTL+ Voltage Reference.** 2/3 VTT ±2% |
| **AGPREF** | N1 | P | **AGP Voltage Reference.** 0.4 VCCQ (1.32V) when VCCQ is 3.3V and 0.5 VCCQ (0.75V) when VCCQ is 1.5V. Check the VT82C694T Design Guide for additional information. AGPREF for 3.3V signaling is generated internally by the VT82C694T. AGPREF for 1.5V signaling is generated on the motherboard. |
| **PCOMP** | AF2 | I | **Compensation.** Connect to GND through a 60 ohm resistor. |
| **TESTIN#** | M25 | I | **Test Input.** NAND tree / tristate mode test select. |

# REGISTERS

## Register Overview

The following tables summarize the configuration and I/O registers of the VT82C694T. These tables also document the power-on default value ("Default") and access type ("Acc") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved / used (essentially the same as RO), and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions following these tables for details). All offset and default values are shown in hexadecimal unless otherwise indicated.

**Table 4. VT82C694T Registers**

**VT82C694T I/O Ports**

| Port # | I/O Port | Default | Acc |
|---|---|---|---|
| 22 | PCI / AGP Arbiter Disable | 00 | RW |
| CFB-8 | Configuration Address | 0000 0000 | RW |
| CFF-C | Configuration Data | 0000 0000 | RW |

## VT82C694T Device 0 Registers - Host Bridge

### Header Registers

| Offset | Configuration Space Header | Default | Acc |
|---|---|---|---|
| 1-0 | Vendor ID | **1106** | RO |
| 3-2 | Device ID | **0691** | RO |
| 5-4 | Command | **0006** | **RW** |
| 7-6 | Status | **0210** | **WC** |
| 8 | Revision ID (CD: V=8, CE: V=C) | **Vn** | RO |
| 9 | Program Interface | 00 | RO |
| A | Sub Class Code | 00 | RO |
| B | Base Class Code | **06** | RO |
| C | Reserved | 00 | — |
| D | Latency Timer | 00 | **RW** |
| E | Header Type | 00 | RO |
| F | Built In Self Test (BIST) | 00 | RO |
| 13-10 | Graphics Aperture Base | **0000 0008** | **RW** |
| 14-27 | Reserved | 00 | — |
| 28-2B | Reserved | 00 | — |
| 2D-2C | Subsystem Vendor ID | 0000 | **W1** |
| 2F-2E | Subsystem ID | 0000 | **W1** |
| 33-30 | Reserved | 00 | — |
| 37-34 | Capability Pointer | **0000 00A0** | RO |
| 3F-38 | Reserved | 00 | — |

### Device-Specific Registers

| Offset | Host CPU Protocol Control | Default | Acc |
|---|---|---|---|
| 50 | Request Phase Control | 00 | RW |
| 51 | Response Phase Control | 00 | RW |
| 52 | Dynamic Defer Timer | **90** | RW |
| 53 | Miscellaneous 1 | **03** | RW |
| 54 | Miscellaneous 2 | 00 | RW |
| 55 | Reserved | 00 | — |

| Offset | DRAM Control | Default | Acc |
|---|---|---|---|
| 59-58 | MA Map Type | **0040** | RW |
| 5F-5A | DRAM Row Ending Address: | | |
| 5A | Bank 0 Ending (HA[31:24]) | **01** | RW |
| 5B | Bank 1 Ending (HA[31:24]) | **01** | RW |
| 5C | Bank 2 Ending (HA[31:24]) | **01** | RW |
| 5D | Bank 3 Ending (HA[31:24]) | **01** | RW |
| 5E | Bank 4 Ending (HA[31:24]) | **01** | RW |
| 5F | Bank 5 Ending (HA[31:24]) | **01** | RW |
| **56** | Bank 6 Ending (HA[31:24]) | **01** | RW |
| **57** | Bank 7 Ending (HA[31:24]) | **01** | RW |
| 60 | DRAM Type | 00 | RW |
| 61 | ROM Shadow Control C0000-CFFFF | 00 | RW |
| 62 | ROM Shadow Control D0000- | 00 | RW |
| 63 | ROM Shadow Control E0000-FFFFF | 00 | RW |
| 64 | DRAM Timing for Banks 0,1 | **EC** | RW |
| 65 | DRAM Timing for Banks 2,3 | **EC** | RW |
| 66 | DRAM Timing for Banks 4,5 | **EC** | RW |
| 67 | DRAM Timing for Banks 6,7 | **EC** | RW |
| 68 | DRAM Control | 00 | RW |
| 69 | DRAM Clock Select | 00 | RW |
| 6A | DRAM Refresh Counter | 00 | RW |
| 6B | DRAM Arbitration Control | **01** | RW |
| 6C | SDRAM Control | 00 | RW |
| 6D | DRAM Control Drive Strength | 00 | RW |
| 6E | ECC Control | 00 | RW |
| 6F | ECC Status | 00 | **RO** |

### Device-Specific Registers (continued)

| Offset | PCI Bus Control | Default | Acc |
|---|---|---|---|
| 70 | PCI Buffer Control | 00 | RW |
| 71 | CPU to PCI Flow Control 1 | 00 | RW |
| 72 | CPU to PCI Flow Control 2 | 00 | RW |
| 73 | PCI Master Control 1 | 00 | RW |
| 74 | PCI Master Control 2 | 00 | RW |
| 75 | PCI Arbitration 1 | 00 | RW |
| 76 | PCI Arbitration 2 | 00 | RW |
| 77 | Chip Test (do not program) | 00 | RW |
| 78 | PMU Control | 00 | RW |
| 79 | PMU Control | 00 | RW |
| 7A | Miscellaneous Control 1 | 00 | RW |
| 7B | Miscellaneous Control 2 | **02** | RW |
| 7C-7D | Reserved | 00 | — |
| 7E-7F | PLL Test Mode (do not program) | 00 | RW |

| Offset | GART/TLB Control | Default | Acc |
|---|---|---|---|
| 83-80 | GART/TLB Control | 0000 0000 | RW |
| 84 | Graphics Aperture Size | 00 | RW |
| 85-87 | Reserved (unassigned) | 00 | — |
| 8B-88 | Gr. Aperture TLB Base Register Base | 0000 0000 | RW |
| 9F-8C | Reserved (unassigned) | 00 | — |

| Offset | AGP Control | Default | Acc |
|---|---|---|---|
| A0 | AGP ID | **02** | RO |
| A1 | AGP Next Item Pointer | 00 | RO |
| A2 | AGP Specification Revision | **20** | RO |
| A3 | Reserved (unassigned) | 00 | — |
| A7-A4 | AGP Status | **1F00 0203** | RO |
| AB-A8 | AGP Command | 0000 0000 | **RW** |
| AC | AGP Control | **08** | **RW** |
| AD | AGP Latency Timer | **02** | RW |
| AE | AGP Miscellaneous Control | 00 | RW |
| AF | Reserved | 00 | — |
| B0 | AGP Compensation Control / Status | **8x** | RW |
| B1 | AGP Drive Strength | **63** | RW |
| B2-BF | Reserved | 00 | — |

| Offset | Miscellaneous Control | Default | Acc |
|---|---|---|---|
| C0-DF | Reserved | 00 | — |
| E0 | Miscellaneous Control | 00 | RW |
| E1-EF | Reserved | 00 | — |
| F7-F0 | BIOS Scratch Registers | 00 | RW |
| F8 | DRAM Arbitration Timer | 00 | RW |
| F9 | VGA Timer | 00 | RW |
| FB-FA | Reserved | 0000 | RW |
| FC | Back-Door Control 1 | 00 | RW |
| FD | Back-Door Control 2 | 00 | RW |
| FF-FE | Back-Door Device ID | 0000 | RW |

## VT82C694T Device 1 - PCI-to-PCI Bridge

### Header Registers

| Offset | Configuration Space Header | Default | Acc |
|---|---|---|---|
| 1-0 | Vendor ID | **1106** | RO |
| 3-2 | Device ID | **8598** | RO |
| 5-4 | Command | **0007** | **RW** |
| 7-6 | Status | **0220** | **WC** |
| 8 | Revision ID | **nn** | RO |
| 9 | Program Interface | 00 | RO |
| A | Sub Class Code | **04** | RO |
| B | Base Class Code | **06** | RO |
| C | Reserved | 00 | — |
| D | Latency Timer | 00 | **RW** |
| E | Header Type | **01** | RO |
| F | Built In Self Test (BIST) | 00 | RO |
| 17-10 | Reserved | 00 | — |
| 18 | Primary Bus Number | 00 | **RW** |
| 19 | Secondary Bus Number | 00 | **RW** |
| 1A | Subordinate Bus Number | 00 | **RW** |
| 1B | Secondary Latency Timer | 00 | RO |
| 1C | I/O Base | **F0** | **RW** |
| 1D | I/O Limit | 00 | **RW** |
| 1F-1E | Secondary Status | 0000 | RO |
| 21-20 | Memory Base | **FFF0** | **RW** |
| 23-22 | Memory Limit (Inclusive) | 0000 | **RW** |
| 25-24 | Prefetchable Memory Base | **FFF0** | **RW** |
| 27-26 | Prefetchable Memory Limit | 0000 | **RW** |
| 3D-28 | Reserved (unassigned) | 00 | — |
| 3F-3E | PCI-to-PCI Bridge Control | 00 | **RW** |

### Device-Specific Registers

| Offset | AGP Bus Control | Default | Acc |
|---|---|---|---|
| 40 | CPU-to-AGP Flow Control 1 | 00 | RW |
| 41 | CPU-to-AGP Flow Control 2 | 00 | RW |
| 42 | AGP Master Control | 00 | RW |
| 43 | AGP Master Latency Timer | 00 | RW |
| 44 | Back-Door Register Control | 00 | RW |
| 45 | Fast Write Control | **72** | RW |
| 47-46 | PCI-to-PCI Bridge Device ID | 0000 | RW |
| 48-7F | Reserved | 00 | — |
| 80 | Capability ID | **01** | **RO** |
| 81 | Next Pointer | 00 | **RO** |
| 82 | Power Management Capabilities 1 | **02** | **RO** |
| 83 | Power Management Capabilities 2 | 00 | **RO** |
| 84 | Power Management Control / Status | 00 | RW |
| 85 | Power Management Status | 00 | **RO** |
| 86 | PCI-PCI Bridge Support Extensions | 00 | **RO** |
| 87 | Power Management Data | 00 | **RO** |
| 88-FF | Reserved | 00 | — |

## Miscellaneous I/O

One I/O port is defined in the VT82C694T: Port 22.

**Port 22 – PCI / AGP Arbiter Disable ..... RW**

**7-2 Reserved** ..... always reads 0

**1 AGP Arbiter Disable**
- 0 Respond to GREQ# signal .....default
- 1 Do not respond to GREQ# signal

**0 PCI Arbiter Disable**
- 0 Respond to all REQ# signals .....default
- 1 Do not respond to any REQ# signals, including PREQ#

This port can be enabled for read/write access by setting bit-7 of Device 0 Configuration Register 78.

## Configuration Space I/O

All registers in the VT82C694T (listed above) are addressed via the following configuration mechanism:

**Mechanism #1**

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

**Port CFB-CF8 - Configuration Address ..... RW**

**31 Configuration Space Enable**
- 0 Disabled..... default
- 1 Convert configuration data port writes to configuration cycles on the PCI bus

**30-24 Reserved** .....always reads 0

**23-16 PCI Bus Number**
Used to choose a specific PCI bus in the system

**15-11 Device Number**
Used to choose a specific device in the system (devices 0 and 1 are defined for the VT82C694T)

**10-8 Function Number**
Used to choose a specific function if the selected device supports multiple functions (only function 0 is defined for the VT82C694T).

**7-2 Register Number (also called the "Offset")**
Used to select a specific DWORD in the VT82C694T configuration space

**1-0 Fixed** .....always reads 0

**Port CFF-CFC - Configuration Data ..... RW**

Refer to PCI Bus Specification Version 2.1 for further details on operation of the above configuration registers.

## Register Descriptions

### Device 0 Header Registers - Host Bridge

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number, function number, and device number equal to zero.

**Device 0 Offset 1-0 - Vendor ID (1106h).....RO**

**15-0 ID Code** (reads 1106h to identify VIA Technologies)

**Device 0 Offset 3-2 - Device ID (0691h) .....RO**

**15-0 ID Code** (reads 0691h to identify the VT82C694T)

**Device 0 Offset 5-4 –Command (0006h).....RW**

**15-10 Reserved** ..... always reads 0

**9 Fast Back-to-Back Cycle Enable** ..... RO
- 0 Fast back-to-back transactions only allowed to the same agent.....default
- 1 Fast back-to-back transactions allowed to different agents

**8 SERR# Enable** ..... RO
- 0 SERR# driver disabled.....default
- 1 SERR# driver enabled

(SERR# is used to report ECC errors).

**7 Address / Data Stepping**..... RO
- 0 Device never does stepping .....default
- 1 Device always does stepping

**6 Parity Error Response**.....**RW**
- 0 Ignore parity errors & continue.....default
- 1 Take normal action on detected parity errors

**5 VGA Palette Snoop**..... RO
- 0 Treat palette accesses normally.....default
- 1 Don't respond to palette accesses on PCI bus

**4 Memory Write and Invalidate Command**..... RO
- 0 Bus masters must use Mem Write.....default
- 1 Bus masters may generate Mem Write & Inval

**3 Special Cycle Monitoring**..... RO
- 0 Does not monitor special cycles.....default
- 1 Monitors special cycles

**2 Bus Master** ..... RO
- 0 Never behaves as a bus master
- 1 Can behave as a bus master .....default

**1 Memory Space** ..... RO
- 0 Does not respond to memory space
- 1 Responds to memory space.....default

**0 I/O Space** ..... RO
- 0 Does not respond to I/O space .....default
- 1 Responds to I/O space

**Device 0 Offset 7-6 – Status (0210h) .....RWC**

**15 Detected Parity Error**
- 0 No parity error detected..... default
- 1 Error detected in either address or data phase. This bit is set even if error response is disabled (command register bit-6). .....write one to clear

**14 Signaled System Error (SERR# Asserted)** .....always reads 0

**13 Signaled Master Abort**
- 0 No abort received ..... default
- 1 Transaction aborted by the master ..... .....write one to clear

**12 Received Target Abort**
- 0 No abort received ..... default
- 1 Transaction aborted by the target ..... .....write one to clear

**11 Signaled Target Abort** .....always reads 0
- 0 Target Abort never signaled

**10-9 DEVSEL# Timing**
- 00 Fast
- 01 Medium .....always reads 01
- 10 Slow
- 11 Reserved

**8 Data Parity Error Detected**
- 0 No data parity error detected ..... default
- 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and VT82C694T was initiator of the operation in which the error occurred. .....write one to clear

**7 Fast Back-to-Back Capable**.....always reads 0

**6 User Definable Features** .....always reads 0

**5 66MHz Capable**.....always reads 0

**4 Supports New Capability list** .....always reads 1

**3-0 Reserved** .....always reads 0

**Device 0 Offset 8 - Revision ID (8nh or Cnh)..... RO**

**7-0 Chip Revision Code**.....CD silicon reads 8nh (n = revision code) .....CE silicon reads Cnh

**Device 0 Offset 9 - Programming Interface (00h)..... RO**

**7-0 Interface Identifier**.....always reads 00

**Device 0 Offset A - Sub Class Code (00h) ..... RO**

**7-0 Sub Class Code**.....reads 00 to indicate Host Bridge

**Device 0 Offset B - Base Class Code (06h) ..... RO**

**7-0 Base Class Code**.. reads 06 to indicate Bridge Device

**Device 0 Offset D - Latency Timer (00h)..... RW**

Specifies the latency timer value in PCI bus clocks.

**7-3 Guaranteed Time Slice for CPU** ..... default=0

**2-0 Reserved** (fixed granularity of 8 clks).. always read 0
Bits 2-1 are writeable but read 0 for PCI specification compatibility. The programmed value may be read back in Offset 75 bits 5-4 (PCI Arbitration 1).

**Device 0 Host Bridge Header Registers (continued)**

**Device 0 Offset E - Header Type (00h).....RO**

**7-0 Header Type Code**..... reads 00: single function

**Device 0 Offset F - Built In Self Test (BIST) (00h) .....RO**

**7 BIST Supported**.....reads 0: no supported functions

**6-0 Reserved** ..... always reads 0

**Device 0 Offset 13-10 - Graphics Aperture Base (00000008h) .....RW**

**31-28 Upper Programmable Base Address Bits**..... def=0

**27-20 Lower Programmable Base Address Bits**..... def=0

These bits behave as if hardwired to 0 if the corresponding Graphics Aperture Size register bit (Device 0 Offset 84h) is 0.

| 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | (This Register) |
|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | (Gr Aper Size) |
| RW | RW | RW | RW | RW | RW | RW | RW | 1M |
| RW | RW | RW | RW | RW | RW | RW | 0 | 2M |
| RW | RW | RW | RW | RW | RW | 0 | 0 | 4M |
| RW | RW | RW | RW | RW | 0 | 0 | 0 | 8M |
| RW | RW | RW | RW | 0 | 0 | 0 | 0 | 16M |
| RW | RW | RW | 0 | 0 | 0 | 0 | 0 | 32M |
| RW | RW | 0 | 0 | 0 | 0 | 0 | 0 | 64M |
| RW | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 128M |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 256M |

**19-0 Reserved** ..... always reads 00008

Note: The locations in the address range defined by this register are prefetchable.

**Device 0 Offset 2D-2C – Subsystem Vendor ID (0000h)R/W1**

**15-0 Subsystem Vendor ID**..... default = 0

This register may be written once and is then read only.

**Device 0 Offset 2F-2E – Subsystem ID (0000h) ..... R/W1**

**15-0 Subsystem ID**..... default = 0

This register may be written once and is then read only.

**Device 0 Offset 37-34 - Capability Pointer (000000A0h) RO**

Contains an offset from the start of configuration space.

**31-0 AGP Capability List Pointer**..... always reads A0h

**Device 0 Configuration Registers - Host Bridge**

These registers are normally programmed once at system initialization time.

**Host CPU Control**

**Device 0 Offset 50 – Request Phase Control (00h).....RW**

**7 CPU Hardwired IOQ (In Order Queue) Size**
Default per strap on pin MAB11#During reset. This register can be written 0 to restrict the chip to one level of IOQ.
0 1-Level
1 4-Level

**6 Read-Around-Write**
0 Disable .....default
1 Enable

**5 Reserved** ..... always reads 0

**4 Defer Retry When HLOCK Active**
0 Disable .....default
1 Enable
Note: always set this bit to 1

**3-1 Reserved** ..... always reads 0

**0 CPU / PCI Master Read DRAM Timing**
0 Start DRAM read after snoop complete.....def
1 Start DRAM read before snoop complete

**Device 0 Offset 51 – Response Phase Control (00h) ..... RW**

**7 CPU Read DRAM 0ws for Back-to-Back Read Transactions**
0 Disable..... default
1 Enable
Setting this bit enables maximum read performance by allowing continuous 0 wait state reads for pipelined line reads. If this bit is not set, there will be at least 1T idle time between read transactions.

**6 CPU Write DRAM 0ws for Back-to-Back Write Transactions**
0 Disable..... default
1 Enable
Setting this bit enables maximum write performance by allowing continuous 0 wait state writes for pipelined line writes ands sustained 3T single writes. If this bit is not set, there will be at least 1T idle time between write transactions.

**5 Reserved** .....always reads 0

**4 Fast Response (HIT/HITM sample 1T earlier)**
0 Disable..... default
1 Enable

**3 Non-Posted IOW**
0 Disable..... default
1 Enable

**2-1 Reserved** .....always reads 0

**0 Concurrent PCI Master / Host Operation**
0 Disable – the CPU bus will be occupied (BPRI asserted) during the entire PCI operation .... def
1 Enable – the CPU bus is only requested before ADS# assertion

**Device 0 Offset 52 – Dynamic Defer Timer (90h) .....RW**

**7 GTL I/O Buffer Pullup**
..... default = inverse of MAB6# Strap
0 Disable
1 Enable .....no-strap default
The default value of this bit is determined by a strap on the MAB6# pin during reset.

**6 RAW Write Retire Policy (After 2 Writes)**
0 Disable .....default
1 Enable

**5 Quick Start Select** ..... default = MAB10 Strap
0 Disable .....no-strap default
1 Enable
The default value of this bit is determined by a strap on the MAB10 pin during reset.

**4-0 Snoop Stall Count**
00 Disable dynamic defer
01-1F Snoop stall count ..... default = 10h

**Device 0 Offset 53 – Miscellaneous 1 (03h) ..... RW**

**7 HREQ**
0 Disable..... default
1 Enable

**6 SDRAM Frequency Higher Than CPU Front Side Bus Frequency**
0 Disable..... default
1 Enable
Setting this bit enables the DRAM subsystem to run at a higher frequency than the CPU FSB frequency. When setting this bit, register bit Rx69[6] must also be set and only SDRAM type DIMM modules may be used. An EDO/SDRAM mix in the DRAM subsystem is not supported in this case.

**5 PCI/AGP Master-to-CPU / CPU-to-PCI/AGP Slave Concurrency**
0 Disable..... default
1 Enable

**4 HPRI Function**
0 Disable..... default
1 Enable

**3 P6Lock Function**
0 Disable..... default
1 Enable

**2 Line Write / Write Back Without Implicit Write Back Data**
0 Disable..... default
1 Enable

**1 PCI Master Pipeline Access**
0 Disable
1 Enable **..... default**

**0 Initialization of Fast Write Address Selection**
0 Tail
1 Head **..... default**

**Device 0 Offset 54 – Miscellaneous 2 (00h) ..... RW**

**7-6 Reserved (Do Not Program)**..... default = 0
**5-3 Reserved** .....always reads 0

**2 Zero Length Write**
0 Disable..... default
1 Enable.....this bit must be programmed to 1

**1 Invalidate CPU Internal Cache on PCI Master Access**
0 Disable..... default
1 Enable

**0 1-1-1-1 PMRDY for PCI Master Access**
0 Disable..... default
1 Enable

**DRAM Control**

These registers are normally set at system initialization time and not accessed after that during normal system operation. Some of these registers, however, may need to be programmed using specific sequences during power-up initialization to properly detect the type and size of installed memory (refer to the VIA Technologies VT82C694T BIOS porting guide for details).

**Table 5. System Memory Map**

| Space | Start | Size | Address Range | Comment |
|---|---|---|---|---|
| DOS | 0 | 640K | 00000000-0009FFFF | Cacheable |
| VGA | 640K | 128K | 000A0000-000BFFFF | Used for SMM |
| BIOS | 768K | 16K | 000C0000-000C3FFF | Shadow Ctrl 1 |
| BIOS | 784K | 16K | 000C4000-000C7FFF | Shadow Ctrl 1 |
| BIOS | 800K | 16K | 000C8000-000CBFFF | Shadow Ctrl 1 |
| BIOS | 816K | 16K | 000CC000-000CFFFF | Shadow Ctrl 1 |
| BIOS | 832K | 16K | 000D0000-000D3FFF | Shadow Ctrl 2 |
| BIOS | 848K | 16K | 000D4000-000D7FFF | Shadow Ctrl 2 |
| BIOS | 864K | 16K | 000D8000-000DBFFF | Shadow Ctrl 2 |
| BIOS | 880K | 16K | 000DC000-000DFFFF | Shadow Ctrl 2 |
| BIOS | 896K | 64K | 000E0000-000EFFFF | Shadow Ctrl 3 |
| BIOS | 960K | 64K | 000F0000-000FFFFF | Shadow Ctrl 3 |
| Sys Bus Init | 1MB D Top 4G-64K | — 64K | 00100000-DRAM Top DRAM Top-FFFEFFFF FFFEFFFF-FFFFFFFF | Can have hole 000Fxxxx alias |

**Device 0 Offset 59-58 - DRAM MA Map Type (0040h) RW**

**15-13 Bank 5/4 MA Map Type (see below)**
**12 Reserved** (Bank 5/4 Virtual Channel Enable)... def=0

**11-9 Bank 7/6 MA Map Type (see below)**
**8 Reserved** (Bank 7/6 Virtual Channel Enable)... def=0

**7-5 Bank 1/0 MA Map Type**
000 8-bit Column Address
001 9-bit Column Address
010 10-bit Column Address.....default
011 11-bit Column Address
100 12-bit Column Address (64Mb)
101 Reserved
11x Reserved

**Bank 0/1 MA Map Type (SDRAM)**
000 16Mbit SDRAM .....default
100 64Mbit SDRAM
101 Reserved
11x Reserved

**4 Reserved** (Bank 1/0 Virtual Channel Enable)... def=0

**3-1 Bank 3/2 MA Map Type (see above)**
**0 Reserved** (Bank 3/2 Virtual Channel Enable)... def=0

**Device 0 Offset 5F-5A – DRAM Row Ending Address:**

**Offset 5A – Bank 0 Ending (HA[31:24]) (01h) ..... RW**
**Offset 5B – Bank 1 Ending (HA[31:24]) (01h)..... RW**
**Offset 5C – Bank 2 Ending (HA[31:24]) (01h) ..... RW**
**Offset 5D – Bank 3 Ending (HA[31:24]) (01h) ..... RW**
**Offset 5E – Bank 4 Ending (HA[31:24]) (01h)..... RW**
**Offset 5F – Bank 5 Ending (HA[31:24]) (01h)..... RW**
**Offset 56 – Bank 6 Ending (HA[31:24]) (01h) ..... RW**
**Offset 57 – Bank 7 Ending (HA[31:24]) (01h) ..... RW**

Note : BIOS is required to fill the ending address registers for all banks even if no memory is populated. The endings have to be in incremental order.

**Device 0 Offset 60 – DRAM Type (00h) ..... RW**

**7-6 DRAM Type for Bank 7/6**
00 Reserved..... default
01 Reserved
10 Reserved
11 SDRAM
**5-4 DRAM Type for Bank 5/4** .....default=FPG
**3-2 DRAM Type for Bank 3/2** .....default=FPG
**1-0 DRAM Type for Bank 1/0** .....default=FPG

**Table 6. Memory Address Mapping Table**

**SDRAM**

| MA: | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 16Mb (0xx) | | | | **11** *11* | 22 PC | 21 24 | 20 23 | 19 10 | 18 9 | 17 8 | 16 7 | 15 6 | 14 5 | 13 4 | 12 3 | Row Bits Col Bits |
| 64Mb (100) 2/4 bank x4, x8, x16; 4-bank x32 | **25/26/27** | **24** *24* | 13 *13* | 12 *12* | 22 PC | 21 **26** | 20 **25** | 19 10 | 18 9 | 17 8 | 16 7 | 15 6 | 14 5 | **11** 4 | 23 3 | x4: 10 col x8: 9 col x16: 8 col x32: 8 col |

"PC" = "Precharge Control" (refer to SDRAM specifications)

16Mb 11x10, 11x9, and 11x8 configurations supported

64Mb x4: 12x10 4bank, 13x10 2bank
x8: 12x9 4bank, 13x9 2bank
x16: 12x8 4bank, 13x8 2bank
x32: 11x8 4bank

**Device 0 Offset 61 - Shadow RAM Control 1 (00h).....RW**

**7-6 CC000h-CFFFFh**
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

**5-4 C8000h-CBFFFh**
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

**3-2 C4000h-C7FFFh**
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

**1-0 C0000h-C3FFFh**
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

**Device 0 Offset 62 - Shadow RAM Control 2 (00h).....RW**

**7-6 DC000h-DFFFFh**
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

**5-4 D8000h-DBFFFh**
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

**3-2 D4000h-D7FFFh**
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

**1-0 D0000h-D3FFFh**
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

**Device 0 Offset 63 - Shadow RAM Control 3 (00h)..... RW**

**7-6 E0000h-EFFFFh**
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

**5-4 F0000h-FFFFFh**
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

**3-2 Memory Hole**
- 00 None ..... default
- 01 512K-640K
- 10 15M-16M (1M)
- 11 14M-16M (2M)

**1-0 SMI Mapping Control**

| | SMM | | Non-SMM | |
|---|---|---|---|---|
| | Code | Data | Code | Data |
| 00 | DRAM | DRAM | PCI | PCI |
| 01 | DRAM | DRAM | DRAM | DRAM |
| 10 | DRAM | PCI | PCI | PCI |
| 11 | DRAM | DRAM | DRAM | DRAM |

**Device 0 Offset 64 - DRAM Timing for Banks 0,1 (ECh)RW**
**Device 0 Offset 65 - DRAM Timing for Banks 2,3 (ECh)RW**
**Device 0 Offset 66 - DRAM Timing for Banks 4,5 (ECh)RW**
**Device 0 Offset 67 - DRAM Timing for Banks 6,7 (ECh)RW**

**SDRAM Settings for Registers 67-64**

**7 Precharge Command to Active Command Period**
- 0 $T_{RP}$ = 2T
- 1 $T_{RP}$ = 3T ..... default

**6 Active Command to Precharge Command Period**
- 0 $T_{RAS}$ = 5T
- 1 $T_{RAS}$ = 6T ..... default

**5-4 CAS Latency**
- 00 1T
- 01 2T
- 10 3T ..... default
- 11 reserved

**3 DIMM Type**
- 0 Standard
- 1 Registered ..... default

**2 ACTIVE Command to CMD Command Period**
- 0 2T
- 1 3T ..... default

**1-0 Bank Interleave**
- 00 No Interleave ..... default
- 01 2-way
- 10 4-way
- 11 Reserved

**Device 0 Offset 68 - DRAM Control (00h).....RW**

**7 SDRAM Open Page Control**
- 0 Always precharge SDRAM banks when accessing EDO/FPG DRAMs.....default
- 1 SDRAM banks remain active when accessing EDO/FPG banks

**6 Bank Page Control**
- 0 Allow only pages of the same bank active..def.
- 1 Allow pages of different banks to be active

**5 Reserved** ..... always reads 0

**4-3 Reserved (Do Not Program)** ..... always reads 0

**2 Burst Refresh**
- 0 Disable .....default
- 1 Enable (burst 4 times)

**1 System Frequency Divider**..... RO
This bit is latched from MAB8# at the rising edge of RESET# (see table below).

**0 System Frequency Divider**..... RO
This bit is latched from MAB12# at the rising edge of RESET#.
- 00 CPU Frequency = 66 MHz
- 01 CPU Frequency = 100 MHz
- 1x CPU Frequency = 133 MHz

Note: See also Rx69[7-6]
Note: MD0 is internally pulled up for EDO detection.

**Device 0 Offset 69 – DRAM Clock Select (00h)..... RW**

**7 CPU Operating Frequency Faster Than DRAM**
- 0 CPU Same As or Equal to DRAM ..... default
- 1 CPU Faster Than DRAM by 33 MHz

**6 DRAM Operating Frequency Faster Than CPU**
- 0 DRAM Same As or Equal to CPU ..... default
- 1 DRAM Faster Than CPU by 33 MHz

| Rx68[1-0] | Rx69[7-6] | CPU / DRAM |
|---|---|---|
| 00 | 00 | 66 / 66 (def) |
| 00 | 01 | 66 / 100† |
| 01 | 10 | 100 / 66 |
| 01 | 00 | 100 / 100 |
| 01 | 01 | 100 / 133† |
| 1x | 10 | 133 / 100 |
| 1x | 00 | 133 / 133 |

†Rx53[6] must also be set to 1 for DRAM > CPU

**5 256Mbit DRAM Support**
- 0 Disable (pin AB22 is DCLKRD) ..... default
- 1 Enable (pin AB22 is MAA14)

**4 DRAM Controller Command Register Output**
- 0 Disable..... default
- 1 Enable

**3 Fast DRAM Precharge for Different Bank**
- 0 Disable..... default
- 1 Enable

**2 DRAM 4K Page Enable (for 64Mbit DRAM)**
- 0 Disable..... default
- 1 Enable

**1 DIMM Type**
- 0 Unbuferred ..... default
- 1 Registered

**0 Reserved** .....always reads 0

**Device 0 Offset 6A - Refresh Counter (00h) .....RW**

**7-0 Refresh Counter** (in units of 16 MCLKs)

00 DRAM Refresh Disabled.....default
01 32 MCLKs
02 48 MCLKs
03 64 MCLKs
04 80 MCLKs
05 96 MCLKs
… …

The programmed value is the desired number of 16-MCLK units minus one.

**Device 0 Offset 6B - DRAM Arbitration Control (01h) RW**

**7-6 Arbitration Parking Policy**

00 Park at last bus owner..... default
01 Park at CPU side
10 Park at AGP side
11 Reserved

**5 Fast Read to Write turn-around**

0 Disable..... default
1 Enable

**4 Memory Module Configuration**.....RO

0 Normal Operation..... default
1 Unused Outputs Tristated (CSB#, DQMB, CKE, MAB, DCLKO)

This bit is latched from MAB7# at the rising edge of RESET#.

**3 MD Bus Second Level Strength Control**

0 Normal slew rate control ..... default
1 More slew rate control

**2 CAS Bus Second Level Strength Control**

0 Normal slew rate control ..... default
1 More slew rate control

**1 Virtual Channel-DRAM Enable**

0 Disable..... default
1 Enable

**0 Multi-Page Open**

0 Disable (page registers marked invalid and no page register update which causes non page-mode operation)
1 Enable ..... default

**Device 0 Offset 6C - SDRAM Control (00h).....RW**

**7-5 Reserved** ..... always reads 0

**4 CKE Configuration**

0 Rx6B[4]=0 CSA = CSA, CSB = CSB, CKE0=CKE0, CKE1 = CKE1

x Rx6B[4]=1 CSA = CSA, CSB = Float, CSB = Float, MAB = Float, CKE0 = CKE0, CKE1 = CKE0

1 Rx6B[4]=0 CSA = CSA, CSB = CSB, CKE3-2 = CSA7-6 CKE5-4 = CSB7-6 CKE1 = GCKE (Global CKE) CKE0 = FENA (FET Enable)

**3 Fast TLB Lookup**

0 Disable .....default

1 Enable

**2-0 SDRAM Operation Mode Select**

000 Normal SDRAM Mode.....default

001 NOP Command Enable

010 All-Banks-Precharge Command Enable (CPU-to-DRAM cycles are converted to All-Banks-Precharge commands).

011 MSR Enable CPU-to-DRAM cycles are converted to commands and the commands are driven on MA[14:0]. The BIOS selects an appropriate host address for each row of memory such that the right commands are generated on MA[14:0].

100 CBR Cycle Enable (if this code is selected, CAS-before-RAS refresh is used; if it is not selected, RAS-Only refresh is used)

101 Reserved

11x Reserved

**Device 0 Offset 6D - DRAM Drive Strength (00h) ..... RW**

**7 ESDRAM Memory Type**

0 Disable..... default

1 Enable

**6-5 Delay DRAM Read Latch**

00 No Delay ..... default

01 0.5 ns

10 1.0 ns

11 1.5 ns

**4 Memory Data Drive** (MD, MECC)

0 6 mA ..... default

1 8 mA

**3 SDRAM Command Drive** (SRAS#, SCAS#, SWE#)

0 16mA ..... default

1 24mA

**2 Memory Address Drive** (MA, WE#)

0 16mA ..... default

1 24mA

**1 CAS# Drive**

0 8 mA ..... default

1 12 mA

**0 RAS# Drive**

0 16mA ..... default

1 24mA

**Device 0 Offset 6E - ECC Control (00h) .....RW**

**7 ECC / EC Mode Select**
- 0 ECC Checking and Reporting.....default
- 1 ECC Checking, Reporting, and Correcting

**6 Reserved** ..... always reads 0

**5 Enable SERR# on ECC / EC Multi-Bit Error**
- 0 Don't assert SERR# for multi-bit errors .....def
- 1 Assert SERR# for multi-bit errors

**4 Enable SERR# on ECC / EC Single-Bit Error**
- 0 Don't assert SERR# for single-bit errors .....def
- 1 Assert SERR# for single-bit errors

**3 ECC / EC Enable - Bank 7/6 (DIMM 3)**
- 0 Disable (no ECC or EC for banks 7/6) ..default
- 1 Enable (ECC or EC per bit-7)

**2 ECC / EC Enable - Bank 5/4 (DIMM 2)**
- 0 Disable (no ECC or EC for banks 5/4) ..default
- 1 Enable (ECC or EC per bit-7)

**1 ECC / EC Enable - Bank 3/2 (DIMM 1)**
- 0 Disable (no ECC or EC for banks 3/2) ..default
- 1 Enable (ECC or EC per bit-7)

**0 ECC / EC Enable - Bank 1/0 (DIMM 0)**
- 0 Disable (no ECC or EC for banks 1/0) ..default
- 1 Enable (ECC or EC per bit-7)

Error checking / correction may be enabled bank-pair by bank-pair (DIMM by DIMM) by using bits 0-2 above. Bank pairs must be populated with 72-bit memory to enable for EC or ECC since the additional data bits must be present in either case. For this reason, if 64-bit memory is populated in a particular bank pair, the corresponding bit 0-2 should be set to 0 to disable both EC and ECC for that bank pair. For those bank pairs that have 72-bit memory available (and have the corresponding bit 0-2 set), either EC or ECC may be selected via bit-7 above (i.e., all enabled bank pairs will use EC or all will use ECC).

If error checking / reporting only (EC) is selected, all read and write cycles will use normal timing. Partial writes (with EC or ECC enabled) will use read-modify-write cycles to maintain correct error correction codes in the additional 8 data bits. If EC and ECC are disabled for a particular bank pair, partial writes to that bank pair will use the byte enables to write only the selected bytes (using normal write cycles and cycle timing). If error correction (ECC) is selected, the first read of a transaction will always have one additional cycle of latency.

| Bit-7 | Bits 2-0 | RMW | Error Checking | Error Correction |
|---|---|---|---|---|
| 0/1 | 0 | No | No | No |
| 0 | 1 | Yes | Yes | No |
| 1 | 1 | Yes | Yes | Yes |

**Device 0 Offset 6F - ECC Status (00h) .....RWC**

**7 Multi-bit Error Detected** ..... write of '1' resets

**6-4 Multi-bit Error DRAM Bank**..... default=0
Encoded value of the bank with the multi-bit error.

**3 Single-bit Error Detected** ..... write of '1' resets

**2-0 Single-bit Error DRAM Bank** ..... default=0
Encoded value of the bank with the single-bit error.

**PCI Bus Control**

These registers are normally programmed once at system initialization time.

**Device 0 Offset 70 - PCI Buffer Control (00h) .....RW**

**7 CPU to PCI Post-Write**
- 0 Disable .....default
- 1 Enable

**6 PCI Master to DRAM Post-Write**
- 0 Disable .....default
- 1 Enable

**5 Reserved** ..... always reads 0

**4 PCI Master to DRAM Prefetch**
- 0 Enable .....default
- 1 Disable

**3 Enhance CPU-to-PCI Write**
- 0 Normal operation .....default
- 1 Reduce 1 cycle when the CPU-to-PCI buffer becomes available after being full (PCI and AGP buses)

**2 PCI Master Read Caching**
- 0 Disable .....default
- 1 Enable

**1 Delay Transaction**
- 0 Disable .....default
- 1 Enable

**0 Slave Device Stopped Idle Cycle Reduction**
- 0 Normal Operation .....default
- 1 Reduce 1 PCI idle cycle when stopped by a slave device (PCI and AGP buses)

**Device 0 Offset 71 - CPU to PCI Flow Control 1 (00h). RW**

**7 Dynamic Burst**
- 0 Disable..... default
- 1 Enable (see note under bit-3 below)

**6 Byte Merge**
- 0 Disable..... default
- 1 Enable

**5 Reserved** .....always reads 0

**4 PCI I/O Cycle Post Write**
- 0 Disable..... default
- 1 Enable

**3 PCI Burst**
- 0 Disable..... default
- 1 Enable (bit7=1 will override this option)

| bit-7 | bit-3 | Operation |
|---|---|---|
| 0 | 0 | Every write goes into the write buffer and no PCI burst operations occur. |
| 0 | 1 | If the write transaction is a burst transaction, the information goes into the write buffer and burst transfers are later performed on the PCI bus. If the transaction is not a burst, PCI write occurs immediately (after a write buffer flush). |
| 1 | x | Every write transaction goes to the write buffer; burstable transactions will then burst on the PCI bus and non-burstable won't. This is the normal setting. |

**2 PCI Fast Back-to-Back Write**
- 0 Disable..... default
- 1 Enable

**1 Quick Frame Generation**
- 0 Disable..... default
- 1 Enable

**0 1 Wait State PCI Cycles**
- 0 Disable..... default
- 1 Enable

**Device 0 Offset 72 - CPU to PCI Flow Control 2 (00h) RWC**

**7 Retry Status**
- 0 No retry occurred.....default
- 1 Retry occurred..... **write 1 to clear**

**6 Retry Timeout Action**
- 0 Retry Forever (record status only).....default
- 1 Flush buffer for write or return all 1s for read

**5-4 Retry Limit**
- 00 Retry 2 times.....default
- 01 Retry 16 times
- 10 Retry 4 times
- 11 Retry 64 times

**3 Clear Failed Data and Continue Retry**
- 0 Flush the entire post-write buffer.....default
- 1 When data is posting and master (or target) abort fails, pop the failed data if any, and keep posting

**2 CPU Backoff on PCI Read Retry Failure**
- 0 Disable .....default
- 1 Backoff CPU when reading data from PCI and retry fails

**1 Reduce 1T for FRAME# Generation**
- 0 Disable .....default
- 1 Enable

**0 Reduce 1T for CPU read PCI slave**
- 0 Disable .....Default
- 1 Enable

**Device 0 Offset 73 - PCI Master Control 1 (00h)..... RW**

**7 Reserved** .....always reads 0

**6 PCI Master 1-Wait-State Write**
- 0 Zero wait state TRDY# response ..... default
- 1 One wait state TRDY# response

**5 PCI Master 1-Wait-State Read**
- 0 Zero wait state TRDY# response ..... default
- 1 One wait state TRDY# response

**4 Reserved** .....always reads 0

**3 Assert STOP# after PCI Master Write Timeout**
- 0 Disable..... default
- 1 Enable

**2 Assert STOP# after PCI Master Read Timeout**
- 0 Disable..... default
- 1 Enable

**1 LOCK# Function**
- 0 Disable..... default
- 1 Enable

**0 PCI Master Broken Timer Enable**
- 0 Disable..... default
- 1 Enable. Force into arbitration when there is no FRAME# 16 PCICLK's after the grant.

**Device 0 Offset 74 - PCI Master Control 2 (00h)..... RW**

**7 PCI Master Read Prefetch by Enhance Command**
- 0 Always Prefetch ..... default
- 1 Prefetch only if Enhance command

**6 Reserved (Do Not Program)**..... default = 0

**5 Reserved** .....always reads 0

**4 Dummy Request**..... default = 0

**3 PCI Delay Transaction Timeout**
- 0 Disable..... default
- 1 Enable

**2 Backoff CPU Immediately on CPU-to-AGP**
- 0 Disable..... default
- 1 Enable

**1-0 CPU/PCI Master Latency Timer Control**
- 00 AGP master reloads MLT timer..... default
- 01 AGP master falling edge reloads MLT timer
- 10 AGP master rising edge resets timer to 00 and AGP master falling edge reloads MLT timer
- 11 Reserved (do not program)

**Device 0 Offset 75 - PCI Arbitration 1 (00h).....RW**

**7 Arbitration Mechanism**
- 0 PCI has priority.....default
- 1 Fair arbitration between PCI and CPU

**6 Arbitration Mode**
- 0 REQ-based (arbitrate at end of REQ#) ..default
- 1 Frame-based (arbitrate at FRAME# assertion)

**5-4 Latency Timer**.....read only, reads Rx0D bits 2:1

**3-0 PCI Master Bus Time-Out**
(force into arbitration after a period of time)
- 0000 Disable .....default
- 0001 1x32 PCICLKs
- 0010 2x32 PCICLKs
- 0011 3x32 PCICLKs
- 0100 4x32 PCICLKs
- ... ...
- 1111 15x32 PCICLKs

**Device 0 Offset 76 - PCI Arbitration 2 (00h) ..... RW**

**7 PCI CPU-to-PCI Post-Write Retry Failed**
- 0 Continue retry attempt..... default
- 1 Go to arbitration

**6 CPU Latency Timer Bit-0**.....RO
- 0 CPU has at least 1 PCLK time slot when CPU has PCI bus
- 1 CPU has no time slot

**5-4 Master Priority Rotation Control**
- 0x Grant to CPU after every PCI master grant..... .....def=00
- 10 Grant to CPU after every 2 PCI master grants
- 11 Grant to CPU after every 3 PCI master grants

With setting 01, the CPU will always be granted access after the current bus master completes, no matter how many PCI masters are requesting. With setting 10, if other PCI masters are requesting during the current PCI master grant, the highest priority master will get the bus after the current master completes, but the CPU will be guaranteed to get the bus after that master completes. With setting 11, if other PCI masters are requesting, the highest priority will get the bus next, then the next highest priority will get the bus, then the CPU will get the bus. In other words, with the above settings, even if multiple PCI masters are continuously requesting the bus, the CPU is guaranteed to get access after every master grant (01), after every other master grant (10) or after every third master grant (11).

**3-2 REQn# to REQ4# Mapping**
- 00 REQ4#..... default
- 01 REQ0#
- 10 REQ1#
- 11 REQ2#

**1 Allow Backoff for CPU-to-PCI Quadword and High Doubleword Read Access to PCI slave**
- 0 Disable..... default
- 1 Enable

**0 REQ4# is High Priority Master**
- 0 Disable..... default
- 1 Enable

**Device 0 Offset 77 - Chip Test Mode (00h) ..... RW**

**7 Reserved (no function)**.....always reads 0

**6-0 Reserved (do not use)**..... default=0

**Device 0 Offset 78 - PMU Control I (00h).....RW**

**7 I/O Port 22 Access**
- 0 CPU access to I/O address 22h is passed on to the PCI bus.....default
- 1 CPU access to I/O address 22h is processed internally

**6 Suspend Refresh Type**
- 0 CBR Refresh.....default
- 1 Self Refresh

**5 Reserved** ..... always reads 0

**4 Dynamic Clock Control**
- 0 Normal (clock is always running).....default
- 1 Clock to various internal functional blocks is disabled when those blocks are not being used

**3 Reserved** ..... always reads 0

**2 GSTOP# Assertion**
- 0 Disable (GSTOP# is always high).....default
- 1 Enable (GSTOP# could be low)

**1 Reserved** ..... always reads 0

**0 Memory Clock Enable (CKE) Function**
- 0 CKE Function Disable.....default
- 1 CKE Function Enable

**Device 0 Offset 79 - PMU Control 2 (00h).....RW**

**7 Cache Controller Module Clock Dynamic Stop**
- 0 Disable.....default
- 1 Enable

**6 DRAM Controller Module Clock Dynamic Stop**
- 0 Disable.....default
- 1 Enable

**5 AGP Controller Module Clock Dynamic Stop**
- 0 Disable.....default
- 1 Enable

**4 PCI Controller Module Clock Dynamic Stop**
- 0 Disable.....default
- 1 Enable

**3 Pseudo Power Good**
- 0 Disable.....default
- 1 Enable

**2 Indicate SIO Request to DRAM Controller**
- 0 Disable.....default
- 1 Enable

**1-0 Reserved** ..... always reads 0

**Device 0 Offset 7A – Miscellaneous Control 1 (00h) ..... RW**

**7 No Time-Out Arbitration for Consecutive Frame Accesses**
- 0 Enable..... default
- 1 Disable

**6-5 Reserved** .....always reads 0

**4 Invalidate PCI / AGP Buffered (Cached) Read Data for CPU to PCI / AGP Accesses**
- 0 Enable..... default
- 1 Disable

**3 Background PCI-to-PCI Write Cycle Mode**
- 0 Disable..... default
- 1 Enable

**2-1 Reserved** .....always reads 0

**0 South Bridge PCI Master Force Timeout When PCI Master Occupancy Timer Is Up**
- 0 Disable..... default
- 1 Enable

**Device 0 Offset 7B – Miscellaneous Control 2 (02h) ..... RW**

**7-2 Reserved** .....always reads 0

**1 PCI Master Access PMRDY Select**
- 0 Tail
- 1 Head **..... default**

**0 PCI Bus Operating Freq.....strapped from MAB5#**
- 0 33 MHz..... default
- 1 66 MHz

**Device 0 Offset 7E – PLL Test Mode (00h)..... RW**

**7-6 Reserved (status)** .....RO

**5-0 Reserved (do not use)**..... default=0

**Device 0 Offset 7F – PLL Test Mode (00h)..... RW**

**7-0 Reserved (do not use)**..... default=0

## GART / Graphics Aperture Control

The function of the Graphics Address Relocation Table (GART) is to translate virtual 32-bit addresses issued by an AGP device into 4K-page based physical addresses for system memory access. In this translation, the upper 20 bits (A31-A12) are remapped, while the lower 12 address bits (A11-A0) are used unchanged.

A one-level fully associative lookup scheme is used to implement the address translation. In this scheme, the upper 20 bits of the virtual address are used to point to an entry in a page table located in system memory. Each page table entry contains the upper 20 bits of a physical address (a "physical page" address). For simplicity, each page table entry is 4 bytes. The total size of the page table depends on the GART range (called the "aperture size") which is programmable in the VT82C694T.

This scheme is shown in the figure below.

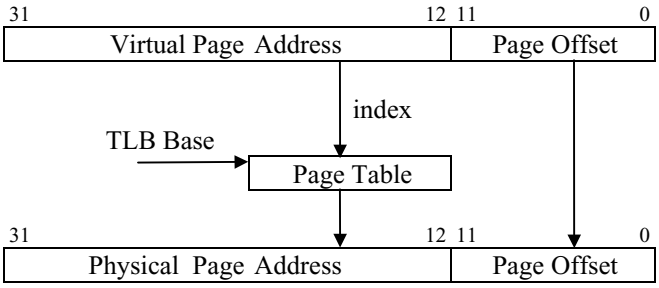



**Figure 3. Graphics Aperture Address Translation**

Since address translation using the above scheme requires an access to system memory, an on-chip cache (called a "Translation Lookaside Buffer" or TLB) is utilized to enhance performance. The TLB in the VT82C694T contains 16 entries. Address "misses" in the TLB require an access of system memory to retrieve translation data. Entries in the TLB are replaced using an LRU (Least Recently Used) algorithm.

Addresses are translated only for accesses within the "Graphics Aperture" (GA). The Graphics Aperture can be any power of two in size from 1MB to 256MB (i.e., 1MB, 2MB, 4MB, 8MB, etc). The base of the Graphics Aperture can be anywhere in the system virtual address space on an address boundary determined by the aperture size (e.g., if the aperture size is 4MB, the base must be on a 4MB address boundary). The Graphics Aperture Base is defined in register offset 10 of device 0. The Graphics Aperture Size and TLB Table Base are defined in the following register group (offsets 84 and 88 respectively) along with various control bits.

**Device 0 Offset 83-80 - GART/TLB Control (00000000h) RW**

**31-16 Reserved** ..... always reads 0

**15-8 Reserved (test mode status)** ..... RO

**7 Flush Page TLB**
- 0 Disable .....default
- 1 Enable

**6-4 Reserved (always program to 0)**..... RW

**3 PCI Master Address Translation for GA Access**
- 0 Addresses generated by PCI Master accesses of the Graphics Aperture will not be translateddefault
- 1 PCI Master GA addresses will be translated

**2 AGP Master Address Translation for GA Access**
- 0 Addresses generated by AGP Master accesses of the Graphics Aperture will not be translateddefault
- 1 AGP Master GA addresses will be translated

**1 CPU Address Translation for GA Access**
- 0 Addresses generated by CPU accesses of the Graphics Aperture will not be translated .....def
- 1 CPU GA addresses will be translated

**0 AGP Address Translation for GA Access**
- 0 Addresses generated by AGP accesses of the Graphics Aperture will not be translated .....def
- 1 AGP GA addresses will be translated

Note: For any master access to the Graphics Aperture range, snoop will not be performed.

**Device 0 Offset 84 - Graphics Aperture Size (00h)..... RW**

**7-0 Graphics Aperture Size**
- 11111111 1M
- 11111110 2M
- 11111100 4M
- 11111000 8M
- 11110000 16M
- 11100000 32M
- 11000000 64M
- 10000000 128M
- 00000000 256M

**Offset 8B-88 - GA Translation Table Base (00000000h) RW**

**31-12 Graphics Aperture Translation Table Base.** Pointer to the base of the translation table in system memory used to map addresses in the aperture range (the pointer to the base of the "Directory" table).

**11-3 Reserved** .....always reads 0

**2 TLB Flush Timing**
- 0 TLB Flush Will Delay Until DRAM Is Idle ..... default
- 1 TLB Flush Is A Static Value

**1 Graphics Aperture Enable**
- 0 Disable..... default
- 1 Enable

Note: To disable the Graphics Aperture, set this bit to 0 and set all bits of the Graphics Aperture Size to 0. To enable the Graphics Aperture, set this bit to 1 and program the Graphics Aperture Size to the desired aperture size.

**0 Reserved** .....always reads 0

## AGP Control

**Device 0 Offset A3-A0 - AGP Capability Identifier (0020C002h) .....RO**

**31-24 Reserved** ..... always reads 00h
**23-20 Major Specification Revision** ..... always reads 2h
Major rev of AGP spec that device conforms to (2.x)
**19-16 Minor Specification Revision** ..... always reads 0h
Minor rev # of AGP spec that device conforms to
**15-8 Pointer to Next Item** ..... always reads C0 (last item)
**7-0 AGP ID** .. (always reads 02 to indicate it is AGP)

**Device 0 Offset A7-A4 - AGP Status (1F000203h).....RO**

**31-24 Maximum AGP Requests**..... always reads 1F†
Max # of AGP requests the device can manage (32)
† See also RxFC[1] and RxFD[4-0]
**23-10 Reserved** .....always reads 0s
**9 Supports SideBand Addressing**..... always reads 1
**8-6 Reserved** .....always reads 0s
**5 4G Supported** (can be written at RxAE[5]..... def=0
**4 Fast Wr Supported** (can be written at AE[4] .. def=0
**3 Reserved** .....always reads 0s
**2 4X Rate Supported** (can be written at AE[2]) . def=0
**1 2X Rate Supported** (can be written at AC[3]) . def=1
**0 1X Rate Supported** ..... always reads 1

**Device 0 Offset AB-A8 - AGP Command (00000000h). RW**

**31-24 Request Depth** (reserved for target) . always reads 0s
**23-10 Reserved** ..... always reads 0s
**9 SideBand Addressing Enable**
0 Disable..... default
1 Enable
**8 AGP Enable**
0 Disable..... default
1 Enable
**7-6 Reserved** ..... always reads 0s
**5 4G Enable**
0 Disable..... default
1 Enable
**4 Fast Write Enable**
0 Disable..... default
1 Enable
**3 Reserved** ..... always reads 0s
**2 4X Mode Enable**
0 Disable..... default
1 Enable
**1 2X Mode Enable**
0 Disable..... default
1 Enable
**0 1X Mode Enable**
0 Disable..... default
1 Enable

**Device 0 Offset AC - AGP Control (08h).....RW**

**7 AGP Disable**.....RO
- 0 Enable .....default
- 1 Disable

This bit is latched from MAB9# at the rising edge of RESET#.

**6 AGP Read Synchronization**
- 0 Disable .....default
- 1 Enable

**5 AGP Read Snoop DRAM Post-Write Buffer**
- 0 Disable .....default
- 1 Enable

**4 GREQ# Priority Becomes Higher When Arbiter is Parked at AGP Master**
- 0 Disable .....default
- 1 Enable

**3 2X Rate Supported** (read also at RxA4[1])
- 0 Not supported
- 1 Supported .....default

**2 LPR In-Order Access (Force Fence)**
- 0 Fence/Flush functions not guaranteed. AGP read requests (low/normal priority and high priority) may be executed before previously issued write requests. .....default
- 1 Force all requests to be executed in order (automatically enables Fence/Flush functions). Low (i.e., normal) priority AGP read requests will never be executed before previously issued writes. High priority AGP read requests may still be executed prior to previously issued write requests as required.

**1 AGP Arbitration Parking**
- 0 Disable .....default
- 1 Enable (GGNT# remains asserted until either GREQ# de-asserts or data phase ready)

**0 AGP to PCI Master or CPU to PCI Turnaround Cycle**
- 0 2T or 3T Timing .....default
- 1 1T Timing

**Device 0 Offset AD – AGP Latency Timer (02h)..... RW**

**7-5 Reserved** .....always reads 0

**4 Choose First or Last Ready of DRAM**
- 0 Last ready chosen ..... default
- 1 First ready chosen

**3-0 AGP Data Phase Latency Timer**..... default = 02h

**Device 0 Offset AE – AGP Miscellaneous Control (00h)RW**

**7-6 Reserved** .....always reads 0

**5 4G Supported**
- 0 4G not supported ..... default
- 1 4G supported

**4 Fast Write Supported**
- 0 Fast Write not supported ..... default
- 1 Fast Write supported

**3 Reserved** .....always reads 0

**2 4x Rate Supported**
- 0 4x Rate not supported..... default
- 1 4x Rate supported

**1-0 Reserved** .....always reads 0

**Device 0 Offset B0 – AGP Pad Control / Status (8xh) ... RW**

**7 AGP 4x Strobe VREF Control**
- 0 STB VREF is STB# and vice versa
- 1 STB VREF is AGPREF ..... **default**

**6 AGP 4x Strobe & GD Pad Drive Strength**
- 0 Drive strength set to compensation circuit default ..... default
- 1 Drive strength controlled by RxB1[7-0]

**5-3 AGP Compensation Circuit N Control Output RO**

**2-0 AGP Compensation Circuit P Control Output. RO**

**Device 0 Offset B1 – AGP Drive Strength (63h) ..... RW**

**7-4 AGP Output Buffer Drive Strength N Ctrl ... def=6**

**3-0 AGP Output Buffer Drive Strength P Ctrl ... def=3**

**Device 0 Offset B2 – AGP Pad Drive / Delay Control ... RW**

**7 GD/GBE/GDS, SBA/SBS Control**

1.5V (Bit-1 = 0)
- 0 SBA/SBS = no cap ..... default
  GD/GBE/GDS = no cap
- 1 SBA/SBS = no cap
  GD/GBE/GDS = **cap**

3.3V (Bit-1 = 1)
- 0 SBA/SBS = **cap** ..... default
  GD/GBE/GDS = no cap
- 1 SBA/SBS = **cap**
  GD/GBE/GDS = **cap**

**6-5 Reserved** ..... always reads 0

**4 GD[31-16] Staggered Delay**
- 0 None ..... default
- 1 GD[31:16] delayed by 1 ns

**3-1 Reserved** ..... always reads 0

**0 GDS Output Delay**
- 0 None ..... default
- 1 GDS[1-0] & GDS[1-0]# delayed by 0.4 ns

Note: GDS1 & GDS1# will be delayed an additional 1ns if bit-4 = 1

**Device 0 Offset E0 – Miscellaneous Control (00h) ..... RW**

**7-1 Reserved** ..... always reads 0

**0 Latch DRAM Data Using**
- 0 Internal DRAM DCLK ..... default
- 1 External Feedback DRAM DCLK

**Device 0 Offset F7-F0 – BIOS Scratch Registers ..... RW**

**7-0 No hardware function** ..... default = 0

**Device 0 Offset F8 – DRAM Arbitration Timer (00h) .. RW**

**7-4 AGP Timer** ..... default = 0

**3-0 Host CPU Timer** ..... default = 0

**Device0 Offset F9 – VGA Timer (00h) ..... RW**

**7-4 VGA High Priority Timer** ..... default = 0

**3-0 VGA Timer** ..... default = 0

**Device 0 Offset FC – Back Door Control 1 (00h) ..... RW**

**7-4 Priority Timer** ..... default = 0

**3-2 Reserved (Do Not Program)** ..... default = 0

**1 Back-Door Max # of AGP Requests** ..... default = 0
- 0 Read of RxA7 always returns a value of 7 .. def
- 1 Read of RxA7 returns the value programmed in RxFD[2-0]

**0 Back-Door Device ID Enable** ..... default = 0
- 0 Use Rx3-2 value for Rx3-2 readback .... default
- 1 Use RxFE-FF Back-Door Device ID for Rx3-2 read

**Device 0 Offset FD – Back-DoorControl 2 (00h) ..... RW**

**7-5 Reserved** ..... always reads 0

**4-0 Max # of AGP Requests** ..... default = 0
(see also RxA7 and RxFC[1])

**Device 0 Offset FF-FE – Back-Door Device ID (0000h) RW**

**15-0 Back-Door Device ID** ..... default=00

## Device 1 Header Registers - PCI-to-PCI Bridge

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number of 0 and function number equal to 0 and device number equal to one.

**Device 1 Offset 1-0 - Vendor ID (1106h).....RO**

**15-0 ID Code** (reads 1106h to identify VIA Technologies)

**Device 1 Offset 3-2 - Device ID (8598h) .....RO**

**15-0 ID Code** (reads 8598h to identify the VT82C694T PCI-to-PCI Bridge device)

**Device 1 Offset 5-4 – Command (0007h).....RW**

**15-10 Reserved** ..... always reads 0

**9 Fast Back-to-Back Cycle Enable** ..... RO
- 0 Fast back-to-back transactions only allowed to the same agent.....default
- 1 Fast back-to-back transactions allowed to different agents

**8 SERR# Enable** ..... RO
- 0 SERR# driver disabled.....default
- 1 SERR# driver enabled

(SERR# is used to report ECC errors).

**7 Address / Data Stepping**..... RO
- 0 Device never does stepping .....default
- 1 Device always does stepping

**6 Parity Error Response**.....**RW**
- 0 Ignore parity errors & continue.....default
- 1 Take normal action on detected parity errors

**5 VGA Palette Snoop (Not Supported)** ..... RO
- 0 Treat palette accesses normally.....default
- 1 Don't respond to palette writes on PCI bus (10-bit decode of I/O addresses 3C6-3C9 hex)

**4 Memory Write and Invalidate Command**..... RO
- 0 Bus masters must use Mem Write.....default
- 1 Bus masters may generate Mem Write & Inval

**3 Special Cycle Monitoring**..... RO
- 0 Does not monitor special cycles.....default
- 1 Monitors special cycles

**2 Bus Master** .....**RW**
- 0 Never behaves as a bus master
- 1 Enable to operate as a bus master on the primary interface on behalf of a master on the secondary interface .....default

**1 Memory Space** .....**RW**
- 0 Does not respond to memory space
- 1 Enable memory space access .....default

**0 I/O Space** .....**RW**
- 0 Does not respond to I/O space
- 1 Enable I/O space access .....default

**Device 1 Offset 7-6 - Status (Primary Bus) (0220h) ....RWC**

**15 Detected Parity Error**.....always reads 0

**14 Signaled System Error (SERR#)** .....always reads 0

**13 Signaled Master Abort**
- 0 No abort received ..... default
- 1 Transaction aborted by the master with Master-Abort (except Special Cycles)..... ..... write 1 to clear

**12 Received Target Abort**
- 0 No abort received ..... default
- 1 Transaction aborted by the target with Target-Abort ..... write 1 to clear

**11 Signaled Target Abort**.....always reads 0

**10-9 DEVSEL# Timing**
- 00 Fast
- 01 Medium .....always reads 01
- 10 Slow
- 11 Reserved

**8 Data Parity Error Detected**.....always reads 0

**7 Fast Back-to-Back Capable**.....always reads 0

**6 User Definable Features** .....always reads 0

**5 66MHz Capable**.....always reads 1

**4 Supports New Capability list** .....always reads 0

**3-0 Reserved** .....always reads 0

**Device 1 Offset 8 - Revision ID (00h)..... RO**

**7-0 VT82C694T Chip Revision Code** (00=First Silicon)

**Device 1 Offset 9 - Programming Interface (00h)..... RO**

This register is defined in different ways for each Base/Sub-Class Code value and is undefined for this type of device.

**7-0 Interface Identifier**.....always reads 00

**Device 1 Offset A - Sub Class Code (04h) ..... RO**

**7-0 Sub Class Code**.reads 04 to indicate PCI-PCI Bridge

**Device 1 Offset B - Base Class Code (06h) ..... RO**

**7-0 Base Class Code**.. reads 06 to indicate Bridge Device

**Device 1 Offset D - Latency Timer (00h)..... RO**

**7-0 Reserved** .....always reads 0

**Device 1 Offset E - Header Type (01h)..... RO**

**7-0 Header Type Code** ..... reads 01: PCI-PCI Bridge

**Device 1 Offset F - Built In Self Test (BIST) (00h)..... RO**

**7 BIST Supported** ..... reads 0: no supported functions

**6 Start Test** ..... write 1 to start but writes ignored

**5-4 Reserved** .....always reads 0

**3-0 Response Code**.....0 = test completed successfully

**Device 1 Offset 18 - Primary Bus Number (00h).....RW**

**7-0 Primary Bus Number** ..... default = 0

This register is read write, but internally the chip always uses bus 0 as the primary.

**Device 1 Offset 19 - Secondary Bus Number (00h).....RW**

**7-0 Secondary Bus Number**..... default = 0

Note: AGP must use these bits to convert Type 1 to Type 0.

**Device 1 Offset 1A - Subordinate Bus Number (00h)....RW**

**7-0 Primary Bus Number** ..... default = 0

Note: AGP must use these bits to decide if Type 1 to Type 1 command passing is allowed.

**Device 1 Offset 1B – Secondary Latency Timer (00h)....RO**

**7-0 Reserved** ..... always reads 0

**Device 1 Offset 1C - I/O Base (f0h).....RW**

**7-4 I/O Base AD[15:12]**..... default = 1111b

**3-0 I/O Addressing Capability** ..... default = 0

**Device 1 Offset 1D - I/O Limit (00h) .....RW**

**7-4 I/O Limit AD[15:12]** ..... default = 0

**3-0 I/O Addressing Capability** ..... default = 0

**Device 1 Offset 1F-1E - Secondary Status (0000h) .....RO**

**15-0 Reserved** ..... always reads 0

**Device 1 Offset 21-20 - Memory Base (fff0h).....RW**

**15-4 Memory Base AD[31:20]**.....default = FFFh

**3-0 Reserved** ..... always reads 0

**Device 1 Offset 23-22 - Memory Limit (Inclusive) (0000h) RW**

**15-4 Memory Limit AD[31:20]** ..... default = 0

**3-0 Reserved** ..... always reads 0

**Device 1 Offset 25-24 - Prefetchable Memory Base (fff0h) RW**

**15-4 Prefetchable Memory Base AD[31:20]**default = FFFh

**3-0 Reserved** ..... always reads 0

**Device 1 Offset 27-26 - Prefetchable Memory Limit (0000h) .....RW**

**15-4 Prefetchable Memory Limit AD[31:20]**.....
..... default = 0

**3-0 Reserved** ..... always reads 0

**Device 1 Offset 3F-3E – PCI-to-PCI Bridge Control (0000h) ..... RW**

**15-4 Reserved** .....always reads 0

**3 VGA-Present on AGP**

0 Forward VGA accesses to PCI Bus..... default

1 Forward VGA accesses to AGP Bus

Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.

**2 Block / Forward ISA I/O Addresses**

0 Forward all I/O accesses to the AGP bus if they are in the range defined by the I/O Base and I/O Limit registers (device 1 offset 1C-1D)
..... default

1 Do not forward I/O accesses to the AGP bus that are in the 100-3FFh address range even if they are in the range defined by the I/O Base and I/O Limit registers.

**1-0 Reserved** .....always reads 0

## Device 1 Configuration Registers - PCI-to-PCI Bridge

### AGP Bus Control

**Device 1 Offset 40 - CPU-to-AGP Flow Control 1 (00h)RW**

**7 CPU-AGP Post Write**
- 0 Disable .....default
- 1 Enable

**6 CPU-AGP Dynamic Burst**
- 0 Disable .....default
- 1 Enable

**5 CPU-AGP One Wait State Burst Write**
- 0 Disable .....default
- 1 Enable

**4 AGP to DRAM Prefetch**
- 0 Disable .....default
- 1 Enable

**3 CPU to AGP Post Write Halt**
- 0 Disable .....default
- 1 Enable

**2 MDA Present on AGP**
- 0 Forward MDA accesses to AGP .....default
- 1 Forward MDA accesses to PCI

Note: Forward despite IO / Memory Base / Limit

Note: MDA (Monochrome Display Adapter) addresses are memory addresses B0000h-B7FFFh and I/O addresses 3B4-3B5h, 3B8-3BAh, and 3BFh (10-bit decode). 3BC-3BE are reserved for printers.

Note: If Rx3E bit-3 is 0, this bit is a don't care (MDA accesses are forwarded to the PCI bus).

**1 AGP Master Read Caching**
- 0 Disable .....default
- 1 Enable

**0 AGP Delay Transaction**
- 0 Disable .....default
- 1 Enable

**Table 7. VGA/MDA Memory/IO Redirection**

| 3E[3] VGA Pres. | 40[2] MDA Pres. | VGA is on | MDA is on | Axxxx, B8xxx Access | B0000 - B7FFF Access | 3Cx, 3Dx I/O | 3Bx I/O |
|---|---|---|---|---|---|---|---|
| 0 | - | PCI | PCI | PCI | PCI | PCI | PCI |
| 1 | 0 | AGP | AGP | AGP | AGP | AGP | AGP |
| 1 | 1 | AGP | PCI | AGP | PCI | AGP | PCI |

**Device 1 Offset 41 - CPU-to-AGP Flow Control 2 (00h) RW**

**7 Retry Status**
- 0 No retry occurred ..... default
- 1 Retry Occurred .....**write 1 to clear**

**6 Retry Timeout Action**
- 0 No action taken except to record status..... def
- 1 Flush buffer for write or return all 1s for read

**5-4 Retry Count**
- 00 Retry 2, backoff CPU ..... default
- 01 Retry 4, backoff CPU
- 10 Retry 16, backoff CPU
- 11 Retry 64, backoff CPU

**3 Post Write Data on Abort**
- 0 Flush entire post-write buffer on target-abort or master abort..... default
- 1 Pop one data output on target-abort or master-abort

**2 CPU Backoff on AGP Read Retry Timeout**
- 0 Disable..... default
- 1 Enable

**1-0 Reserved** .....always reads 0

**Device 1 Offset 42 - AGP Master Control (00h)..... RW**

**7 Read Prefetch for Enhance Command**
- 0 Always Perform Prefetch ..... default
- 1 Prefetch only if Enhance Command

**6 AGP Master One Wait State Write**
- 0 Disable..... default
- 1 Enable

**5 AGP Master One Wait State Read**
- 0 Disable..... default
- 1 Enable

**4 Extend AGP Internal Master for Efficient Handling of Dummy Request Cycles**
- 0 Disable..... default
- 1 Enable

This bit is normally set to 1.

**3 AGP Delay Transaction Timeout**
- 0 Disable..... default
- 1 Enable

**2 Prefetch Disable when Delay Transaction Occured**
- 0 Normal operation..... default
- 1 Disable prefetch when doing fast response to the previous delay transaction or doing read caching

**1 Reserved** .....always reads 0

**0 Shorten AGP Master to TRFCTL**
- 0 Disable..... default
- 1 Enable

**Device 1 Offset 43 - AGP Master Latency Timer (00h) RW**

**7-4 Host to AGP Time slot**
- 0 Disable (no timer) .....default
- 1 16 GCLKs
- 2 32 GCLKs
- … …
- F 128 GCLKs

**3-0 AGP Master Time Slot**
- 0 Disable (no timer) .....default
- 1 16 GCLKs
- 2 32 GCLKs
- … …
- F 128 GCLKs

**Device 1 Offset 44 – Backdoor Register Control (00h). RW**

**7-5 Reserved** ..... always reads 0

CD Silicon:

**4-1 Reserved (CD)**..... always reads 0

CE Silicon:

**4 Rx1F-1E Reflect Status in Rx7-6 (CE)**
- 0 Rx1F-1E always read 0.....default
- 1 Rx1F-1E read same as Rx7-6

**3 Back Door Register for Rx83[2], D2 Support (CE)**
- 0 Disable .....default
- 1 Enable

**2 Back Door Register for Rx83[1], D1 Support (CE)**
- 0 Disable .....default
- 1 Enable

**1 Back Door Register for Rx82[5], Device Specific Initialization (CE)**
- 0 Disable .....default
- 1 Enable

**0 Back Door Register for AGP Device ID**
- 0 Disable .....default
- 1 Enable

**Device 1 Offset 45 – Fast Write Control (72h)..... RW**

**7 Force Fast Write Cycle to be QW Aligned** (if Rx45[6] = 0)
- 0 Disable..... default
- 1 Enable

**6 Merge Multiple CPU Transactions Into One Fast Write Burst Transaction**
- 0 Disable
- 1 Enable**..... default**

**5 Merge Multiple CPU Write Cycles To Memory Offset 23-20 Into Fast Write Burst Cycles** (if Rx45[6] = 0)
- 0 Disable
- 1 Enable**..... default**

**4 Merge Multiple CPU Write Cycles To Prefetchable Memory Offset 27-24 Into Fast Write Burst Cycles** (if Rx45[6] = 0)
- 0 Disable
- 1 Enable**..... default**

**3 Reserved** .....always reads 0

**2 Fast Write Burst 4T Max (No Slave Flow Control)**
- 0 Disable..... default
- 1 Enable

**1 Fast Write Fast Back to Back**
- 0 Disable
- 1 Enable**..... default**

**0 Fast Write Initial Block 1 Wait State**
- 0 Disable..... default
- 1 Enable

| Rx45 Bits 7-4 | CPU Write Address in Mem1 | CPU Write Address in Mem2 | Fast Write Cycle Alignment |
|---|---|---|---|
| x1xx | - | - | QW aligned, burstable |
| 0000 | - | - | DW aligned, nonburstable |
| x010 | 0 | 0 | n/a |
| 0010 | 0 | 1 | DW aligned, non-burstable |
| x010 | 1 | - | QW aligned, burstable |
| x001 | 0 | 0 | n/a |
| x001 | - | 1 | QW aligned, burstable |
| 0001 | 1 | 0 | DW aligned, non-burstable |
| x011 | 0 | 0 | n/a |
| x011 | 1 | - | QW aligned, burstable |
| x011 | 0 | 1 | QW aligned, burstable |
| 1000 | - | - | QW aligned, non-burstable |
| 1010 | 0 | 1 | QW aligned, non-burstable |
| 1001 | 1 | 0 | QW aligned, non-burstable |

**Device 1 Offset 47-46 – PCI-to-PCI Bridge Device ID ..RW**

**15-0 PCI-to-PCI Bridge Device ID** ..... default = 0000

**Device 1 Offset 80 – Capability ID (01h)..... RO**

**7-0 Capability ID** .....always reads 01h

**Device 1 Offset 81 – Next Pointer (00h)..... RO**

**7-0 Next Pointer: Null** .....always reads 00h

**Device 1 Offset 82 – Power Mgmt Capabilities 1 (02h).. RO**

**7-0 Power Mgmt Capabilities**.....always reads 02h

**Device 1 Offset 83 – Power Mgmt Capabilities 2 (00h).. RO**

**7-0 Power Mgmt Capabilities**.....always reads 00h

**Device 1 Offset 84 – Power Mgmt Ctrl/Status (00h) ..... RW**

**7-2 Reserved** .....always reads 0

**1-0 Power State**

00 D0 ..... default
01 -reserved-
10 -reserved-
11 D3 Hot

**Device 1 Offset 85 – Power Mgmt Status (00h) ..... RO**

**7-0** Power Mgmt Status.....default = 00

**Device 1 Offset 86 – P2P Br. Support Extensions (00h). RO**

**7-0** P2P Bridge Support Extensions .....default = 00

**Device 1 Offset 87 – Power Management Data (00h)..... RO**

**7-0** Power Management Data .....default = 00

# ELECTRICAL SPECIFICATIONS

## Absolute Maximum Ratings

| Parameter | Min | Max | Unit |
|---|---|---|---|
| Case operating temperature | 0 | 85 | $^{O}C$ |
| Storage temperature | –55 | 125 | $^{O}C$ |
| Input voltage | –0.5 | 5.5 | Volts |
| Output voltage ($V_{CC}$ = 3.1 - 3.6V) | –0.5 | $V_{CC}$ + 0.5 | Volts |

Note: Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

## DC Characteristics

$T_C$=0-85$^{O}$C, $V_{CC}$=3.3V+/-5%, GND=0V

| Symbol | Parameter | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{IL}$ | Input low voltage | –0.50 | 0.8 | V | |
| $V_{IH}$ | Input high voltage | 2.0 | $V_{CC}$+0.5 | V | |
| $V_{IU}$ | Input max undershoot | –1.0 | –1.5 | V | Duration 2ns max |
| $V_{IO}$ | Input max overshoot | $V_{CC}$+1.0 | $V_{CC}$+1.5 | V | Duration 2ns max |
| $V_{OL}$ | Output low voltage | - | 0.45 | V | $I_{OL}$=4.0mA |
| $V_{OH}$ | Output high voltage | 2.4 | - | V | $I_{OH}$=–1.0mA |
| $I_{IL}$ | Input leakage current | - | +/-10 | uA | $0<V_{IN}<V_{CC}$ |
| $I_{OZ}$ | Tristate leakage current | - | +/-20 | uA | $0.45<V_{OUT}<V_{CC}$ |

## Power Characteristics

$T_C$=0-85$^{O}$C, $V_{CC}$=3.3V+/-5%, GND=0V

| Symbol | Parameter | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|
| $I_{CC}$ | Power Supply Current – VCC | | | mA | Max operating frequency |
| $I_{SUS}$ | Power Supply Current – VSUS | | | mA | Max operating frequency |
| $I_{CCA}$ | Power Supply Current – VCCA | | | mA | Max operating frequency |
| $I_{CCQ}$ | Power Supply Current – VCCQ | | | mA | Max operating frequency |
| $I_{TT}$ | Power Supply Current – VTT | | | mA | Max operating frequency |
| $I_{GTLREF}$ | Power Supply Current – GTLREF | | | uA | Max operating frequency |
| $I_{AGPREF}$ | Power Supply Current – AGPREF | | | uA | Max operating frequency |
| $P_D$ | Power Dissipation | | 3.5 | W | Max operating frequency |

## AC Timing Specifications

AC timing specifications provided are based on external zero-pf capacitance load. Min/max cases are based on the following table:

**Table 8. AC Timing Min / Max Conditions**

| Parameter | Min | Max | Unit |
|---|---|---|---|
| 3.3V Power (VCC, VSUS, VCCA) | 3.135 | 3.465 | Volts |
| Case Temperature | 0 | 85 | $^{o}$C |

Drive strength for each output pin is programmable. See Rx6D for details.

**Table 9. AC Timing – Host CPU Interface**

| Signal | Min Delay | Max Delay | Setup | Hold | Unit |
|---|---|---|---|---|---|
| HA# Bus | | | | | ns |
| HD# Bus | | | | | ns |
| ADS# | | | | | ns |
| BNR# | | | | | ns |
| DBSY# | | | | | ns |
| DRDY# | | | | | ns |
| HIT# | | | | | ns |
| HITM# | | | | | ns |
| HLOCK# | | | | | ns |
| HREQ# Bus | | | | | ns |
| BPRI# | | | | | ns |
| DEFER# | | | | | ns |
| HTRDY# | | | | | ns |
| RS# Bus | | | | | ns |

**Table 10. AC Timing – DRAM Interface**

| Signal | Min Delay | Max Delay | Setup | Hold | Unit |
|---|---|---|---|---|---|
| MD Bus | | | | | ns |
| MECC Bus | | | | | ns |
| CKE Bus | | | | | ns |
| MAA Bus | | | | | ns |
| MAB# Bus | | | | | ns |
| CSA# Bus | | | | | ns |
| CSB# Bus | | | | | ns |
| DQMA Bus | | | | | ns |
| DQMB Bus | | | | | ns |
| SRAS# Bus | | | | | ns |
| SCAS# Bus | | | | | ns |
| SWE# Bus | | | | | ns |

# MECHANICAL SPECIFICATIONS

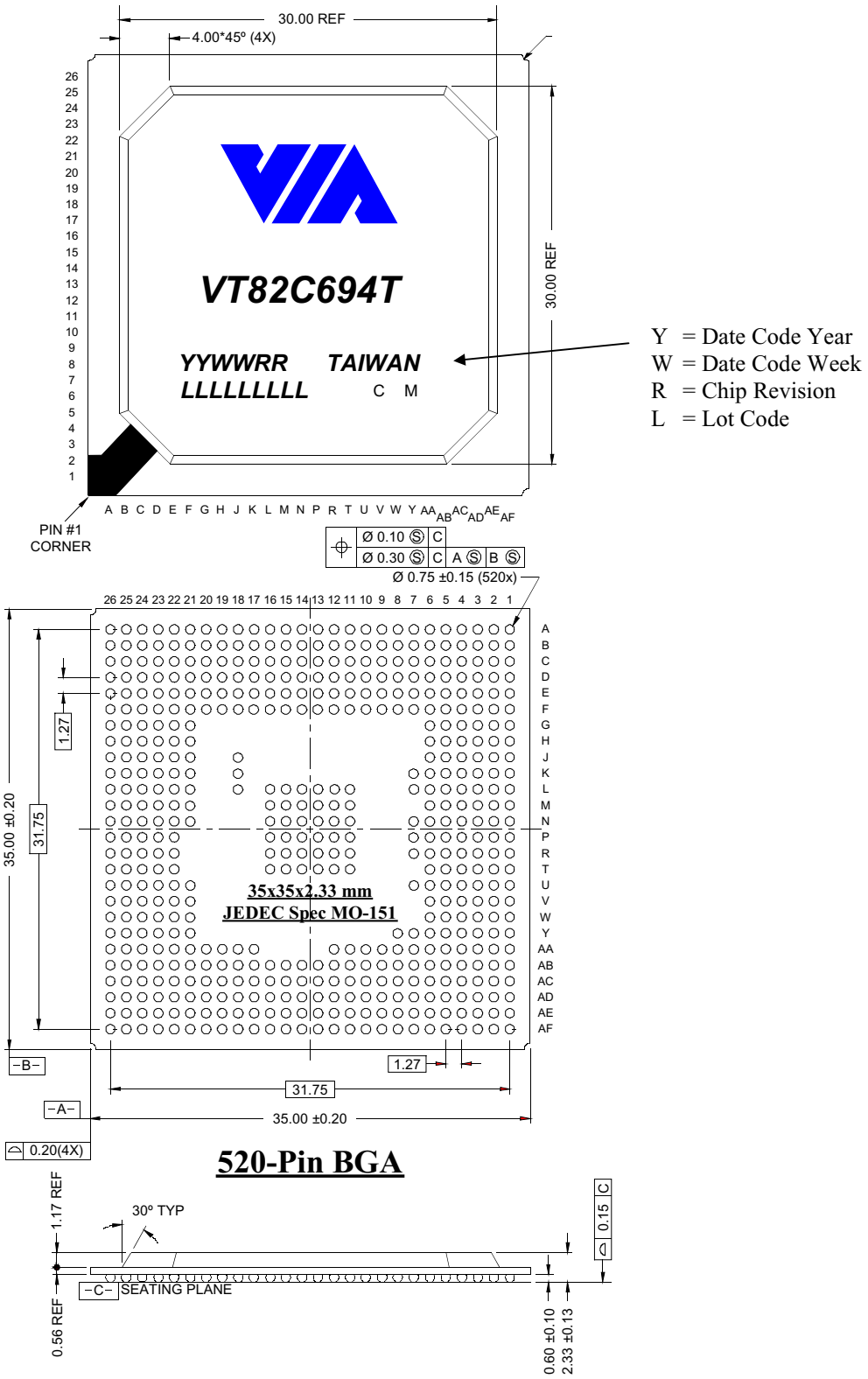



**Figure 4. Mechanical Specifications - 520-Pin Ball Grid Array Package**