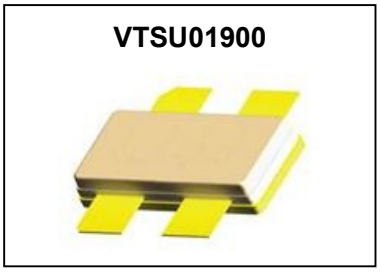
900W, 100V RF Power N-channel MOSFETs

Description

The VTSU01900 is a 900-watt, N-channel MOSFETs, designed for pulsed or CW applications at frequencies up to 200 MHz. It's suitable for use in industrial, scientific and medical applications.

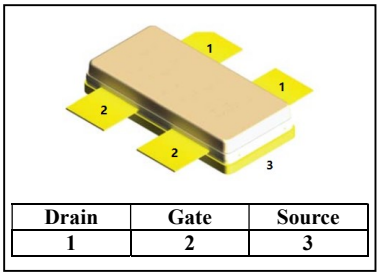


- Typical Performance (In Demo Fixture): V_{DD} = 100 Volts, I_{DQ} = 500 mA, Pulse CW, Pulse Width=1ms, Duty cycle=10%

Frequency	Gp (dB)	P_{OUT} (W)	η_D (%)
120 MHz	20	900	65

- Typical Performance (In Demo Fixture): V_{DD} = 100 Volts, I_{DQ} = 500 mA, CW

Frequency	Gp (dB)	P_{OUT} (W)	η_D (%)
120 MHz	24	550	68



Drain	Gate	Source
1	2	3

Figure 1. Pin Connection

Features

- Common source configuration, push pull
- Excellent thermal stability, low HCI drift
- Low $R_{DS(on)}$
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{(BR)DSS}$	250	V
Drain-Gate Voltage (RGS = 1MΩ)	V_{DGR}	250	V
Gate-Source Voltage	V_{GS}	-20 to +20	V
Drain Current	I_D	20	A
Power Dissipation	P_{DISS}	630	W
Storage Temperature Range	Tstg	-65 to 150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature	T_J	200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Junction-Case Thermal Resistance	R_{thJC}	0.30	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_{CASE} = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit

DC Characteristics

Drain-Source Voltage V_{GS}=0, I_{DS}=100mA	$V_{(BR)DSS}$	250			V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 100V, V_{GS} = 0 V)	I_{DSS}			1	mA
Gate-Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0 V)	I_{GSS}			250	nA
Gate Threshold Voltage (V_{DS} = 10V, I_D = 250 mA)	V_{GS}(th)	2.0		4.0	V
Drain-Source Voltage (On state) (V_{GS} = 10V, I_D = 10 A)	$V_{DS(ON)}$		2.5	3.6	V
Forward Transconductance (V_{DS} = 10 V, I_D = 2.5 A)	g_{FS}	3.0			S
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =100 V, f = 1 MHz)	C_{ISS}		501		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =100 V, f = 1 MHz)	C_{OSS}		136		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =100 V, f = 1 MHz)	C_{RSS}		5.8		pF

Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 100 Vdc, I_{DQ} = 2×250mA, f = 120 MHz, Pulse CW, Pulse Width=1ms, Duty cycle=10%.

Output Power	P_{OUT}		900		W
Power Gain@ P_{OUT}=900W	Gp		20		dB
Drain Efficiency@ P_{OUT}=900W	η_D		65		%

Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 100 Vdc, I_{DQ} = 2×250mA, f = 120 MHz, CW,.

Output Power	P_{OUT}	450	550		W
Power Gain@ P_{OUT}=550W	Gp		24		dB
Drain Efficiency@ P_{OUT}=550W	η_D		68		%

Reference Circuit of Test Fixture Schematic

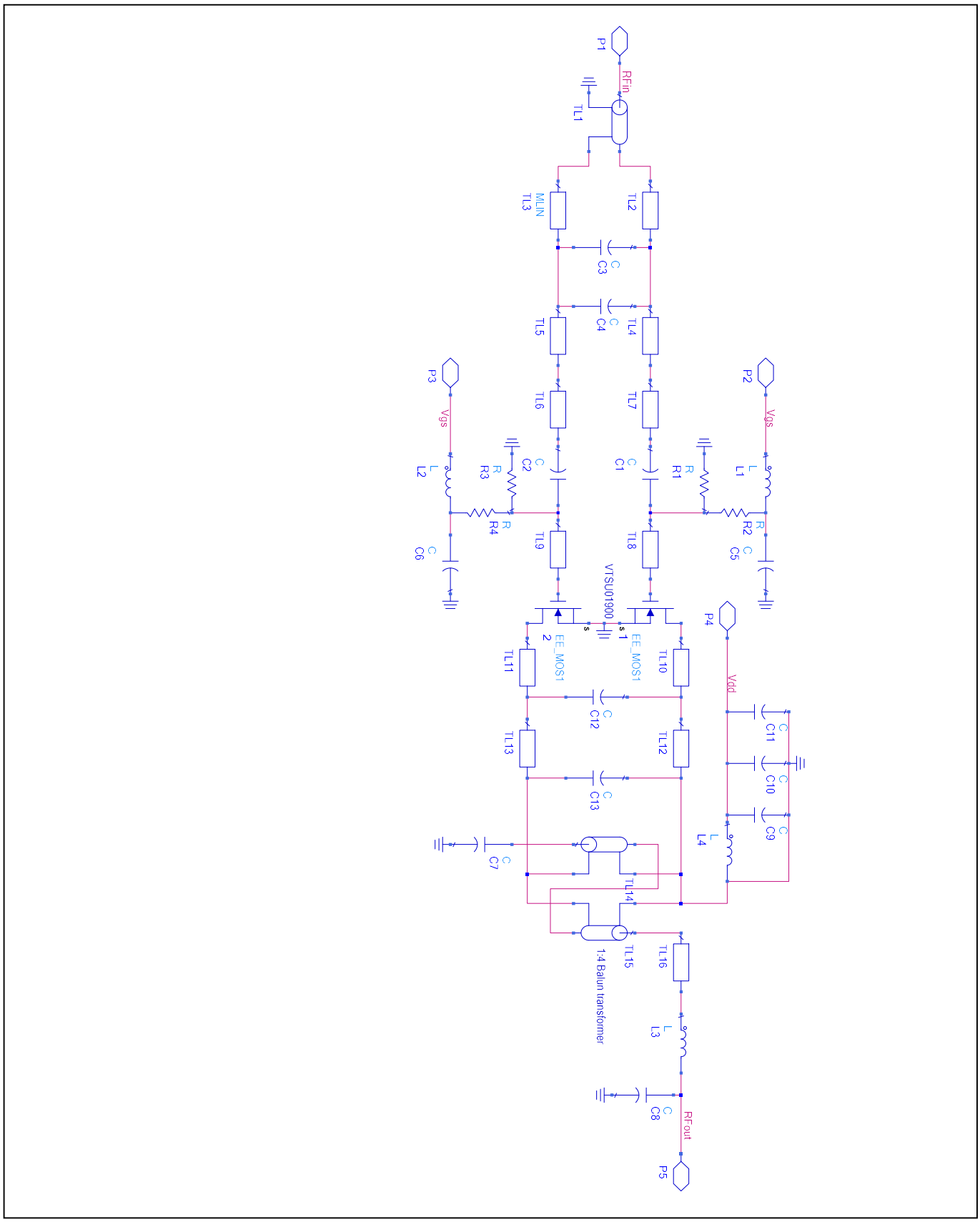


Figure 2. 120 MHz Test Circuit Schematic Reference

Table 5. Test Circuit Component Designations and Values

Component	Description
TL1	25Ω 0.25λ
TL2,TL3	Length18.5mm * width5 mm
TL4,TL5	Length 9.5mm * width5 mm
TL6,TL7	Length 12mm * width9 mm
TL8,TL9	Length 5.5mm * width9 mm
TL10,TL11	Length 9mm * width16.5 mm
TL12,TL13	Length 9mm * width1 mm
TL14,TL15	1：4 Balun transformer，copper tubes 46X38mm
C1,C2,C5,C6	1000 pF ATC 800B ceramic chip capacitor
C3	220 pF ATC 800B ceramic chip capacitor
C4	240 pF ATC 800B ceramic chip capacitor
C7	43 pF ATC 800B ceramic chip capacitor
C8	5.6 pF ATC 800B ceramic chip capacitor
C9	470 pF ATC 800B ceramic chip capacitor
C12	43 pF ATC 800B ceramic chip capacitor
C13	20 pF ATC 800B ceramic chip capacitor
C10	2200 pF ATC 100C ceramic chip capacitor
C11	100 µF / 200 V aluminum electrolytic capacitor
R1,R3	15 Ω 1/4 W, surface mount chip resistor
R2,R4	30 Ω 1/4 W, surface mount chip resistor
L1,L2	470 nH chip Inductor
L3	78 nH chip Inductor
L4	390 nH chip Inductor
PCB	1.58mm thickness, FR4, 1 oz. copper both sides

TYPICAL CHARACTERISTICS

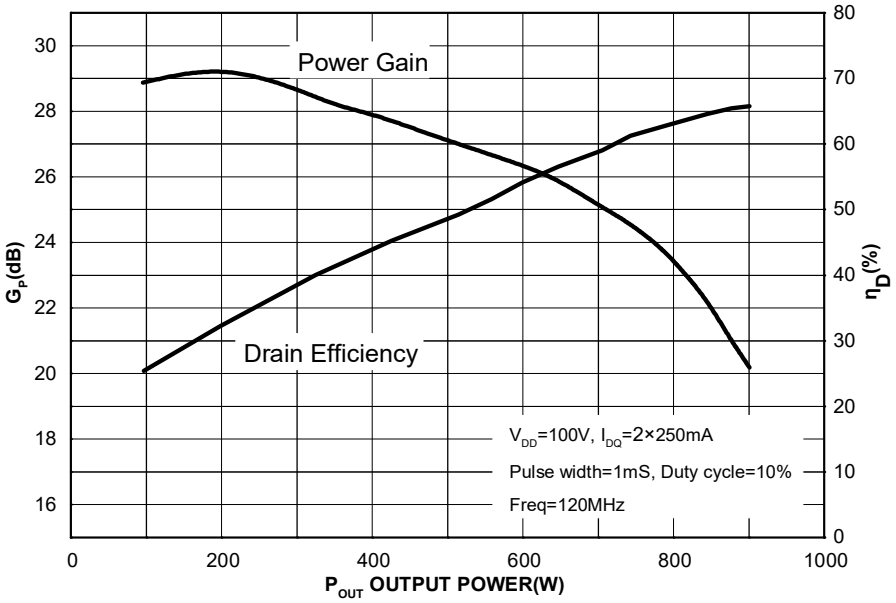


Figure 3. Power gain and drain efficiency as function of output power

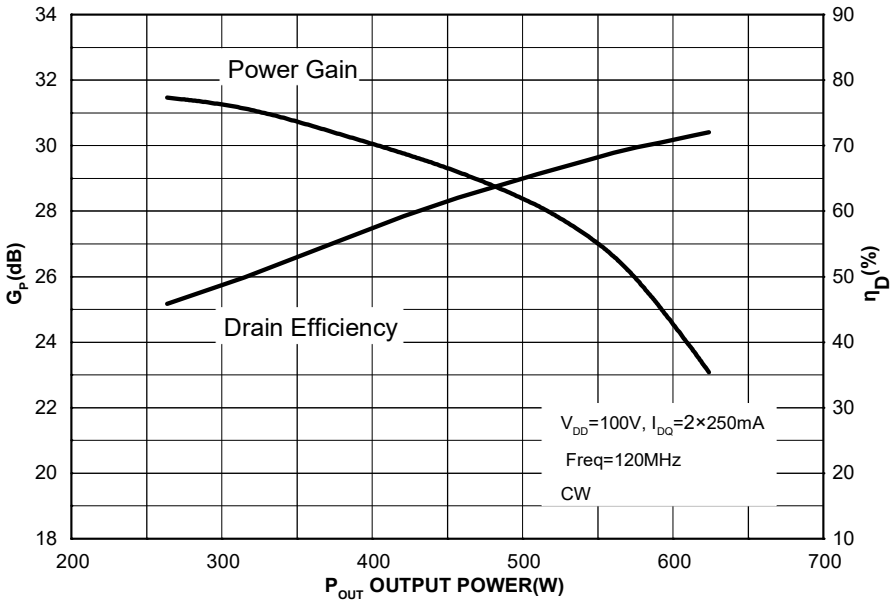
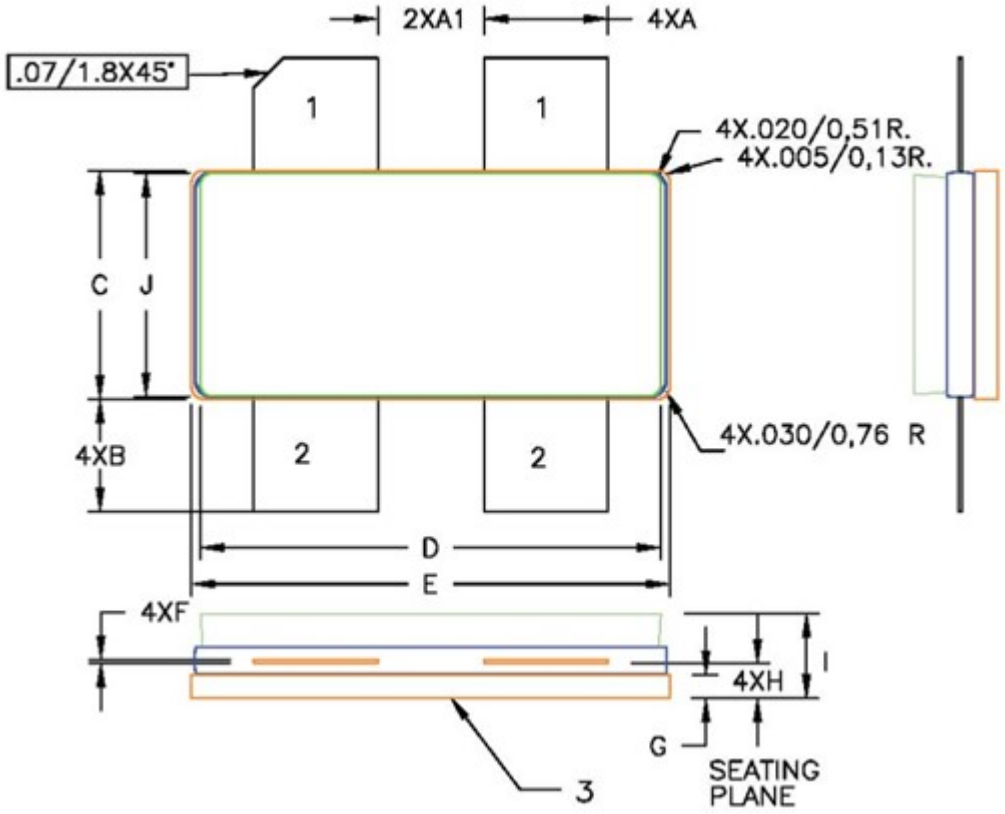


Figure 4. Power gain and drain efficiency as function of output power(CW)

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads(1—Drain,2—Gate,3—Source)



UNIT	A	A1	B	C	D	E	F	G	H	I	J
mm	5.59 5.10	4.83 4.32	5.33 4.32	9.91 9.65	20.02 19.61	20.70 20.45	1.15 0.08	1.14 0.89	1.7 1.45	4.32 3.18	9.53 9.27

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-VD3					28/11/2016

Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2016/11/28	Rev 1.0	Create Production Datasheet

Disclaimers