



175W, 50V RF Power N-channel MOSFETs

Description

The VTSV02175 is a 175-watt, gold metallized N-channel MOSFETs, designed for HF/VHF/UHF commercial and industrial applications at frequencies up to 200 MHz.

- Typical Performance (In Demo Fixture): $V_{DD} = 50$ Volts, $I_{DQ} = 250$ mA, CW.

Frequency	Gp (dB)	P_{OUT} (W)	η_D (%)
175 MHz	15.5	190	63

Features

- Gold metallization
- Common source configuration
- Excellent thermal stability, low HCI drift
- Low $R_{DS(on)}$
- Pb-free, RoHS-compliant

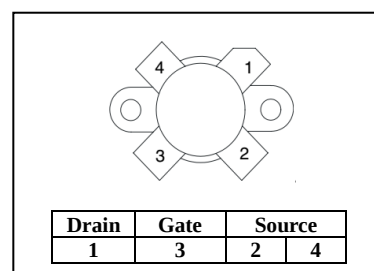
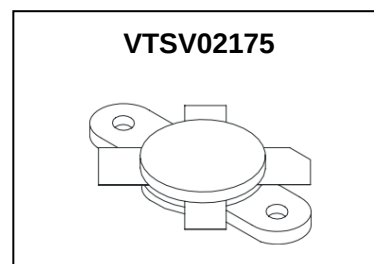


Figure 1. Pin Connection

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{(BR)DSS}$	130	V
Drain-Gate Voltage (RGS = 1M Ω)	V_{DGR}	130	V
Gate-Source Voltage	V_{GS}	-40 to +40	V
Drain Current	I_D	20	A
Power Dissipation	P_{DISS}	400	W
Storage Temperature Range	T_{stg}	-65 to 150	$^{\circ}C$
Case Operating Temperature	T_c	150	$^{\circ}C$
Operating Junction Temperature	T_j	200	$^{\circ}C$

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Junction-Case Thermal Resistance	R_{thJC}	0.46	$^{\circ}C/W$

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_{CASE} = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics

Drain-Source Voltage $V_{GS}=0, I_{DS}=100mA$	$V_{(BR)DSS}$	130			V
Zero Gate Voltage Drain Leakage Current	I_{DSS}			50	mA



($V_{DS} = 50V$, $V_{GS} = 0V$)					
Gate-Source Leakage Current ($V_{GS} = 20V$, $V_{DS} = 0V$)	I_{GSS}			300	nA
Gate Quiescent Voltage ($V_{DS} = 10V$, $I_D = 10mA$)	$V_{GS(Q)}$				V
Drain-Source Voltage (On state) ($V_{GS} = 10V$, $I_D = 10A$)	$V_{DS(ON)}$			2.5	V
Forward Transconductance ($V_{DS} = 10V$, $I_D = 5A$)	g_{FS}	5			mho
Common Source Input Capacitance ($V_{GS} = 0V$, $V_{DS} = 50V$, $f = 1MHz$)	C_{ISS}		422		pF
Common Source Output Capacitance ($V_{GS} = 0V$, $V_{DS} = 50V$, $f = 1MHz$)	C_{OSS}		241		pF
Common Source Feedback Capacitance ($V_{GS} = 0V$, $V_{DS} = 50V$, $f = 1MHz$)	C_{RSS}		19		pF

Functional Tests (In Demo Test Fixture, 50 ohm system) : $V_{DD} = 50Vdc$, $I_{DQ} = 250mA$, $f = 175MHz$, CW

Output Power	P_{OUT}	175	190		W
Power Gain @ $P_{OUT}=175W$	G_p	14	15.5		dB
Drain Efficiency @ $P_{OUT}=175W$	η_D	55	63		%
Load Mismatch, $P_{OUT}=175W$, All Phase angles	Load Mismatch	10 : 1			VSWR

Table 5. V_{GS} sorts

Symbol	Value	Symbol	Value	Symbol	Value
AA	1.5 - 1.6	E	2.4 - 2.5	P	3.3 - 3.4
BB	1.6 - 1.7	F	2.5 - 2.6	Q	3.4 - 3.5
CC	1.7 - 1.8	G	2.6 - 2.7	R	3.5 - 3.6
DD	1.8 - 1.9	H	2.7 - 2.8	S	3.6 - 3.7
EE	1.9 - 2.0	J	2.8 - 2.9	T	3.7 - 3.8
A	2.0 - 2.1	K	2.9 - 3.0	U	3.8 - 3.9
B	2.1 - 2.2	L	3.0 - 3.1	V	3.9 - 4.0
C	2.2 - 2.3	M	3.1 - 3.2		
D	2.3 - 2.4	N	3.2 - 3.3		



Reference Circuit of Test Fixture Schematic

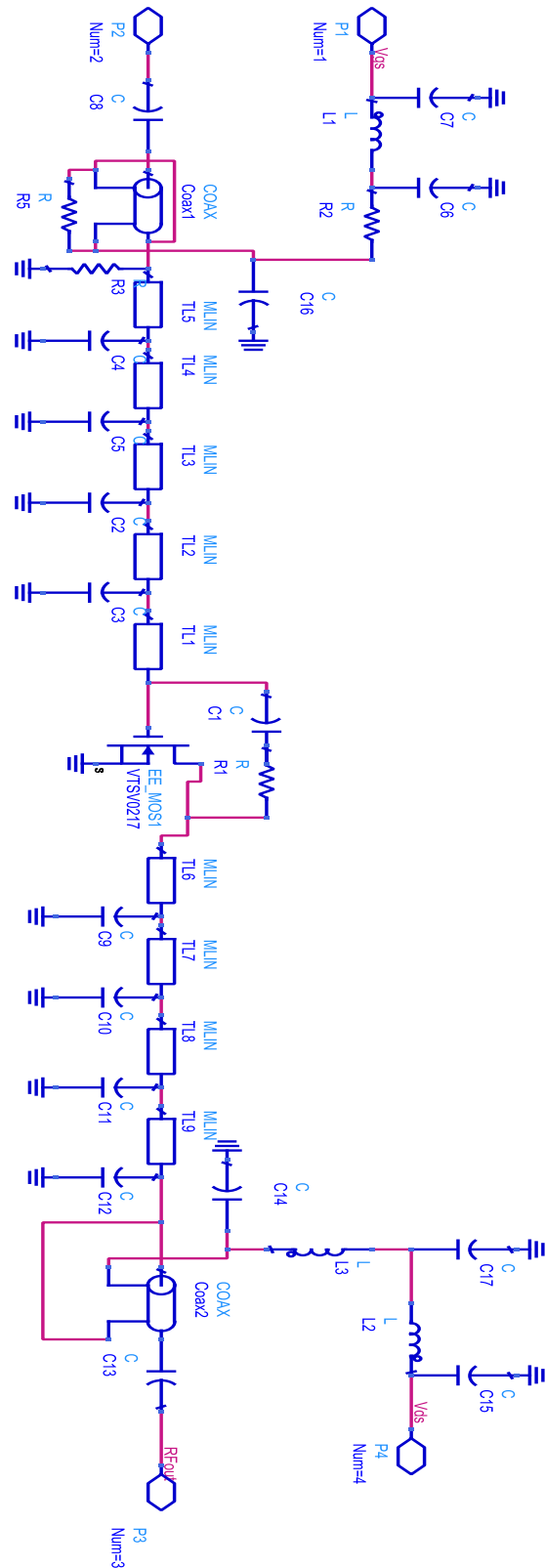


Figure 2. 175 MHz Test Circuit Schematic Reference



Table 6. Test Circuit Component Designations and Values

Component	Description
TL1,TL6	Length 50mm * width 17 mm
TL2,TL4,TL7	Length 1.5mm * width 17 mm
TL3	Length 3mm * width 17 mm
TL5	Length 2mm * width 17 mm
TL8	Length 2.5mm * width 17 mm
TL9	Length 1.5mm * width 10 mm
COAX1	1:4, Balun transformer, 25ohm, 2mm diameter, L=150mm, with ferrite core
COAX2	1:4,25ohm, 3.6mm diameter, L=150mm, with ferrite core
C8,C13	470 pF ATC 100B ceramic chip capacitor
C1	0.01 μ F / 500 V surface mount ceramic chip capacitor
C6,C7,C17	0.01 mF / 500 V surface mount ceramic chip capacitor
C2	Arco 423, 16-100PF
C5,C10,C11	Arco 404 12-65pF
C3	120 pF ATC 100B ceramic chip capacitor
C4	43 pF ATC 100B ceramic chip capacitor
C9	30 pF ATC 100B ceramic chip capacitor
C12	91 pF ATC 100B ceramic chip capacitor
C14,C16	1200 pF ATC 700B ceramic chip capacitor
C15	2000 μ F / 63 V aluminum electrolytic capacitor
R1	560 Ω 1 W, surface mount chip resistor
R2	360 Ω 1/2 W, surface mount chip resistor
R3	470 Ω 1 W, surface mount chip resistor
L1,L2,L3	470 nH chip Inductor
PCB	1.58mm thickness, FR4, 1 oz. copper both sides

TYPICAL CHARACTERISTICS

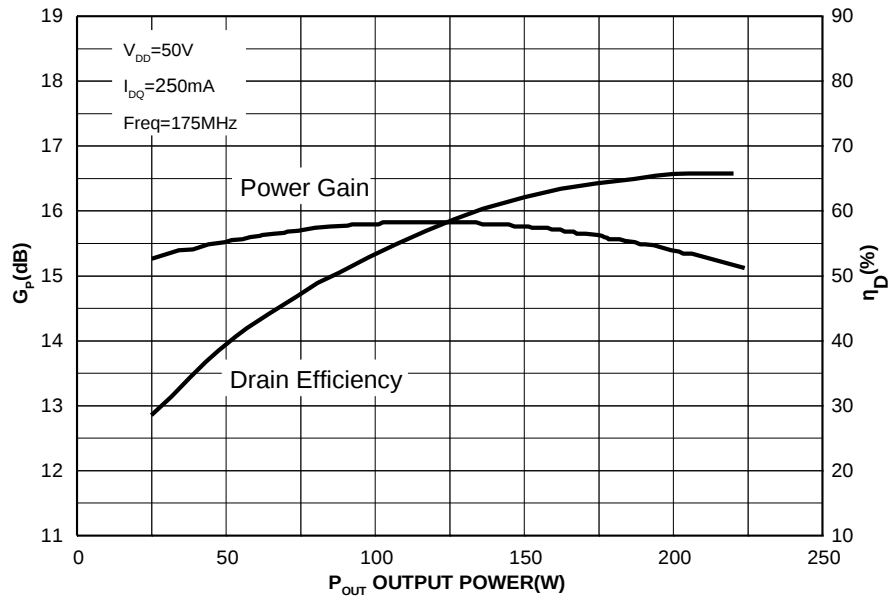
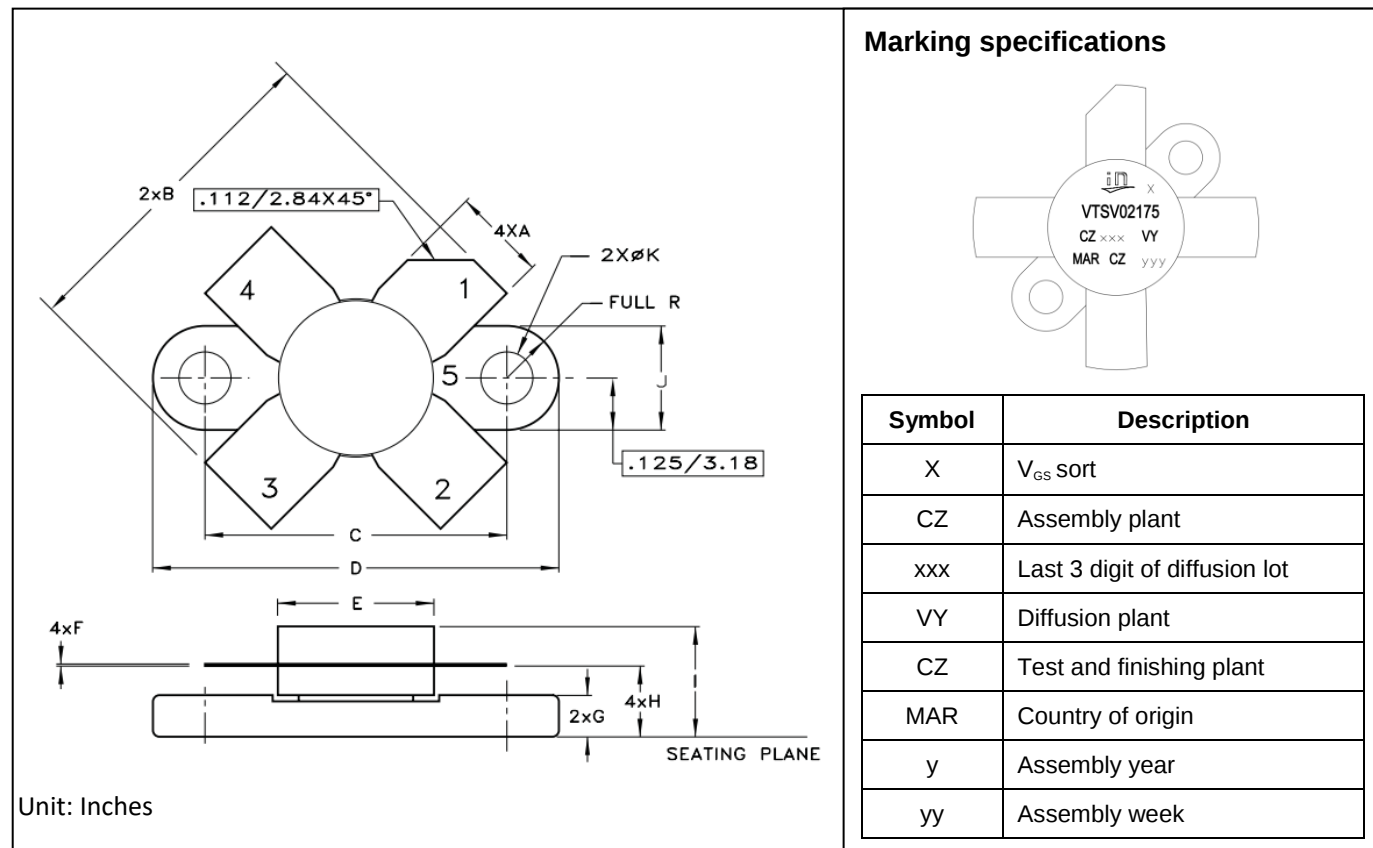


Figure 3. Power gain and drain efficiency as function of output power



Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads



UNIT	A	B	C	D	E	F	G	H	I	J	K
mm	5.84	20.83	18.54	24.89	9.78	0.15	2.67	4.57	7.14	6.48	3.30
	5.59	19.81	18.29	24.64	9.40	0.10	2.16	4.06		6.22	3.05
inches	0.230	0.820	0.730	0.980	0.385	0.006	0.105	0.180	0.281	0.255	0.130
	0.220	0.780	0.720	0.970	0.370	0.004	0.085	0.160		0.245	0.120

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-VD2					28/11/2016



Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2016/11/28	Rev 1.0	Create Product Datasheet
2017/03/16	Rev 1.1	Product Datasheet
		Add V _{GS} soft information and marking specification
2017/09/25	Rev 1.2	Product Datasheet
		Update marking specification

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