VISION VV5402 Monolithic Sensor

Multi-standard Monochrome CMOS Image Sensor.

PRODUCT DATASHEET

DISTINCTIVE CHARACTERISTICS

- Complete Video Camera on a single chip
- EIA/CCIR standard compatible
- Low power operation (250mW Typical)
- Integral 75Ω driver
- Control options pin selectable for ease of use
- Low light operation to 0.5 lux
- Automatic Exposure and Gain Control
- Automatic Black Level Calibration
- Linear or Gamma corrected output option
- Industry standard 48 pin LCC package

GENERAL DESCRIPTION

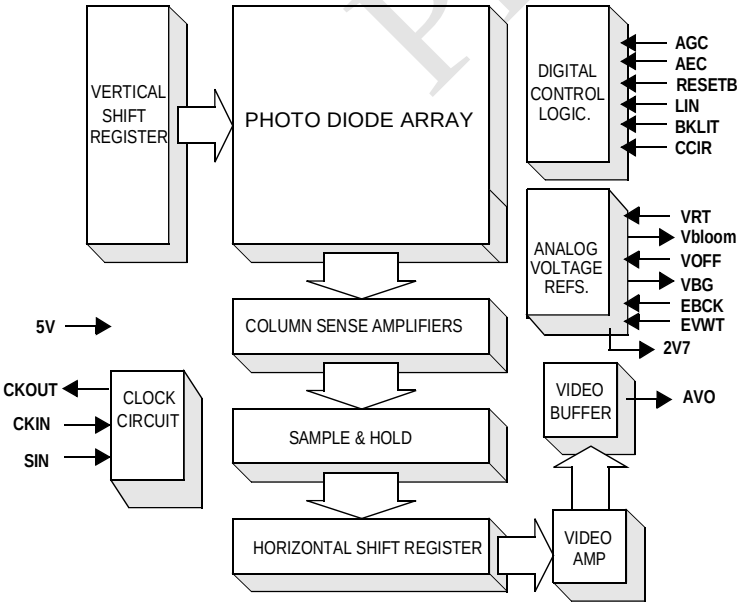
The VV5402 is a highly-integrated VLSI camera device based on VISION's unique CMOS sensor technology. It is suitable for applications requiring a composite video output with minimum external circuitry.

The device incorporates a 388 x 295 pixel image sensor and all the necessary support circuits to generate fully formatted composite video into a 75Ω load.

Automatic control of exposure, gain and black level allow use of a single fixed-aperture lens over a wide range of operating conditions. Normal and Backlit modes further enhance difficult scene types.

All major control functions are pin selectable giving maximum flexibility with ease of use. The VV5402 offers a complete camera system with only a few external components.

BLOCK DIAGRAM



Pixel Format	384 x 287 (CCIR) 320 x 243 (EIA)
Pixel Size	12µm x 12µm
Array Size	4.66mm x 3.54mm
Min. illumination	0.5 lux (Standard Clock)
S/N	Typically 52dB
Exposure control	Automatic (to 146000:1)
Gain Control	Automatic (to +20dB)
Power Supply	5v ±5%
Power	< 300 mW
Temperature	0^{o}C - 40^{o}C

Contents

Video Output

The VV5402 delivers a fully-formatted composite monochrome video signal. Standards options include EIA (320 x 244) and CCIR (384 x 287). On chip signal conditioning allows user-selection of linear or gamma-corrected output.

The integrated 75Ω driver eliminates the need for additional active components to drive standard loads, including double terminated lines.

Automatic Exposure and Gain Control

Automatic exposure and gain control are enabled with AEC=1 (pin 21) and AGC=1 (pin22). However, If AEC is inhibited by pin 21, AGC is also inhibited. Inhibiting AEC or AGC by taking pin 21 or 22 low freezes the current value(s) for these.

Automatic Exposure Control (AEC)

The VV5402 controls exposure over a range of 99,000:1 in EIA mode and 146,000:1 in CCIR mode, and operates at illumination levels as low as 0.5 lux at standard clock frequencies. (The system clock frequency can be reduced to provide increased sensitivity.)

Automatic exposure control is achieved by varying pixel current integration time according to the average light level on the sensor. This integration time can vary from one pixel clock period to one frame period.

Pixels above a threshold white level are counted every frame, and the number at the end of the frame defines the image exposure. If the image is other than correctly exposed, a new value for integration time is calculated and applied for the next frame. Corrections are either ±1/8 or ±1/64, depending upon the degree of over or under exposure.

Automatic Gain Control (AGC)

The VV5402 automatically increases the system gain of its output stage if with the current gain setting and maximum exposure the image is too dark. Gain can be varied from x1 to x16 in times-two steps, giving five different gain settings.

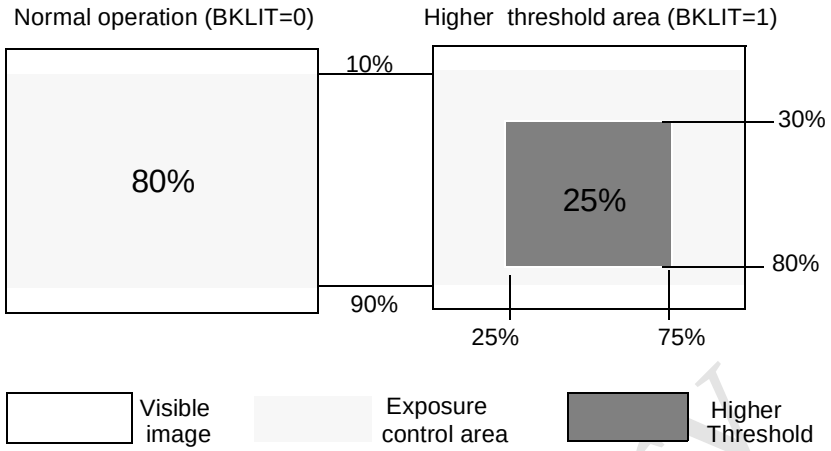
If the scene is too dark and the integration period has almost reached its maximum value, the gain value is incremented by one step (times two). In the same frame period the exposure value is divided by two, halving the integration period. The exposure controller then increases the exposure value as necessary. Similarly if the image is too bright and the integration period is short then gain will be reduced by one step (divide by two) and the exposure value will be doubled. The exposure controller can then adjust the exposure value as necessary to provide a correctly exposed image.

Backlit Mode

The VV5402 can be configured to operate in two auto-exposure modes, selected by the BKLIT pin (pin28) state. The default mode (BKLIT = 0) provides exposure control for normally illuminated scenes. For scenes where a bright background can cause the foreground subject to be severely under exposed, the ‘Backlit’ mode (BKLIT = 1) offers superior performance.

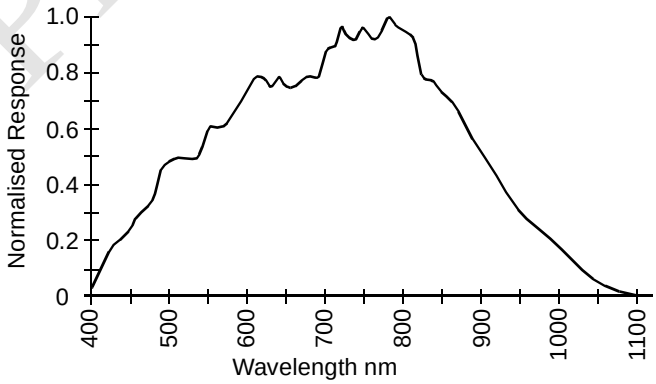
‘Backlit Mode’ (BKLIT=1) operates by using a higher threshold level for the exposure control comparator over the central area of an image, which is therefore exposed for longer and so enhanced. The area in which the higher comparator threshold is used when BKLIT=1 is illustrated below:

Backlit Mode Threshold Area:



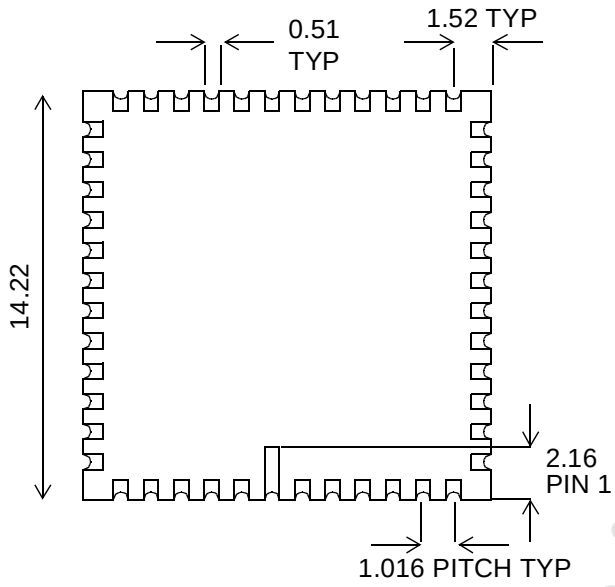
Note: The threshold level used for the central area is a preset mutiple of the normal mode reference level, and is not alterable.

Spectral Response

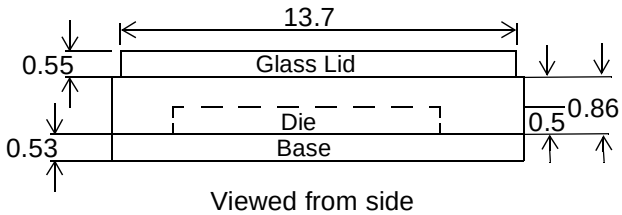


SPECIFICATIONS

Package Details



Viewed from below



Viewed from side

The optical array is centred within the package to a tolerance of ± 0.2 mm, and rotated no more than ± 0.5^{o}

Tolerances on package dimensions ±10%

Glass lid placement is controlled so that no package overhang exists.

All dimensions in millimetres

Absolute Maximum Ratings

Parameter	Value
Supply Voltage	-0.5 to +7.0 volts
Voltage on other input pins	-0.5 to V_{DD} + 0.5 volts
Temperature under bias	-15^{o}C to 85^{o}C
Storage Temperature	-30^{o}C to 125^{o}C
Maximum DC TTL output Current Magnitude	10mA (per o/p, one at a time, 1sec. duration)

Note: Stresses exceeding the Absolute Maximum Ratings may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{DD}	Operating supply voltage	4.75	5.0	5.25	Volts	
V_{IH}	Input Voltage Logic “1”	2.4		V_{DD}+0.5	Volts	
V_{IL}	Input Voltage Logic “0”	-0.5		0.8	Volts	
T_A	Ambient Operating Temperature	0		70	^oC	Still air

AC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
CKIN	EIA Crystal frequency		12.0000		MHz	1
CKIN	CCIR Crystal frequency		14.7456		MHz	1

1. Pixel Clock = $^{CKIN}/_2$

Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
I_{DCC}	Digital supply current		10		mA	1
I_{ADD}	Analog supply current		25		mA	1
I_{DD}	Overall supply current		35		mA	1
V_{REF2V7}	Internal voltage reference		2.700		Volts	
V_{BG}	Internal bandgap reference		1.22		Volts	
V_{OH}	Output Voltage Logic “1”	2.4			Volts	I_{OH} = 2mA
V_{OL}	Output Voltage Logic “0”			0.6	Volts	I_{OL} = -2mA
I_{ILK}	Input Leakage current	-1			µA	V_{IH} on input
				1	µA	V_{IL} on input

Typical conditions, V_{DD} = 5.0 V, T_A = 27^oC

1. Digital and Analogue outputs unloaded - add output current.

Operating Characteristics

Parameter	min.	typ.	max.	units	Note
Dark Current Signal		50		mV/Sec	Modal pixel voltage due to photodiode leakage under zero illumination with Gain=1 ($V_{dark} = (V_{t1} - V_{t2})/(t1-t2)$, averaged over two different frames)
Sensitivity		6		V/Lux·Sec	V_{Ave}/Lux·10ms, where Lux gives 50% saturation with Gain=1 and Exposure=10ms
Min. Illumination		0.5		Lux	Standard CCIR clock
Shading		TBA		%	Variance of V_{ave} over eight equal blocks at 50% saturation level illumination
Random Noise		-52		dB	RMS variance of all pixels, at 66% saturation, over four frames
Smear		TBA		%	Ratio of V_{ave} of the area outside a rectangle 25 lines high illuminated at 500x$V_{50\%}$ level to V_{Ave} of the rectangle
Flicker		TBA		%	Variation of V_{ave} of one line from field to field at 66% saturation level illumination
Lag		TBA		%	Average residual signal with no illumination in the field following one field of 66% sat. illumination
Blooming		TBA			Ratio of spot illumination level that produces 0.1xV_{sat} output from immediately around the spot to the V_{sat} spot illumination level (pinhole target)

Note: Devices are normaly not 100% tested for the above characterisation parameters, other than Dark Current Signal (see Blemish Specification below).

All voltage (V_A, V_{ave}, V_{sat}, $V_{xx\%}$) measurements are referenced to the black level, V_{black}, and spot blemishes are excluded (see Blemish Specification below). $V_{xx\%}$ refers to the output that is xx% of saturation, that is peak white.

Test Conditions

The sensor is tested using the example support circuit illustrated later in this document. Standard imaging conditions used for optical tests employ a tungsten halogen lamp to uniformly illuminate the sensor (to better than 0.5%), or to illuminate specific areas. A neutral density filter is used to control the level of llumination where required.

Illumination Colour Temp.	3200^{o} K
Clock Frequency	Std. CCIR
Exposure	Maximum
Gain	x1
Auto. Gain Control (AGC)	Off
Correction mode	Linear

Blemish Specification

A Blemish is an area of pixels that produces output significantly different from its surrounding pixels for the same illumination level. The definition of a Blemish Pixel varies according to testing conditions as follows:

Test	Exposure	Illumination	Blemish Pixel output definition
1 - Black Frame	Minimum	Black	Differing more than ± 100mV. from modal value.
2 - Dark Current	Maximum	Black	Output more than three times the modal value (see Dark Current Signal above).
3 - Pixel Variation	Mid range	66% Sat.	Differing more than ±35mV from modal value. Note: The mode of pixel values must be within ±70 mV of 66% of V_{sat} for all devices.

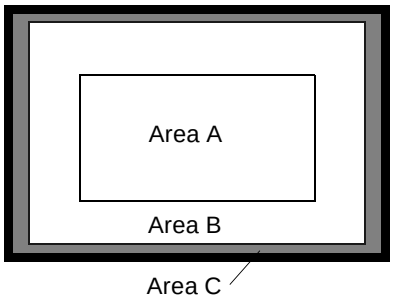
Note: Gain is set to Minimum and Correction set to Linear for all tests; measurement of blemishes for Test 3 is conducted under standard illumination (see above), set to produce average output of 66% saturation level.

The pixel area of the sensor is divided into the following areas to qualify the blemish specification:

Area A is the central area of the array as defined by the box with sides 50% of the linear height and 50% of the linear width of the array.

Area C is 10 vertical pixels by 10 horizontal pixels around the edge of the array.

Area B is the remaining area of the array.



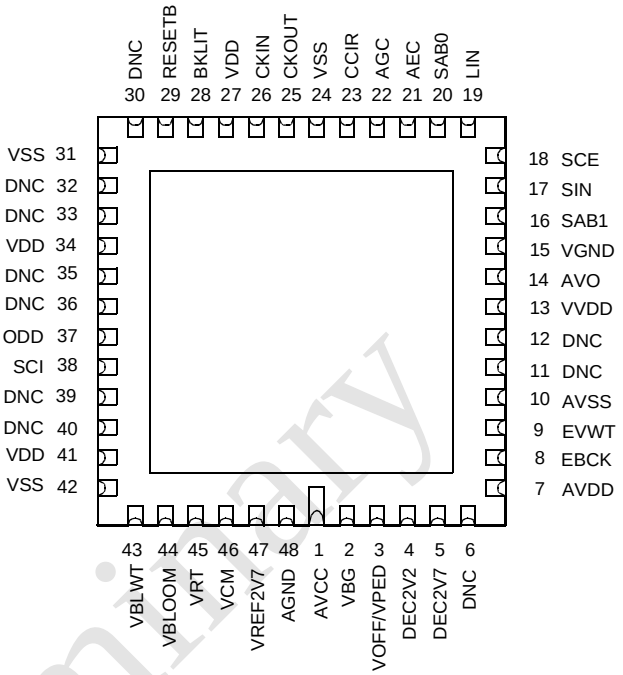
The blemish specification is then defined as follows:

Image Area	Max. No. of Blemishes	Notes
Area A	0	This is the most critical image area
Area B	4	Unconnected single pixels
	1	Of up to four connected pixels (2x2 max.)
Area C	Any number	Blemishes in this area are not significant, but the device shall, however, have no row or column (>50% of row or column) faults in any area.

Pinout Diagram

48 Pin LCC

Viewed from top of package



Pins Marked “DNC” must be left ‘floating’.

PIN LIST

Pin	Name	Type	Description
POWER SUPPLIES			
1	AVCC	PWR	Core analogue power and reference supplies.
7	AVDD	PWR	output stage power. AVDD3 output stage logic.
10	AVSS	GND	Output stage ground. AVSS3 output stage logic.
13	VVDD	PWR	75ohm buffer supply.
15	VGND	GND	75ohm buffer ground.
24,31	VSS	GND	Digital padring & logic ground.
27,34	VDD	PWR	Digital padring & logic power.
41	DVDD	PWR	Core digital power.
42	DVSS	GND	Core digital ground.
48	AGND	GND	Core analogue ground and reference supplies.

Pin	Name	Type	Description
ANALOGUE VOLTAGE REFERENCES			
2	VBG	OA	Internal bandgap reference voltage (1.22V nominal). Requires external 0.1uF capacitor.
3	VOFF/ VPED	IA	Pedestal DAC & Offset Comp. DAC bias. Connect to VBG or external reference.
4	DEC2V2	OA	Decouple 2.2V reference. Requires external 0.1uF capacitor.
5	DEC2V7	OA	Decouple 2.7V reference. Requires external 0.1uF capacitor.
8	EBCK	IA	External black level bias. Internally generated. Decouple to VGND
9	EVWT	IA	External white pixel threshold for exposure control. Decouple to VGND
43	VBLWT	IA	Defines white level for clamp circuitry. Requires external 0.1uF capacitor.
44	VBLOOM	OA	Anti-blooming voltage reference. Requires external 0.1uF capacitor.
45	VRT	IA	Pixel reset voltage. Connect to VREF2V7 or external reference.
46	VCM	IA	Offset DAC common mode input. Connect to VREF2V7.
47	VREF2V7	OA	Internally generated 2.7V reference. Requires external 4.7uF capacitor.
ANALOGUE OUTPUTS			
14	AVO	OA	Buffered Analogue video out. Can drive a doubly terminated 75ohm load.
SYSTEM CLOCKS			
25	CKOUT	OD	Oscillator output. Connect Crystal for standard timing.
26	CKIN	ID	Oscillator input. Connect Crystal for standard timing.
IMAGE TIMING SIGNALS			
37	ODD	OD	Odd/even field signal. (ODD = 1 for odd fields, ODD = 0 for even)

Pin	Name	Type	Description
DIGITAL CONTROL SIGNALS			
16	SAB1	ID↓	Chip Address, Bit 1
17	SIN	ID↓	Used to reset video timing control logic without resetting any other part of VV5402. Resets video logic on the falling edge of the SIN pulse.
18	SCE	ID↓	Scan Mode Enable - only relevant to test mode.
19	LIN	ID↓	Gamma corrected or Linear output. LIN = 0, gamma corrected output, LIN = 1, linear output. Default is gamma.
20	SAB0	ID↓	Chip Address, Bit 0
21	AEC	ID↑	Automatic exposure control. AEC = 1, auto exposure is enabled; AEC = 0 auto exposure **and** auto gain control are disabled.
22	AGC	ID↑	Automatic gain control enable. AGC = 1, auto-gain is enabled (if AEC = 1); AGC = 0, auto-gain is disabled.
23	CCIR	ID↑	Select default video mode for power-on. CCIR = 1 for CCIR video. EIA video mode is selected when CCIR = 0. Default is CCIR if unconnected
28	BKLIT	ID↓	Normal or Backlit exposure control mode. BKLIT = 0, normal mode; BKLIT = 1, backlit mode. Default is normal. See Exposure Control for details.
29	RESETB	ID↑	Active low camera reset. All camera systems are reset to power-on state.
38	SCI	ID↓	Scan Chain Input - only relevant to test mode.
OTHER PINS			
6, 11, 12, 30, 32, 33, 35, 36, 39, 40		DNC	DO NOT CONNECT. These pins must be left ‘floating’ for correct operation.

Key:

OA - Analogue output
OD - Digital output
OD↓ - Digital output with internal pull-down
BI - Bidirectional
IA - Analogue input
ID - Digital input
ID↑ - Digital input with internal pull-up
DNC- Do Not Connect

VIDEO STANDARDS

The VV5402 has 2 different video format modes, producing CCIR or EIA standard composite Monochrome video output. Line standards and frequencies are as follows:

Video Mode	Format	Image (Pixels)	Crystal Frequency	CCIR pin
CCIR	4:3	384 x 287	14.7456 MHz	1
EIA	4:3	320 x 243	12.0000 MHz	0

VV5402 Video Modes

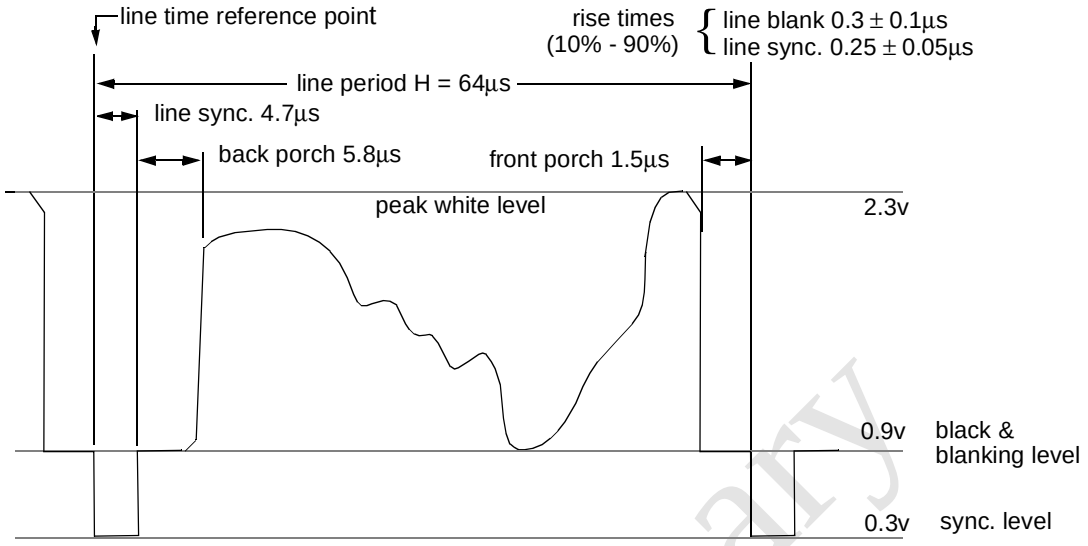
Video signal Characteristics

The following table summarises the composite video output levels (AVO) for the two standards, which are graphically illustrated on the following pages:

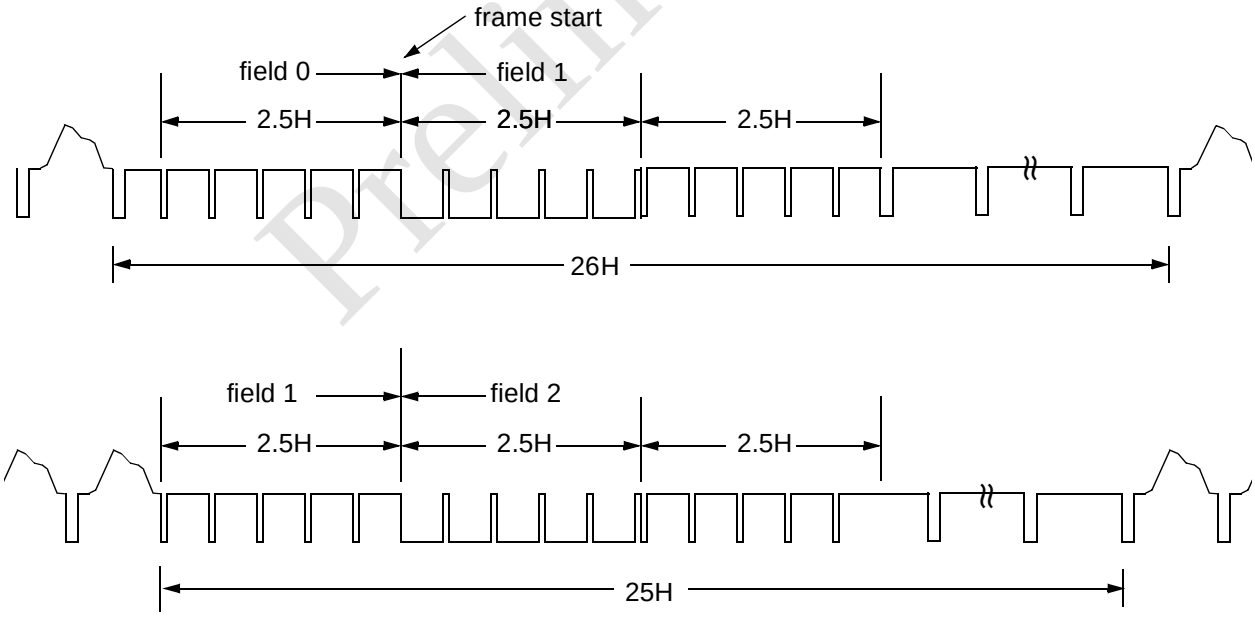
Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{Sync}	CCIR, EIA Sync. level		0.3		V	
V_{blank}	CCIR, EIA Blanking level		0.9		V	DC reference level
V_{black}	CCIR Black level		0.9		V	
	EIA Black level		1.0		V	
V_{Sat}	CCIR Saturation level		2.3		V	Peak White; AVO clipped at this level
	EIA Saturation level		2.4		V	

Note: All measurements are made with AVO driving one 75Ω load.

CCIR Timing Diagram

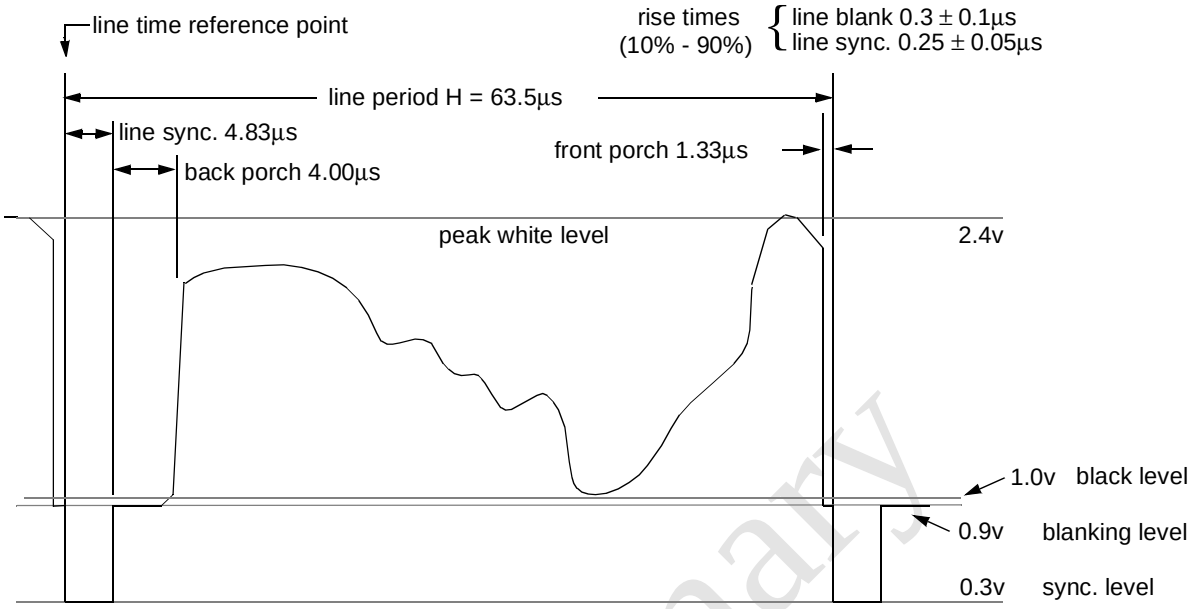


CCIR composite video signal - line level timing

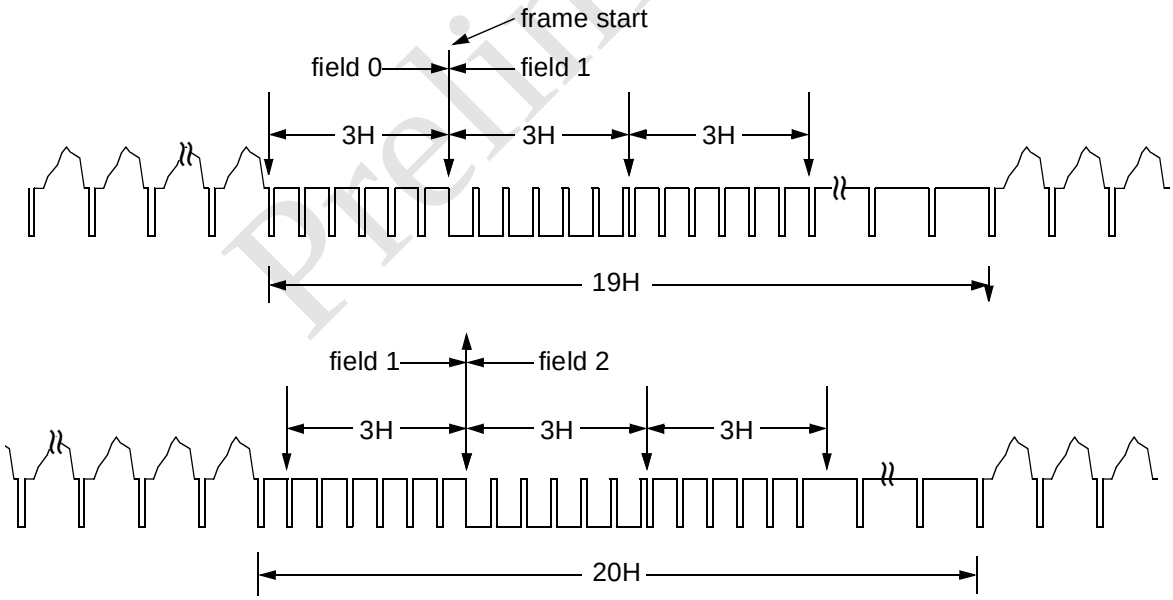


CCIR composite video signal - field level timing

EIA Timing Diagrams

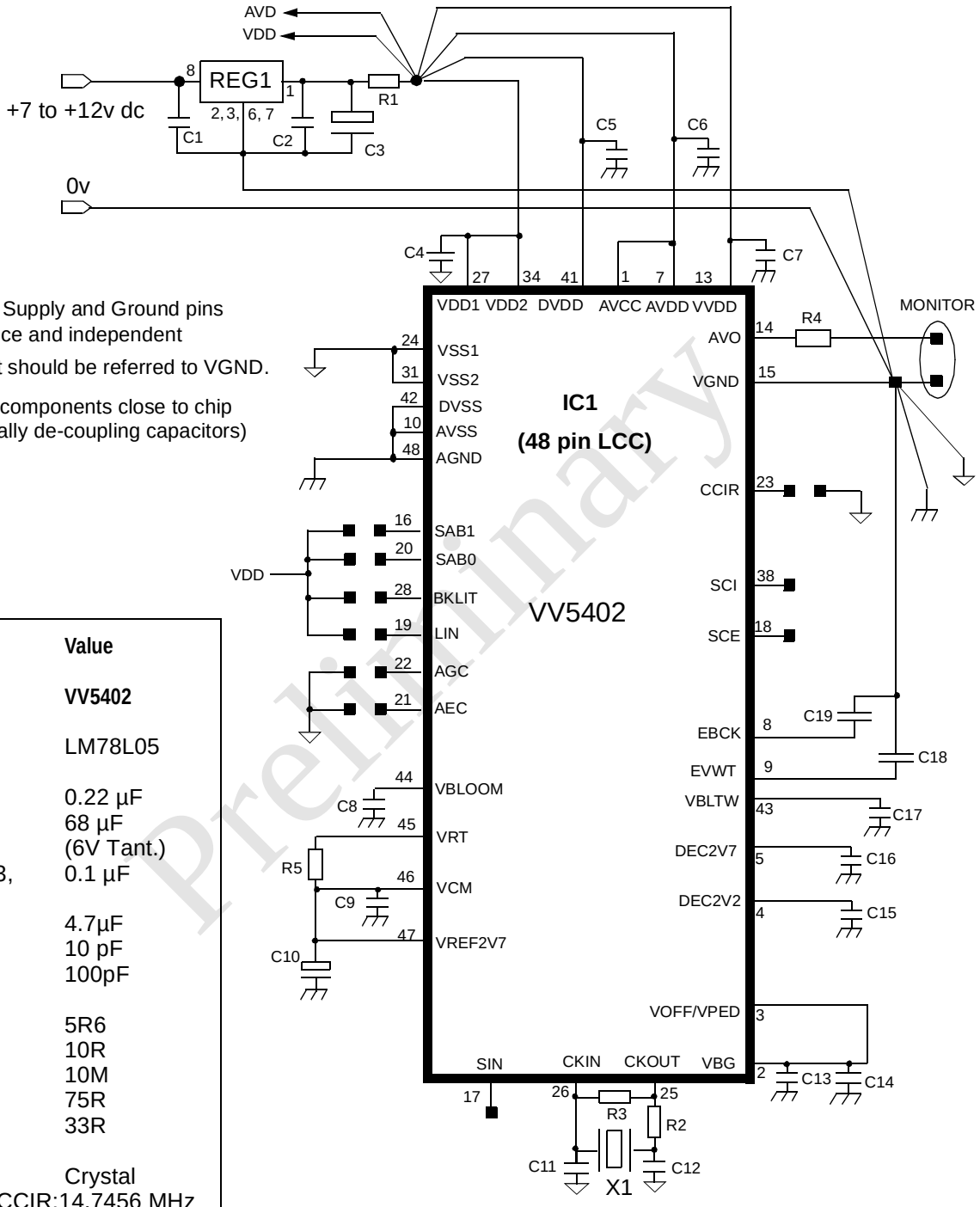


EIA composite video signal - line level timing



EIA composite video signal - field level timing

EXAMPLE SUPPORT CIRCUIT



1. Keep nodes Supply and Ground pins low impedance and independent
2. Video output should be referred to VGND.
3. Keep circuit components close to chip pins (especially de-coupling capacitors)

Component	Value
IC1	**VV5402**
REG1	LM78L05
C1,C2	0.22 µF
C3	68 µF (6V Tant.)
C4-C9,C13, C16-C19	0.1 µF
C10	4.7µF
C11, C12	10 pF
C14	100pF
R1	5R6
R2	10R
R3	10M
R4	75R
R5	33R
X1	Crystal CCIR:14.7456 MHz EIA:12.0000 MHz

Use Surface Mount components throughout.

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