



VX1129 / VX1128

HIGH QUALITY VIDEO DECODER
PROGRESSIVE PROCESSOR AND
TIMING CONTROLLER

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1 OVERVIEW

1.1 DESCRIPTION

VX1129/VX1128 is a progressive video processor IC, consists of video decoder, 3-D deinterlacer, picture enhancement engine, the scaling engine specially designed for video apps – the Relács, T-con for LCD panel timing control. It receives NTSC / PAL / SECAM analog video signal from DVD or TV, or digitized interlaced video stream (BT. 656 or bt. 601) from video decoder or MPEG video decoder. VX1129/VX1128 can perform high quality picture enhancement such as video noise reduction, sharpening, black-level extension, and Gamma correction, and converts it into non-interlaced formats for direct display on progressive devices, such as LCD displays, DTV, projectors, or PC monitors. Its output resolution covers 640x480, 720x480, 800x480, 854x480, 800x600, 1024x768, 1280x720, 1280x768, 1280x1024. VX1129/VX1128 provides theater quality progressive scan video with VXIS's innovated *Motion Adaptive-3D Deinterlace Algorithm*, 3-2 pull down with automatic film mode detection, *Edge Preserving Pixel Interpolation*, frame-rate conversion, synchronization regeneration, and automatic source mode detection. The font-based

on-screen-display(OSD), universal rogrammable timing control makes it become a highly integrated, most cost-efficient LCD video processor. The VX1129 (VX1128 without this function) can also receives progressive digital R,G,B signal from PC or DVD to perform PIP processing or direct progressive output for Mutimedia panel.

1.2 APPLICATION

- Portable DVD
- Car TV
- Small/middle size LCD TV
- PDP TV
- Multimedia panel

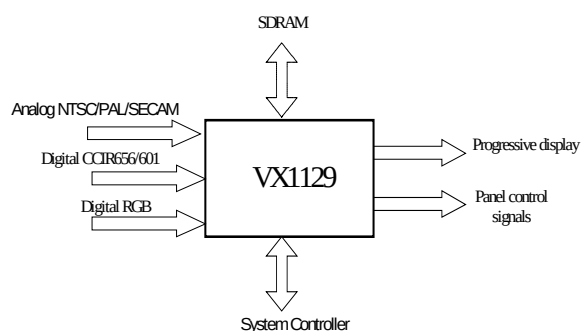


Figure 1.1 Interface for VX1129

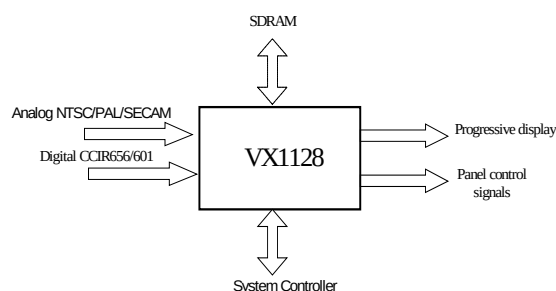


Figure 1.2 Interface for /VX1128

1.3 FEATURES

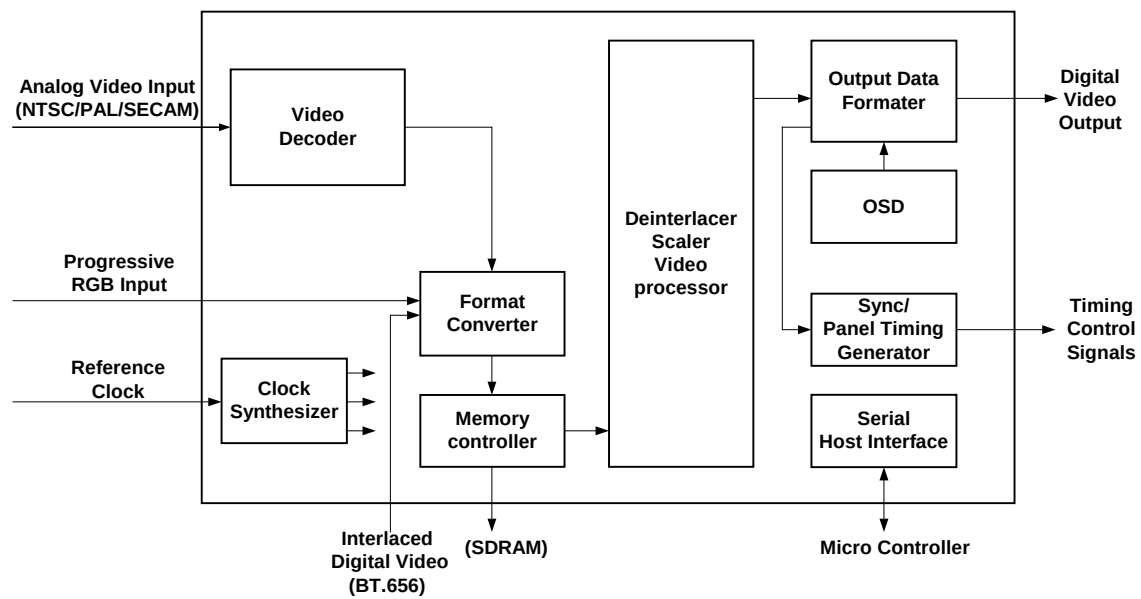
- Support Various Analog Video Input Formats
 - 6 Analog inputs : 6x CVBS or 4x CVBS + 1x S-video or 3x S-video or 1x CVBS + 1x S-video + 1x YpbPr
 - Support NTSC, NTSC-Japan, PAL (B, D, G, H, I, M, N, Nc) and SECAM video standard
- 10-bit A/D converters with fixed sampling clock
- Automatic Clamp Control (ACC) for CVBS and S-video
- Automatic gain control (AGC) / automatic chroma gain control
- Three analog preprocessing channels with digitally controlled AGC/clamp
- Horizontal and vertical Sync Detection
- Automatic detection of 50/60Hz field frequency and automatic switching between standards PAL, (Nc), PAL M, SECAM and NTSC
- Adaptive comb filter for two dimensions chrominance / luminance separation
- PAL delay line for correcting PAL phase errors and chroma noise cancellation
- VBI slicer supporting closed caption
- Macro-vision copyright detection
- Support Various Digital Video Input Formats
 - ITU-R BT.656
 - 8/16-Bit ITU-R BT.601 + Horizontal Sync + Vertical Sync
 - 24-Bit 4:4:4 YUV + Horizontal Sync + Vertical Sync
 - 24-Bit progressive RGB + Horizontal Sync + Vertical Sync for PIP
- Support Various Digital Video Output Formats
 - 24/18/16-Bit RGB + Horizontal Sync + Vertical Sync
 - 24/18/16-Bit 4:4:4 YUV + Horizontal Sync + Vertical Sync
 - 24/18/16-Bit 4:4:4 YPbPr (with Embedded Horizontal and Vertical Sync on Y)
 - 16-Bit 4:2:2 YUV + Horizontal Sync + Vertical Sync
 - 24-Bit 4:4:4 Interlaced YPbPr (with Embedded Horizontal and Vertical Sync on Y)
- Support Video-on-Progressive_RGB with Build-In PIP
- Frame rate up-conversion to 60 Hz for PAL & SECAM
- 2D or Motion-Adaptive 3D(with SDRAM) Deinterlace
- Edge-Preserving Pixel Interpolation
- Automatic Video Source Detection
- Embedded Scaling Engine (Relacs), Supporting Output Resolution 640x480, 720x480 800x480, 854x480, 800x600, 1024x768, 1280x720, 1280x768, 1280x1024.
- Programmable Zoom/Shrink Scale with Anamorphic / Panoramic /4:3 / 16:9 Zoom Support
- Brightness, Contrast, Saturation, and Hue Adjustment

Product Specification**High Quality Video Processor**

- Color Transient Improvement, Adaptive Black-Level Extension, Skin Tone Enhancement.
- Video Noise Reduction
- Frequency Directive Picture Sharpening
- 3-Channel 10-Bit Build-In Color gamma Look-Up Table for Video Fine-Tune
- Synchronization Re-Generation to Perform Stable Video.
- Host Interface Compatible with Two-Wire IIC, Serial Interface
- OSD with 128 Build-in and 64 Programmable Font and Attribute Table, 16 Colors at same Time from 16,777,216-Color Template, Blinking, and Blending
- R/G/B input/output port swap & rotation control
- 8 pins of programmable panel timing control signals
- One 20 MHz crystal request only
- 2.5V / 3.3V power supply with 5V tolerant digital I/O

1.4 BLOCK DIAGRAM

1.4.1 BLOCK DIAGRAM OF VX1129



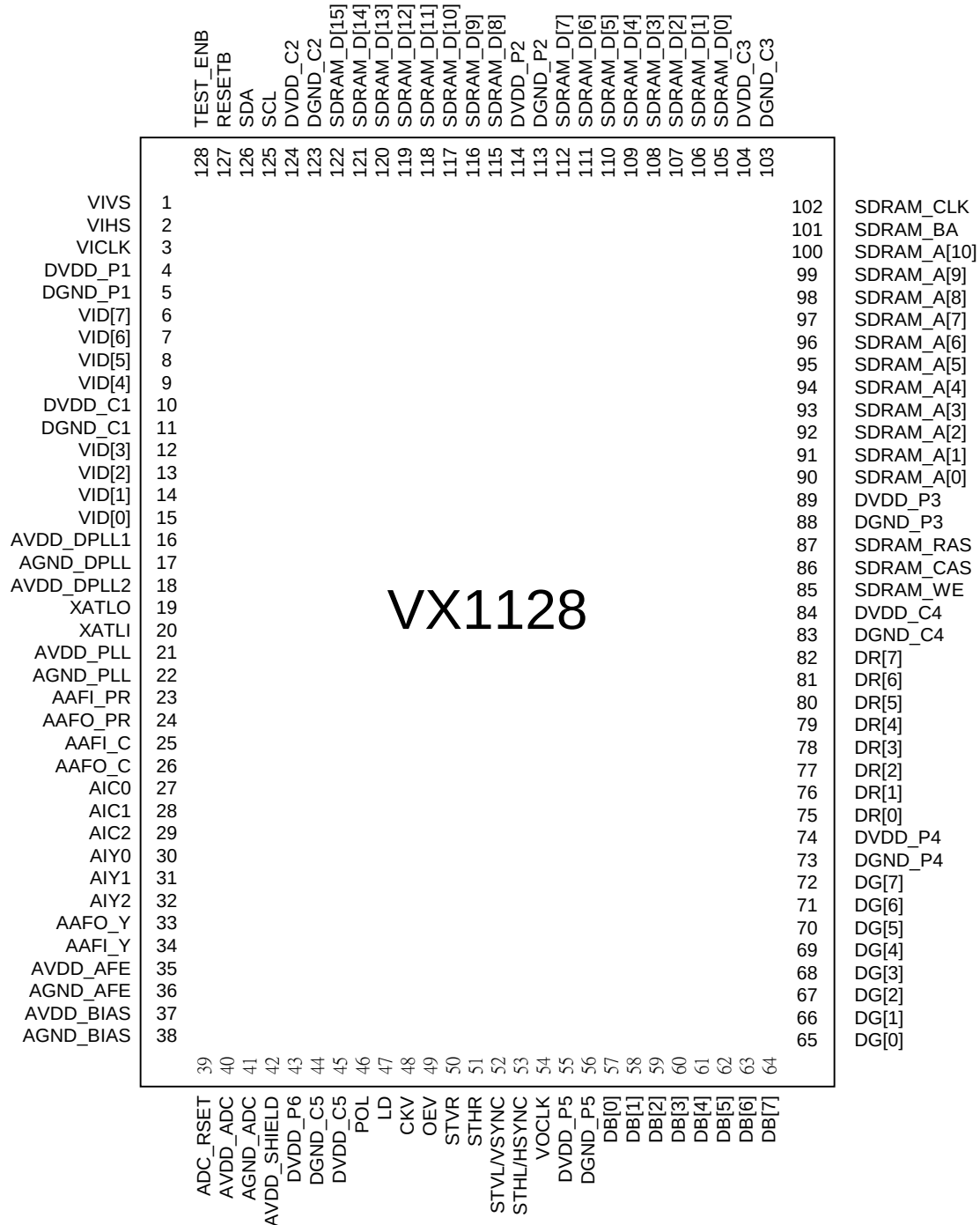
1.5 PINOUT DIAGRAM

1.5.1 PINOUT DIAGRAM OF VX1129

EXV1[3]	1	EXV1[4]
EXV1[2]	2	EXV1[5]
EXV1[1]	3	EXV1[6]
EXV1[0]	4	EXV1[7]
VIVS	5	EXV2[0]
VIHS	6	EXV2[1]
VICLK	7	EXV2[2]
DVDD_P1	8	EXV2[3]
DGND_P1	9	EXV2[4]
VID[7]	10	EXV2[5]
VID[6]	11	EXV2[6]
VID[5]	12	EXV2[7]
VID[4]	13	TEST_ENB
DVDD_C1	14	RESETB
DGND_C1	15	SDA
VID[3]	16	SCL
VID[2]	17	DVDD_C2
VID[1]	18	DGND_C2
VID[0]	19	SDRAM_D[15]
AVDD_DPLL1	20	SDRAM_D[14]
AGND_DPLL	21	SDRAM_D[13]
AVDD_DPLL2	22	SDRAM_D[12]
XATLO	23	SDRAM_D[11]
XATLI	24	SDRAM_D[10]
AVDD_PLL	25	SDRAM_D[9]
AGND_PLL	26	SDRAM_D[8]
AAFI_PR	27	DVDD_P2
AAFO_PR	28	DGND_P2
AAFI_C	29	SDRAM_D[7]
AAFO_C	30	SDRAM_D[6]
AIC0	31	SDRAM_D[5]
AIC1	32	SDRAM_D[4]
AIC2	33	SDRAM_D[3]
AIY0	34	SDRAM_D[2]
AIY1	35	SDRAM_D[1]
AIY2	36	SDRAM_D[0]
AAFO_Y	37	DVDD_C3
AAFI_Y	38	DGND_C3
AVDD_AFE	39	SDRAM_CLK
AGND_AFE	40	SDRAM_BA
AVDD_BIAS	41	
AGND_BIAS	42	
ADC_RSET	43	
AVDD_ADC	44	
AGND_ADC	45	
AVDD_SHIELD	46	
EXV3[7]	47	
EXV3[6]	48	
EXV3[5]	49	
EXV3[4]	50	
EXV3[3]	51	
EXV3[2]	52	
EXV3[1]	53	
EXV3[0]	54	
VIVSP	55	
VIHSP	56	
VICLK_P	57	
DGND_P6	58	
DVDD_P6	59	
DGND_C5	60	
DVDD_C5	61	
POL	62	
LD	63	
CKV	64	
OEV	65	
STVR	66	
STHR	67	
STLV/SHV	68	
STHL/SHV	69	
VOCLK	70	
DVDD_P5	71	
DGND_P5	72	
DB[0]	73	
DB[1]	74	
DB[2]	75	
DB[3]	76	
DB[4]	77	
DB[5]	78	
DB[6]	79	
DB[7]	80	
		SDRAM_A[10]
		SDRAM_A[9]
		DVDD_P7
		DGND_P7
		SDRAM_A[8]
		SDRAM_A[7]
		SDRAM_A[6]
		SDRAM_A[5]
		SDRAM_A[4]
		SDRAM_A[3]
		SDRAM_A[2]
		SDRAM_A[1]
		SDRAM_A[0]
		DVDD_P3
		DGND_P3
		SDRAM_RAS
		SDRAM_CAS
		SDRAM_WE
		DVDD_C4
		DGND_C4
		DR[7]
		DR[6]
		DR[5]
		DR[4]
		DR[3]
		DR[2]
		DR[1]
		DR[0]
		DVDD_P4
		DGND_P4
		DVDD_C6
		DGND_C6
		DG[7]
		DG[6]
		DG[5]
		DG[4]
		DG[3]
		DG[2]
		DG[1]
		DG[0]

VX1129

1.5.2 PINOUT DIAGRAM OF VX1128



1.6 PIN ASSIGNMENT

1.6.1 PIN ASSIGNMENT OF VX1129

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	EXV1[3]	41	AVDD_BIAS	81	DG[0]	121	SDRAM_BA
2	EXV1[2]	42	AGND_BIAS	82	DG[1]	122	SDRAM_CLK
3	EXV1[1]	43	ADC_RSET	83	DG[2]	123	DGND_C3
4	EXV1[0]	44	AVDD_ADC	84	DG[3]	124	DVDD_C3
5	VIVS	45	AGND_ADC	85	DG[4]	125	SDRAM_D[0]
6	VIHS	46	AVDD_SHIELD	86	DG[5]	126	SDRAM_D[1]
7	VICLK	47	EXV3[7]	87	DG[6]	127	SDRAM_D[2]
8	DVDD_P1	48	EXV3[6]	88	DG[7]	128	SDRAM_D[3]
9	DGND_P1	49	EXV3[5]	89	DGND_C6	129	SDRAM_D[4]
10	VID[7]	50	EXV3[4]	90	DVDD_C6	130	SDRAM_D[5]
11	VID[6]	51	EXV3[3]	91	DGND_P4	131	SDRAM_D[6]
12	VID[5]	52	EXV3[2]	92	DVDD_P4	132	SDRAM_D[7]
13	VID[4]	53	EXV3[1]	93	DR[0]	133	DGND_P2
14	DVDD_C1	54	EXV3[0]	94	DR[1]	134	DVDD_P2
15	DGND_C1	55	VIVSP	95	DR[2]	135	SDRAM_D[8]
16	VID[3]	56	VIHSP	96	DR[3]	136	SDRAM_D[9]
17	VID[2]	57	VICLKP	97	DR[4]	137	SDRAM_D[10]
18	VID[1]	58	DGND_P6	98	DR[5]	138	SDRAM_D[11]
19	VID[0]	59	DVDD_P6	99	DR[6]	139	SDRAM_D[12]
20	AVDD_DPLL1	60	DGND_C5	100	DR[7]	140	SDRAM_D[13]
21	AGND_DPLL	61	DVDD_C5	101	DGND_C4	141	SDRAM_D[14]
22	AVDD_DPLL2	62	POL	102	DVDD_C4	142	SDRAM_D[15]
23	XATLO	63	LD	103	SDRAM_WE	143	DGND_C2
24	XATLI	64	CKV	104	SDRAM_CAS	144	DVDD_C2
25	AVDD_PLL	65	OEVS	105	SDRAM_RAS	145	SCL
26	AGND_PLL	66	STVR	106	DGND_P3	146	SDA
27	AAFI_PR	67	STHR	107	DVDD_P3	147	RESET_B
28	AAFO_PR	68	STVL/VSYN	108	SDRAM_A[0]	148	TEST_ENB
29	AAFI_C	69	STHL/HSYN	109	SDRAM_A[1]	149	EXV2[7]
30	AAFO_C	70	VOCLK	110	SDRAM_A[2]	150	EXV2[6]
31	AIC0	71	DVDD_P5	111	SDRAM_A[3]	151	EXV2[5]
32	AIC1	72	DGND_P5	112	SDRAM_A[4]	152	EXV2[4]
33	AIC2	73	DB[0]	113	SDRAM_A[5]	153	EXV2[3]
34	AIY0	74	DB[1]	114	ADRAM_A[6]	154	EXV2[2]
35	AIY1	75	DB[2]	115	SDRAM_A[7]	155	EXV2[1]
36	AIY2	76	DB[3]	116	SDRAM_A[8]	156	EXV2[0]
37	AAFO_Y	77	DB[4]	117	DGND_P7	157	EXV1[7]
38	AAFI_Y	78	DB[5]	118	DVDD_P7	158	EXV1[6]
39	AVDD_AFE	79	DB[6]	119	SDRAM_A[9]	159	EXV1[5]
40	AGND_AFE	80	DB[7]	120	SDRAM_A[10]	160	EXV1[4]

1.6.2 PIN ASSIGNMENT OF VX1128

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	VIVS	39	ADC_RSET	65	DG[0]	103	DGND_C3
2	VIHS	40	AVDD_ADC	66	DG[1]	104	DVDD_C3
3	VICLK	41	AGND_ADC	67	DG[2]	105	SDRAM_D[0]
4	DVDD_P1	42	AVDD_SHIELD	68	DG[3]	106	SDRAM_D[1]
5	DGND_P1	43	DVDD_P6	69	DG[4]	107	SDRAM_D[2]
6	VID[7]	44	DGND_C5	70	DG[5]	108	SDRAM_D[3]
7	VID[6]	45	DVDD_C5	71	DG[6]	109	SDRAM_D[4]
8	VID[5]	46	POL	72	DG[7]	110	SDRAM_D[5]
9	VID[4]	47	LD	73	DGND_P4	111	SDRAM_D[6]
10	DVDD_C1	48	CKV	74	DVDD_P4	112	SDRAM_D[7]
11	DGND_C1	49	OEVS	75	DR[0]	113	DGND_P2
12	VID[3]	50	STVR	76	DR[1]	114	DVDD_P2
13	VID[2]	51	STHR	77	DR[2]	115	SDRAM_D[8]
14	VID[1]	52	STVL/VSYN	78	DR[3]	116	SDRAM_D[9]
15	VID[0]	53	STHL/HSYN	79	DR[4]	117	SDRAM_D[10]
16	AVDD_DPLL1	54	VOCLK	80	DR[5]	118	SDRAM_D[11]
17	AGND_DPLL	55	DVDD_P5	81	DR[6]	119	SDRAM_D[12]
18	AVDD_DPLL2	56	DGND_P5	82	DR[7]	120	SDRAM_D[13]
19	XATLO	57	DB[0]	83	DGND_C4	121	SDRAM_D[14]
20	XATLI	58	DB[1]	84	DVDD_C4	122	SDRAM_D[15]
21	AVDD_PLL	59	DB[2]	85	SDRAM_WE	123	DGND_C2
22	AGND_PLL	60	DB[3]	86	SDRAM_CAS	124	DVDD_C2
23	AAFI_PR	61	DB[4]	87	SDRAM_RAS	125	SCL
24	AAFO_PR	62	DB[5]	88	DGND_P3	126	SDA
25	AAFI_C	63	DB[6]	89	DVDD_P3	127	RESET_B
26	AAFO_C	64	DB[7]	90	SDRAM_A[0]	128	TEST_ENB
27	AIC0			91	SDRAM_A[1]		
28	AIC1			92	SDRAM_A[2]		
29	AIC2			93	SDRAM_A[3]		
30	AIY0			94	SDRAM_A[4]		
31	AIY1			95	SDRAM_A[5]		
32	AIY2			96	ADRAM_A[6]		
33	AAFO_Y			97	SDRAM_A[7]		
34	AAFI_Y			98	SDRAM_A[8]		
35	AVDD_AFE			99	SDRAM_A[9]		
36	AGND_AFE			100	SDRAM_A[10]		
37	AVDD_BIAS			101	SDRAM_BA		
38	AGND_BIAS			102	SDRAM_CLK		

1.7 PIN DESCRIPTION

Video Input Pins			
Name	Type	Description	Notes
VID [7:0]	I	Digital Video Input Data(BT 656/601 / Y)	
VIHS	I	Digital Video Input Horizontal Synchronization	
VIVS	I	Digital Video Input Vertical Synchronization	
VICLK	I	Digital Video Input Clock	
EXV1[7:0]	I	Digital progressive video input data for PIP (R / Cb / CbCr)	Vx1129 only
EXV2[7:0]	I	Digital progressive video input data for PIP (G / Cr)	Vx1129 only
EXV3[7:0]	I	Digital progressive video input data for PIP (B)	Vx1129 only
VIHSP	I	Digital progressive video input Horizontal Synchronization	Vx1129 only
VIVSP	I	Digital progressive video input Vertical Synchronization	Vx1129 only
VICLKp	I	Digital progressive video input Clock	Vx1129 only
Video Output Pins			
Name	Type	Description	Notes
DR [7:0]	O _{TS1}	R/V/Pr/BT656 Digital Video Output	
DG [7:0]	O _{TS1}	G/Y Digital Video Output	
DB [7:0]	O _{TS1}	B/U/Pb Digital Video Output	
HSYNC /	O ₁	Video Output Horizontal Synchronization /	
STHL		Composite Synchronization /	
		STHL for TCON	
VSYNC /	O ₁	Video Output Vertical Synchronization /	
STVL		STVL for TCON	
VOCLK	O ₂	Video Output Clock / BT656 Output Clock	
STHR	I/O ₁	TCON Horizontal start address	
STVR	I/O ₁	TCON Vertical start address	
POL	I/O ₁	TCON Polarity Selection	
LD	I/O ₁	TCON Latch	
CKV	I/O ₁	TCON Sample Clock	
OEV	I/O ₁	TCON Output Enable	
External SDRAM I/O Pins			
Name	Type	Description	Notes
SDRAM_D [15:0]	I/O ₁	SDRAM Data Bus	
SDRAM_A [10:0]	O _{T1}	SDRAM Address Bus	
SDRAM_CLK	O _{T2}	SDRAM Clock	
SDRAM_RAS	O _{T1}	SDRAM Row Address Strobe (Active Low)	
SDRAM_CAS	O _{T1}	SDRAM Column Address Strobe (Active Low)	
SDRAM_WE	O _{T1}	SDRAM Write Enable (Active Low)	
SDRAM_BA	O _{T1}	SDRAM Bank	
Analog I/O Pins			
Name	Type	Description	Notes
AIY0	AI	Analog Composite or Luminance Input	
AIY1	AI	Analog Composite or Luminance Input	
AIY2	AI	Analog Composite or Luminance Input	

AIC0	AI	Analog Composite or Chrominance Input	
AIC1	AI	Analog Composite or Chrominance Input or Pb Input	
AIC2	AI	Analog Composite or Chrominance Input or Pr Input	
Auxiliary Analog I/O Pins (8)			
Name	Type	Description	Notes
AAFO_Y	AO	Analog Signal to Optional External Anti-Alias Filter of Y-channel	
AAFO_C	AO	Analog Signal to Optional External Anti-Alias Filter of C/Pb-channel	
AAFO_PR	AO	Analog Signal to Optional External Anti-Alias Filter of Pr-channel	
AAFIY	AI	Analog Signal from Optional External Anti-Alias Filter of Y-channel	
AAFIC	AI	Analog Signal from Optional External Anti-Alias Filter of C/Pb-channel	
AAFI_PR	AI	Analog Signal from Optional External Anti-Alias Filter of Pr-channel	
ADC_RSET	AI	Connect to an External Resister for Setting the Bias Current of ADC	
Miscellaneous I/O Pins			
Name	Type	Description	Notes
/RESET	I _S	Chip Reset (Active Low)	
XTALO	XO	Crystal Output	
XTALI	XI	Crystal Input	
SDA	I/O ₁	Host Interface Serial Data / Address	
SCL	I _S	Host Interface Serial Clock	
/TEST_EN	I _{PU}	Test Mode Enable (Active Low)	
Power Pins			
Name	Type	Description	Notes
AVDD_PLL	P ₃₃	Analog 3.3V Supply For PLL	Qty: 1
AVDD_AFE	P ₃₃	Analog 3.3V Supply For AFE	Qty: 1
AVDD_BIAS	P ₃₃	Analog 3.3V Supply For BIAS	Qty: 1
AVDD_ADC	P ₃₃	Analog 3.3V Supply For ADC	Qty: 1
AVDD_SHIELD	P ₃₃	Analog 3.3V Supply For Shielding	Qty: 1
AVDD_DPLL1	P ₂₅	Digital 2.5V Supply For PLL	Qty: 1
AVDD_DPLL2	P ₂₅	Digital 2.5V Supply For PLL	Qty: 1
DVDD_P1~7	P ₂₅	Digital 3.3V Supply For I/O	Qty: 7

DVDD_C1~6	P ₂₅	Digital 2.5V Supply For CORE	Qty: 6
AGND_PLL	G	Analog Ground For PLL	Qty: 1
AGND_AFE	G	Analog Ground For AFE	Qty: 1
AGND_BIAS	G	Analog Ground For BIAS	Qty: 1
AGND_ADC	G	Analog Ground For ADC	Qty: 1
AGND_DPLL	G	Digital Ground For PLL	Qty: 1
DGND_P1~7	G	Digital Ground For I/O	Qty: 7
DGND_C1~6	G	Digital Ground For CORE	Qty: 6

1.8 PACKAGE

- 1129 160-Pin HQFP
- 1128 128-Pin LQFP-EP