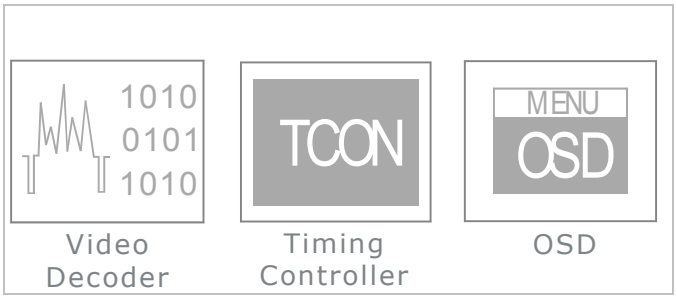
VX1828B

VIDEO PROCESSOR FOR MIDDLE SIZE LCD PANEL



REVISION HISTORY

Revision	Date	Pages	Description
0.1	2005.06.09	64	Initial Draft
0.2	2005.06.14	64	Update panel support

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1. FEATURE

VIDEO DECODER

- Composite and S-Video Inputs: NTSC and NTSC-Japan; PAL (B, D, G, H, I, M, N, Nc)
- 6 Analog Inputs: Capable of 2xCVBS+2xS-Video or 4xCVBS+1xS-Video Inputs
- Support CCIR656 Input/Output
- Analog Automatic Gain Control
- 10-Bit 2-Channel A/D Converters with Fixed Sampling Clock
- Require Only One Crystal (20 MHz) for All Standards
- Automatic Mode Detection
- Internal Phase Lock Loop to Generate Video Clock
- 2-D Comb Filter for Luminance and Chrominance Separation
- Precise Chrominance Demodulation
- Internal Buffers for Video Stability Control
- Frequency Directive 2-D Sharpening
- Brightness, Contrast, Color, and Tint Adjustments
- Adaptive Black-Level Extension
- Video Noise Reduction
- Chrominance Transient Improvement
- EZ-Gamma Programming Hardware Support
- MacroVision Copy Right Detection

OSD

- 160-Character Font Memory (128 built-in plus 32 user-defined characters)
- Alpha-Blending with OSD Content and Video
- Blinking and Highlight Function

LCD DISPLAY CONTROL

- Build-in Universal T-CON for 480/960/1200/1440/1920x234 analog LCD panels
- Digital RGB Independent Output Line-Inversion, Offset, and Ratio Control
- Built-In Video DAC for Analog RGB Output

INTERFACE

- Two-Wire Serial Host Interface Compatible with IIC Interface
- 2.5/3.3V Power Supply
- 5-Volt Tolerant Digital I/O; Optional open-drain panel interface
- 100-Pin LQFP Package

2. GENERAL DESCRIPTION

VX1828B is a high quality video processor IC for middle size LCD panel application. VX1828B can accept digital or analog video inputs, then output digital or analog video signals. The digital input is CCIR656 and the analog input is NTSC/PAL video signals from TV tuner, DVD, or VCR sources, including weak and distorted signals. VX1828B decodes these video inputs into R/G/B analog signals or CCIR656 digital format. The R/G/B analog signals directly drive the panel with build-in timing controller.

The build-in automatic gain control (AGC) and 10-bit 2-channel AD converters maintain high-resolution video quality, and with automatic video mode detection, user can freely switch and adjust variety of signal source. The multiple internal adaptive PLLs also can help precisely extract pixel clock from video source and perform sharp-and-keen color demodulation. Adaptive 2-D comb-filter, 2-D sharpening, and synchronization are implemented with build-in line-buffers.

The output format of VX1828B directly supports 480/960/1200/1440/1920x234 analog TFT-LCD modules.

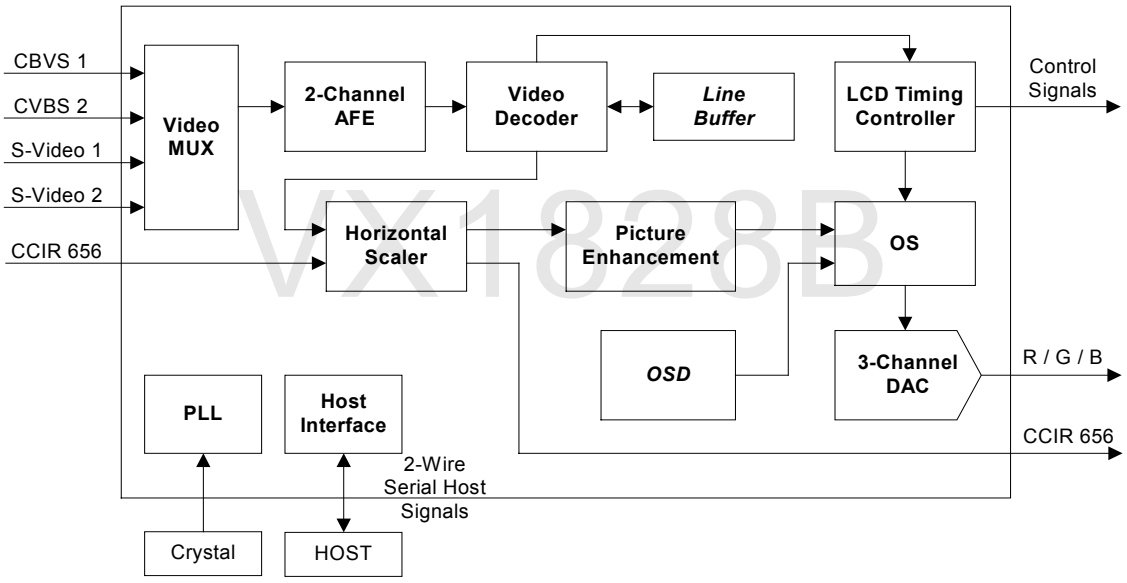
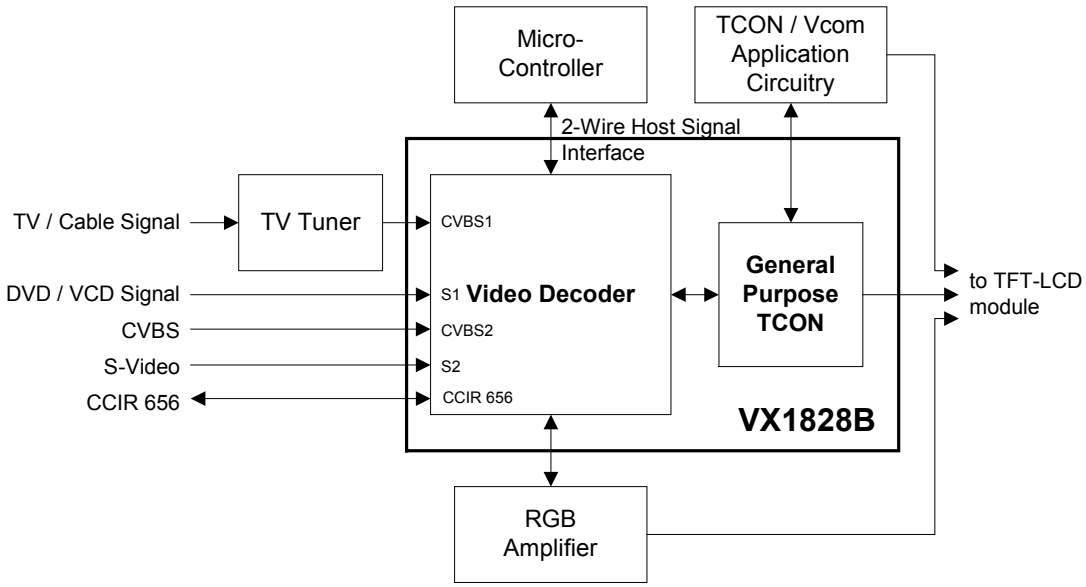


Figure 2.1 Block Diagram

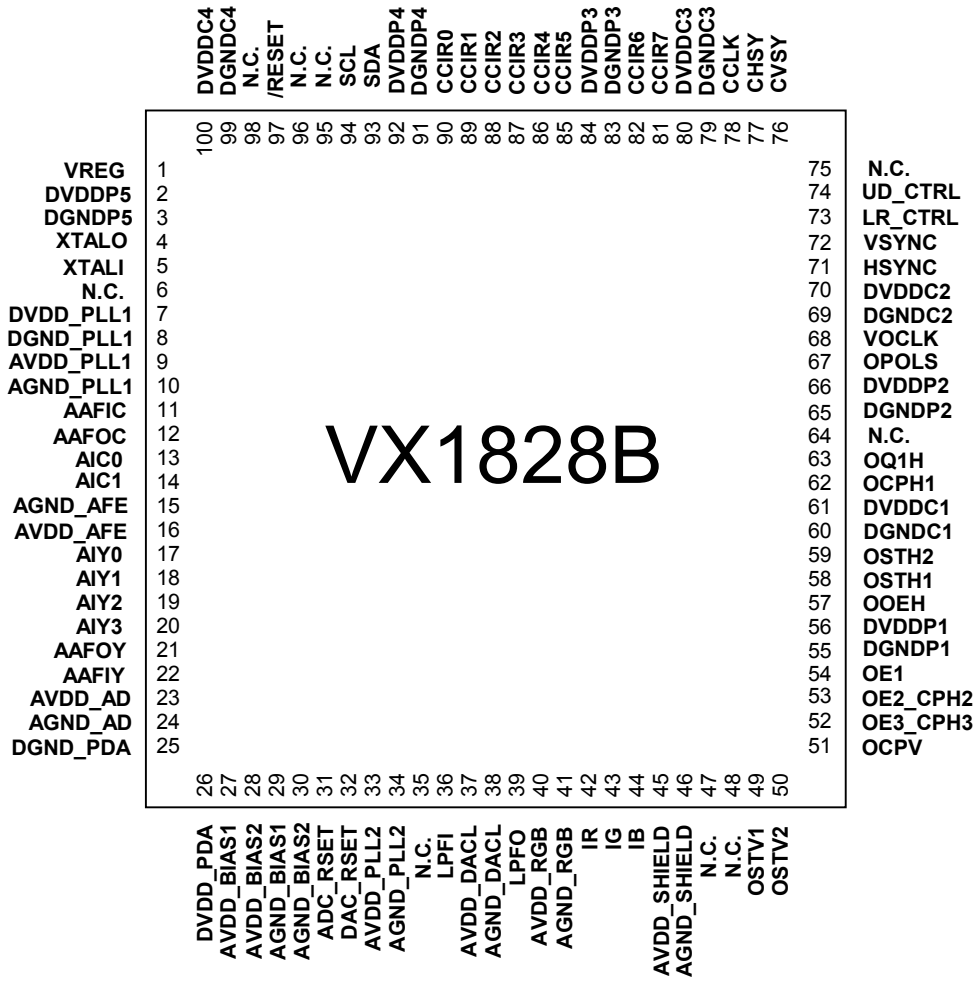
3. APPLICATION



4. PIN CONFIGURATION

4.1 PINOUT DIAGRAM

LQFP100



4.2 PIN ASSIGNMENT

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	VREG	26	DVDD_PDA	51	OCPV	76	CVSY
2	DVDDP5	27	AVDD_BIAS1	52	OE3_CPH3	77	CHSY
3	DGNDP5	28	AVDD_BIAS2	53	OE2_CPH2	78	CCLK
4	XTALO	29	AGND_BIAS1	54	OE1	79	DGNDC3
5	XTALI	30	AGND_BIAS2	55	DGNDP1	80	DVDDC3
6	N.C.	31	ADC_RSET	56	DVDDP1	81	CCIR7
7	DVDD_PLL1	32	DAC_RSET	57	OOEH	82	CCIR6
8	DGND_PLL1	33	AVDD_PLL2	58	OSTH1	83	DGNDP3
9	AVDD_PLL1	34	AGND_PLL2	59	OSTH2	84	DVDDP3
10	AGND_PLL1	35	N.C.	60	DGNDC1	85	CCIR5
11	AAFIC	36	LPFI	61	DVDDC1	86	CCIR4
12	AAFOC	37	AVDD_DACL	62	OCPH1	87	CCIR3
13	AIC0	38	AGND_DACL	63	OQ1H	88	CCIR2
14	AIC1	39	LPFO	64	N.C.	89	CCIR1
15	AGND_AFE	40	AVDD_RGB	65	DGNDP2	90	CCIR0
16	AVDD_AFE	41	AGND_RGB	66	DVDDP2	91	DGNDP4
17	AIY0	42	IR	67	OPOLS	92	DVDDP4
18	AIY1	43	IG	68	VOCLK	93	SDA
19	AIY2	44	IB	69	DGNDC2	94	SCL
20	AIY3	45	AVDD_SHIELD	70	DVDDC2	95	N.C.
21	AAFOY	46	AGND_SHIELD	71	HSYNC	96	N.C.
22	AAFIY	47	N.C.	72	VSYNC	97	/RESET
23	AVDD_AD	48	N.C.	73	LR_CTRL	98	N.C.
24	AGND_AD	49	OSTV1	74	UD_CTRL	99	DGNDC4
25	DGND_PDA	50	OSTV2	75	N.C.	100	DVDDC4

4.3 PIN DESCRIPTION

Video Analog Input Pins (6)

Name	Type	Description	Notes
AIY3	AI	Analog Composite Input	
AIY2	AI	Analog Composite Input	
AIY1	AI	Analog Composite or Luminance Input	
AIY0	AI	Analog Composite or Luminance Input	
AIC1	AI	Analog Chrominance Input	
AIC0	AI	Analog Chrominance Input	

Auxiliary Analog I/O Pins (8)

NAME	Type	Description	Notes
AAFOY	AO	Analog Signal to Optional External Anti-Alias Filter of Y-channel	
AAFOC	AO	Analog Signal to Optional External Anti-Alias Filter of C-channel	
AAFIY	AI	Analog Signal from Optional External Anti-Alias Filter of Y-channel	
AAFIC	AI	Analog Signal from Optional External Anti-Alias Filter of C-channel	
LPFO	AO	Output to DAC Reconstruction Filter	
LPFI	AI	Input from DAC Reconstruction Filter	
ADC_RSET	AI	Connect to an External Resister for Setting the Bias Current of ADC	
DAC_RSET	AI	Connect to an External Resister for Setting the Output Current of DAC	

CCIR Input/Output Pins (11)

NAME	Type	Description	Notes
CCIR0~7	I/O_1	CCIR656 Data Input/Output	
CCLK	I/O_1	CCIR656 Clock Input/Output	
CHSY	I/O_1	CCIR656 HSYNC Input/Output	
CVSY	I/O_1	CCIR656 VSYNC Input/Output	

Video Output Pins (6)

Name	Type	Description	Notes
IR	AO	Analog Video Output Red	Note 1
IG	AO	Analog Video Output Green	Note 1
IB	AO	Analog Video Output Blue	Note 1
HSYNC	I/O_1	Video Output Horizontal Synchronization	Note 2
VSYNC	I/O_1	Video Output Vertical Synchronization	Note 2
VOCLK	I/O_2	Video Output Clock	Note 2

T-CON Pins (14)

Name	Type	Description	Notes
OPOLS	O_1	Polarity Alternating Signal for Video	
OE3_CPH3	O_1	Output Enable Control Signal for Gate Driver / 3rd Source Driver Shift Clock	
OE2_CPH2	O_1	Output Enable Control Signal for Gate Driver / 2nd Source Driver Shift Clock	
OE1	O_1	Output Enable Control Signal for Gate Driver	
OSTV2	I/O_1	Gate Driver Start Pulse	
OSTV1	I/O_1	Gate Driver Start Pulse	
OCPV	O_1	Gate Driver Shift Clock	
OCPH1	O_1	Source Driver Shift Clock	
OSTH1	I/O_1	Source Driver Start Pulse	
OSTH2	I/O_1	Source Driver Start Pulse	
OOEH	O_1	Output Enable Control Signal for Source Driver	
OQ1H	O_1	Analog Signal Rotate Indicator for Delta-aligned RGB Panel	
UD_CTRL	O_1	Output for LCD Panel Up/Down Switch	
LR_CTRL	O_1	Output for LCD Panel Left/Right Switch	

Note 1: Order of IR, IG, and IB could be changed by programmable registers.

Note 2: HSYNC, VSYNC, VOCLK could be selected as PWM output individually.

Miscellaneous I/O Pins (5)

Name	Type	Description	Notes
XTALO	XO	Crystal Output	
XTALI	XI	Crystal Input	
SDA	I/O_1	Host Interface Serial Data / Address	
SCL	I_S	Host Interface Serial Clock	
/RESET	I_S	Chip Reset (Active Low)	

Power Pins (41)

Name	Type	Description	Notes
DVDDC1~4	P_{25}	Digital Supply 2.5V for Core	
DVDDP1~5	P_{25}	Digital Supply 3.3V for I/O	
DVDD_PLL1	P_{33}	Digital Supply 3.3V for PLL1	
DVDD_PDA	P_{33}	Digital Supply 3.3V for PLL2, ADC, and DAC	
AVDD_PLL1	P_{33}	Analog Supply 3.3V for PLL1	
AVDD_AFE	P_{33}	Analog Supply 3.3V for AFE	
AVDD_AD	P_{33}	Analog Supply 3.3V for ADC	
AVDD_BIAS1	P_{33}	Analog Supply 3.3V for BIAS	
AVDD_BIAS2	P_{33}	Analog Supply 3.3V for BIAS	
AVDD_PLL2	P_{33}	Analog Supply 3.3V for PLL2	
AVDD_DACL	P_{33}	Analog Supply 3.3V for PLL2 DAC	
AVDD_RGB	P_{33}	Analog Supply 3.3V for RGB DAC	
AVDD_SHIELD	P_{33}	Analog Supply 3.3V for Shielding	
VREG	P_{25}	Regulator Output 2.5V	
DGNDC1~4	G	Digital Ground for Core	
DGNDP1~5	G	Digital Ground for I/O	
DGND_PLL1	G	Digital Ground for PLL1	
DGND_PDA	G	Digital Ground for PLL2, ADC, and DAC	
AGND_PLL1	G	Analog Ground for PLL1	
AGND_AFE	G	Analog Ground for Analog Front End	
AGND_AD	G	Analog Ground for ADC	
AGND_BIAS1	G	Analog Ground for BIAS	
AGND_BIAS2	G	Analog Ground for BIAS	
AGND_PLL2	G	Analog Ground for PLL2	
AGND_DACL	G	Analog Ground for PLL DAC	
AGND_RGB	G	Analog Ground for RGB DAC	

AGND_SHIELD	G	Analog Ground 3.3V for Shielding	

4.4 PIN-TYPE DEFINITION

TYPE	DEFINITION
I	5V Tolerant Input
I_S	5V Tolerant Schmitt Trigger Input
I_{PU}	5V Tolerant Input with Internal Pull-Up Resistor
I_{PD}	5V Tolerant Input with Internal Pull-Down Resistor
O_1	TTL Output Group 1 (4 mA)
O_{TS1}	Tri-State Output Group 1 (4 mA)
I/O_1	5V Tolerant Input/TTL Output Group 1 (4 mA)
I/O_2	5V Tolerant Input/TTL Output Group 2 (8 mA)
XI, XO	Crystal Pin
AI	Analog Input Pin
AO	Analog Output Pin
P	Power Pin
G	Ground Pin

5. FUNCTION DESCRIPTION

5.1 ANALOG INPUT CONFIGURATION

VX1828B has 6 analog video input pins that can be configured by the register, AISEL as follows.

Table 5.1 Analog Input Configurations

AISEL	Video Source		
	CVBS	S-Video	
		Y	C
0000	AIY<0>		
0001	AIY<1>		
0010	AIY<2>		
0011-0101	*Reserved*		
0110		AIY<0>	AIC<0>
0111		AIY<1>	AIC<1>
1000-1001	*Reserved*		
1010	AIY<3>		
1011-1111	*Reserved*		

5.2 POWER-DOWN OPTION

In CCIR input mode, the VX1828B provides the option to power down the line-lock sampling and demodulation circuits.

5.3 MODE DETECTION

Automatic video mode detection is built in, discriminating between NTSC, PAL-M, PAL-Nc and other PAL formats. Manual override of automatic mode detection is available that is controlled by the ML525 (NTSC and PALM) and MVSTD (NTSC and other PAL) registers.

Table 5.2 Manual Mode Settings

ML525	MVSTD	Mode
0	0	PAL (Combination N)
0	1	PAL (B,D,G,H,I,N)
1	0	PAL (M)
1	1	NTSC

5.4 COLOR-TRANSIENT IMPROVEMENT (CTI)

The color-transient improvement (CTI) engine in VX1828B works adaptively to sharpen the transition of chrominance edges to perform sharp and keen edges for every objects and overall clearer video to the viewers.

5.5 LUMA/CHROMA ADJUSTMENT

Contrast is adjusted by register CONTRAST. This provides a range of gain from zero up to 255/128 - almost 2X. A value of CONTRAST = 128 provides a gain of 1.

Brightness is adjusted by register BRIGHTNESS. This provides an adjustment of +127 to -128 to luma which is clipped if necessary to achieve the required range of 64 to 940.

Hue is adjusted by register HUE. The value of HUE is added as a color phase adjustment.

Saturation is adjusted by register SATURATION. The color components are multiplied by

SATURATION, the result is divided by 128. This provides a range of gain from zero up to 255/128 - almost 2X. A value of SATURATION = 128 provides a gain of 1.

5.6 TWO-DIMENSIONAL SHARPNESS

The VX1828B offers three peaking filters for different frequency response in horizontal sharpness engine. The gain for each filter is adjustable from 0 to 14 dB and individually controlled with registers, PEAK_ADJ1, PEAK_ADJ2, and PEAK_ADJ3 (*Figure 5.1*). The clipping filter is adjustable with the registers PEAK_CLIP_MIN and PEAK_CLIP_MAX.

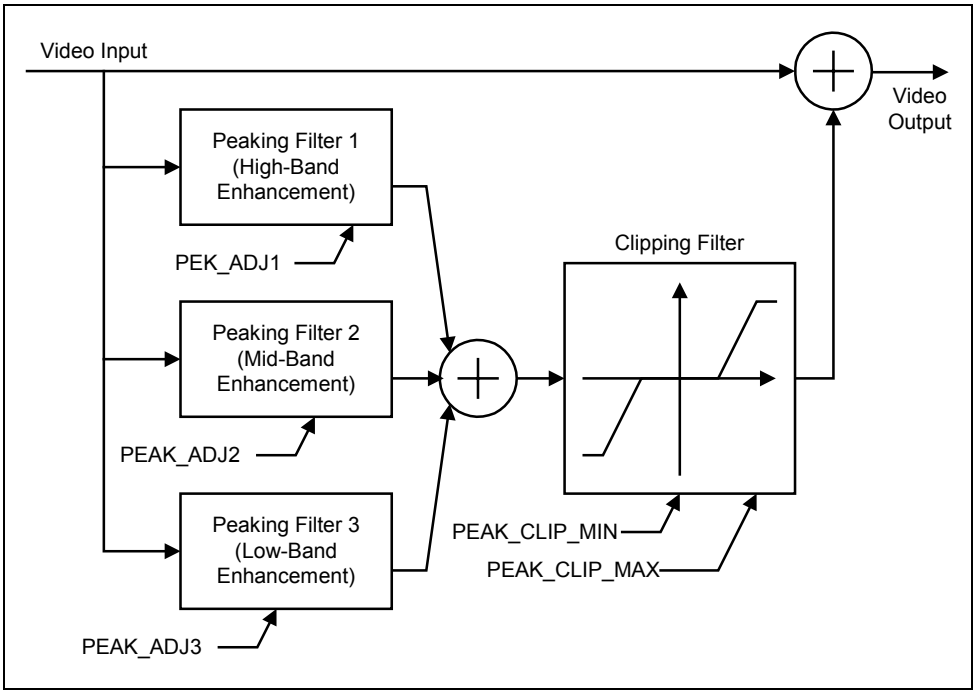


Figure 5.1 VX1828B Horizontal Sharpness Engine

5.7 BLACK-LEVEL EXTENSION (BLE)

Basic idea of black level extension is to enhance the contrast of the luminance in the dark potion of the picture. The advantage of this function is to make the object more solid, apparent, and noticeable to the viewers. The BLE function works adaptively, depending on the average luminance of the picture. The Luminance transform function for BLE is controlled by three parameters, BKXLVL, BKXMAX, and BKXSLP (*Figure 5.2*).

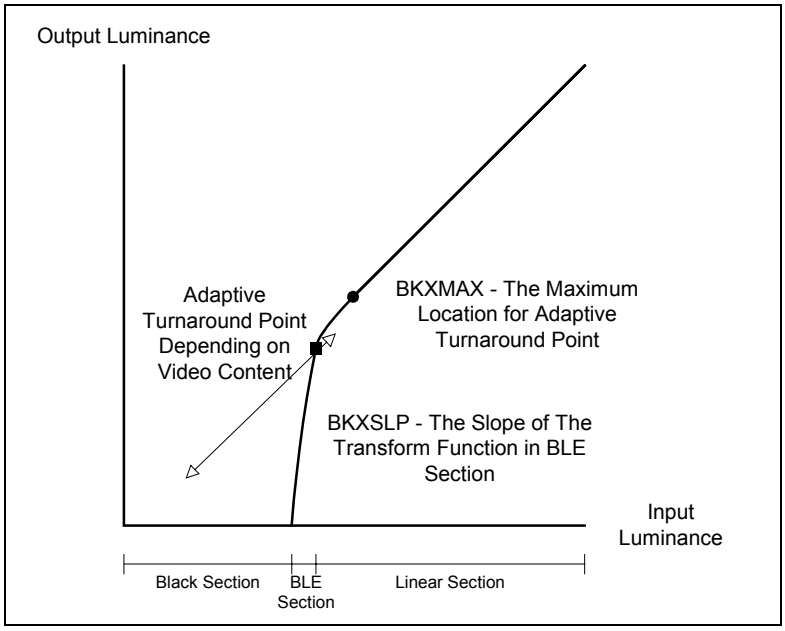
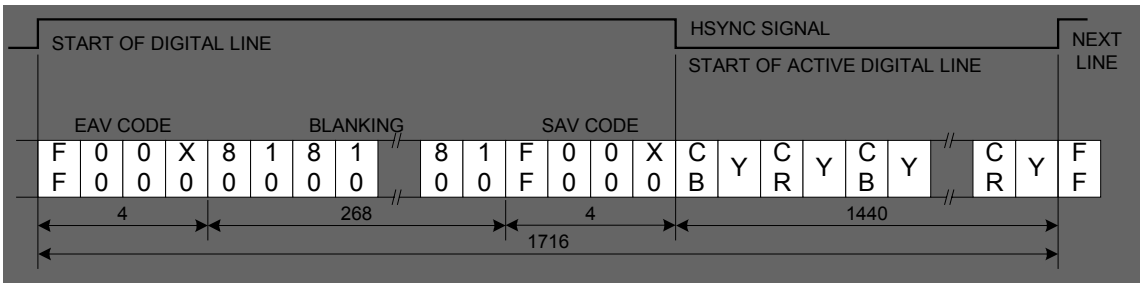


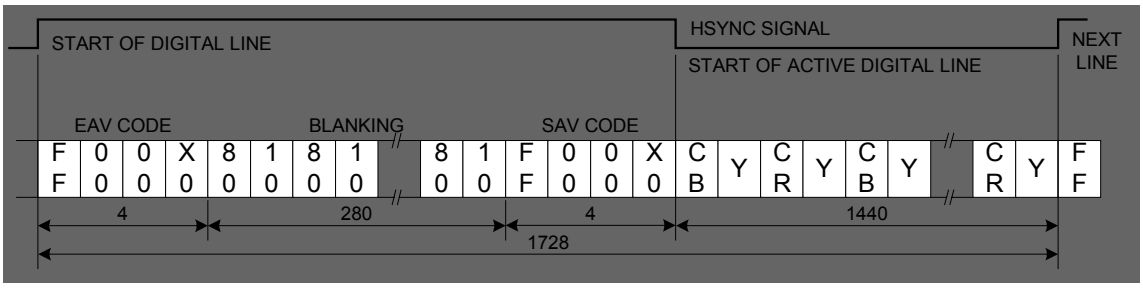
Figure 5.2 BLE Transform Function

5.8 INTERLACE DIGITAL INTERFACE

VX1828B supports either CCIR656 input or output. The CCIR656 data stream includes a 4:2:2 YCbCr data multiplexed into an 8-bit stream: $Cb_0Y_0Cr_0Y_1Cb_2Y_2Cr_2$, etc. Following figures illustrate the format for 525/60 and 625/50 video systems, respectively.



CCIR 656 8-bit parallel interface data format for 525/60 video systems



CCIR 656 8-bit parallel interface data format for 625/50 video systems

The X symbol in EAV and SAV is used to indicate field and H-sync information by the rules as follows:

	Even field		Odd field	
	EAV	SAV	EAV	SAV
X[3:0]	1101	1100	1001	1000

5.9 GAMMA CORRECTION

The VX1828B provides an alternative way to perform video transform effect with an easier approach,

called EZ-Gamma configuration. Built-in the registers, 33 tapes of intermediate points form the approximate curve for basic video transformation process such as Gamma correction, or room-temperature compensation (*Figure 5.3*). Each intermediate point is programmable in the register map, from register CLUTABLE00 to register CLUTABLE32. Shown in the figure, these 33 tapes of points conform to build a piecewise linear curve where the points between the intermediate points are calculated from linear interpolation.

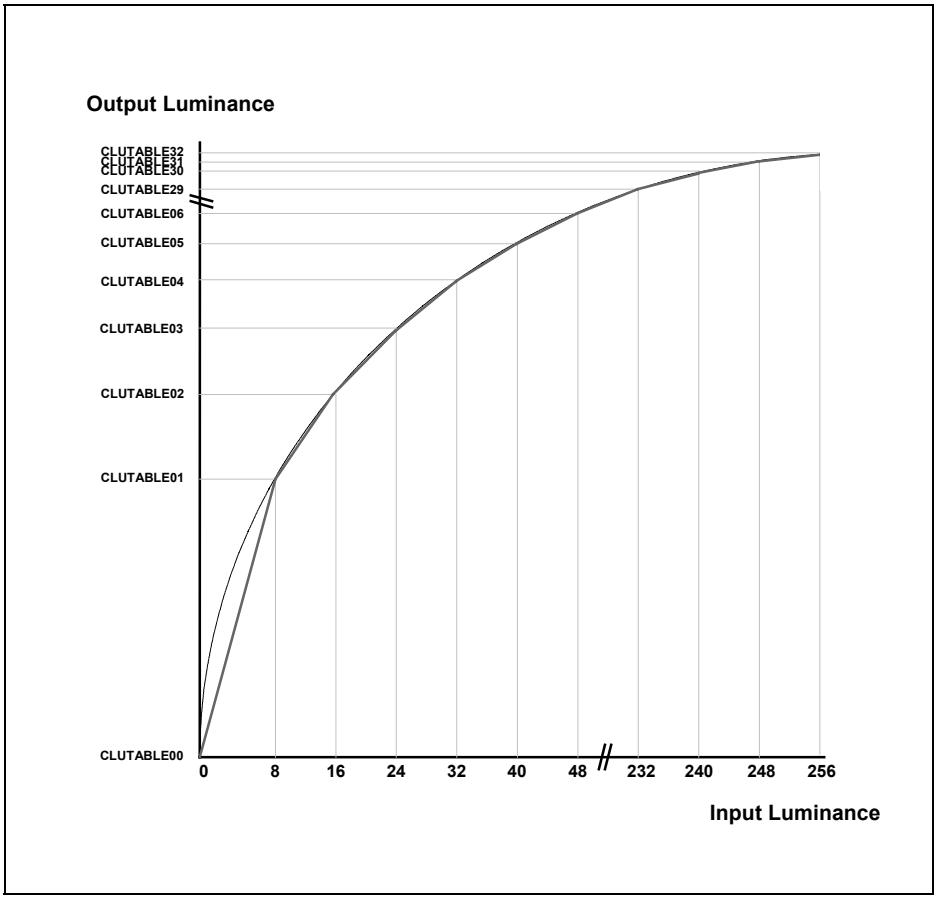


Figure 5.3 EZ-Gamma Transform Curve

For some specific users that the Gamma correction is the most concern, the VX1828B provides an easiest way to program and modify Gamma correction. If the register CLUTABLE_PGR[4] is set to zero, above 33-tape piecewise linear curve is applied. If the register CLUTABLE_PGR[4] is set to one, a set of build-in table with Gamma correction from 0.75 to 1.9 and 3 sets for specific LCD panel correction, and can be selected by the register CLUTABLE_PGR[3:0]. For details refer to *Table 5.3*.

Table 5.3 EZ-Gamma Configurations

CLUTABLE_PGR	Function	CLUTABLE_PGR	Function
00h-0Fh	Using user-programmed table 7Bh – 9Bh	18h (default)	Gamma = 1.4
10h	Gamma = 0.75	19h	Gamma = 1.5
11h	Gamma = 0.8	1Ah	Gamma = 1.6
12h	Gamma = 0.85	1Bh	Gamma = 1.7
13h	Gamma = 0.9	1Ch	Gamma = 1.9
14h	Gamma = 1.0	1Dh	LCD Panel 1
15h	Gamma = 1.1	1Eh	LCD Panel 2
16h	Gamma = 1.2	1Fh	LCD Panel 3
17h	Gamma = 1.3		

5.10 ON-SCREEN-DISPLAY (OSD)

5.10.1 OSD INTRODUCTIONS

The VX1828B integrates VXIS's font-based on-screen display (OSD) unit, which can display a total of up to 256 characters in a single screen, with each font in 16 pixels x 20 pixels format. There are up to 160 build-in fonts stored in the internal Random-Access-Memory (RAM) and Read-Only-Memory (ROM).

5.10.2 OSD DISPLAY BLOCKS

The build-in OSD system divides the screen display into three basic sections, the title, content, and bottom blocks, and the user can customize the size and position for each display block by host commands (*Figure 5.4*).

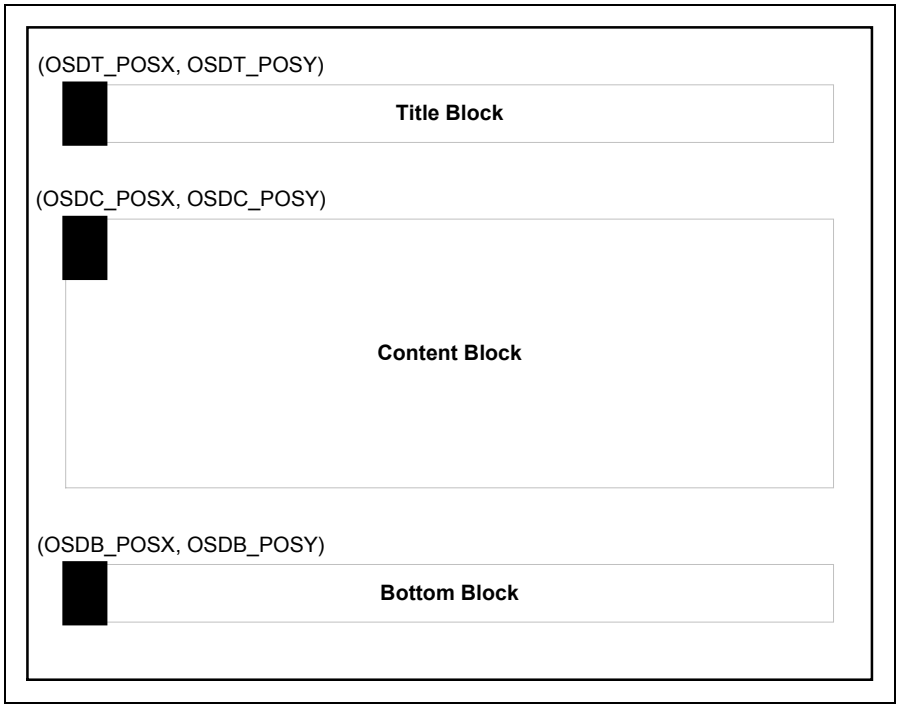


Figure 5.4 OSD Display Blocks

The title and bottom blocks are restricted to display one line of text commonly for header or page notes; and the content block displays multiple lines of text for main OSD information. The sizes and the positions for each individual block are adjustable through registers (*Table 5.4*). Each displaying block cannot be overlapped with others. For details of the register setting, check OSD section in register description chapter.

Table 5.4 Position and Size Registers

Register		Description
OSDT_POSX	OSDT_POSY	Position registers for title block
OSDC_POSX	OSDC_POSY	Position registers for content block
OSDB_POSX	OSDB_POSY	Position registers for bottom block
OSDC_SIZEX	OSDC_SIZEY	Size registers for content block

5.10.3 OSD OPERATIONS

The VX1828's OSD unit is font-based entry. All information that is going to be shown in the screen must be translated into fonts, which is in 16 pixel x 20 pixel resolution each, then put into the screen.

There are two types of OSD memories embedded in VX1828. One is called the “font memory”, which stores all the fonts currently being used on the screen. The font memory stores up to 160 characters, in which 128 characters are hard-wired in the embedded ROM, and the user can program the other 32 characters by the register.

Table 5.5 Font Memory Table

Index (Hex)	00h	01h	02h	03h	04h	05h	06h	07h	08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh
Character	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P
Index (Hex)	10h	11h	12h	13h	14h	15h	16h	17h	18h	19h	1Ah	1Bh	1Ch	1Dh	1Eh	1Fh
Character	Q	R	S	T	U	V	W	X	Y	Z	a	b	c	d	e	f
Index (Hex)	20h	21h	22h	23h	24h	25h	26h	27h	28h	29h	2Ah	2Bh	2Ch	2Dh	2Eh	2Fh
Character	g	h	i	j	k	l	m	n	o	p	q	r	s	t	u	v
Index (Hex)	30h	31h	32h	33h	34h	35h	36h	37h	38h	39h	3Ah	3Bh	3Ch	3Dh	3Eh	3Fh
Character	w	x	y	z												
Index (Hex)	40h	41h	42h	43h	44h	45h	46h	47h	48h	49h	4Ah	4Bh	4Ch	4Dh	4Eh	4Fh
Character	▶	▲	▼	!	,	.	;	:	'	"	#	%	&	@	/	(
Index (Hex)	50h	51h	52h	53h	54h	55h	56h	57h	58h	59h	5Ah	5Bh	5Ch	5Dh	5Eh	5Fh
Character	)	[	]	+	−	÷	<	=	>	?		¢	$	£		○
Index (Hex)	60h	61h	62h	63h	64h	65h	66h	67h	68h	69h	6Ah	6Bh	6Ch	6Dh	6Eh	6Fh
Character	◉	●	0	1	2	3	4	5	6	7	8	9	♪			■
Index (Hex)	70h	71h	72h	73h	74h	75h	76h	77h	78h	79h	7Ah	7Bh	7Ch	7Dh	7Eh	7Fh
Character										^	˅	¯	_	|	|	□
Index (Hex)	A0h	A1h	A2h	A3h	A4h	A5h	A6h	A7h	A8h							
Character	CR	2B	3B	4B	5B	6B	7B	8B	9B							

CR: Character Return / Line Feed

nB: Number of Space Characters

Another type of memory is called the “command memory”, which stores the sequence of the font that is appearing on the screen. The command memory consists of one 256 x 8-bit RAMs, which stores 256 font indexes.

To utilize the various characters stored in the font memory, we need to program the 256 x 8 bits command memory (RAM). The command memory basically stores the indexes of characters to compose the information or paragraphs appearing on the screen. Each index is 8 bits in width so the

command memory is able to store up 256 indexes. In other words, the monitor screen would be able to show at most 256 characters at a time for the OSD display.

The command memory is roughly separated into three blocks for title, content, and bottom block displays. Except the title block is always located at the top of the command memory address, the content and the bottom blocks are located according to the registers, OSDC_START (5Fh.7-0) and OSDB_START (6Dh.7-0). For example (*Figure 5.5*), if we would like to show “VXIS” as the title block, “Hello!” as the content block, and “OK” as the bottom block, the command memory will then be configured as follows.

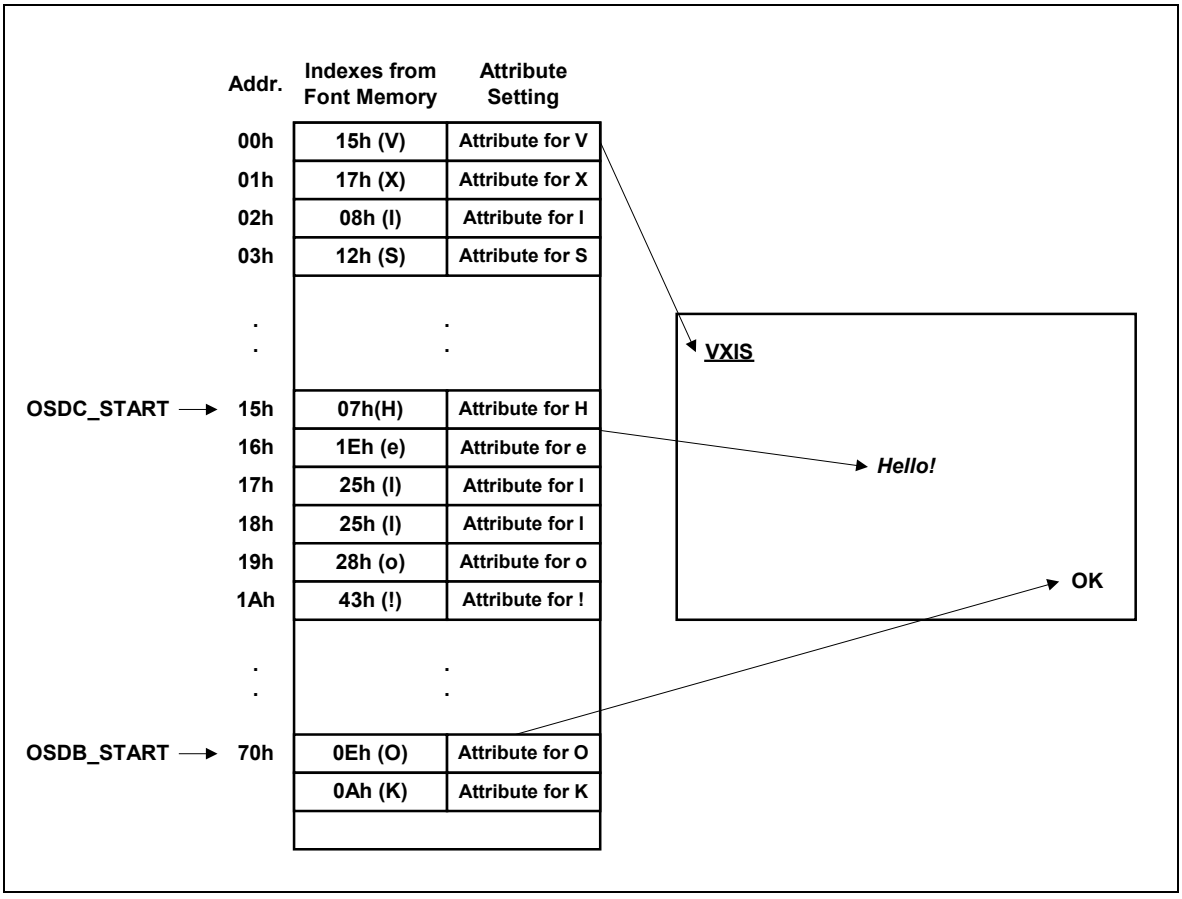


Figure 5.5 OSD Command Memory

5.11 LCD TIMING CONTROLLER (T-CON)

VX1828B contains a universal TCON for various panels of different venders and panel sizes. Parameters can be set to fit customer's specification.

Pin OPOLS, OCPV, OOEH, OE1, OE2, OE3, OSTV1/2 and OCPH can be independently programmed to change polarity.

Pin OPOLS, OE3, OE2, OE1, OSTV2, OSTV1, OCPV, OCPH1, OSTH1, OSTH2, OOEH, UD_CTRL and LR_CTRL can be independently programmed to open-drain output pads. Under open-drain output mode, an external pull-up resistor is required.

5.12 PULSE WIDTH MODULE (PWM)

VX1828B provides two PWM modules with adjustable frequency and duty cycle controlled by 2 16-bit programmable registers, as the following equation.

$$\text{output frequency} : \frac{20MHz}{PWM\_L + PWM\_H + 2}$$

$$\text{output duty cycle} : \frac{PWM\_H}{PWM\_L + PWM\_H}$$

The PWM output signals are multiplexed with other output signals. Please refer to register PWM0(43h) in register description chapter for more detail.

6. REGISTER DESCRIPTION

6.1 REGISTER MAP

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
01	RST1	-	RESET / CLEAR							
02	G1	8A	PWDN_at_CCIR	-			AISEL			
05	G4	D8	-	-	MMODE	ML525	MVSTD	MDEFV	-	
06	AFE0	28	-	AFE_SYNC_EN	VT		VB		CLAMP_MODE	
07	AFE1	CA	STARTUP_EN	PUMP_EN	VCLAMPW		CPW_LVL		CPS_LVL	
09	AFE3	88	VCLAMP_EN	-	VINI		CMPLVL			
0A	AFE4	40	AFE_OFFSET							
0B	AFE5	80	PUPW							
0C	AFE6	40	PDNW							
0E	TG0	06	INV_FLD	FIX_BLVL	DLDC	DCDC	PED	BLVL_SEL		
0F	TG1	AA	HERRORLIM		HACCLIM		VLIMSEL		VSRSEL	
10	TG2	20	-	DVPRES	CLAMPM					
11	TG3	00	SPATH	MAGCY_EN	MAGCY					
12	TG4	15	SPCTH	-	STBASE		SEEDCW		PHADJ	
13	YC0	10	-	-	-	LRFDC				
16	YC3	00	-	-	VSHARPNESS					
17	DM0	79	PGSTEP		BSYN_SEL	DVMASK	CNR	DCKILL	PGSEL	
18	DM1	20	MAGCC_EN	MAGCC						
19	DM2	55	ADJSEL		-	-	PC1		PC2	
1A	DM3	00	-	-	-	-	-	-	-	-
1B	DM4	40	BCAGC							
1C	CCIR0	38	bypass_scaler	ForceBlue	FVSEL	BLUE_EN	TSPD			
1D	PADJ00	00	-							
1E	PADJ01	80	BRIGHTNESS							
1F	PADJ02	80	CONTRAST							
20	PADJ03	80	SATURATION							
21	PADJ04	60	-	-	HUE					
22	PADJ05	10	BKXON	BKXAUTO	YDLY [2:0]		CEN	VNR	UVINV	
23	PADJ06	46	BKXLVL							
24	PADJ07	64	BKXMAX							
25	PADJ08	00	BKXTPIN							
26	PADJ09	FF	BKXSLP							
27 (R)	PADJ0A	-	BKXPCONT							
2A	TC32	25	CPH_MODE[2:0]		RATE1_CNT_N[4:0]					
2B	TC33	24	RATE1_PARAM_A[7:0]							
2C	TC34	00	RATE1_PARAM_A[15:8]							
2D	TC35	00	RATE1_PARAM_A[23:16]							
2E	PEAK1	20	PEAK_EN	PEAK_CLIP_MIN						
2F	PEAK2	00	-	-	PEAK_ADJ1					
30	PEAK3	00	-	-	PEAK_ADJ2					
31	PEAK4	00	-	-	PEAK_ADJ3					
32	RGBFIL	7F	RGB_FIL_EN	PEAK_CLIP_MIX						
33	TC36	00	RATE1_PARAM_A[31:24]							
34	TC37	24	RATE1_PARAM_B[7:0]							
35	TC38	00	RATE1_PARAM_B[15:8]							
36	TC39	00	RATE1_PARAM_B[23:16]							
37	TC40	00	RATE1_PARAM_B[31:24]							
38	TC41	13	CPH_DLY[1:0]		RATE2_CNT_N[4:0]					

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
39	TC42	49	RATE2_PARA_A[7:0]							
3A	OS7	00	AOUT_OFF	VOCLKP	HSYNCP	VSYNCP	VOCLKD2	-	OTRI_CLK	OTRI
3B	OS8	A9	HS_WIDTH					VS_WIDTH		
3C	OS9	94	HSHIFT							
3D	OSA	00	VSHIFT							
3E	OSB	00	BOTTOM_MASK							
3F	OSC	00	TOP_MASK							
40	OSD	00	LEFT_MASK							
41	OSE	00	RIGHT_MASK							
42	OSF	00	PG_SEL			PG_LEVEL				
43	PWM0	00	-		PWM_SEL1		PWM_SEL2		PWM_SEL3	
44	TC43	4A	RATE2_PARAM_A[15:8]							
49	TC44	02	RATE2_PARAM_A[23:16]							
4A	TC45	00	RATE2_PARAM_A[31:24]							
4B	TC46	49	RAET2_PARAM_B[7:0]							
4C	TC47	48	RATE2_PARAM_B[15:8]							
4D	TC48	02	RATE2_PARAM_B[23:16]							
4E	TC49	00	RATE2_PARAM_B[31:24]							
4F	TC50	1F	-	-	-	RATE3_CNT_N[4:0]				
50	OSD0	00	OSD_ADDR							
51	OSD1	00	OSD_DATA							
52	OSD2	E0	OSD_ALPHA				-	OSDT_EN	OSDC_EN	OSDB_EN
53	OSD3	08	-	-	OSD_BLINK					
54	OSD4	04	-	-	OSDT_SIZEX					
55	OSD5	00	-	-	OSDT_HLSTART					
56	OSD6	00	-	-	OSDT_HLSTOP					
57	OSD7	00	-	-	OSDT_BLSTART					
58	OSD8	00	-	-	OSDT_BLSTOP					
59	OSD9	28	OSDT_POSX							
5A	OSD10	10	OSDT_POSY							
5B	OSD11	82	OSDT_BGCLR				OSDT_FGCLR			
5C	OSD12	B4	OSDT_HLBGCLR				OSDT_HLFGCLR			
5D	OSD13	10	-	-	OSDC_SIZEX					
5E	OSD14	08	-	-	-	OSDC_SIZEY				
5F	OSD15	04	OSDC_START							
60	OSD16	40	OSDC_POSX							
61	OSD17	1A	OSDC_POSY							
62	OSD18	00	-	-	-	OSDC_HLY_START				
63	OSD19	00	-	-	-	OSDC_HLY_STOP				
64	OSD20	01	-	-	OSDC_HLX_START					
65	OSD21	00	-	-	OSDC_HLX_STOP					
66	OSD22	00	-	-	-	OSDC_BLY_START				
67	OSD23	00	-	-	-	OSDC_BLY_STOP				
68	OSD24	01	-	-	OSDC_BLX_START					
69	OSD25	00	-	-	OSDC_BLX_STOP					
6A	OSD26	1F	OSDC_BGCLR				OSDC_FGCLR			
6B	OSD27	6a	OSDC_HLBGCLR				OSDC_HLFGCLR			
6C	OSD28	08	-	-	OSDB_SIZEX					
6D	OSD29	84	OSDB_START							
6E	OSD30	88	OSDB_POSX							
6F	OSD31	6C	OSDB_POSY							
70	OSD32	00	-	-	OSDB_HLSTART					
71	OSD33	00	-	-	OSDB_HLSTOP					
72	OSD34	00	-	-	OSDB_BLSTART					
73	OSD35	00	-	-	OSDB_BLSTOP					
74	OSD36	79	OSDB_BGCLR				OSDB_FGCLR			
75	OSD37	3E	OSDB_HLBGCLR				OSDB_HLFGCLR			
76	TC51	55	RATE3_PARAM_A[7:0]							
77	TC52	55	RATE3_PARAM_A[15:8]							
78	TC53	55	RATE3_PARAM_A[23:16]							
79	TC54	55	RATE3_PARAM_A[31:24]							

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
7A	GM00	18	GAMMA_EN	-	-	CLUTABLE_PGR				
7B-9B	GM01-GM21		CLUTABLE00 - CLUTABLE32							
9C	TC55	00	RATE3_PARAM_B[7:0]							
9D	TC56	00	RATE3_PARAM_B[15:8]							
9E	TC57	00	RATE3_PARAM_B[23:16]							
9F	TC58	00	RATE3_PARAM_B[31:24]							
A3	TC22	15	OEH_START							
A4	TC23	23	OEH_END							
A5	TC24	00	-	-	-	-	-	STH_ON[10:8]		
A6	TC25	74	STH_ONT[7:0]							
A7	TC26	00	-	CPH_SEL_A[10:8]			-	CPH_SEL_B[10:8]		
A8	TC27	00	CPH_SEL_A[7:0]							
A9	TC28	00	CPH_SEL_B[7:0]							
AA	TC29	70	-	CPH_SEL_C[10:8]			-	CPHSEL_D[10:8]		
AB	TC30	FF	CPH_SEL_C[7:0]							
AC	TC31	00	CPH_SEL_D[7:0]							
AD	TC9	6D	OEV_START							
AE	TC10	14	OEV_END							
AF	TC11	14	OEV_MASK_START							
B0	OSB0	00	-	-	-	-	-	-	-	INV_FRP
B1	OSB1	80	R_BIAS							
B2	OSB2	80	G_BIAS							
B3	OSB3	80	B_BIAS							
B4	OSB4	80	R_RATIO							
B5	OSB5	80	G_RATIO							
B6	OSB6	80	B_RATIO							
B7	OSB7	00	R_BIAS_N							
B8	OSB8	00	G_BIAS_N							
B9	OSB9	00	B_BIAS_N							
BA	OSBA	80	R_RATIO_N							
BB	OSBB	80	G_RATIO_N							
BC	OSBC	80	B_RATIO_N							
BD	OSBD	00	RGB_SEL			GAIN_R				
BE	OSBE	00	-			GAIN_G				
BF	OSBF	00	o_output_upsample	-		GAIN_B				
C0	TC0	0E	OEV_SWAP	CPH_OEV_SEL	Q1H_INV	-	OEH_SEL	LNR	UND	POLS_INV
C1	TC1	38	-	-	-			-		
C2	TC6	18	-	STV_ON						
C3	TC21	0A	POL_INV_ON							
C4	TC2	00	CPV_P	OEH_P	OE1_P	OE2_P	OE3_P	STV_P	CPH_P	-
C5	TC3	00	POLS_T	-	OE3_T	OE2_T	OE1_T	STV2_T	STV1_T	CPV_T
C6	TC4	00	UD_CTRL	UD_CTRL_T	LR_CTRL	LR_CTRL_T	CPH1_T	STH1_T	STH2_T	OEH_T
C7	TC5	00	OEV_MODE[3:0]				-	-	ZOOM_MODE[1:0]	
C8	TC12	0A	CPV1_RISE							
C9	TC13	2E	CPV1_FALL							
CA	TC14	43	CPV2_RISE							
CB	TC15	5E	CPV2_FALL							
CC	TC7	0D	STV_START							
CD	TC8	5D	STV_END							
CE			-							
CF	TC16		OEV_MASK_LSB[3:0]				-	-	-	OEV_MASK_SEL
D0	Status	-	-	-	AGC_STATUS					
D1	Status	-	DAGC_STATUS							
D2	Status	-	BLKLEV_STATUS							
D3	Status	-	NOISE MORE	PHALT	IS443	VPRES	MODE [1:0]		FINEAGC	MVVALID
D4	Status	-	CAGC_STATUS							
D5	Status	-	CCPRES	CC525	-	-	-	-	-	LLOCK
D6	TC17	0D	-				DROP_PER_N			

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
D7	TC18	5D	V_DROP_L1				V_DROP_I2			
D8	TC19	28	V_DROP_L3				V_DROP_L4			
D9	TC20	66	DOUBLE_PER_N				V_DOUBLE_L			
DC	OSD38	00	-				-	-	CW_FONT_ADDR[9:8]	
DD	OSD39	00	OSD_FONT_ADDR[7:0]							
DE	OSD40	00	OSD_FONT_DATA[15:8]							
DF	OSD41	00	OSD_FONT_DATA[7:0]							
E0	PWM1	FF	PWM1_L0							
E1	PWM2	FF	PWM1_L1							
E2	PWM3	FF	PWM1_H0							
E3	PWM4	FF	PWM1_H1							
E4	PWM5	FF	PWM2_L0							
E5	PWM6	FF	PWM2_L1							
E6	PWM7	FF	PWM2_H0							
E7	PWM8	FF	PWM2_H1							
E8	CCIR1	08	-	-	-	ccir_out_en	CCLFC1		CCLFC2	
EA	CCIR2	40	ccir_in_en	autontpa	setntpa	infmt	insigsel		hsyncip	vsyncfldp
EB	CCIR3	00	-						hsync_dly	
EC	CCIR4	77	ccin_dly				ccout_dly			
ED	TG5	00	BLVL_STEP			MBLKADJ	-			
EE	TG6	00	M_BLVL							
FD	CW0	00	-	CW_DEST [2:0]			-	-	CW_INIT_ADDR [9:8]	
FE	CW1	00	CW_INIT_ADDR [7:0]							
FF	CW2	00	CW_DATA							

6.2 REGISTER DETAILS

6.2.1 GLOBAL REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
01 (W)	RST1	-	RESET / CLEAR							
02	G1	8A	PWDN_at_CCIR	-			AISEL			
05	G4	D8	-	-	MMODE	ML525	MVSTD	MDEFV	-	

RESET Software reset all circuits by writing 5Ah

CLEAR Software reset all circuits other than registers by writing A5h

PWDN_at_CCIR Power down decoder circuit at CCIR input mode

AISEL Analog video input selection (df. = 1010)

AISEL	Video Source		
	CVBS	S-Video	
		Y	C
0000	AIY<0>		
0001	AIY<1>		
0010	AIY<2>		
0011-0101	*Reserved*		
0110		AIY<0>	AIC<0>
0111		AIY<1>	AIC<1>
1000-1001	*Reserved*		
1010	AIY<3>		
1011-1111	*Reserved*		

MMODE Manual mode on

In manual mode, input video mode is manually set through registers ML525 and MVSTD.

ML525 / MVSTD Manual mode settings, see Table 4.2.1.2 for details

Table 6.2.1.2 Manual Mode Settings

ML525	MVSTD	Mode
0	0	PAL (Combination N)
0	1	PAL (B,D,G,H,I,N)
1	0	PAL (M)
1	1	NTSC

MDEFV	0	Startup mode selection control for NTSC region
	1	Startup mode selection control for PAL region

6.2.2 ANALOG-FRONT-END REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
06	AFE0	28	-	AFE_SYNC_EN	VT		VB		CLAMP_MODE	
07	AFE1	CA	STARTUP_EN	PUMP_EN	VCLAMPW		CPW_LVL		CPS_LVL	
09	AFE3	88	VCLAMP_EN	-	VINI		CMPLVL			
0A	AFE4	40	AFE_OFFSET							
0B	AFE5	80	PUPW							
0C	AFE6	40	PDNW							

AFE_SYNC_EN

0 Analog synchronization reference OFF (df.)

1 Analog synchronization reference ON

[VT,VB] Combined together to provide 16 level of sync tip detection. Normally distributed between 0 ~ 1.5V

CLAMP_MODE

00 Search-&-lock clamp mode

The sync tip level of active Y-channel is determined by the AFE_OFFSET. Clamping of Y-channel is set by charge pump; clamping of C-channel is set by voltage driver. The unused channel is fixed at voltage level specified by VINI[1:0]. (df.)

10 Enhanced clamp mode

The sync tip level of active Y-channel is clamped at the internal fixed value, which reduces the acquisition time introduced by AFE_OFFSET. The active C-channel is clamped by voltage driver. The unused channel is fixed at voltage level specified by VINI[1:0].

11 Steady clamp mode

The sync tip level of all channels, active or unused, are clamped at the internal fixed value, except the active C-channel is clamped by voltage driver.

STARTUP_EN START-UP charge-pump control enable (df. = ON)

PUMP_EN Charge-pump control enable (df. = ON)

VCLAMPW Voltage clamp circuit activation control

0 20 active cycles (df.)

1 40 active cycles

2 60 active cycles

3 80 active cycles

CPW_LVL Strength adjustment of weak charge pump. It is used for fine

	clamp in normal condition. 0 Pumping strength is 1 Iw 1 Pumping strength is 2 Iw 2 Pumping strength is 4 Iw (df.) 3 Pumping strength is 8 Iw
CPS_LVL	Strength adjustment of strong charge pump. It is used when starting up. 0 Pumping strength is 8 Iw 1 Pumping strength is 16 Iw 2 Pumping strength is 32 Iw (df.) 3 Pumping strength is 64 Iw
VCLAMP_EN	Voltage-clamping enable
VINI	Specify the initial voltage level of unselected channels 0 1/2 VDD (df.) 1 1/3 VDD 2 1/6 VDD 3 VSS
CMPLVL	Threshold level selection of comparator before PLL input terminal Level = 0.430+0.0478 * CMPLVL (df. = 8h)
AFE_OFFSET	Offset level of AFE. (df. = 40h)
PUPW	Width of pull-up pulse in charge-pump circuit. (df. = 80h)
PDNW	Width of pull-down pulse in charge-pump circuit. (df. = 40h)

6.2.4 VIDEO TIMING GENERATION REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
0E	TG0	06	INV_FLD	FIX_BLVL	DLDC	DCDC	PED	BLVL_SEL		
0F	TG1	AA	HERRORLIM		HACCLIM		VLIMSEL		VSRSEL	
10	TG2	20	-	DVPRES	CLAMPM					
11	TG3	00	SPATH	MAGCY_EN	MAGCY					
12	TG4	15	SPCTH	-	STBASE		SEEDCW		PHADJ	
ED	TG5	00	BLVL_STEP			MBLKADJ	-			
EE	TG6	00	M_BLVL							

INV_FLD Internal field indicator polarity inversion (df. = OFF)

FIX_BLVL Fix the value of blank level while removing the sync tip

0 Automatic detected level (df.)

1 Blank level specified by M_BLVL

DLDC Disable luma digital clamp (df. = Enable)

DCDC Disable chroma digital clamp (df. = Enable)

PED

0 If NTSC-J or PAL, black NOT including a pedestal (df.)

1 If NTSC or PAL(M), black including a pedestal.

BLVL_SEL The lowest blank level in LAGC.

0 224/236

1 208/220

2 192/204

3 176/188

4 160/172

5 144/156

6 128/140 (df.)

7 112/124

HERRORLIM Error limit of horizontal Synchronization loop filter input

0 -3 ~ +3

1 -7 ~ +7

2 -15 ~ +15 (df.)

3 -63 ~ +63

HACCLIM Accumulator limit of horizontal synchronization loop filter

0 -16 ~ +16

1 -32 ~ +32

2 -64 ~ +64 (df.)

3 -128 ~ +128

VLIMSEL Line number adjustment limit for vertical synchronization

	0 -8 ~ +8
	1 -24 ~ +24
	2 -40 ~ +40 (df.)
	3 -56 ~ +56
VSRSEL	Line number adjustment slew rate for vertical synchronization
	0 -3 ~ +3
	1 –7 ~ +7
	2 -15 ~ +15 (df.)
	3 -31 ~ +31
DVPRES	Disable VPRES
CLAMPM	Clamping start position control with respect to HSYNC (df. = 32).
SPATH	Spike amplitude threshold for video noise estimation
	0 6 (df.)
	1 16
MAGCY_EN	Enable manual setting AGC of luma channel (df. = OFF)
MAGCY	Value of manual setting AGC of luma channel
SPCTH	Spike count threshold for video noise estimation
	0 32 (df.)
	1 48
STBASE	STBASE is seed generation loop filter gain
	00 1/512
	01 1/1024 (df.)
	01 1/2048
	11 1/4096
SEEDCW	1st order loop filter coefficient for line-lock seed generation
	0 4096
	1 8192 (df)
	2 16384
	3 32768
PHADJ	2nd order loop filter coefficient for line-lock seed generation
	1. 128
	2. 256 (df)
	3. 512
	4. 1024
MBLKADJ	Blank level tracking step selection
	0 Auto adjust (df.)
	1 Manual selection

BLVL_STEP	Blank level tracking step in manual selection mode
M_BLVL	Specify black level when FIX_BLVL=1.

6.2.5 YC SEPARATION REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
13	YC0	10	-	-	-	LRFDC				
16	YC3	00	-	-	VSHARPNESS					

LRFDC Left and right pixel fading control

VSHARPNESS Vertical sharpness enhancement (Only available under composite video input). Minimum value is 00h; maximum value is 3Fh.

6.2.6 DEMODULATION REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
17	DM0	79	PGSTEP		BSYN_SEL	DVMASK	CNR	DCKILL	PGSEL	
18	DM1	20	MAGCC_EN	MAGCC						
19	DM2	55	ADJSEL		-	-	PC1		PC2	
1A	DM3	00	-	-	-	-	-	-	-	-
1B	DM4	40	BCAGC							

PGSTEP Select seed coarse generation step for chroma synchronization

0 Step = 1

1 Step = 2 (df.)

2 Step = 4

3 Step = 8

BSYN_SEL Chroma synchronization method selection

0 Burst locking strategy

1 Line length locking strategy (df.)

DVMASK Video mask during vertical blanking period enable (df. = Enable)

CNR Color noise reduction enable. If set, successive lines of Cr/Cb are averaged. For PAL, cancels alternating component of Hanover Bars (df. = Enable)

DCKILL Disable CKILL

0 Automatic Color Kill function (df.)

1 Disable the CKILL function

PGSEL Gain selection for burst synchronization

0 x0.5

1 x1.0 (df.)

2 x2.0

3 x4.0

MAGCC_EN Enable manual setting AGC of chroma channel (df. = OFF)

MAGCC Value of manual setting AGC of chroma channel

ADJSEL Adjustment gain selection for chroma synchronization

0 x8

1 x4 (df.)

2 x2

3 x1

PC1 1st order loop filter coefficient for chroma synchronization

0 256

	1 512 (df.)
	2 1024
	3 2048
PC2	2nd order loop filter coefficient for chroma synchronization
	0 1
	1 2 (df.)
	2 4
	3 8
BCAGC	Burst error gain for burst error estimation

6.2.7 CCIR REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
1C	CCIR0	38	bypass_ scaler	ForceBlue	FVSEL	BLUE_EN	TSPD			
E8	CCIR1	08				ccir_out_en	CCLFC1		CCLFC2	
EA	CCIR2	40	ccir_in_en	autontpa	setntpa	infmt	insigsel		hsyncip	vsyncfldp
EB	CCIR3	00							hsync_dly	
EC	CCIR4	77	ccin_dly				ccout_dly			

bypass_scaler Turn off scaling function of cc_scale_pre (df. = Disable)

ForceBlue Force the display change to blue screen (df. = Disable)

FVSEL VSYNC type selection

0 Not equal length VSYNC for even and odd field

1 Equal length VSYNC (df.)

BLUE_EN Blue screen control enable (df. = Enable)

TSPD Transition speed of blue screen, see Table 6.2.7.1 for details

Table 6.2.7.1 Transition Speed of Blue Screen

TSPD	Transition Criteria
0	Immediately change to blue when VPRES = 0
1	Wait 8 field to change to blue after VPRES = 0
2	Wait 16 field to change to blue after VPRES = 0
3	Wait 24 field to change to blue after VPRES = 0
4	Wait 32 field to change to blue after VPRES = 0
5	Wait 40 field to change to blue after VPRES = 0
6	Wait 48 field to change to blue after VPRES = 0
7	Wait 56 field to change to blue after VPRES = 0
8	Wait 64 field to change to blue after VPRES = 0
9	Wait 72 field to change to blue after VPRES = 0
10	Wait 80 field to change to blue after VPRES = 0
11	Wait 88 field to change to blue after VPRES = 0
12	Wait 96 field to change to blue after VPRES = 0
13	Wait 104 field to change to blue after VPRES = 0
14	Wait 112 field to change to blue after VPRES = 0
15	Never change to blue when VPRES = 0

ccir_out_en

0 Disable CCIR656 interface output (df.)

1 CCIR656 interface output enable

CCLFC1 Loop Filter C1

0 x4096

1 x2048

2 x1024 (df.)

3 x8192

CCLFC2	Loop Filter C2
	0 x1 (df.)
	1 x4
	2 x16
	3 x64
ccir_in_en	0 Set CVBS or S-video interface as video source (df.)
	1 Set CCIR656 interface as video source
autontpa	0 Manual define CCIR656 as 525-line or 625-line
	1 Auto detect CCIR656 as 525-line or 625-line (df.)
setntpa	0 Manual define set CCIR656 as 525-line standard (df.)
	1 Manual define set CCIR656 as 625-line standard
infmt	0 8-bit CCIR656 with embedded HSYNC/VSYNC (df.)
	1 8-bit CCIR656 with external HSYNC/VSYNC
insigsel	Video input synchronization format
	0 Equaled VSYNC (262.5 HSYNC per VSYNC) (df.)
	1 Non-equaled VSYNC (262/263 HSYNC per VSYNC)
	2 Equaled FIELD (262.5 HSYNC per FIELD)
	3 Non-equaled FIELD (262/263 HSYNC per FIELD)
hsyncip	0 hsync polarity unchanged (df.)
	1 inverse hsync polarity
vsyncfldp	0 Input vsync/field polarity unchanged (df.)
	1 inverse vsync/field polarity
hsync_dly	CCIR656 interface output hsync delay
	0. 0 cycle (df.)
	1. 1 cycle
	2. 2 cycle
	3. 3 cycle
ccin_dly	Internal clock CC_CLK phase delay from CCLK/FSC4
ccout_dly	CCIR656 output clock CCLK phase delay from CK27

Table 6.2.7.2 CC_CLK and CCLK Clock Phase Delay

ccin_dly	Phase delay	ccout_dly	Phase Delay
0	-8.4 ns	0	-8.4 ns
1	-7.2 ns	1	-7.2 ns
2	-6.0 ns	2	-6.0 ns
3	-4.8 ns	3	-4.8 ns
4	-3.6 ns	4	-3.6 ns
5	-2.4 ns	5	-2.4 ns
6	-1.2 ns	6	-1.2 ns
7	0 (df.)	7	0 (df.)

8	1.2 ns	8	1.2 ns
9	2.4 ns	9	2.4 ns
10	3.6 ns	10	3.6 ns
11	4.8 ns	11	4.8 ns
12	6.0 ns	12	6.0 ns
13	7.2 ns	13	7.2 ns
14	8.4 ns	14	8.4 ns
15	9.6 ns	15	9.6 ns

6.2.8 PICTURE ADJUSTMENT REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
1D	PADJ00	00	-							
1E	PADJ01	80	BRIGHTNESS							
1F	PADJ02	80	CONTRAST							
20	PADJ03	80	SATURATION							
21	PADJ04	60	-	-	HUE					
22	PADJ05	18	BKXON	BKXAUTO	YDLY [2:0]			CEN	VNR	UVINV
23	PADJ06	46	BKXLVL							
24	PADJ07	64	BKXMAX							
25	PADJ08	00	BKXTPIN							
26	PADJ09	FF	BKXSLP							
27 (R)	PADJ0A	-	BKXPCONT							

BRIGHTNESS Brightness adjustment

CONTRAST Contrast adjustment

SATURATION Saturation adjustment

HUE Hue adjustment

YDLY Y channel delay control

CEN Color transient improvement (CTI) enable

0 CTI enable (df.)

1 CTI disable

VNR Video noise reduction (VNR) enable

UVINV UV inversion

BKXON Black-level extension (BLE) enable

BKXAUTO

0 Manually setting black-level extension

1 Automatically setting black-level extension

BKXLVL Black-level threshold. Luminance below the value is considered as black.

BKXMAX The maximum location of adaptive turnaround point

BKXTPIN Parameter for manually setting black-level extension

BKXSLP The slope of the transform function in BLE section

BKXPCONT Readout parameter for manually setting black-level extension

6.2.9 PEAKING AND RGB-FILTER REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
2E	PEAK1	20	PEAK_EN	PEAK_CLIP_MIN						
2F	PEAK2	00	-	-	PEAK_ADJ1					
30	PEAK3	00	-	-	PEAK_ADJ2					
31	PEAK4	00	-	-	PEAK_ADJ3					
32	RGBFIL	7F	RGB_ FIL_EN	PEAK_CLIP_MIX						

PEAK_EN Horizontal sharpening enable

PEAK_CLIP_MIN Clipping filter parameter

PEAK_ADJ1 Weighting of horizontal video sharpening in high-frequency

PEAK_ADJ2 Weighting of horizontal video sharpening in mid-frequency

PEAK_ADJ3 Weighting of horizontal video sharpening in low-frequency

PEAK_CLIP_MAX Clipping filter parameter

RGB_FIL_EN Low pass filter enable. It gets rid of 13.5 MHz noise frequency. (df. = Disable)

6.2.10 OUTPUT FORMAT REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
3A	OS7	00	AOUT_OFF	VOCLKP	HSYNCP	VSYNCP	VOCLKD2	-	OTRI_CLK	OTRI
3B	OS8	A9	HS_WIDTH					VS_WIDTH		
3C	OS9	94	HSHIFT							
3D	OSA	00	VSHIFT							
3E	OSB	00	BOTTOM_MASK							
3F	OSC	00	TOP_MASK							
40	OSD	00	LEFT_MASK							
41	OSE	00	RIGHT_MASK							
42	OSF	00	PG_SEL			PG_LEVEL				

AOUT_OFF Analog video output disable

VOCLKP Change the polarity of AVCLK (TCON clock)

HSYNCP Pin HSYNC polarity

VSYNCP Pin VSYNC polarity

VOCLKD2 0 VOCLK's frequency equals 1x output data rate (df.)

1 VOCLK's frequency equals 0.5x output data rate

OTRI_CLK VOCLK high impedance enable

OTRI Video/Hsync/Vsync outputs high impedance enable

HS_WIDTH Width of video output horizontal synchronization

Actual synchronization-width = 13 + (HS_WIDTH x 4) in pixels

VS_WIDTH Width of video output vertical synchronization

Actual synchronization-width = 1 + VS_WIDTH in lines

HSHIFT Video output horizontal shifting

VSHIFT Video output vertical shifting

BOTTOM_MASK Number of lines masked from the bottom of a frame

TOP_MASK Number of lines masked from the top of a frame

LEFT_MASK Number of pixels masked from the left-hand-side of a frame

RIGHT_MASK Number of pixels masked from the right-hand-side of a frame

PG_SEL Embedded pattern type selection

PG_LEVEL Gray level of embedded pattern (= ho to h1F, 32 steps)

Table 6.2.10.1 Embedded pattern selection

PG_SEL	Pattern Type	Gray level
000	None	-
001	Red field	32
010	Green field	32
011	Blue field	32
100	White field	32
101	Black field	32
110	DAC Min. Output	-
111	DAC Max. Output	-

6.2.11 OSD REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
50	OSD0	00	OSD_ADDR							
51	OSD1	00	OSD_DATA							

OSD_ADDR OSD command memory address

OSD_DATA OSD command memory data

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
52	OSD2	E0	OSD_ALPHA				-	OSDT_EN	OSDC_EN	OSDB_EN

OSD_ALPHA OSD alpha-blending. See following equation.

$$\text{OSD Displaying Color} = \frac{\text{Video Color} \times \text{OSD\_ALPHA} + \text{OSD Color} \times (16 - \text{OSD\_ALPHA})}{16}$$

OSDT_EN OSD title block display enable

OSDC_EN OSD content block display enable

OSDB_EN OSD bar block display enable

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
53	OSD3	08	-	-	OSD_BLINK					

OSD_BLANK OSD blinking rate

$$\text{OSD Blinking Rate} = \frac{30}{\text{OSD\_BLINK} \times 4}\ \text{Hz}$$

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
54	OSD4	04	-	-	OSDT_SIZEX					
55	OSD5	00	-	-	OSDT_HLSTART					
56	OSD6	00	-	-	OSDT_HLSTOP					
57	OSD7	00	-	-	OSDT_BLSTART					
58	OSD8	00	-	-	OSDT_BLSTOP					
59	OSD9	28	OSDT_POSX							
5A	OSD10	10	OSDT_POSY							

OSDT_SIZEX OSD title block horizontal length in character. Valid settings are 01h – 26h for small fonts; 01h – 13h for large fonts.

OSDT_HLSTART OSD title block highlight start position

OSDT_HLSTOP OSD title block highlight stop position

OSDT_BLSTART OSD title block blink start position

OSDT_BLSTOP OSD title block blink stop position

OSDT_POSX OSD title block horizontal initial position. Incrementing by 1 reflects 1 pixels shifting rightwards. Minimum value is 03h.

OSDT_POSY OSD title block vertical initial position. Incrementing by 1 reflects 1 lines shifting downwards. Minimum value is 01h.

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
5B	OSD11	82	OSDT_BGCLR				OSDT_FGCLR			
5C	OSD12	B4	OSDT_HLBGCLR				OSDT_HLFGCLR			

OSDT_BGCLR OSD title block background color selection, see Table 6.2.11.1 for details

Table 6.2.11.1 OSD Color Assignment

Color Bits	Color	Color Bits	Color
0000	Black	1000	Transparent
0001	Blue	1001	Royal Blue
0010	Green	1010	Medium Aquamarine
0011	Aqua	1011	Light Green
0100	Red	1100	Orange
0101	Fuchsia	1101	Hot Pink
0110	Yellow	1110	Silver
0111	White	1111	Gray

OSDT_FGCLR OSD title block foreground color selection, see Table 6.2.11.1 for details

OSDT_HLBGCLR OSD title block high-lighted background color selection, see Table 6.2.11.1 for details

OSDT_HLFGCLR OSD title block high-lighted foreground color selection, see Table 6.2.11.1 for details

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
5D	OSD13	10	-	-	OSDC_SIZEX					
5E	OSD14	08	-	-	-	OSDC_SIZEY				
5F	OSD15	04	OSDC_START							
60	OSD16	40	OSDC_POSX							
61	OSD17	1A	OSDC_POSY							
62	OSD18	00	-	-	-	OSDC_HLY_START				
63	OSD19	00	-	-	-	OSDC_HLY_STOP				
64	OSD20	01	-	-	OSDC_HLX_START					

65	OSD21	00	-	-	OSDC_HLX_STOP	
66	OSD22	00	-	-	-	OSDC_BLY_START
67	OSD23	00	-	-	-	OSDC_BLY_STOP
68	OSD24	01	-	-	OSDC_BLX_START	
69	OSD25	00	-	-	OSDC_BLX_STOP	

OSDC_SIZEX OSD content block horizontal length in character

OSDC_SIZEY OSD content block vertical length in character. Valid settings are 01h – 15h for small fonts; 01h – 0Ah for large fonts.

OSDC_START OSD content block start address in OSD command memory

OSDC_POSX OSD content block horizontal initial position. Incrementing by 1 reflects 1 pixels shifting rightwards. Minimum value is 03h.

OSDC_POSY OSD content block vertical initial position. Incrementing by 1 reflects 1 lines shifting downwards. Minimum value is 01h.

OSDC_HLY_START OSD content block highlight vertical start position

OSDC_HLY_STOP OSD content block highlight vertical stop position

OSDC_HLX_START OSD content block highlight horizontal start position

OSDC_HLX_STOP OSD content block highlight horizontal stop position

OSDC_BLY_START OSD content block blink vertical start position

OSDC_BLY_STOP OSD content block blink vertical stop position

OSDC_BLX_START OSD content block blink horizontal start position

OSDC_BLX_STOP OSD content block blink horizontal stop position

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
6A	OSD26	1F	OSDC_BGCLR				OSDC_FGCLR			
6B	OSD27	6a	OSDC_HLBGCLR				OSDC_HLFGCLR			

OSDC_BGCLR OSD content block background color selection, see Table 6.2.11.1 for details

OSDC_FGCLR OSD content block foreground color selection, see Table 6.2.11.1 for details

OSDC_HLBGCLR OSD content block high-lighted background color selection, see Table 6.2.11.1 for details

OSDC_HLFGCLR OSD content block high-lighted foreground color selection, see Table 6.2.11.1 for details

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
6C	OSD28	08	-	-	OSDB_SIZEX					
6D	OSD29	84	OSDB_START							
6E	OSD30	88	OSDB_POSX							

6F	OSD31	6C	OSDB_POSY		
70	OSD32	00	-	-	OSDB_HLSTART
71	OSD33	00	-	-	OSDB_HLSTOP
72	OSD34	00	-	-	OSDB_BLSTART
73	OSD35	00	-	-	OSDB_BLSTOP

OSDB_SIZEX OSD bar block horizontal length in character

OSDB_START OSD bar block start address in OSD command memory

OSDB_POSX OSD bar block horizontal initial position. Incrementing by 1 reflects 1 pixels shifting rightwards. Minimum value is 03h.

OSDB_POSY OSD bar block vertical initial position. Incrementing by 1 reflects 1 lines shifting downwards. Minimum value is 01h.

OSDB_HLSTART OSD bar block highlight start position

OSDB_HLSTOP OSD bar block highlight stop position

OSDB_BLSTART OSD bar block blink start position

OSDB_BLSTOP OSD bar block blink stop position

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
74	OSD36	79	OSDB_BGCLR				OSDB_FGCLR			
75	OSD37	3E	OSDB_HLBGCLR				OSDB_HLFGCLR			

OSDB_BGCLR OSD bar block background color selection, see Table 6.2.11.1 for details

OSDB_FGCLR OSD bar block foreground color selection, see Table 6.2.11.1 for details

OSDB_HLBGCLR OSD bar block high-lighted background color selection, see Table 6.2.11.1 for details

OSDB_HLFGCLR OSD bar block high-lighted foreground color selection, see Table 6.2.11.1 for details

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
DC	OSD38	00	-				-		OSD_FONT_ADDR[9:8]	
DD	OSD39	00	OSD_FONT_ADDR[7:0]							
DE	OSD40	00	OSD_FONT_DATA[15:8]							
DF	OSD41	00	OSD_FONT_DATA[7:0]							

OSD_FONT_ADDR OSD FONT RAM address (default = 00h)

OSD_FONT_DATA Data to be written into OSD control sequence RAM whose location indicated by OSD_FONT_ADDR (default = 00h)

6.2.12 EZ-GAMMA PROGRAMMING REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
7A	GM00	18	GAMMA_EN	-	-	CLUTABLE_PGR				
7B-9B	GM01-GM21		CLUTABLE00 - CLUTABLE32							

GAMMA_EN EZ-Gamma enable (df. = OFF)

CLUTABLE_PGR EZ-Gamma programming selection. Default is 18h. For detail see Table 6.2.12.1.

Table 6.2.12.1

CLUTABLE_PGR Value	Function	CLUTABLE_PGR Value	Function
00h-0Fh	Using user-programming table 7Bh – 9Bh	*18h (default)*	Gamma = 1.4
10h	Gamma = 0.75	*19h*	Gamma = 1.5
11h	Gamma = 0.8	*1Ah*	Gamma = 1.6
12h	Gamma = 0.85	*1Bh*	Gamma = 1.7
13h	Gamma = 0.9	*1Ch*	Gamma = 1.9
14h	Gamma = 1.0	*1Dh*	LCD Panel 1
15h	Gamma = 1.1	*1Eh*	LCD Panel 2
16h	Gamma = 1.2	*1Fh*	LCD Panel 3
17h	Gamma = 1.3		

6.2.13 LINE INVERSION REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
B0	OSB0	00	-	-	-	-	-	-	-	INV_FRP
B1	OSB1	00	R_BIAS							
B2	OSB2	00	G_BIAS							
B3	OSB3	00	B_BIAS							
B4	OSB4	00	R_RATIO							
B5	OSB5	00	G_RATIO							
B6	OSB6	00	B_RATIO							
B7	OSB7	00	R_BIAS_N							
B8	OSB8	00	G_BIAS_N							
B9	OSB9	00	B_BIAS_N							
BA	OSBA	00	R_RATIO_N							
BB	OSBB	00	G_RATIO_N							
BC	OSBC	00	B_RATIO_N							
BD	OSBD	00	RGB_SEL			GAIN_R				
BE	OSBE	00	-			GAIN_G				
BF	OSBF	00	o_output_upsample	-		GAIN_B				

INV_FRP FRP polarity

R_BIAS / G_BIAS / B_BIAS / R_RATIO / G_RATIO / B_RATIO / R_BIAS_N / G_BIAS_N / B_BIAS_N / R_RATIO_N / G_RATIO_N / B_RATIO_N

Output RGB bias and ratio adjustment

RGB_SEL RGB output pin select

Table 6.2.13.1 RGB MUX Setting

RGB_SEL [2]	RGB_SEL [1]	RGB_SEL[0]	RESULT
0	0	0	Red – Green – Blue (Default)
0	0	1	Red – Blue – Green
0	1	0	Blue – Red – Green
0	1	1	Blue – Green – Red
1	0	0	Green – Red – Blue
1	0	1	Green – Blue – Red
1	1	0	reserved
1	1	1	reserved

GAIN_R Red channel gain (0.77~1.23)

GAIN_G Green channel gain (0.77~1.23)

GAIN_B Blue channel gain (0.77~1.23)

GAIN_B[4] = 1 : GAIN = 1 + 0.015625 x GAIN_B[3:0]

GAIN_B[4] = 0 : GAIN = 1 - 0.015625 x GAIN_B[3:0]

o_output_upsample

0 output pixel rate unchanged (df.)

1 double output pixel rate

4.2.14 TIMING CONTROLLER REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
C0	TC0	0E	OEV_SWAP	CPH_OEV_SEL	Q1H_INV	-	OEH_SEL	LNR	UND	POLS_INV
C1	TC1	38	-	-	-			-		
C4	TC2	00	CPV_P	OEH_P	OE1_P	OE2_P	OE3_P	STV_P	CPH_P	-
C5	TC3	00	POLS_T	-	OE3_T	OE2_T	OE1_T	STV2_T	STV1_T	CPV_T
C6	TC4	00	UD_CTRL	UD_CTRL_T	LR_CTRL	LR_CTRL_T	CPH1_T	STH1_T	STH2_T	OEH_T
C7	TC5	00	-	OEV_MODE[2:0]			-	-	ZOOM_MODE[1:0]	

OEV_SWAP Pin OE1 and OE3 swap enable

CPH_OEV_SEL To select CPH2~3 or OEV2~3 as outputs of Pin OE2 and OE3

Q1H_INV To change polarity of Pin OQ1H

OEH_SEL
0 OOEH edge-trigger
1 OOEH active low (df.)

LNR
0 Left-right reverse
1 Normal scan (df.)

UND
0 Up-side-down
1 Normal scan (df.)

POLS_INV To change polarity of Pin OPOLS

CPV_P OCPV polarity change

OEH_P OOEH polarity change

OE1_P OE1 polarity change

OE2_P OE2 polarity change

OE3_P OE3 polarity change

STV_P OSTV1/OSTV2 polarity change

CPH_P OCPH polarity change

POLS_T OPOLS open drain output

OE3_T OE3 open drain output

OE2_T OE2 open drain output

OE1_T OE1 open drain output

STV2_T OSTV2 open drain output

STV1_T OSTV1 open drain output

CPV_T OCPV open drain output

UD_CTRL Pin UD_CTRL output

UD_CTRL_T UD_CTRL open drain output

LR_CTRL Pin LR_CTRL output

LR_CTRL_T LR_CTRL open drain output

CPH1_T OCPH1 open drain output

STH1_T	OSTH1 open drain output
STH2_T	OSTH2 open drain output
OEH_T	OOEH open drain output
CPH_P	OCPH1 polarity change
ZOOM_MODE	00 normal mode
	01 zoom in mode
	10 zoom out mode
	11 unused
OEV_MODE	see Table 6.2.14.1

Table 6.2.14.1 Resolution Settings

OEV_MODE[2:0]	Gate Enable Signals	Line double Type
000	OEV1~3	STV double
001	OEV1~2	STV double
010	OEV1	CPV double
011	OEV1~3	CPV double
100	SHARP mode	
101	NEC mode	

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
C2	TC6	18	STV_ON							
CC	TC7	06	STV_START							
CD	TC8	10	STV_END							
AD	TC9	6D	OEV_START							
AE	TC10	14	OEV_END							
AF	TC11	14	OEV_MASK_START							
C8	TC12	0A	CPV1_RISE							
C9	TC13	2E	CPV1_FALL							
CA	TC14	43	CPV2_RISE							
CB	TC15	5E	CPV2_FALL							
CF	TC16	00	OEV_MASK_LSB[3:0]				-	-	-	OEV_MASK_SEL
D6	TC17	0D	-				DROP_PER_N			
D7	TC18	5D	V_DROP_L1				V_DROP_L2			
D8	TC19	28	V_DROP_L3				V_DROP_L4			
D9	TC20	66	DOUBLE_PER_N				V_DOUBLE_L			

STV_ON The line no. of the first line displayed on screen

STV_START STV pulse starting point

STV_END STV pulse ending point

OEV_START OEV pulse starting point

OEV_END OEV pulse ending point

OEV_MASK_START, OEV_MASK_LSB[3:0]

	Starting point to disable OEV
OEV_MASK_SEL	Mode of disabling OEV
	0: mask back portion of OEV
	1: mask front portion of OEV
CPV1_RISE	First CPV rise point
CPV1_FALL	First CPV fall point
CPV2_RISE	Second CPV rise point
CPV2_FALL	Second CPV fall point
DROP_PER_N	Drop 2 lines for every DROP_PER_N lines
V_DROP_L1, V_DROP_L2	The 2 lines dropped in odd field
V_DROP_L3, V_DROP_L4	The 2 lines dropped in even field
DOUBLE_PER_N	1 line double-scanned for every DOUBLE_PER_N lines
V_DOUBLE_L	The line double-scanned in DOUBLE_PER_N lines

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
C3	TC21	0A	POL_INV_ON							
A3	TC22	15	OEH_START							
A4	TC23	23	OEH_END							
A5	TC24	00	-	-	-	-	-	STH_ON[10:8]		
A6	TC25	74	STH_ON[7:0]							

POL_INV_ON	OPOLS alternating polarity time
OEH_START	OEH pulse starting point
OEH_END	OEH pulse ending point
STH_ON	STH active point

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
A7	TC26	00	-	CPH_SEL_A[10:8]			-	CPH_SEL_B[10:8]		
A8	TC27	00	CPH_SEL_A[7:0]							
A9	TC28	00	CPH_SEL_B[7:0]							
AA	TC29	70	-	CPH_SEL_C[10:8]			-	CPH_SEL_D[10:8]		
AB	TC30	FF	CPH_SEL_C[7:0]							
AC	TC31	00	CPH_SEL_D[7:0]							

CPH_SEL_A, CPH_SEL_B	To select different rate of CPH for horizontal zoom, refer to Fig
CPH_SEL_C, CPH_SEL_D	

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
2A	TC31	25	CPH_MODE			RATE1_CNT_N				
2B	TC32	24	RATE1_PARAM_A[7:0]							
2C	TC33	00	RATE1_PARAM_A[15:8]							
2D	TC34	00	RATE 1_PARAM_A[23:16]							
33	TC35	00	RATE1_PARAM_A[31:24]							
34	TC36	24	RATE1_PARAM_B[7:0]							
35	TC37	00	RATE1_PARAM_B[15:8]							
36	TC38	00	RATE1_PARAM_B[24:16]							

37	TC39	00	RATE1_PARAM_B[31:24]

CPH_MODE 001 CPH consists of rate1 only

011 CPH switches between rate1 and rate2

111 CPH switches between rate1, rate2 and rate3

RATE1_CNT_N parameter to set rate1

RATE1_PARAM_A parameter to set rate1

RATE1_PARAM_A parameter to set rate1

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
38	TC41	13	CPH_DLY[1:0]		-	RATE2_CNT_N				
39	TC42	49	RATE2_PARAM_A[7:0]							
44	TC43	4A	RATE2_PARAM_A[15:8]							
49	TC44	02	RATE2_PARAM_A[23:16]							
4A	TC45	00	RATE2_PARAM_A[31:24]							
4B	TC46	49	RATE2_PARAM_B[7:0]							
4C	TC47	48	RATE2_PARAM_B[15:8]							
4D	TC48	02	RATE2_PARAM_B[24:16]							
4E	TC49	00	RATE2_PARAM_B[31:24]							

CPH_DLY[1:0] To set clock phases of CPH2 and CPH3

RATE2_CNT_N parameter to set rate2

RATE2_PARAM_A parameter to set rate2

RATE2_PARAM_A parameter to set rate2

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
4F	TC50	1F	-	-	-	RATE3_CNT_N				
76	TC51	55	RATE3_PARAM_A[7:0]							
77	TC52	55	RATE3_PARAM_A[15:8]							
78	TC53	55	RATE3_PARAM_A[23:16]							
79	TC54	55	RATE3_PARAM_A[31:24]							
9C	TC55	00	RATE3_PARAM_B[7:0]							
9D	TC56	00	RATE3_PARAM_B[15:8]							
9E	TC57	00	RATE3_PARAM_B[24:16]							
9F	TC58	00	RATE3_PARAM_B[31:24]							

RATE3_CNT_N parameter to set rate3

RATE3_PARAM_A parameter to set rate3

RATE3_PARAM_A parameter to set rate3

6.2.15 STATUS REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
D0	Status	-	-	-	AGC_STATUS					
D1	Status	-	DAGC_STATUS							
D2	Status	-	BLKLEV_STATUS							
D3	Status	-	NOISE MORE	PHALT	IS443	VPRES	MODE [1:0]		FINEAGC	MVVALID
D4	Status	-	CAGC_STATUS							
D5	Status	-	CCPRES	CC525	-	-	-	-	-	LLOCK

AGC_STATUS Controls gain of analog composite/luma and chroma inputs

DAGC_STATUS Internal digital automatic gain control value

BLKLEV_STATUS Black level. 0 means no change. (ref: 7'b1000110 = 70d)

NOISE_MORE Video noise detection. 1 represents there is more noise

PHALT Phase switching signal of PAL signal

IS443 Carrier frequency detection

0 3.58 MHz

1 4.43 MHz

VPRES Coarse lock status. Set when sync of proper height and duration has been detected on 32 successive lines; reset if sync is not detected on 32 successive lines.

0 Unlock

1 Locked

MODE

0 PAL (Combination N)

1 PAL (B, D, G, H, I, N)

2 PAL (M)

3 NTSC

FINEAGC Automatic gain control stability indication

0 Unstable

1 Stable

MVVALID MacroVision protect detection

0 MacroVision protect waveform exist

1 None MacroVision protect waveform

CAGC_STATUS Chroma automatic gain control value

CCPRES CCIR656 input video present, only available when ccir_in_en set

CC525

0 CCIR656 input video is 525-line format (df.)

1 CCIR656 input video is 625-line format

LLOCK Indication of successive lines

0 Successive lines available exist

1 No successive lines available

6.2.16 PWM REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
43	PWM0	00	-		PWM_SEL1		PWM_SEL2		PWM_SEL3	
E0	PWM1	FF	PWM1_L0							
E1	PWM2	FF	PWM1_L1							
E2	PWM3	FF	PWM1_H0							
E3	PWM4	FF	PWM1_H1							
E4	PWM5	FF	PWM2_L0							
E5	PWM6	FF	PWM2_L1							
E6	PWM7	FF	PWM2_H0							
E7	PWM8	FF	PWM2_H1							

PWM_SEL select sel_pwm1 sel_pwm2 sel_pwm3 output source.

00: sel_pwm1=vsync_vga sel_pwm2=hsync_vga sel_pwm3=voclk_o

01: sel_pwm1=0 sel_pwm2=0 sel_pwm3=0

10: sel_pwm1=pwm1 sel_pwm2= pwm1 sel_pwm3= pwm1

11: sel_pwm1=pwm2 sel_pwm2= pwm2 sel_pwm3= pwm2

PWM1_L PWM1 LOW level value.

PWM1_H PWM1 HIGH level value.

PWM2_L PWM2 LOW level value.

PWM2_H PWM2 HIGH level value.

6.2.17 CONTINUOUS WRITE REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
FD	CW0	00	-	CW_DEST [2:0]			-	-	CW_INIT_ADDR [9:8]	
FE	CW1	00	CW_INIT_ADDR [7:0]							
FF	CW2	00	CW_DATA							

CW_DEST Continuous write destination selection

0 None
1 OSD command memory
2 OSD font memory
3 CLUT R / Pr
4 CLUT G / Y
5 CLUT B / Pb
6 CLUT all
7 OSD command memory

CW_INIT_ADDR Continuous write initial address

CW_DATA Continuous write data

7. ELECTRICAL CHARACTERISTICS

7.1 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Supply Voltage For Digital Core (2.5V Nominal)	V_{CCD}	-0.5	3.0	V
Supply Voltage For Digital I/O (3.3V Nominal)	V_{DDD}	-0.5	4.0	V
Supply Voltage For Analog Core (3.3V Nominal)	V_{DDA}	-0.5	4.0	V
Input Voltage For Digital I/O (5V Tolerant)	V_{ID}	-0.5	V_{DDD} + 0.5	V
Input Voltage For Analog Core	V_{IA}	-0.5	V_{DDA} + 0.5	V
Junction Temperature	T_J	-40	125	°C
Storage Temperature	T_{STG}	-55	125	°C
Lead Temperature (Vapor Phase Soldering, 40 Seconds)	T_L	-	215	°C
Electronic Discharge	T_{ESD}	-2000	2000	V

7.2 RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage For Digital Core (2.5V Nominal)	V_{CCD}	2.25	2.5	2.75	V
Supply Voltage For Digital I/O (3.3V Nominal)	V_{DDD}	3.0	3.3	3.6	V
Supply Voltage For Analog Core (3.3V Nominal)	V_{DDA}	3.1	3.3	3.5	V
Ambient Operation Temperature	T_A	0	-	70	°C
Package Case Temperature	T_A	-	-	115	°C
Total Power Dissipation	P_{TOT}	-	390	-	mW

7.3 DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input (I, I_S, I_{PU}, I_{PD})					
High Level Input Voltage	V_{IH}	0.65 V_{DDD}	-	-	V
Low Level Input Voltage	V_{IL}	-	-	0.35V_{DDD}	V
Leakage Current[1]	I_L	0	-	500	μA
Output (O_1, O_{TS1})					
High Level Output Voltage	V_{OH}	2.4	-	-	V
Low Level Output Voltage	V_{OL}	-	-	0.4	V
Tri-State Output Leakage Current	I_L	-25	-	25	μA
Input/TTL Output (I/O_1, I/O_2)					
High Level Input Voltage	V_{IH}	0.65 V_{DDD}	-	-	V
Low Level Input Voltage	V_{IL}	-	-	0.35V_{DDD}	V
High Level Output Voltage	V_{OH}	2.4	-	-	V
Low Level Output Voltage	V_{OL}	-	-	0.4	V
Pull-Up/Down Resistor					
Pull-Up Resistor	R_{PU}	59	74	94	Ωk
Pull-Down Resistor	R_{PD}	63	77	97	Ωk

[1] No leakage current flown when input voltage is V_{DDD} or 0. The maximum occurs at transitions.

7.4 ANALOG-FRONT-END SPECIFICATION

Parameter	Symbol	Min	Typ	Max	Unit
Variable Gain Amplifier					
Program Resolution	-	-	6	-	bit
Gain Range	-	1	-	6	-
ADC					
Resolution	-	-	10	-	bit
Sampling frequency	-	-	40	-	MHz

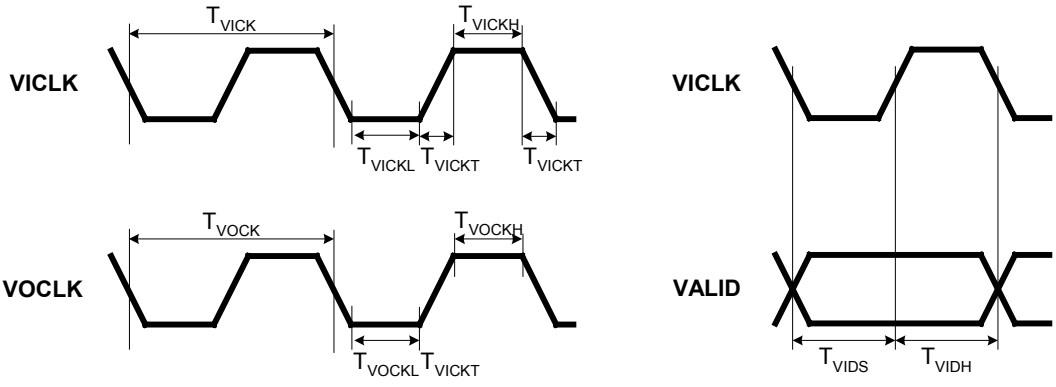
7.5 DAC SPECIFICATION

Parameter	Symbol	Min	Typ	Max	Unit
Resolution	-	-	10	-	Bit
Spurious-Free Dynamic Range	SFDR	61	-	-	dB
Signal-To-Noise-And-Distortion	SINAD	57	-	-	dB
Conversion Frequency	-	54	-	-	MHz
Power Consumption	-	-	100	-	mW
Output Current	-	-	-	35	mA
Glitch Energy	-	-	-	10	ps * V
Output Voltage Compliance	-	0	-	1.3	V
Supply Voltage	-	-	3.3	-	V

7.6 AC CHARACTERISTICS

7.6.1 DIGITAL VIDEO INTERFACE

Parameter	Symbol	Min	Typ	Max	Unit
Input Clock					
Video input clock VICLK[1] frequency	F_{VICK}		27		MHz
Video input clock VICLK period	T_{VICK}		37.04		ns
Video input clock VICLK width high	T_{VICKH}		18.52		ns
Video input clock VICLK width low	T_{VICKL}		18.52		ns
Video input clock VICLK transition time	T_{VICKT}		5		ns
Output Clock					
Video output clock VOCLK[2] frequency	F_{VOCK}		27		MHz
Video output clock VOCLK period	T_{VOCK}		37.04		ns
Video output clock VOCLK width high	T_{VOCKH}		18.52		ns
Video output clock VOCLK width low	T_{VOCKL}		18.52		ns
Video Input					
Video input data setup time to VICLK	T_{VIDS}	5			ns
Video input data hold time from VICLK	T_{VIDH}	1			ns
Video Output					
Video output data delay from VOCLK	T_{VODH}		7		ns

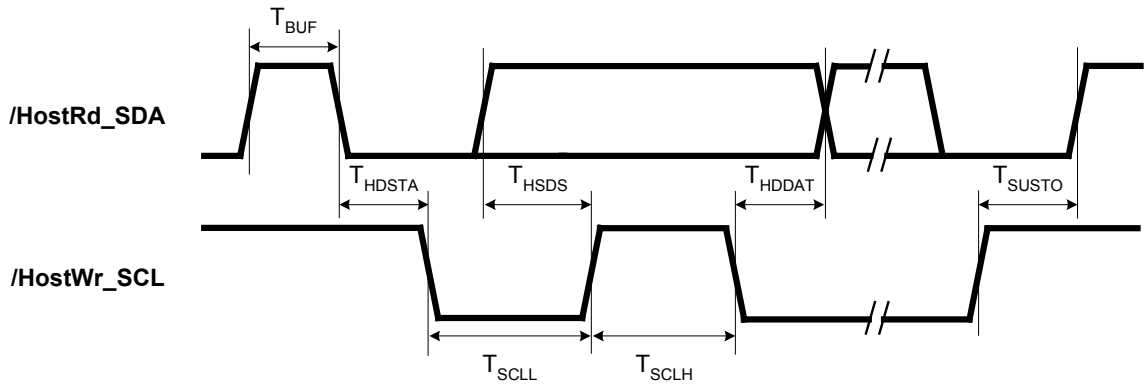


Digital Video Interface Timing

[1] In CCIR input mode, VICLK is input at CCLK.
[2] In CCIR output mode, VOCLK is output at CCLK.

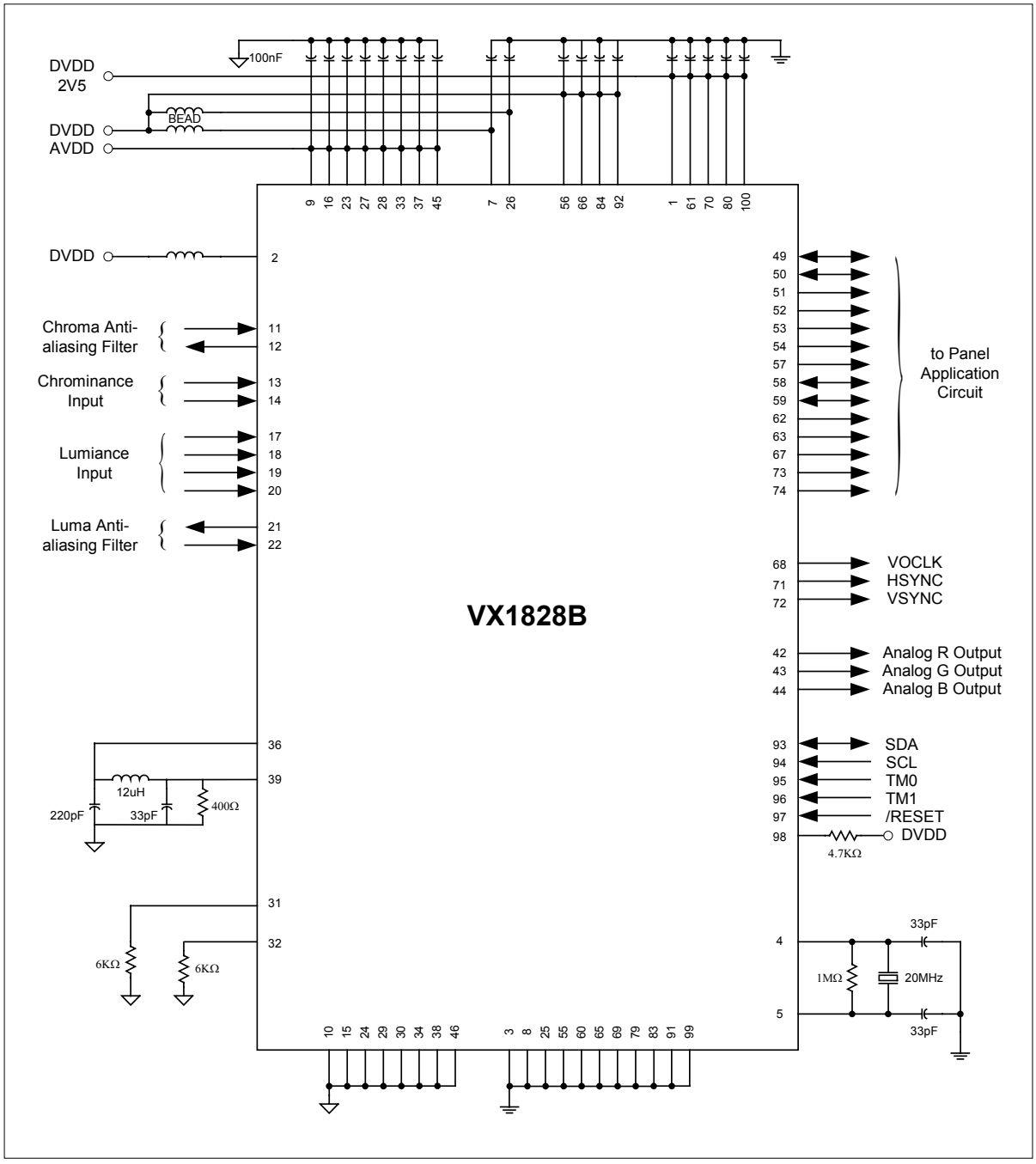
7.6.2 HOST INTERFACE

Parameter	Symbol	Min	Typ	Max	Unit
SCL Clock Frequency	F_{SCL}	-	100	-	KHz
Serial Bus Free Time Between STOP and START Condition	T_{BUF}	4.7	-	-	μs
Serial Bus Hold Time For START Condition	T_{HDSTA}	4.0	-	-	μs
SCL Clock Width Low	T_{SCLL}	4.7	-	-	μs
SCL Clock Width High	T_{SCLH}	4.0	-	-	μs
Serial Data Setup Time	T_{HSDS}	0.5	-	-	μs
Serial Data Hold Time	T_{HSDH}	-	-	0	μs
Serial Bus Setup Time For STOP Condition	T_{SUSTO}	4.0	-	-	μs

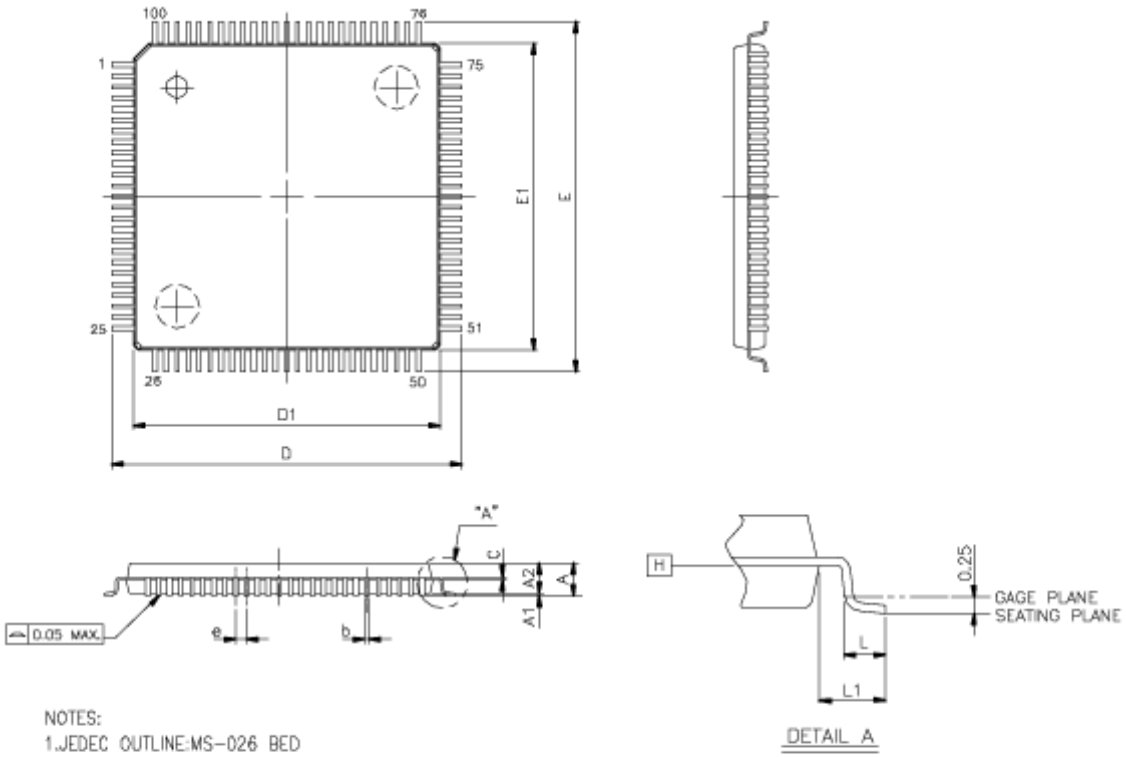


Host Interface Timing

8. IC CONNECTION DIAGRAM



9. PACKAGE DIMENSION



NOTES:
1.JEDEC OUTLINE:MS-026 BED

2.DATUM PLANE [H] IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

3.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLDWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H].

4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	0.127	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		