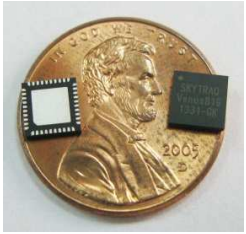
Venus816

Dual-RF Input
Integrated Antenna Switch
Active Antenna Short Circuit Protection

Single-Chip GPS Receiver

Datasheet



5mm x 5mm

Version 3.0

OVERVIEW

The Venus816 is a single-chip GPS receiver containing RF and baseband in a 5mm x 5mm QFN40 package. Featuring high performance SkyTraq Venus 8 positioning engine, the Venus816 provides good sensitivity and very short TTFF with no host interaction needed. Venus816 targets high-volume cost-sensitive consumer GPS applications.

RF FEATURES

- Integrated LNA with high-gain (20 dB typ.) and low NF (0.9 dB typ.)
- Cascaded system noise figure of 1.2 dB typical
- Support RF dual-input for passive antenna and active antenna
- Integrated antenna switching with active antenna current detection
- Integrated 50mA current limiting for active antenna biasing short circuit protection
- Support 16.367667MHz 0.5ppm and 2.5ppm TCXO

BASEBAND FEATURES

- 167 acquisition/tracking channels
- 40Hz maximum update rate
- Support QZSS, WAAS, MSAS, EGNOS, GAGAN
- 16 million time-frequency hypothesis testing per second
- 1 second hot start TTFF
- 3.5 second TTFF with AGPS
- 29 second cold start TTFF
- 2.5m CEP position accuracy
- Multipath detection and suppression
- Jamming detection and mitigation
- 7-day extended ephemeris AGPS
- Stand-alone solution, no host needed
- RoHS compliant

TECHNICAL SPECIFICATIONS

Receiver Type	L1 Frequency GPS C/A code SBAS Capable QZSS Capable
Accuracy	Position 2.5m CEP Velocity 0.1m/sec Timing 12ns
Open Sky TTFF	Hot start 1 second Cold start 29 seconds average
Reacquisition	< 1s
Sensitivity	Cold start -148dBm Tracking -161dBm
Update Rate	1 / 2 / 4 / 5 / 8 / 10 / 20 / 25 / 40 Hz update rate default 1Hz
Dynamics	4G
Operational Limits	Altitude < 18,000m or Velocity < 515m/s, not exceeding both
Datum	Default WGS-84
Interface	UART LVTTL level
Baud Rate	4800 / 9600 / 19200/ 38400 / 57600 / 115200 / 230400 software selectable default 9600
Protocol	NMEA-0183 V3.01, GGA, GLL, GSA, GSV, RMC, VTG, ZDA and SkyTraq Binary
Main Supply Voltage	3.3V+/-10%, 1.2V+/-10%
Backup Voltage	1.2V+/-10%
Current Consumption	

Acquisition	Tracking
15mA @ 3.3V 49mA @ 1.2V	15mA @ 3.3V 21mA @ 1.2V

With 90% Efficiency 3.3V-to-1.2V DC/DC Switching Regulator
Acquisition: 35mA @ 3.3V Tracking: 24mA @ 3.3V

Operating Temperature	-40 ~ +85 deg-C
Storage Temperature	-40 ~ +125 deg-C
Package	5mm x 5mm QFN40

BLOCK DIAGRAM

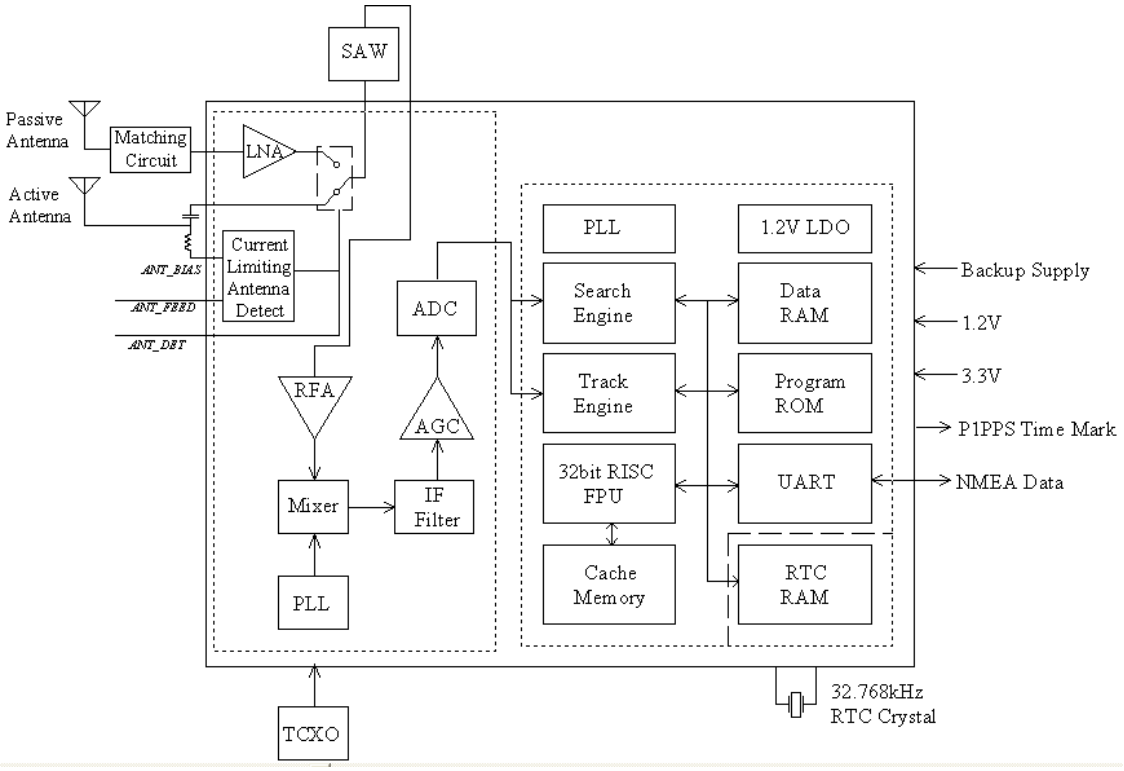


Figure-1 Block Diagram

RF SUBSYSTEM

The RFIC section implements a low-IF architecture with a 4MHz IF. The received 1575.42MHz GPS signal is amplified by a 20dB gain 0.9dB noise figure LNA, and then output to an external SAW filter. An RF amplifier provides further amplification, reducing the noise figure requirements for the mixer stage. After down-conversion, the signal is band-pass filtered and amplified by an Automatic Gain Control (AGC) stage. The IF signal is then digitized into 2bit sign/magnitude and sent to the baseband subsystem.

LNA

A high-performance LNA is available for use with systems with an external passive antenna.

The LNA noise figure is the largest single contributor to overall system sensitivity in GPS signal reception. The internal LNA allows excellent performance to be achieved from a low-power GPS receiver without requiring any additional active components.

The LNA input requires a minimum of external matching components to achieve good RF gain with minimal noise figure. Although attention should be paid to track lengths and interference throughout the design, the LNA input matching circuit is the only RF circuit critically sensitive to layout.

The LNA output includes internal 50Ω matching for connection to the mixer input, either directly or via an optional external filter.

ANTENNA SWITCH

An antenna switch is included to allow selection of either the LNA_IN (pin-16) RF path, or the ANT_IN (pin-15) RF path, to connect to a single RF output ANT_SW_OUT (pin-24). This is useful in systems where two antenna sources can be provided.

The antenna switch is driven from the antenna current detector block. The antenna switch will transfer the RF input from the default LNA_IN (pin-16) over to ANT_IN (pin-15), when the antenna current detector block senses a current being consumed from an external active antenna. The switching threshold is typically 1mA with some hysteresis

ANTENNA CURRENT DETECTOR

The antenna current detector is designed to monitor the supply current to an external active antenna and provide a logic output, ANT_DET (pin-25). This is used to indicate if the current is within an expected range. The current monitor senses the current which passes through the ANT_BIAS (pin-14) output.

ANT_DET (pin-25) is connected to the switchover control of the internal antenna switch. The antenna switch will transfer the route of the RF input path from the internal LNA, supplied from the LNA_IN input (pin-16), across to ANT_IN (pin-15), through to the ANT_SW_OUT output (pin-24), when current is detected.

ANT_BIAS (pin-14) should be connected to the core connection of a coax socket via an isolating choke for an external active antenna, in conjunction with ANT_IN (pin-15) connected to the same core connection of the socket via a dc-blocking capacitor. When an external active antenna is connected, DC current to drive the active antenna will flow through ANT_BIAS (pin-14), and the antenna current detector.

ANTENNA SWITCH OVERRIDE

The antenna switch (and antenna current detector) can be overridden by externally driving ANT_DET (pin-25) from a low-impedance external source, at VCC (pin-26) or GND levels.

The external source applied to ANT_DET (pin-25) must be able to source >300uA into the pin, or sink >70uA out of the pin to allow guaranteed levels to be set.

MIXER RF INPUT

The mixer RF input, MIX_IN (pin-27), is a single-ended 50Ω input designed to interface either to ANT_SW_OUT (pin-24) or to the output of an external SAW filter. The image reject mixer ensures that the receiver's full sensitivity is achieved without an external filter. For applications where additional selectivity is required, an external filter can be added between the ANT_SW_OUT and MIX_IN pins.

IF FILTER

The Venus816 includes a fully integrated IF filter which provides good interference rejection with no additional external components. The band-pass filter has a nominal bandwidth of 2.2 MHz; the nominal center frequency is preset to 4.092MHz. These parameters ensure very low implementation loss in all frequency plan configurations.

AGC and ADC

The Venus816 features a linear IF chain with 2-bit SIGN / MAG ADC. An AGC system is included to provide 50 dB of gain control range so that the output signal level is held at an optimum level at the input of the ADC. The MAG bit controls the AGC loop, such that the MAG bit is active high for approximately 33% of the time. The SIGN and MAG signals are latched by the falling edge of the sample clock by the ADC. The SIGN and MAG signals are re-sampled on the rising edge of CLK at the baseband. The AGC time constant is determined by a single external capacitor, connected between VAGC (pin-7) and GND. The settling-time of the AGC is within 10ms with a 10nF capacitor.

HARDWARE CONFIGURATION

The RF front-end can be configured to change the LNA Gain/Linearity and the Mixer Gain/Linearity by means of the settings on the HW_CFG (pin-36) logic input. The adjustment of the gain and linearity allow the Venus816 to be used in differing environments, either with significant co-located interference sources (e.g. mobile phone) or no interference sources (e.g. PND).

HW_CFG	LNA Gain	LNA IIP3	Mixer Buffer Gain
1	20dB	-6dBm	32dB
0	17dB	-12dBm	24dB

BASEBAND SUBSYSTEM

The Venus816 baseband implements all the needed function for GPS signal acquisition, tracking, decoding, and navigation solution. It is optimized for GPS applications requiring high performance. Major blocks within the chip are: GPS signal processing engine, 32bit RISC processor, peripheral interface, and memory.

GPS SIGNAL PROCESSING ENGINE

The signal-processing engine comprise of a signal parameter search engine and a track engine. Both implement carrier frequency wipe-off, pseudorandom code removal, plus coherent and incoherent integration required for indoors high-sensitivity signal processing.

The signal parameter search engine can be configured to search full code space and several frequencies simultaneously, or full code space of all satellites simultaneously. Massive correlator design, allows extremely high signal acquisitions speed and high sensitivity performance.

32BIT RISC

The internal 32bit RISC is a 7-stage pipelined processor. The processor handles all time-critical GPS related functions, management controls, and navigation solutions.

CACHE MEMORY

Cache memory subsystem consists of 16Kbyte I-cache, and 2Kbyte D-cache.

BATERY-BACKED RTC AND RAM

The real-time clock circuitry and a small block of SRAM is included on-chip to retain time and the necessary GPS data for rapid warm start and hot-start operation.

DATA RAM

The chip contains SRAM needed for stand-alone operation. The on-chip SRAM is designed for low-power and high-speed single cycle access.

PROGRAM ROM

The chip implements program ROM on-chip.

UART

2 set of UART is supported for Venus816 in QFN40 package. Currently only UART1 is used.

REGULATOR

3.3V-to-1.2V LDO regulator is implemented on-chip for powering the power-cut region containing the real-time clock circuitry and data backup memory.

PLL

The signal parameter search engine requires high clock rate. It is generated from GPS reference clock through the on-chip PLL. A divided-down PLL clock is selected to clock the 32bit RISC.

PIN CONFIGURATION

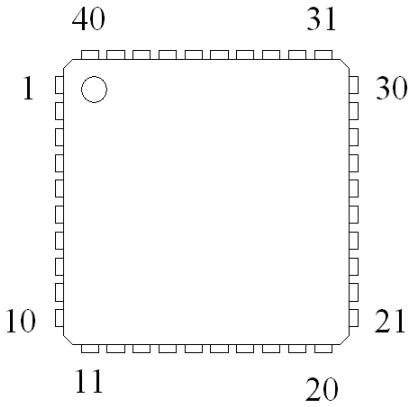


Figure-2 Pin-Out QFN40 (Top-View)

Table-1 Venus816 Pin-Out

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V12I	11	DET_V12I	21	P1PPS	31	TXD1
2	V12I	12	RTC_OSCI	22	V12I	32	PPM_SEL
3	V33I	13	RTC_OSCO	23	BB_GND	33	V12I
4	BB_GND	14	RF_ANT_BIAS	24	RF_ANT_SW_OUT	34	RF_VCC
5	RSTN	15	RF_ANT_IN	25	RF_ANT_DET	35	RF_TCXO_IN
6	RF_ANT_FEED	16	RF_LNA_IN	26	RF_VCC	36	RF_HW_CFG
7	RF_VAGC	17	RF_RX_EN	27	RF_MIX_IN	37	BB_GND
8	V12O_LDO	18	RF_VCC_LNA	28	BB_GND	38	VDD_IFINTF
9	V33I_LDO	19	RXD2	29	V33I	39	V12I
10	V12I_RTC	20	TXD2	30	RXD1	40	BB_GND

SIGNAL DESCRIPTION

Table-2 Venus816 Signal Description

Pin No.	Signal Name	Signal Type	Description
1	V12I	Power	Baseband core voltage supply input, 1.2V
2	V12I	Power	Baseband core voltage supply input, 1.2V
3	V33I	Power	Baseband I/O voltage supply input, 3.3V
4	BB_GND	Power	Baseband ground
5	RSTN	Input	Baseband reset input, active low. Connect to 33K/1uF RC delay, reset supervisor IC, or GPIO pin for software controlled reset.
6	RF_ANT_FEED	Power	Power supply to external active antenna, via RF_ANT_BIAS Connect to RF_VCC
7	RF_VAGC	Bi-Dir	Connect to AGC filter capacitor, 10nF
8	V12O_LDO	Power	On-chip 3.3V-to-1.2V LDO regulator 1.2V output, max current 24mA. Must not use it to drive baseband core V12I input
9	V33I_LDO	Power	On-chip 3.3V-to-1.2V LDO regulator voltage input Input range 2.5V ~ 3.6V, DC current ~30uA
10	V12I_RTC	Power	Baseband backup supply input, 1.2V
11	DET_V12I	Input	Detect existence of V12I supply voltage. Connect to baseband core 1.2V voltage supply
12	RTC_OSCI	Input	RTC oscillator input
13	RTC_OSCO	Output	RTC oscillator output
14	RF_ANT_BIAS	Output	External antenna bias output. Connect to external antenna on RF_ANT_IN. Use capacitor to DC block the bias from the RF_ANT_IN input
15	RF_ANT_IN	Input	RF input from external antenna. DC bias on this pin. DC blocking capacitor required.
16	RF_LNA_IN	Input	RF input, via on-chip LNA. DC bias on this pin. Connect either direct to passive GNSS antenna element, or to grounded components using a DC blocking capacitor.
17	RF_RX_EN	Input	Receiver enable, connect to RF_VCC
18	RF_VCC_LNA	Power	Analogue power supply for LNA
19	RXD2	Input	UART input, 3.3V I/O
20	TXD2	Output	UART output, 3.3V I/O
21	P1PPS	Output	1 pulse per second output, 3.3V I/O
22	V12I	Power	Baseband core voltage supply input, 1.2V
23	BB_GND	Power	Baseband ground
24	RF_ANT_SW_OUT	Output	Antenna switch output
25	RF_ANT_DET	Bi-Dir	External-antenna connected detect output (controls internal antenna switch)
26	RF_VCC	Power	RF voltage supply input, 3.3V
27	RF_MIX_IN	Input	Mixer input
28	BB_GND	Power	Baseband ground
29	V33I	Power	Baseband I/O voltage supply input, 3.3V
30	RXD1	Input	UART input, 3.3V I/O
31	TXD1	Output	UART output, 3.3V I/O
32	PPM_SEL	Input	TCXO ppm selection 0: +/-2.5ppm 1: +/-0.5ppm
33	V12I	Power	Baseband core voltage supply input, 1.2V
34	RF_VCC	Power	RF voltage supply input, 3.3V

35	RF_TCXO_IN	Input	frequency reference input, 16.367667MHz
36	RF_HW_CFG	Input	Hardware configuration pin
37	BB_GND	Power	Baseband ground
38	VDD_IFINTF	Power	Baseband IF interface I/O voltage supply input, 3.3V
39	V12I	Power	Baseband core voltage supply input, 1.2V
40	BB_GND	Power	Baseband ground
41	*RF_GND*	*Power*	*The center ground paddle is the RF ground*

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Min.	Max.	Unit
Baseband Core Supply Voltage	V12I	-0.3	1.44	Volt
Baseband Backup Supply Voltage	V12I_RTC	-0.3	1.44	Volt
RF Supply Voltage	RF_VCC	-0.3	3.6	Volt
LNA Input Power	LNA_IN_{MAX}		+3	dB
Electrostatic Discharge Immunity (HBM)	ESD	2		kV
Operating Temperature		-40	+85	^{o}C
Storage Temperature		-40	+150	^{o}C
Solder Reflow Temperature			260	^{o}C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Minimum	Typical	Maximum	Units
Baseband Core Supply Voltage	V12I	1.08	1.2	1.32	Volt
Baseband Backup Supply Voltage	V12I_RTC	1.08	1.2	1.32	Volt
Baseband Interface Supply Voltage	V33I	3.0	3.3	3.6	Volt
RF Supply Voltage	RF_VCC	2.7		3.6	Volt
Junction Operating Temperature	Tj	-40	25	125	^{o}C

DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units
RF Section Supply Current (with LNA)	I_{RF_VCC}		15		mA
RF Section Supply Current (without LNA)	I_{RF_VCC}		10		mA
RF Section Supply Current (RX_EN=0)	I_{RF_VCC}			10	uA
Baseband Core Logic Current (Peak)	I_{V12I}		49		mA
Baseband Core Logic Current (Tracking)	I_{V12I}		21		mA

AC ELECTRICAL CHARACTERISTICS, LNA

Parameter	Symbol	Min.	Typ.	Max.	Units
LNA Supply Current (HW_CFG=1)	I_{VCC_LNA}		5		mA
LNA Supply Current (HW_CFG=0)	I_{VCC_LNA}		3		mA
Forward Gain (HW_CFG=1)	S_{21_LNA}		20		dB
Forward Gain (HW_CFG=0)	S_{21_LNA}		17		dB
Noise Figure (HW_CFG=1)	NF_{LNA}		0.9		dB
Noise Figure (HW_CFG=0)	NF_{LNA}		0.9		dB
Input Compression Point	IP_{1dB}		-13		dBm
Input IP3 (HW_CFG=1)	$IIP3_{LNA}$		-6		dBm
Input IP3 (HW_CFG=0)	$IIP3_{LNA}$		-12		dBm
Input 50ohm Return Loss	S_{11_LNA}		-8		dB
Output 50ohm Return Loss	S_{22_LNA}		-15		dB

AC ELECTRICAL CHARACTERISTICS, EXTERNAL ANTENNA PATH

Parameter	Symbol	Min.	Typ.	Max.	Units
Insertion Loss, ANT_IN to ANT_SW_OUT	IL_{ANTSW}		0.7		dB
Isolation Between Switch Input Ports	$ISOL_{ANTSW}$		-20		dB
S_{11}, into 50 Ω, ANT_IN enabled	$S11_{ANTSW}$		-15		dB
S_{22}, into 50 Ω, ANT_SW_OUT enabled	$S22_{ANTSW}$		-15		dB

DC Electrical Characteristics, Antenna Current Detector

Parameter	Min.	Typ.	Max.	Units
Current Threshold for ANT_DET = HI		1		mA
Current Threshold for ANT_DET = LO		0.85		mA
ANT_FEED to ANT_BIAS Drop-out Voltage, 10mA load		0.075		V
ANT_FEED to ANT_BIAS Drop-out Voltage, 5mA load		0.04		V
Short-circuit Current Limit, ANT_BIAS			50	mA

AC ELECTRICAL CHARACTERISTICS, RECEIVER

Parameter	Min.	Typ.	Max.	Units
Voltage Gain of Mixer and Low Noise Buffer (HW_CFG=1)		32		dB
Voltage Gain of Mixer and Low Noise Buffer (HW_CFG=0)		24		dB
Noise Figure, f_{RF} = 1570 MHz To 1580 MHz, Input to MIX_IN		6.5		dB
IF Center Frequency (16.368 MHz reference)		+4.092		MHz
IF Center Frequency (16.367667 MHz reference)		+4.124		MHz
Cascaded Noise Figure with On-Chip LNA		1.2		dB
Mixer Image Rejection	20	30		dB
AGC Range		50		dB
Reference Clock Input		16.367667 16.368		MHz
External oscillator drive level	0.2	1	1.7	Vpp
IF Filter -3dB Bandwidth		2.2		MHz
LO SSB phase noise		-82 @ 1kHz offset -82 @ 10kHz offset -85 @ 100kHz offset		dBc/Hz
P1dB Compression Point at Mixer Input		-13		dBm

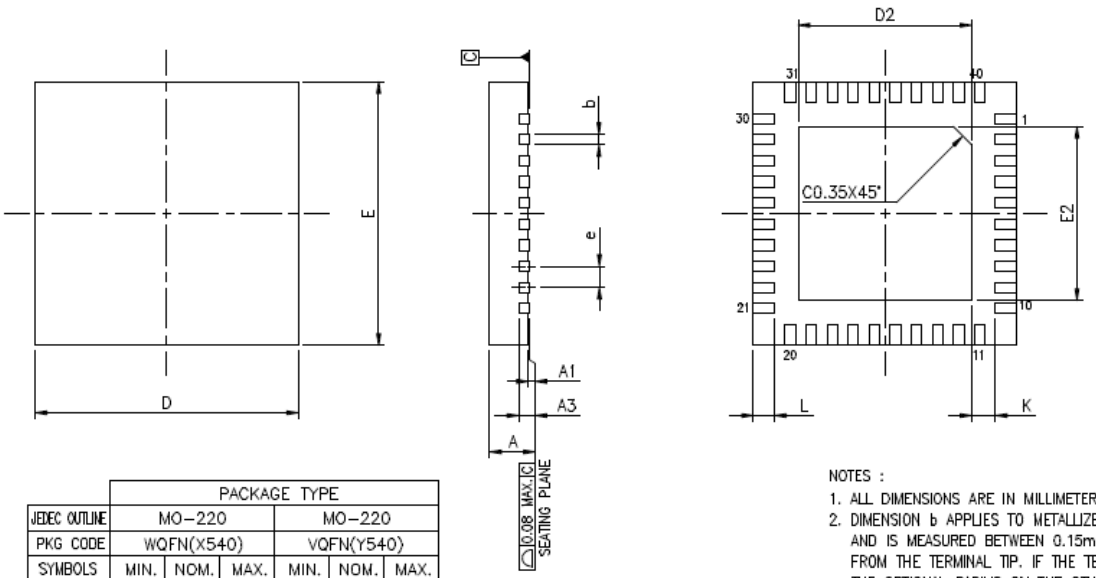
DC CHARACTERISTICS OF 3.3V I/O

Parameter	Symbol	Min.	Typ.	Max.	Units
Input Low Voltage	V_{IL}	-0.3		0.8	Volt
Input High Voltage	V_{IH}	2.0		V33I + 0.3	Volt
Output Low Voltage, Iol = 4mA	V_{OL}			0.4	Volt
Output High Voltage, Ioh = 4mA	V_{OH}	2.4			Volt
Input Leakage Current	I_{IN}		+/-10		uA

RESET TIMING

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Reset duration	T1	10			TCXO Clock

MECHANICAL SPECIFICATIONS



	PACKAGE TYPE					
JEDEC OUTLINE	MO-220			MO-220		
PKG CODE	WQFN(X540)			VQFN(Y540)		
SYMBOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90
A1	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.20 REF.			0.20 REF.		
b	0.15	0.20	0.25	0.15	0.20	0.25
D	5.00 BSC			5.00 BSC		
E	5.00 BSC			5.00 BSC		
e	0.40 BSC			0.40 BSC		
K	0.20	—	—	0.20	—	—

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

	E2			D2			L			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
153X153 MIL	3.20	3.30	3.35	3.20	3.30	3.35	0.35	0.40	0.45	V	X	N/A
2 159X159 MIL	3.69	3.79	3.84	3.69	3.79	3.84	0.25	0.30	0.35	V	X	N/A

MARKING INFORMATION

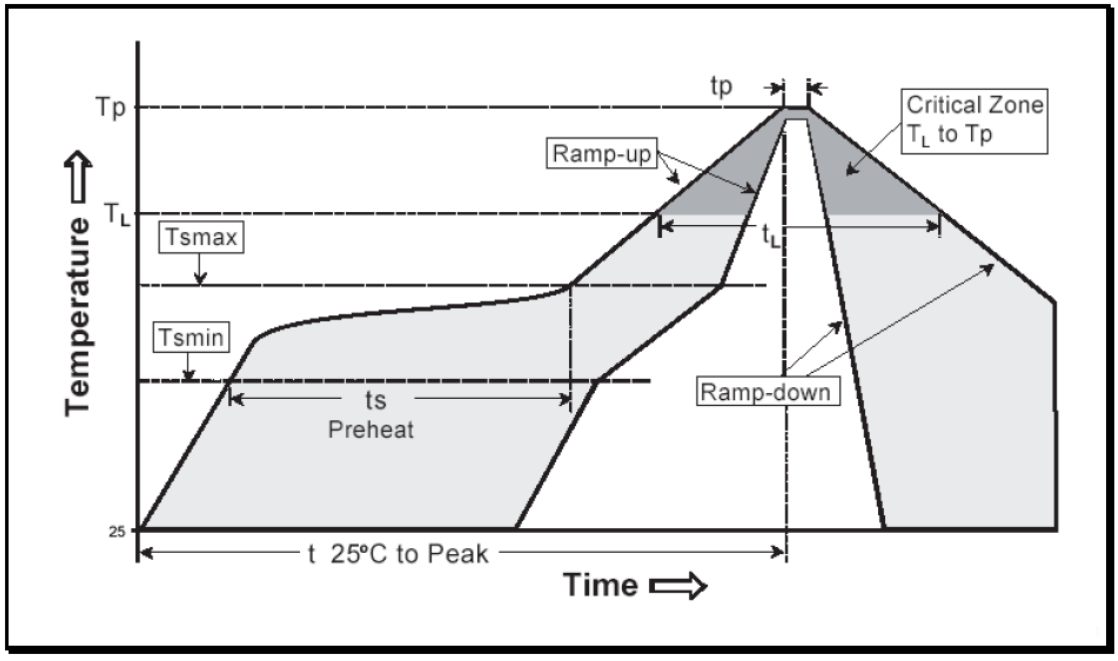
1320: date code

GK: internal code

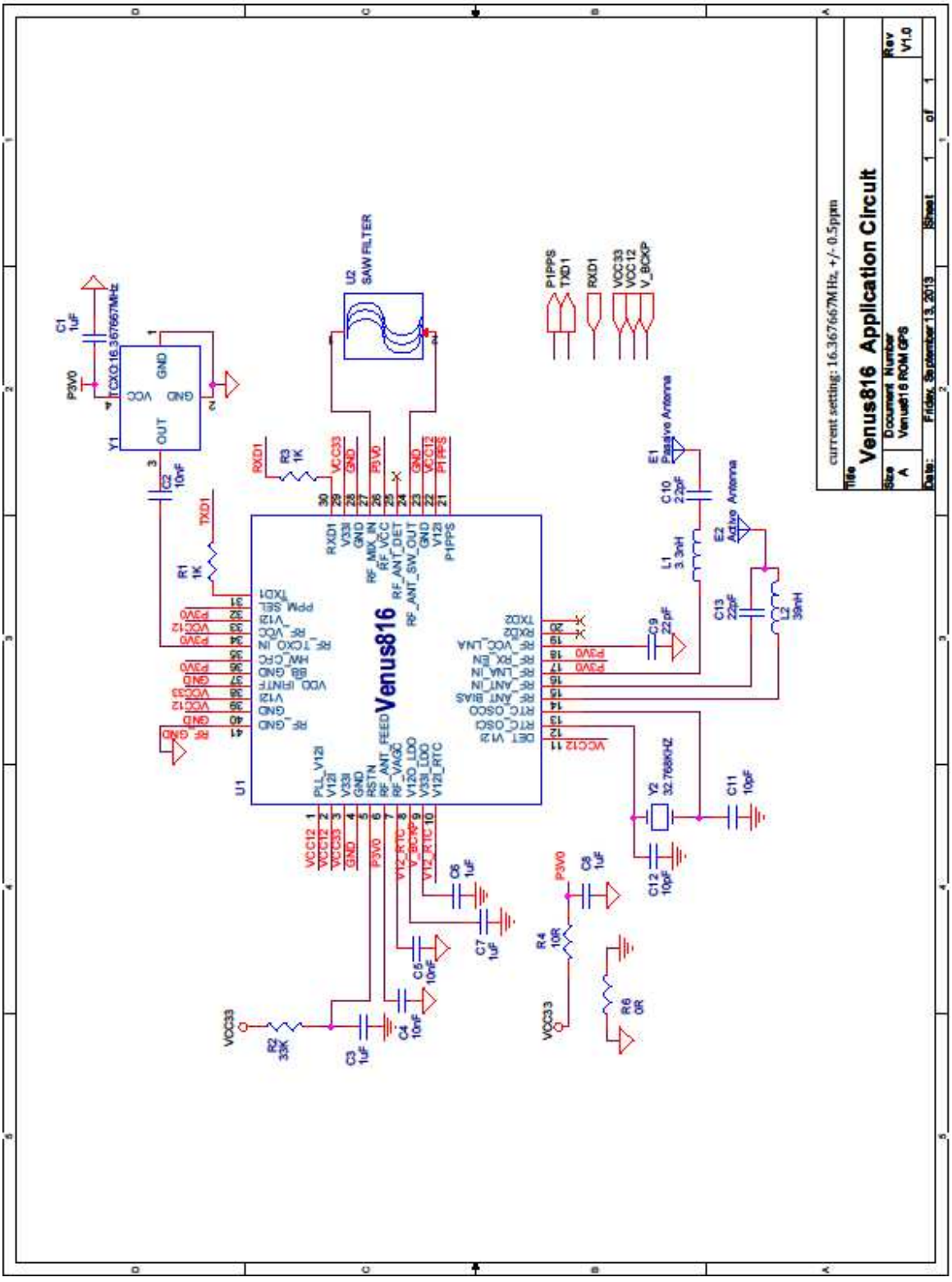
RECOMMANDED REFLOW TEMPERATURE PROFILE

Profile Feature	SnPb Eutectic Assembly	Lead (Pb) Free Assembly
Average Ramp-up Rate (T_L to T_P)	3°C/s (max)	3°C/s (max)
Preheat		
Temperature Min. (T_{smin})	100°C	150°C
Temperature Max. (T_{smax})	150°C	200°C
Time (Min. to Max) (t_s)	60 - 120s	60 - 80s
Ramp Up		
Tsmax to t_L	-	3°C/s (max)
Time 25°C to Peak Temperature	6 mins. (max)	8 mins. (max)
Reflow		
Temperature (t_L)	183°C	217°C
Time maintained above t_L	60 - 150s	60 - 150s
Peak Temperature (t_p)	240 ±5°C	260 +0/-5°C
Time Within 5°C of Actual Peak Temperature (t_p)	10 - 30s	20 - 40s
Ramp-Down		
Ramp-Down Rate	6°C/s (max)	6°C/s (max)

Reflow Profile (Reference JEDEC J-STD-020)



REFERENCE SCHEMATIC



Bill of Material

Item	Quantity	Reference	Part	Tolerance
1	5	C1, C3, C6, C7, C8	1uF capacitor	± 5%
2	3	C2, C4, C5	10nF capacitor	± 5%
3	1	C9, C10, C13	22pF capacitor	± 5%
4	2	C11, C12	10pF capacitor	± 5%
5	1	E1	GPS passive antenna	
6	1	E2	GPS active antenna	
7	1	L1	3.3nH inductor	± 3nH
8	1	L2	39nH inductor	± 5%
9	1	R1, R3	1K ohm resistor	± 5%
10	2	R2	33K ohm resistor	± 5%
11	1	R4	10 ohm resistor	± 5%
12	1	R6	0 ohm resistor	± 5%
13	1	U1	Venus816	
14	1	U2	GPS SAW filter	
15	1	Y1	+/-0.5ppm 16.367667MHz TCXO	
16	1	Y2	32.768kHz crystal	

ORDERING INFORMATION

Part Number	Description
Venus816	Venus8 Single Chip GPS Receiver, QFN40, ROM version

REVISION HISTORY

Revision	Date	Description
3.0	Oct 17, 2014	Update pin-8 V12O_LDO description
2.0	Oct 17, 2014	Update current consumption
1.0	Sep. 14, 2013	Initial release