



# STW12NK95Z

N-channel 950V - 0.69Ω - 10A - TO-247  
Zener - Protected SuperMESH™ PowerMOSFET

## General features

Type	V <sub>DSS</sub> (@T <sub>jmax</sub> )	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>w</sub>
STW12NK95Z	950 V	< 0.90Ω	10 A	230W

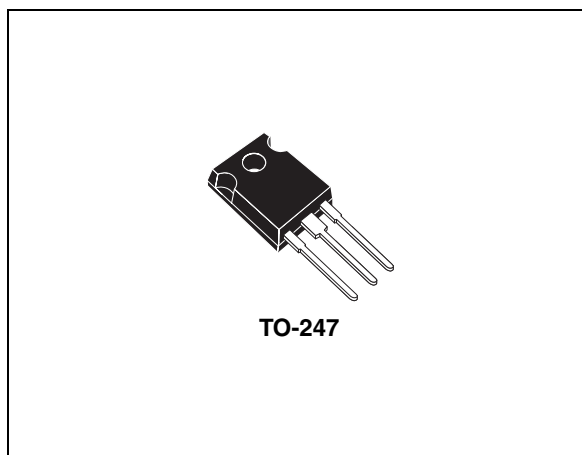
- Gate charge minimized
- 100% avalanche tested
- Extremely high dv/dt capability

## Description

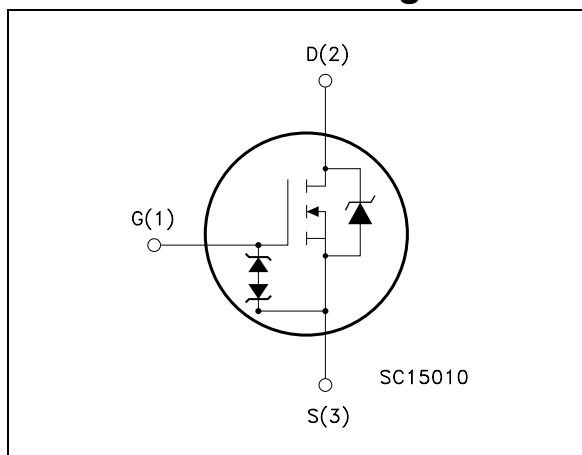
The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications.

## Applications

- Switching application



## Internal schematic diagram



## Order codes

Part number	Marking	Package	Packaging
STW12NK95Z	W12NK95Z	TO-247	Tube

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	950	V
$V_{DGR}$	Drain-gate voltage ( $R_{GS} = 20K\Omega$ )	950	V
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ C$	10	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ C$	6.3	A
$I_{DM}^{(1)}$	Drain current (pulsed)	40	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ C$	230	W
	Derating Factor	1.85	W/ $^\circ C$
$V_{ESD (G-S)}$	Gate source ESD (HBM-C=100pF, R=1,5K $\Omega$ )	6000	V
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^\circ C$

1. Pulse width limited by safe operating area

2.  $I_{SD} \leq 10A$ ,  $di/dt \leq 200A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq T_{JMAX}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case Max	0.54	$^\circ C/W$
$R_{thj-a}$	Thermal resistance junction-ambient Max	50	$^\circ C/W$
$T_l$	Maximum lead temperature for soldering purpose	300	$^\circ C$

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ Max)	10	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25^\circ C$ , $I_d = I_{AR}$ , $V_{dd} = 50V$ )	500	mJ

**Table 4. Gate-source zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}$	Gate-source breakdown voltage	$I_{gs}=\pm 1\text{mA}$ (Open Drain)	30			V

## 1.1 Protection features of gate-to-source zener diodes

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1mA, V_{GS} = 0$	950			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating},$ $T_c = 125^{\circ}C$			1 50	$\mu A$ $\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{GS} = 0$ )	$V_{GS} = \pm 20V$			$\pm 10$	$\mu A$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100\mu A$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 5 A$		0.69	0.9	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15V, I_D = 5A$		12		S
$C_{iss}$	Input capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		3500		pF
$C_{oss}$	Output capacitance			280		pF
$C_{rss}$	Reverse transfer capacitance			58		pF
$C_{osseq}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0V \text{ to } 760V$		117		pF
$Q_g$	Total gate charge	$V_{DD} = 760V, I_D = 10A$		113		nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 10V$		19	152	nC
$Q_{gd}$	Gate-drain charge	(see <a href="#">Figure 15</a> )		60		nC

1. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

2.  $C_{osseq}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 475V, I_D = 5A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see <a href="#">Figure 14</a> )		31		ns
$t_r$	Rise Time			20		ns
$t_{d(off)}$	Turn-off Delay Time	$V_{DD} = 475V, I_D = 5A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see <a href="#">Figure 14</a> )		88		ns
$t_f$	Fall Time			55		ns

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				10	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				40	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=8.3A, V_{GS}=0$			1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD}=10,$		728		ns
$Q_{rr}$	Reverse recovery charge	$di/dt = 100A/\mu s,$		78		$\mu C$
$I_{RRM}$	Reverse recovery current	$V_{DD}=50V, T_j=25^\circ C$		21.6		A
$t_{rr}$	Reverse recovery time	$I_{SD}=10A,$		964		ns
$Q_{rr}$	Reverse recovery charge	$di/dt = 100A/\mu s,$		11		$\mu C$
$I_{RRM}$	Reverse recovery current	$V_{DD}=50V, T_j=150^\circ C$		23		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

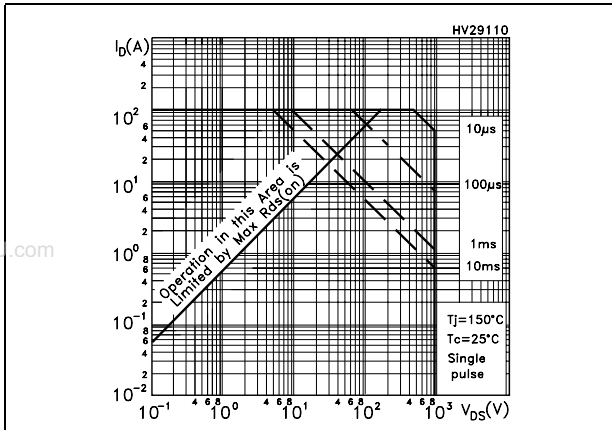


Figure 2. Thermal impedance

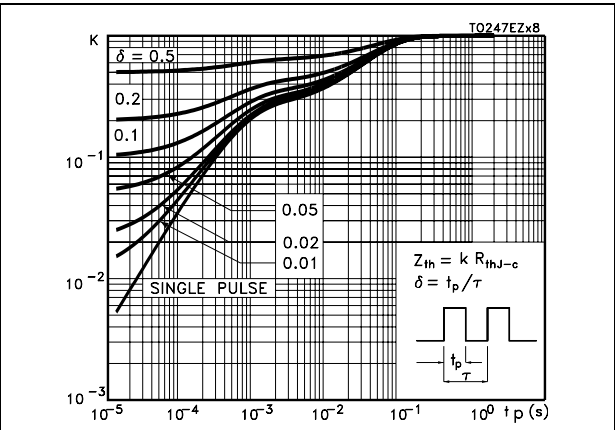


Figure 3. Output characteristics

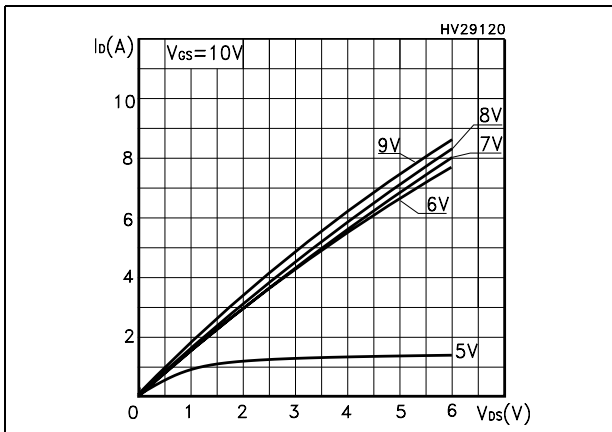


Figure 4. Transfer characteristics

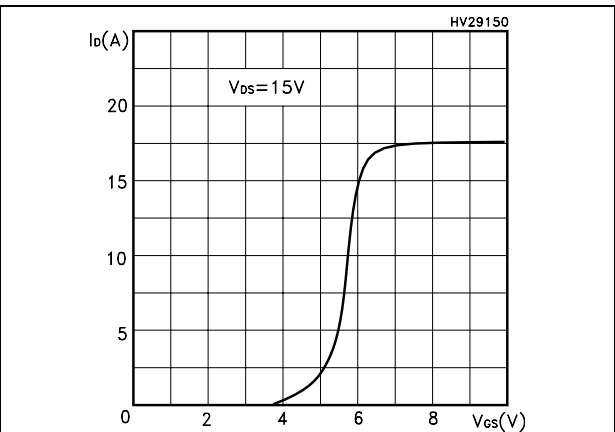


Figure 5. Transconductance

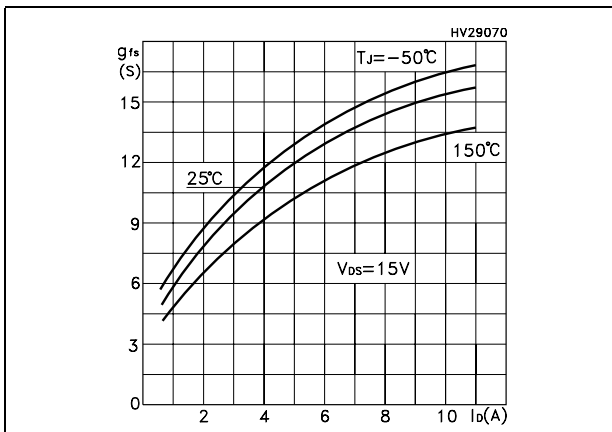


Figure 6. Static drain-source on resistance

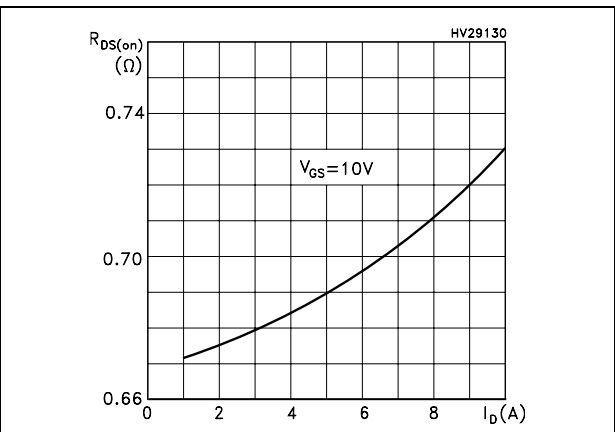


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

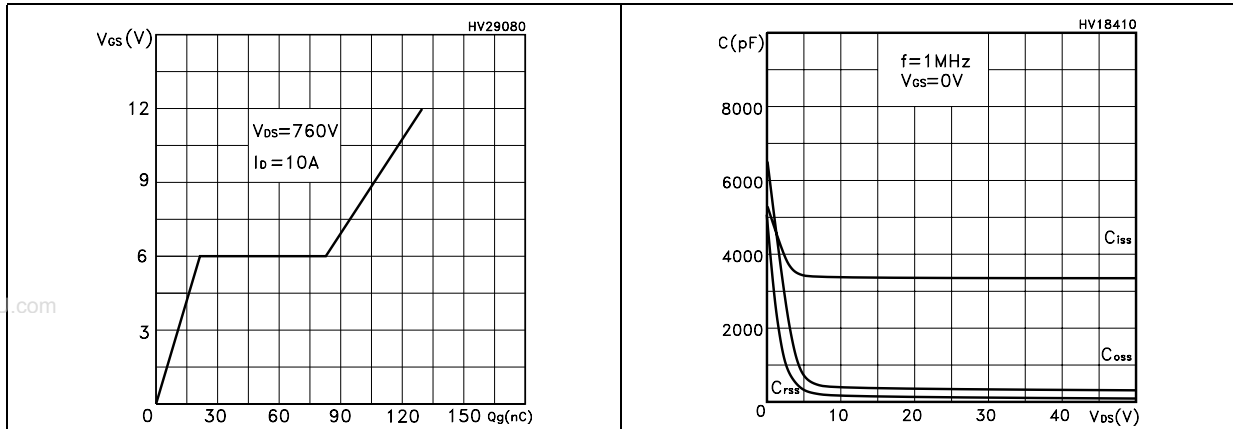


Figure 9. Normalized gate threshold voltage vs temperature

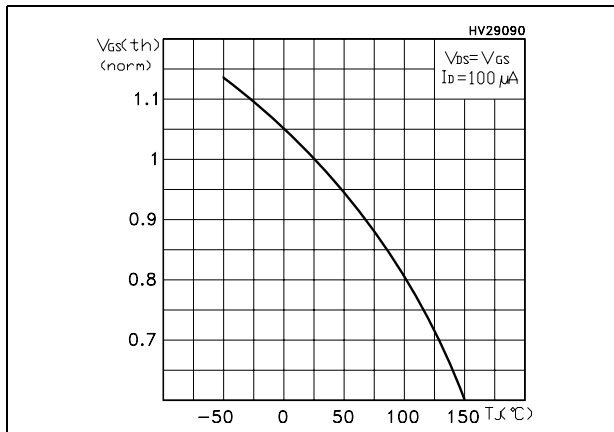


Figure 10. Normalized on resistance vs temperature

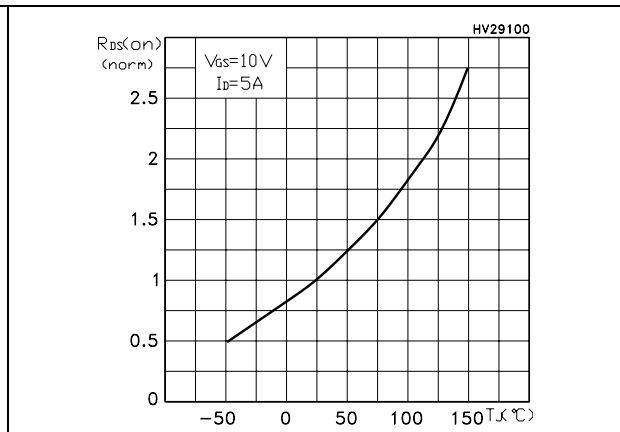


Figure 11. Source-drain diode forward characteristics

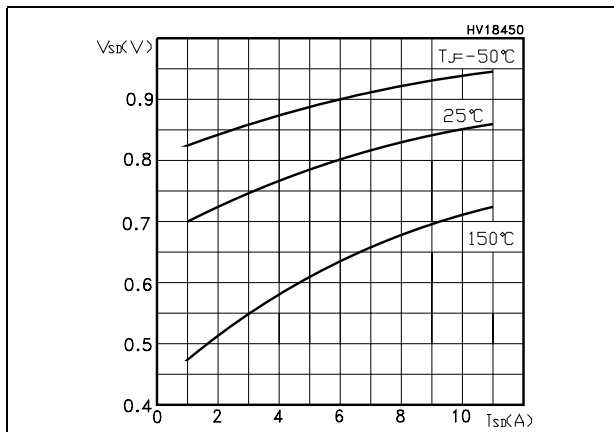


Figure 12. Normalized BV<sub>DSS</sub> vs temperature

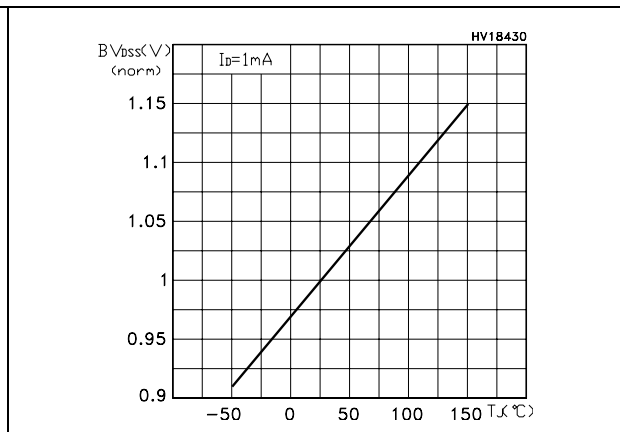
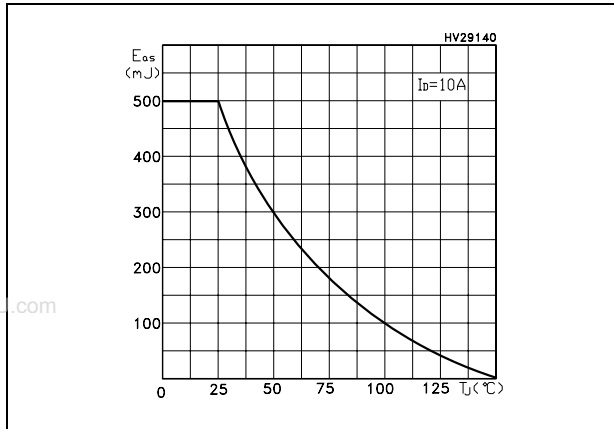




Figure 13. Maximum avalanche energy vs temperature



### 3 Test circuit

Figure 14. Switching times test circuit for resistive load

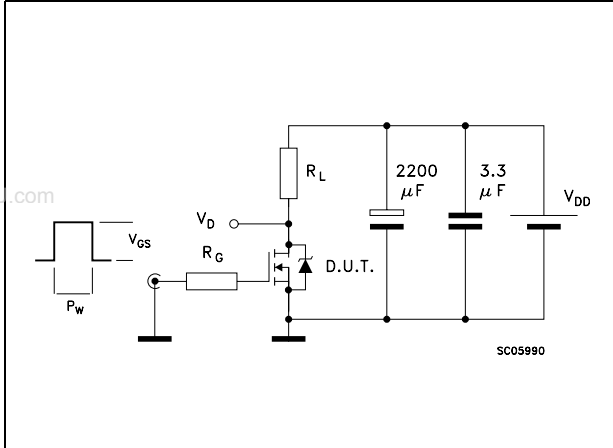


Figure 15. Gate charge test circuit

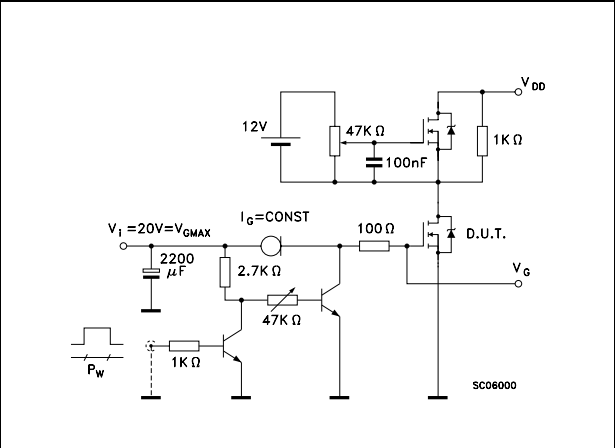


Figure 16. Test circuit for inductive load switching and diode recovery times

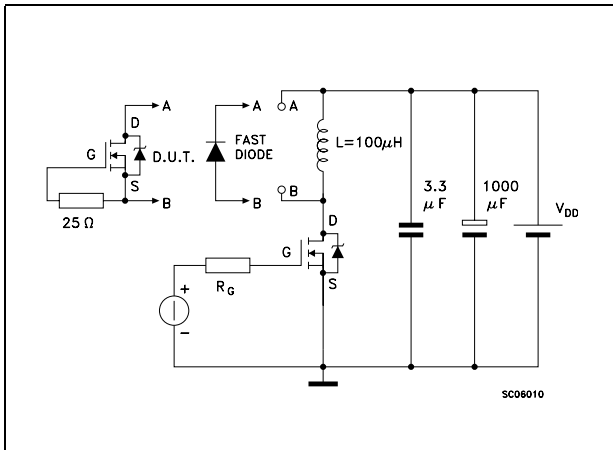


Figure 17. Unclamped Inductive load test circuit

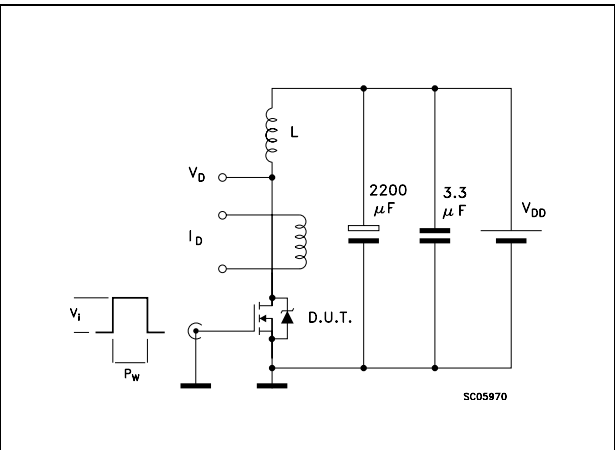


Figure 18. Unclamped inductive waveform

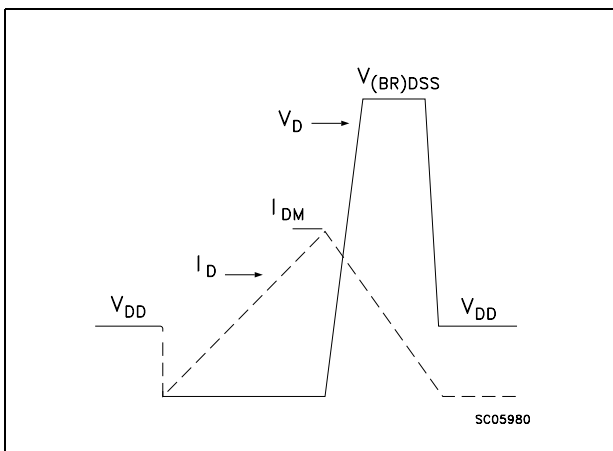
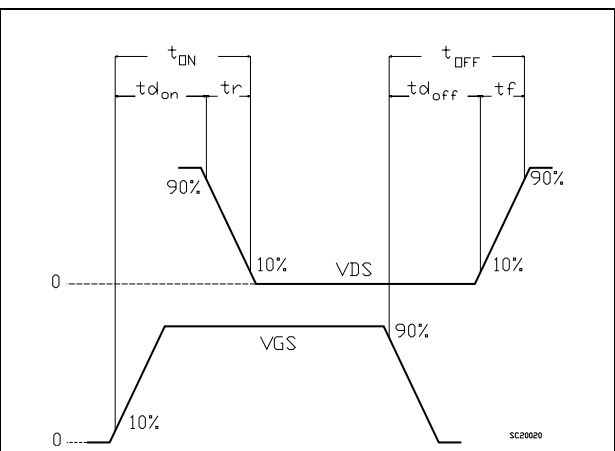


Figure 19. Switching time waveform

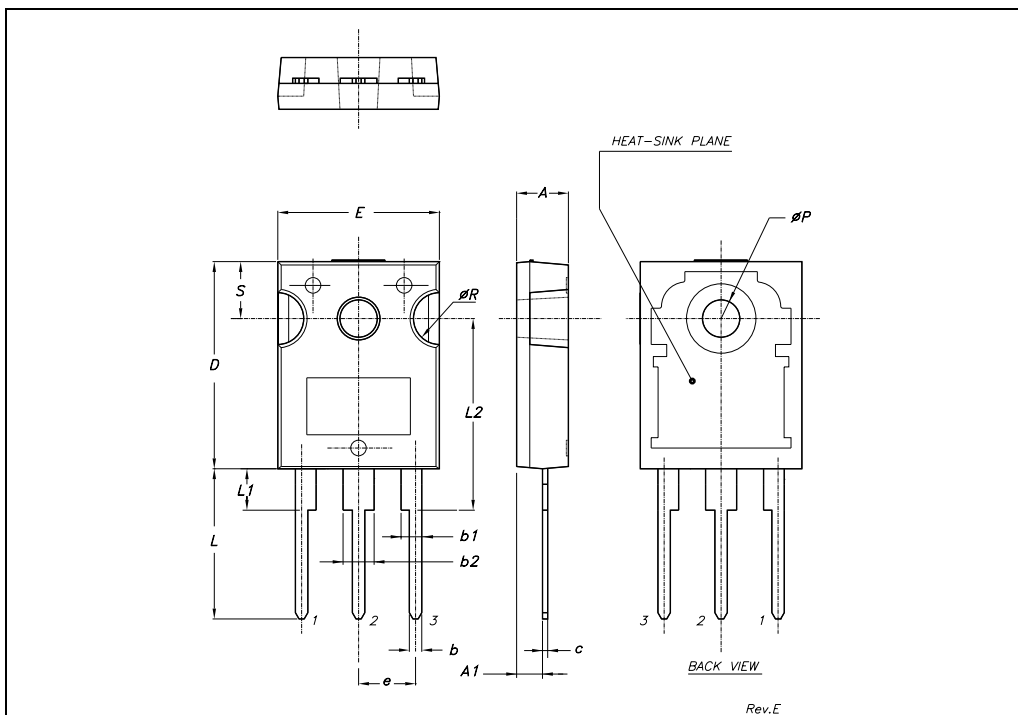


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



## 5 Revision history

**Table 9. Revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
16-Jan-2006	1	Initial release.
01-Aug-2006	2	New template, no content change

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