



440BX AGPset Spread Spectrum Frequency Synthesizer

Features

- Maximized EMI suppression using Cypress's Spread Spectrum Technology
- Single chip system frequency synthesizer for Intel® 440BX AGPset
- Two copies of CPU output
- Six copies of PCI output
- One 48-MHz output for USB
- One 24-MHz output for SIO
- Two buffered reference outputs
- One IOAPIC output
- Thirteen SDRAM outputs provide support for 3 DIMMs
- Spread Spectrum feature always enabled
- I²C™ interface for programming
- Power management control inputs
- Smooth CPU frequency switching from 66.8–124 MHz

Key Specifications

CPU Cycle-to-Cycle Jitter: 250 ps
 CPU to CPU Output Skew: 175 ps
 PCI to PCI Output Skew: 500 ps

V_{DDQ3}: 3.3V±5%
 V_{DDQ2}: 2.5V±5%
 SDRAMIN to SDRAM0:12 Delay: 3.7 ns typ.

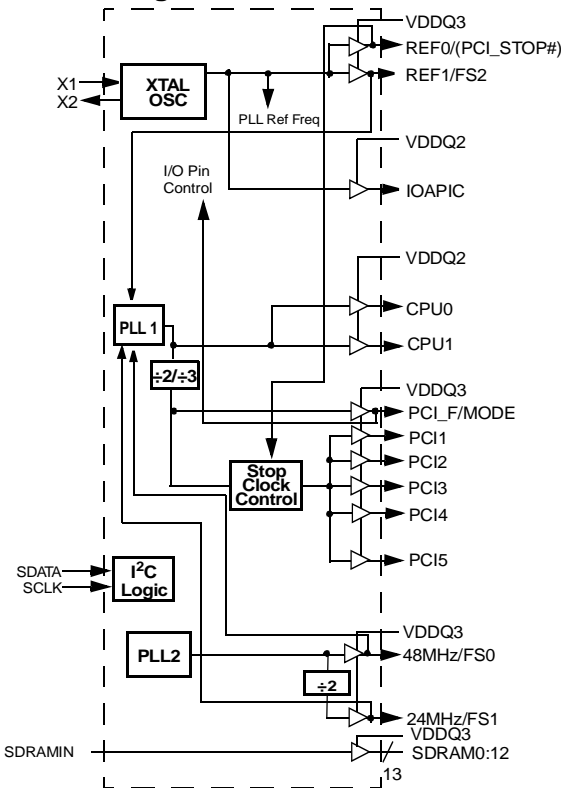
Table 1. Mode Input Table^[1]

| Mode | Pin 2 |
|------|-----------|
| 0 | PCI_STOP# |
| 1 | REF0 |

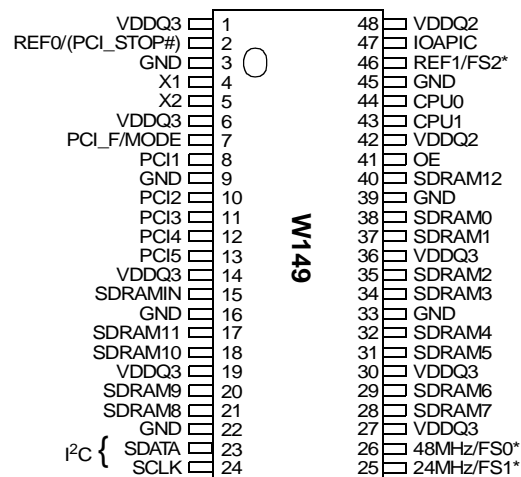
Table 2. Pin Selectable Frequency

| Input Address | | | CPU0:1 (MHz) | PCI_F, 1:5 (MHz) | Spread % |
|---------------|-----|-----|--------------|------------------|----------|
| FS2 | FS1 | FS0 | | | |
| 1 | 1 | 1 | 100 | 33.3 (CPU/3) | -0.5 |
| 1 | 1 | 0 | (Reserved) | | |
| 1 | 0 | 1 | 100 | 33.3 (CPU/3) | ±0.5 |
| 1 | 0 | 0 | 103 | 34.3 (CPU/3) | -0.5 |
| 0 | 1 | 1 | 66.8 | 33.4 (CPU/2) | -0.5 |
| 0 | 1 | 0 | 83.3 | 41.7 (CPU/2) | -0.5 |
| 0 | 0 | 1 | 66.8 | 33.4 (CPU/2) | ±0.5 |
| 0 | 0 | 0 | 124 | 41.3 (CPU/3) | -0.5 |

Logic Block Diagram



Pin Configuration^[2]



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Notes:

1. Mode input latched at power-up.
2. Internal pull up resistors(*) should not be relied upon for setting I/O pins HIGH. Pin function with parentheses determined by MODE pin resistor strapping.

Pin Definitions

| Pin Name | Pin No. | Pin Type | Pin Description |
|----------------------|---|----------|---|
| CPU0:1 | 44, 43 | O | CPU Clock Outputs: See <i>Tables 2 and 6</i> for detailed frequency information. Output voltage swing is controlled by voltage applied to VDDQ2. |
| PCI1:5 | 8, 10, 11, 12, 13 | O | PCI Clock Outputs 1 through 5: These five PCI clock outputs are controlled by the PCI_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ3. |
| PCI_F/MODE | 7 | I/O | Fixed PCI Clock Output: Frequency is set by the FS0:1 inputs or through serial input interface, see <i>Tables 2 and 6</i> . This output is not affected by the PCI_STOP# input. Upon power-up the mode input will be latched, which will determine the function of pin 2, REF0/(PCI_STOP#). See <i>Table 1</i> . |
| OE | 41 | I | Output Enable Input: When brought LOW, all outputs are placed in a high-impedance state. When brought HIGH, all clock outputs activate. |
| IOAPIC | 47 | O | IOAPIC Clock Output: Provides 14.318-MHz fixed frequency. The output voltage swing is controlled by VDDQ2. |
| 48MHz/FS0 | 26 | I/O | 48-MHz Output: 48 MHz is provided in normal operation. In standard systems, this output can be used as the reference for the Universal Serial Bus. Upon power-up, FS0 input will be latched, which will set clock frequencies as described in <i>Table 2</i> . This output does not have the Spread Spectrum feature. |
| 24MHz/FS1 | 25 | I/O | 24-MHz Output: 24 MHz is provided in normal operation. In standard systems, this output can be used as the clock input for a Super I/O chip. Upon power-up FS1 input will be latched, which will set clock frequencies as described in <i>Table 2</i> . This output does not have the Spread Spectrum feature. |
| REF1/FS2 | 46 | I/O | I/O Dual-Function REF1 and FS2 pin: Upon power-up, FS2 input will be latched which will set clock frequencies as described in <i>Table 2</i> . When an output, this pin provides a fixed clock signal equal in frequency to the reference signal provided at the X1/X2 pins. |
| REF0/ (PCI_STOP#) | 2 | I/O | Fixed 14.318-MHz Output 0 or PCI_STOP# Pin: Function is determined by the MODE input. When set as an input, the PCI_STOP# input enables the PCI 1:5 outputs when HIGH and causes them to remain at logic 0 when LOW. The PCI_STOP signal is latched on the rising edge of PCI_F. Its effects take place on the next PCI_F clock cycle. When an output, this pin provides a fixed clock signal equal in frequency to the reference signal provided at the X1/X2 pins. |
| SDRAMIN | 15 | I | Buffered Input Pin: The signal provided to this input pin is buffered to 13 outputs (SDRAM0:12). |
| SDRAM0:12 | 38, 37, 35, 34, 32, 31, 29, 28, 21, 20, 18, 17, 40 | O | Buffered Outputs: These thirteen dedicated outputs provide copies of the signal provided at the SDRAMIN input. The swing is set by VDDQ3, and they are deactivated when CLK_STOP# input is set LOW. |
| SCLK | 24 | I | Clock pin for I ² C circuitry. |
| SDATA | 23 | I/O | Data pin for I ² C circuitry. |
| X1 | 4 | I | Crystal Connection or External Reference Frequency Input: This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input. |
| X2 | 5 | I | Crystal Connection: An input connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected. |
| VDDQ3 | 1, 6, 14, 19, 27, 30, 36 | P | Power Connection: Power supply for core logic, PLL circuitry, SDRAM outputs, PCI outputs, reference outputs, 48-MHz output, and 24-MHz output. Connect to 3.3V supply. |
| VDDQ2 | 42, 48 | P | Power Connection: Power supply for IOAPIC and CPU0:1 output buffers. Connect to 2.5V, or 3.3V. |
| GND | 3, 9, 16, 22, 33, 39, 45 | G | Ground Connections: Connect all ground pins to the common system ground plane. |

Overview

The W149 was developed as a single chip device to meet the clocking needs of the Intel 440BX AGPset. In addition to the typical outputs provided by standard 100-MHz 440BX AGPset FTGs, the W149 adds a thirteen output buffer, supporting SDRAM DIMM modules in conjunction with the chipset.

Cypress proprietary spread spectrum frequency synthesis technique is a feature of the CPU and PCI outputs. This feature reduces the peak EMI measurements of not only the output signals and their harmonics, but also of any other clock signals that are properly synchronized to them.

Functional Description

I/O Pin Operation

Pins 7, 25, 26, 46 are dual-purpose I/O pins. Upon power-up these pins act as logic inputs, allowing the determination of assigned device functions. A short time after power-up, the logic state of each pin is latched and the pins become clock outputs. This feature reduces device pin count by combining clock outputs with input select pins.

An external 10-k Ω "strapping" resistor is connected between the I/O pin and ground or V_{DD} . Connection to ground sets a latch to "0", connection to V_{DD} sets a latch to "1". *Figure 1* and *Figure 2* show two suggested methods for strapping resistor connections.

Upon W149 power-up, the first 2 ms of operation is used for input logic selection. During this period, the four I/O pins (7, 25, 26, 46) are three-stated, allowing the output strapping resistor on the I/O pins to pull each pin and its associated capacitive clock load to either a logic HIGH or LOW state. At the end of the 2-ms period, the established logic "0" or "1" condition of the I/O pin is latched. Next the output buffer is enabled, converting the I/O pins into operating clock outputs. The 2-ms timer starts when V_{DD} reaches 2.0V. The input bits can only be reset by turning V_{DD} off and then back on again.

It should be noted that the strapping resistors have no significant effect on clock output signal integrity. The drive impedance of clock output is $<40\Omega$ (nominal), which is minimally affected by the 10-k Ω strap to ground or V_{DD} . As with the series termination resistor, the output strapping resistor should be placed as close to the I/O pin as possible in order to keep the interconnecting trace short. The trace from the resistor to ground or V_{DD} should be kept less than two inches in length to prevent system noise coupling during input logic sampling.

When the clock outputs are enabled following the 2-ms input period, the specified output frequency is delivered on the pin, assuming that V_{DD} has stabilized. If V_{DD} has not yet reached full value, output frequency initially may be below target but will increase to target once V_{DD} voltage has stabilized. In either case, a short output clock cycle may be produced from the CPU clock outputs when the outputs are enabled.

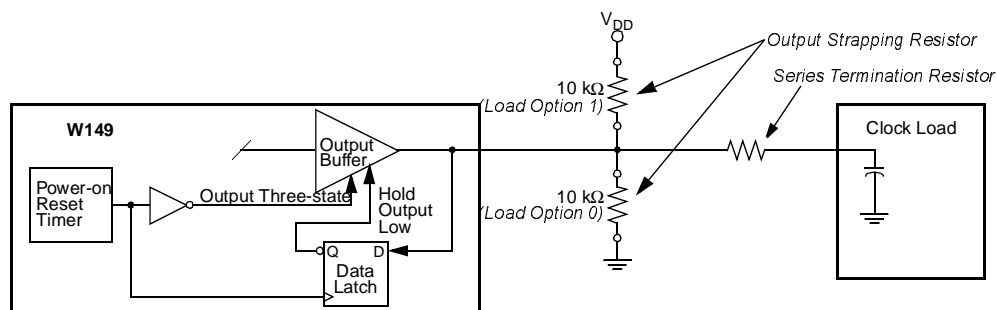


Figure 1. Input Logic Selection Through Resistor Load Option

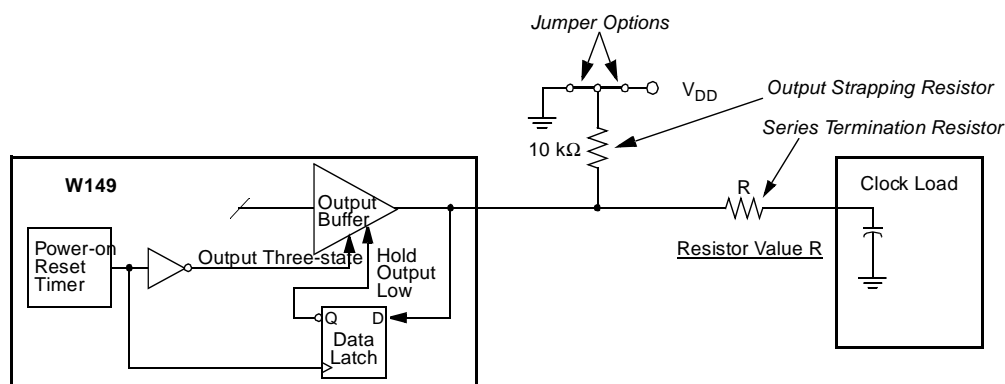


Figure 2. Input Logic Selection Through Jumper Option

Spread Spectrum Clocking

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 3*.

As shown in *Figure 3*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is:

$$dB = 6.5 + 9 \cdot \log_{10}(P) + 9 \cdot \log_{10}(F)$$

Where *P* is the percentage of deviation and *F* is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 4*. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is either -0.5% or $\pm 0.5\%$ of the selected frequency. *Figure 4* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

Spread Spectrum clocking cannot be deactivated on the W149.

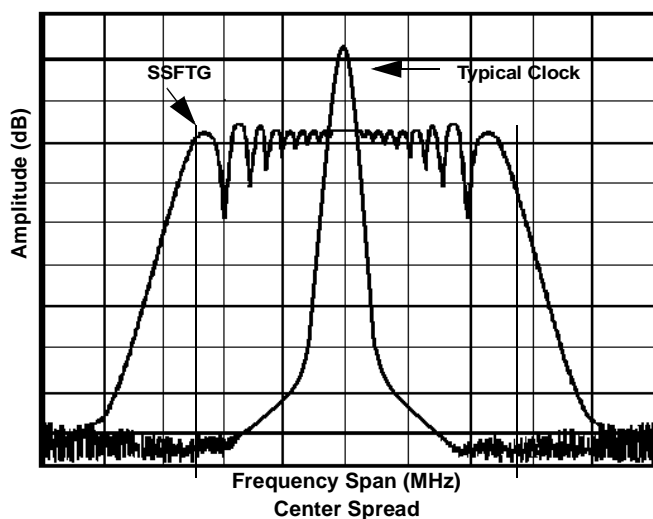


Figure 3. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation

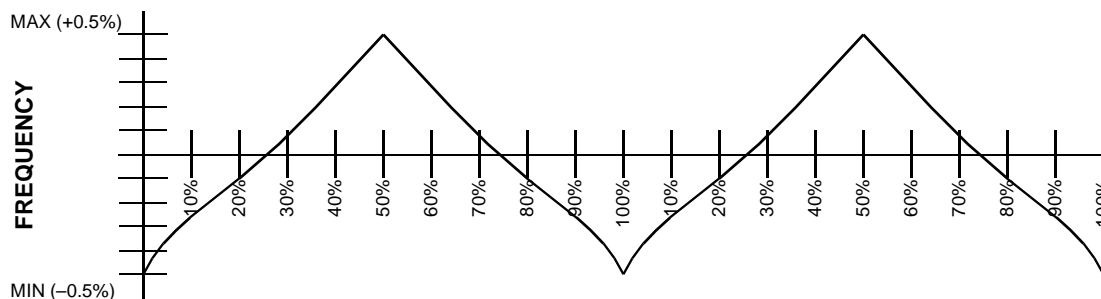


Figure 4. Typical Modulation Profile

Serial Data Interface

The W149 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the W149 initializes with default register settings, therefore the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDATA and SCLOCK. In motherboard applications, SDATA and SCLOCK are typically driven by two logic outputs of the

chipset. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions. *Table 3* summarizes the control functions of the serial data interface.

Operation

Data is written to the W149 in eleven bytes of eight bits each. Bytes are written in the order shown in *Table 4*.

Table 3. Serial Data Interface Control Functions Summary

| Control Function | Description | Common Application |
|-------------------------------|--|--|
| Clock Output Disable | Any individual clock output(s) can be disabled. Disabled outputs are actively held LOW. | Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused PCI slots. |
| CPU Clock Frequency Selection | Provides CPU/PCI frequency selections through software. Frequency is changed in a smooth and controlled fashion. | For alternate microprocessors and power management options. Smooth frequency transition allows CPU frequency change under normal system operation. |
| Output Three-state | Puts clock output into a high-impedance state. | Production PCB testing. |
| (Reserved) | Reserved function for future device revision or production device testing. | No user application. Register bit must be written as 0. |

Table 4. Byte Writing Sequence

| Byte Sequence | Byte Name | Bit Sequence | Byte Description |
|---------------|---------------|-------------------------|---|
| 1 | Slave Address | 11010010 | Commands the W149 to accept the bits in Data Bytes 0–6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the W149 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver). |
| 2 | Command Code | Don't Care | Unused by the W149, therefore bit values are ignored ("Don't Care"). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus. |
| 3 | Byte Count | Don't Care | Unused by the W149, therefore bit values are ignored ("Don't Care"). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus. |
| 4 | Data Byte 0 | Refer to <i>Table 5</i> | The data bits in Data Bytes 0–7 set internal W149 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to <i>Table 5</i> , Data Byte Serial Configuration Map. |
| 5 | Data Byte 1 | | |
| 6 | Data Byte 2 | | |
| 7 | Data Byte 3 | | |
| 8 | Data Byte 4 | | |
| 9 | Data Byte 5 | | |
| 10 | Data Byte 6 | | |
| 11 | Data Byte 7 | | |

Writing Data Bytes

Each bit in Data Bytes 0–7 control a particular device function except for the “reserved” bits which must be written as a logic 0. Bits are written MSB (most significant bit) first, which is bit 7. *Table 5* gives the bit formats for registers located in Data Bytes 0–7.

Table 6 details additional frequency selections that are available through the serial data interface.

Table 7 details the select functions for Byte 0, bits 1 and 0.

Table 5. Data Bytes 0–7 Serial Configuration Map

| Bit(s) | Affected Pin | | Control Function | Bit Control | | Default | | | | | | | | | | | | | | | |
|--------------------|----------------|---|---|--------------------|--------------|---|---|---|------------------|---|---|------------|---|---|------------------|---|---|--------------------------|--|--|----|
| | Pin No. | Pin Name | | 0 | 1 | | | | | | | | | | | | | | | | |
| Data Byte 0 | | | | | | | | | | | | | | | | | | | | | |
| 7 | -- | -- | Don't Care | -- | -- | 0 | | | | | | | | | | | | | | | |
| 6 | -- | -- | SEL_2 | See <i>Table 6</i> | | 0 | | | | | | | | | | | | | | | |
| 5 | -- | -- | SEL_1 | See <i>Table 6</i> | | 0 | | | | | | | | | | | | | | | |
| 4 | -- | -- | SEL_0 | See <i>Table 6</i> | | 0 | | | | | | | | | | | | | | | |
| 3 | -- | -- | Hardware/Software Frequency Select | Hardware | Software | 0 | | | | | | | | | | | | | | | |
| 2 | -- | -- | Don't Care | -- | -- | 0 | | | | | | | | | | | | | | | |
| 1–0 | -- | -- | <table border="0"> <tr> <td>Bit 1</td> <td>Bit 0</td> <td>Function (See <i>Table 7</i> for function details)</td> </tr> <tr> <td>0</td> <td>0</td> <td>Normal Operation</td> </tr> <tr> <td>0</td> <td>1</td> <td>(Reserved)</td> </tr> <tr> <td>1</td> <td>0</td> <td>Normal Operation</td> </tr> <tr> <td>1</td> <td>1</td> <td>All Outputs Three-stated</td> </tr> </table> | Bit 1 | Bit 0 | Function (See <i>Table 7</i> for function details) | 0 | 0 | Normal Operation | 0 | 1 | (Reserved) | 1 | 0 | Normal Operation | 1 | 1 | All Outputs Three-stated | | | 00 |
| Bit 1 | Bit 0 | Function (See <i>Table 7</i> for function details) | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | Normal Operation | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | (Reserved) | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | Normal Operation | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | All Outputs Three-stated | | | | | | | | | | | | | | | | | | | |
| Data Byte 1 | | | | | | | | | | | | | | | | | | | | | |
| 7 | -- | -- | (Reserved) | -- | -- | 0 | | | | | | | | | | | | | | | |
| 6 | -- | -- | (Reserved) | -- | -- | 0 | | | | | | | | | | | | | | | |
| 5 | -- | -- | (Reserved) | -- | -- | 0 | | | | | | | | | | | | | | | |
| 4 | -- | -- | (Reserved) | -- | -- | 0 | | | | | | | | | | | | | | | |
| 3 | 40 | SDRAM12 | Clock Output Disable | Low | Active | 1 | | | | | | | | | | | | | | | |
| 2 | -- | -- | (Reserved) | -- | -- | 0 | | | | | | | | | | | | | | | |
| 1 | 43 | CPU1 | Clock Output Disable | Low | Active | 1 | | | | | | | | | | | | | | | |
| 0 | 44 | CPU0 | Clock Output Disable | Low | Active | 1 | | | | | | | | | | | | | | | |
| Data Byte 2 | | | | | | | | | | | | | | | | | | | | | |
| 7 | -- | -- | (Reserved) | -- | -- | 0 | | | | | | | | | | | | | | | |
| 6 | 7 | PCI_F | Clock Output Disable | Low | Active | 1 | | | | | | | | | | | | | | | |
| 5 | -- | -- | (Reserved) | -- | -- | 0 | | | | | | | | | | | | | | | |
| 4 | 13 | PCI5 | Clock Output Disable | Low | Active | 1 | | | | | | | | | | | | | | | |
| 3 | 12 | PCI4 | Clock Output Disable | Low | Active | 1 | | | | | | | | | | | | | | | |
| 2 | 11 | PCI3 | Clock Output Disable | Low | Active | 1 | | | | | | | | | | | | | | | |
| 1 | 10 | PCI2 | Clock Output Disable | Low | Active | 1 | | | | | | | | | | | | | | | |
| 0 | 8 | PCI1 | Clock Output Disable | Low | Active | 1 | | | | | | | | | | | | | | | |
| Data Byte 3 | | | | | | | | | | | | | | | | | | | | | |
| 7 | -- | -- | (Reserved) | -- | -- | 0 | | | | | | | | | | | | | | | |
| 6 | -- | -- | (Reserved) | -- | -- | 0 | | | | | | | | | | | | | | | |
| 5 | 26 | 48MHz | Clock Output Disable | Low | Active | 1 | | | | | | | | | | | | | | | |
| 4 | 25 | 24MHz | Clock Output Disable | Low | Active | 1 | | | | | | | | | | | | | | | |
| 3 | -- | -- | (Reserved) | -- | -- | 0 | | | | | | | | | | | | | | | |
| 2 | 21, 20, 18, 17 | SDRAM8:11 | Clock Output Disable | Low | Active | 1 | | | | | | | | | | | | | | | |

Table 5. Data Bytes 0–7 Serial Configuration Map (continued)

| Bit(s) | Affected Pin | | Control Function | Bit Control | | Default |
|--------------------|-------------------|----------|----------------------|-------------|--------|---------|
| | Pin No. | Pin Name | | 0 | 1 | |
| 1 | 32, 31, 29, 28 | SDRAM4:7 | Clock Output Disable | Low | Active | 1 |
| 0 | 38, 37, 35, 34 | SDRAM0:3 | Clock Output Disable | Low | Active | 1 |
| Data Byte 4 | | | | | | |
| 7 | -- | -- | (Reserved) | -- | -- | 0 |
| 6 | -- | -- | (Reserved) | -- | -- | 0 |
| 5 | -- | -- | (Reserved) | -- | -- | 0 |
| 4 | -- | -- | (Reserved) | -- | -- | 0 |
| 3 | -- | -- | (Reserved) | -- | -- | 0 |
| 2 | -- | -- | (Reserved) | -- | -- | 0 |
| 1 | -- | -- | (Reserved) | -- | -- | 0 |
| 0 | -- | -- | (Reserved) | -- | -- | 0 |
| Data Byte 5 | | | | | | |
| 7 | -- | -- | (Reserved) | -- | -- | 0 |
| 6 | -- | -- | (Reserved) | -- | -- | 0 |
| 5 | -- | -- | (Reserved) | -- | -- | 0 |
| 4 | 47 | IOAPIC | Clock Output Disable | Low | Active | 1 |
| 3 | -- | -- | (Reserved) | -- | -- | 0 |
| 2 | -- | -- | (Reserved) | -- | -- | 0 |
| 1 | 46 | REF1 | Clock Output Disable | Low | Active | 1 |
| 0 | 2 | REF0 | Clock Output Disable | Low | Active | 1 |
| Data Byte 6 | | | | | | |
| 7 | -- | -- | (Reserved) | -- | -- | 0 |
| 6 | -- | -- | (Reserved) | -- | -- | 0 |
| 5 | -- | -- | (Reserved) | -- | -- | 0 |
| 4 | -- | -- | (Reserved) | -- | -- | 0 |
| 3 | -- | -- | (Reserved) | -- | -- | 0 |
| 2 | -- | -- | (Reserved) | -- | -- | 0 |
| 1 | -- | -- | (Reserved) | -- | -- | 0 |
| 0 | -- | -- | (Reserved) | -- | -- | 0 |
| Data Byte 7 | | | | | | |
| 7 | -- | -- | (Reserved) | -- | -- | 0 |
| 6 | -- | -- | (Reserved) | -- | -- | 0 |
| 5 | -- | -- | (Reserved) | -- | -- | 0 |
| 4 | -- | -- | (Reserved) | -- | -- | 0 |
| 3 | -- | -- | (Reserved) | -- | -- | 0 |
| 2 | -- | -- | (Reserved) | -- | -- | 0 |
| 1 | -- | -- | (Reserved) | -- | -- | 0 |
| 0 | -- | -- | (Reserved) | -- | -- | 0 |

Table 6. Additional Frequency Selections through Serial Data Interface Data Bytes^[3]

| Input Conditions | | | Output Frequency | | Spread % |
|------------------------|----------------|----------------|----------------------------|---------------------|------------|
| Data Byte 0, Bit 3 = 1 | | | CPU0:1, SDRAM0:12 (MHz) | PCI_F, 1:5 (MHz) | |
| Bit 6 SEL_2 | Bit 5 SEL_1 | Bit 4 SEL_0 | | | |
| 1 | 1 | 1 | 100.2 | 33.4 | -0.5 |
| 1 | 1 | 0 | (Reserved) | (Reserved) | (Reserved) |
| 1 | 0 | 1 | 100 | 33.3 | ±0.5 |
| 1 | 0 | 0 | 103 | 34.3 | -0.5 |
| 0 | 1 | 1 | 66.8 | 33.4 | -0.5 |
| 0 | 1 | 0 | 83.3 | 41.65 | -0.5 |
| 0 | 0 | 1 | 66.8 | 33.4 | ±0.5 |
| 0 | 0 | 0 | 124 | 41.3 | -0.5 |

Table 7. Select Function for Data Byte 0, Bits 0:1

| Function | Input Conditions | | Output Conditions | | | | |
|------------------|------------------|-------|-------------------|------------------|-------------------|--------|--------|
| | Data Byte 0 | | CPU0:1 | PCI_F, PCI1:5 | REF0:1, IOAPIC | 48MHZ | 24MHZ |
| | Bit 1 | Bit 0 | | | | | |
| Normal Operation | X | 0 | Note 1 | Note 1 | 14.318 MHz | 48 MHz | 24 MHz |
| Three-state | 1 | 1 | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z |

Note:

3. CPU and PCI frequency selections are listed in *Table 2* and *Table 6*.

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions

above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

| Parameter | Description | Rating | Unit |
|------------------|--|--------------|------|
| V_{DD}, V_{IN} | Voltage on any pin with respect to GND | -0.5 to +7.0 | V |
| T_{STG} | Storage Temperature | -65 to +150 | °C |
| T_B | Ambient Temperature under Bias | -55 to +125 | °C |
| T_A | Operating Temperature | 0 to +70 | °C |
| ESD_{PROT} | Input ESD Protection | 2 (min) | kV |

DC Electrical Characteristics: $T_A = 0^\circ\text{C to } +70^\circ\text{C}; V_{DDQ3} = 3.3\text{V}\pm 5\%; V_{DDQ2} = 2.5\text{V}\pm 5\%$

| Parameter | Description | Test Condition | Min. | Typ. | Max. | Unit | |
|-----------------------|-----------------------------------|---|-------------------------|------|----------------|------|----|
| Supply Current | | | | | | | |
| I_{DD} | 3.3V Supply Current | CPU0:1 = 100 MHz Outputs Loaded ^[4] | | 260 | | mA | |
| I_{DD} | 2.5V Supply Current | CPU0:1 = 100 MHz Outputs Loaded ^[4] | | 25 | | mA | |
| Logic Inputs | | | | | | | |
| V_{IL} | Input Low Voltage | | GND - 0.3 | | 0.8 | V | |
| V_{IH} | Input High Voltage | | 2.0 | | $V_{DD} + 0.3$ | V | |
| I_{IL} | Input Low Current ^[5] | | | | -25 | μA | |
| I_{IH} | Input High Current ^[5] | | | | 10 | μA | |
| Clock Outputs | | | | | | | |
| V_{OL} | Output Low Voltage | | $I_{OL} = 1\text{ mA}$ | | 50 | mV | |
| V_{OH} | Output High Voltage | | $I_{OH} = 1\text{ mA}$ | 3.1 | | V | |
| V_{OH} | Output High Voltage | CPU0:1, IOAPIC | $I_{OH} = -1\text{ mA}$ | 2.2 | | V | |
| I_{OL} | Output Low Current | CPU0:1 | $V_{OL} = 1.25\text{V}$ | 27 | 57 | 97 | mA |
| | | PCI_F, PCI1:5 | $V_{OL} = 1.5\text{V}$ | 20.5 | 53 | 139 | mA |
| | | IOAPIC | $V_{OL} = 1.25\text{V}$ | 40 | 85 | 140 | mA |
| | | REF0:1 | $V_{OL} = 1.5\text{V}$ | 25 | 37 | 76 | mA |
| | | 48MHz 24MHz | $V_{OL} = 1.5\text{V}$ | 25 | 37 | 76 | mA |
| I_{OH} | Output High Current | CPU0:1 | $V_{OH} = 1.25\text{V}$ | 25 | 55 | 97 | mA |
| I_{OH} | Output High Current | PCI_F, PCI1:5 | $V_{OH} = 1.5\text{V}$ | 31 | 55 | 139 | mA |
| | | IOAPIC | $V_{OH} = 1.25\text{V}$ | 40 | 87 | 155 | mA |
| | | REF0:1 | $V_{OH} = 1.5\text{V}$ | 27 | 44 | 94 | mA |
| | | 48MHz 24MHz | $V_{OH} = 1.5\text{V}$ | 27 | 44 | 94 | mA |
| | | | | 25 | 37 | 76 | mA |

Notes:

- All clock outputs loaded with 6" 60Ω traces with 22-pF capacitors.
- W149 logic inputs have internal pull-up devices (pull-ups not full CMOS level).

DC Electrical Characteristics: (continued) $T_A = 0^\circ\text{C to } +70^\circ\text{C}$; $V_{DDQ3} = 3.3\text{V}\pm 5\%$; $V_{DDQ2} = 2.5\text{V}\pm 5\%$

| Parameter | Description | Test Condition | Min. | Typ. | Max. | Unit |
|-----------------------------------|--|--------------------------|------|------|------|------|
| Crystal Oscillator | | | | | | |
| V_{TH} | X1 Input threshold Voltage ^[6] | $V_{DDQ3} = 3.3\text{V}$ | | 1.65 | | V |
| C_{LOAD} | Load Capacitance, Imposed on External Crystal ^[7] | | | 14 | | pF |
| $C_{IN,X1}$ | X1 Input Capacitance ^[8] | Pin X2 unconnected | | 28 | | pF |
| Pin Capacitance/Inductance | | | | | | |
| C_{IN} | Input Pin Capacitance | Except X1 and X2 | | | 5 | pF |
| C_{OUT} | Output Pin Capacitance | | | | 6 | pF |
| L_{IN} | Input Pin Inductance | | | | 7 | nH |

Notes:

6. X1 input threshold voltage (typical) is $V_{DDQ3}/2$.
7. The W149 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 14 pF; this includes typical stray capacitance of short PCB traces to crystal.
8. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

AC Electrical Characteristics
 $T_A = 0^\circ\text{C to } +70^\circ\text{C}$; $V_{DDQ3} = 3.3\text{V}\pm 5\%$; $V_{DDQ2} = 2.5\text{V}\pm 5\%$; $f_{XTL} = 14.31818\text{ MHz}$

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output; Spread Spectrum clocking is disabled.

CPU Clock Outputs, CPU_F, CPU1 (Lump Capacitance Test Load = 20 pF)

| Parameter | Description | Test Condition/Comments | CPU = 66.6 MHz | | | CPU = 100 MHz | | | Unit |
|-----------|--|---|----------------|------|------|---------------|------|------|----------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| t_P | Period | Measured on rising edge at 1.25V | 15 | | 15.5 | 10 | | 10.5 | ns |
| t_H | High Time | Duration of clock cycle above 2.4V, at min. edge rate (1.5 V/ns) | 5.6 | | | 3.3 | | | ns |
| t_L | Low Time | Duration of clock cycle below 0.4V, at min. edge rate (1.5 V/ns) | 5.3 | | | 3.1 | | | ns |
| t_R | Output Rise Edge Rate | Measured from 0.4V to 2.4V | 1.5 | | 4 | 1.5 | | 4 | V/ns |
| t_F | Output Fall Edge Rate | Measured from 2.4V to 0.4V | 1.5 | | 4 | 1.5 | | 4 | V/ns |
| t_D | Duty Cycle | Measured on rising and falling edge at 1.5V, at min. edge rate (1.5 V/ns) | 45 | | 55 | 45 | | 55 | % |
| t_{JC} | Jitter, Cycle-to-Cycle | Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles. | | | 200 | | | 200 | ps |
| t_{SK} | Output Skew | Measured on rising edge at 1.5V | | | 250 | | | 250 | ps |
| f_{ST} | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. | | | 3 | | | 3 | ms |
| Z_o | AC Output Impedance | Average value during switching transition. Used for determining series termination value. | | 20 | | | 20 | | Ω |

SDRAM Clock Outputs, SDRAM, SDRAM0:11 (Lump Capacitance Test Load = 30 pF)

| Parameter | Description | Test Condition/Comments | CPU = 66.6 MHz | | | CPU = 100 MHz | | | Unit |
|------------------|--|---|----------------|------|------|---------------|------|------|------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| t _P | Period | Measured on rising edge at 1.5V | 30 | | | 30 | | | ns |
| t _H | High Time | Duration of clock cycle above 2.4V, at min. sdge rate (1.5 V/ns) | 5.6 | | | 3.3 | | | ns |
| t _L | Low Time | Duration of clock cycle below 0.4V, at min. sdge rate (1.5 V/ns) | 5.3 | | | 3.1 | | | ns |
| t _R | Output Rise Edge Rate | Measured from 0.4V to 2.4V | 1.5 | | 4 | 1.5 | | 4 | V/ns |
| t _F | Output Fall Edge Rate | Measured from 2.4V to 0.4V | 1.5 | | 4 | 1.5 | | 4 | V/ns |
| t _{PLH} | Prop Delay LH | Input edge rate faster than 1 V/ns | 1 | | 5 | 1 | | 5 | ns |
| t _{PHL} | Prop Delay HL | Input edge rate faster than 1 V/ns | 1 | | 5 | 1 | | 5 | ns |
| t _D | Duty Cycle | Measured on rising and falling edge at 1.5V, at min. sdge rate (1.5 V/ns) | 45 | | 55 | 45 | | 55 | % |
| t _{JC} | Jitter, Cycle-to-Cycle | Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles. | | | 250 | | | 250 | ps |
| t _{SK} | Output Skew | Measured on rising edge at 1.5V | | | 250 | | | 250 | ps |
| t _O | CPU to PCI Clock Skew | Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output. | 1.5 | | 4 | 1.5 | | 4 | ns |
| f _{ST} | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. | | | 3 | | | 3 | ms |
| Z _O | AC Output Impedance | Average value during switching transition. Used for determining series termination value. | | 30 | | | 30 | | Ω |

PCI Clock Outputs, PCI_F and PCI1:5 (Lump Capacitance Test Load = 30 pF)

| Parameter | Description | Test Condition/Comments | CPU = 66.6/100 MHz | | | Unit |
|-----------------|--|---|--------------------|------|------|------|
| | | | Min. | Typ. | Max. | |
| t _P | Period | Measured on rising edge at 1.5V | 30 | | | ns |
| t _H | High Time | Duration of clock cycle above 2.4V | 12.0 | | | ns |
| t _L | Low Time | Duration of clock cycle below 0.4V | 12.0 | | | ns |
| t _R | Output Rise Edge Rate | Measured from 0.4V to 2.4V | 1 | | 4 | V/ns |
| t _F | Output Fall Edge Rate | Measured from 2.4V to 0.4V | 1 | | 4 | V/ns |
| t _D | Duty Cycle | Measured on rising and falling edge at 1.5V | 45 | | 55 | % |
| t _{JC} | Jitter, Cycle-to-Cycle | Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles. | | | 250 | ps |
| t _{SK} | Output Skew | Measured on rising edge at 1.5V | | | 500 | ps |
| t _O | CPU to PCI Clock Skew | Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output. | 1.5 | | 4 | ns |
| f _{ST} | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. | | | 3 | ms |
| Z _O | AC Output Impedance | Average value during switching transition. Used for determining series termination value. | | 30 | | Ω |

IOAPIC Clock Output (Lump Capacitance Test Load = 20 pF)

| Parameter | Description | Test Condition/Comments | CPU = 66.6/100 MHz | | | Unit |
|-----------------|--|---|--------------------|------|------|------|
| | | | Min. | Typ. | Max. | |
| f | Frequency, Actual | Frequency generated by crystal oscillator | 14.31818 | | | MHz |
| t _R | Output Rise Edge Rate | Measured from 0.4V to 2.0V | 1 | | 4 | V/ns |
| t _F | Output Fall Edge Rate | Measured from 2.0V to 0.4V | 1 | | 4 | V/ns |
| t _D | Duty Cycle | Measured on rising and falling edge at 1.25V | 45 | | 55 | % |
| f _{ST} | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. | | | 1.5 | ms |
| Z _O | AC Output Impedance | Average value during switching transition. Used for determining series termination value. | | 15 | | Ω |

REF0:1 Clock Output (Lump Capacitance Test Load = 20 pF)

| Parameter | Description | Test Condition/Comments | CPU = 66.6/100 MHz | | | Unit |
|-----------------|--|---|--------------------|------|------|------|
| | | | Min. | Typ. | Max. | |
| f | Frequency, Actual | Frequency generated by crystal oscillator | 14.318 | | | MHz |
| t _R | Output Rise Edge Rate | Measured from 0.4V to 2.4V | 0.5 | | 2 | V/ns |
| t _F | Output Fall Edge Rate | Measured from 2.4V to 0.4V | 0.5 | | 2 | V/ns |
| t _D | Duty Cycle | Measured on rising and falling edge at 1.5V. | 45 | | 55 | % |
| f _{ST} | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. | | | 3 | ms |
| Z _O | AC Output Impedance | Average value during switching transition. Used for determining series termination value. | | 40 | | Ω |

48-MHz Clock Output (Lump Capacitance Test Load = 20 pF= 66.6/100 MHz)

| Parameter | Description | Test Condition/Comments | CPU = 66.6/100 MHz | | | Unit |
|-----------------|--|---|--------------------|------|------|------|
| | | | Min. | Typ. | Max. | |
| f | Frequency, Actual | Determined by PLL divider ratio (see m/n below) | 48.008 | | | MHz |
| f _D | Deviation from 48 MHz | (48.008 – 48)/48 | +167 | | | ppm |
| m/n | PLL Ratio | (14.31818 MHz x 57/17 = 48.008 MHz) | 57/17 | | | |
| t _R | Output Rise Edge Rate | Measured from 0.4V to 2.4V | 0.5 | | 2 | V/ns |
| t _F | Output Fall Edge Rate | Measured from 2.4V to 0.4V | 0.5 | | 2 | V/ns |
| t _D | Duty Cycle | Measured on rising and falling edge at 1.5V | 45 | | 55 | % |
| f _{ST} | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. | | | 3 | ms |
| Z _o | AC Output Impedance | Average value during switching transition. Used for determining series termination value. | | 40 | | Ω |

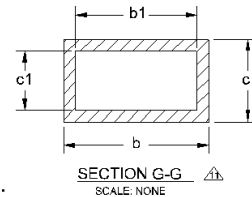
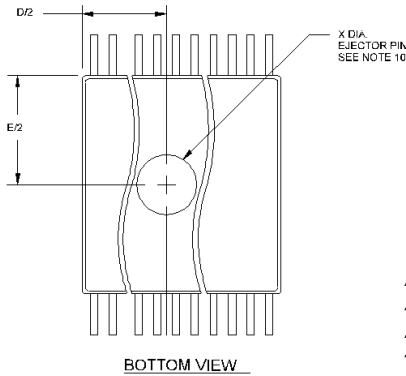
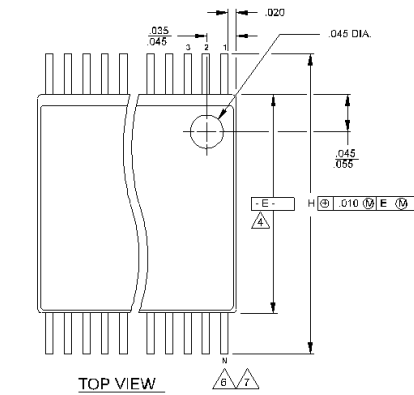
24-MHz Clock Output (Lump Capacitance Test Load = 20 pF= 66.6/100 MHz)

| Parameter | Description | Test Condition/Comments | CPU = 66.6/100 MHz | | | Unit |
|-----------------|--|---|--------------------|------|------|------|
| | | | Min. | Typ. | Max. | |
| f | Frequency, Actual | Determined by PLL divider ratio (see m/n below) | 24.004 | | | MHz |
| f _D | Deviation from 24 MHz | (24.004 – 24)/24 | +167 | | | ppm |
| m/n | PLL Ratio | (14.31818 MHz x 57/34 = 24.004 MHz) | 57/34 | | | |
| t _R | Output Rise Edge Rate | Measured from 0.4V to 2.4V | 0.5 | | 2 | V/ns |
| t _F | Output Fall Edge Rate | Measured from 2.4V to 0.4V | 0.5 | | 2 | V/ns |
| t _D | Duty Cycle | Measured on rising and falling edge at 1.5V | 45 | | 55 | % |
| f _{ST} | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. | | | 3 | ms |
| Z _o | AC Output Impedance | Average value during switching transition. Used for determining series termination value. | | 40 | | Ω |

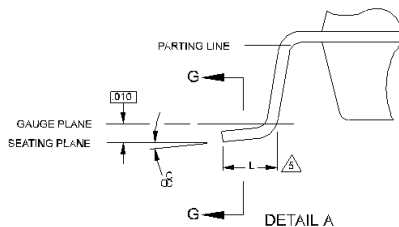
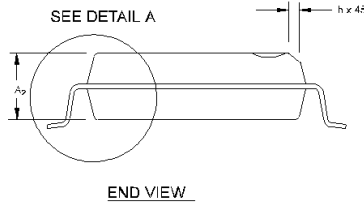
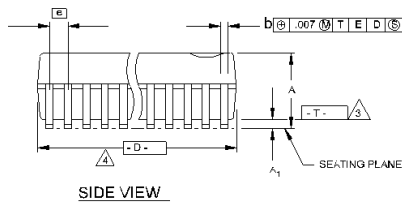
Ordering Information

| Ordering Code | Package Name | Package Type |
|---------------|--------------|-----------------------|
| W149 | H | 48-Pin SSOP (300-mil) |

Document #: 38-00856-A

Package Diagram
48-Pin Shrink Small Outline Package (SSOP, 300 mils)

NOTES:

- 1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
- 2. DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
- 3. "T" IS A REFERENCE DATUM.
- 4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .005 INCHES PER SIDE.
- 5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
- 6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
- 7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
- 8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
- 9. CONTROLLING DIMENSION: INCHES.
- 10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.
- 11. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 INCHES AND .010 INCHES FROM THE LEAD TIPS.
- 12. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-118, VARIATIONS AA, AB, EXCEPT CHAMFER DIMENSION h. JEDEC SPECIFICATION FOR h IS .015/.025".


Summary of nominal dimensions in inches:

Body Width: 0.296
Lead Pitch: 0.025
Body Length: 0.625
Body Height: 0.102

| Symbol | COMMON DIMENSIONS | | | NOTE VARIATIONS | 4 D | | | 6 N |
|--------|-------------------|------|-------|-----------------|------|------|------|-----|
| | MIN. | NOM. | MAX. | | MIN. | NOM. | MAX. | |
| A | .095 | .102 | .110 | AA | .620 | .625 | .630 | 48 |
| A | .088 | .090 | .092 | AB | .720 | .725 | .730 | 56 |
| b | .008 | .010 | .0135 | | | | | |
| b | .008 | .010 | .012 | | | | | |
| c | .005 | - | .010 | | | | | |
| c | .005 | .006 | .0085 | | | | | |
| D | SEE VARIATIONS | | | 4 | | | | |
| E | .292 | .296 | .299 | | | | | |
| e | .025 BSC | | | | | | | |
| H | .400 | .406 | .410 | | | | | |
| h | .010 | .013 | .016 | | | | | |
| L | .024 | .032 | .040 | | | | | |
| N | SEE VARIATIONS | | | 6 | | | | |
| X | .085 | .093 | .100 | 10 | | | | |
| α | 0° | 5° | 8° | | | | | |

THIS TABLE IN INCHES

| Symbol | COMMON DIMENSIONS | | | NOTE VARIATIONS | 4 D | | | 6 N |
|--------|-------------------|-------|-------|-----------------|-------|-------|-------|-----|
| | MIN. | NOM. | MAX. | | MIN. | NOM. | MAX. | |
| A | 2.41 | 2.59 | 2.79 | AA | 15.75 | 15.88 | 16.00 | 48 |
| A | 0.20 | 0.31 | 0.41 | AB | 18.29 | 18.42 | 18.54 | 56 |
| A | 2.24 | 2.29 | 2.34 | | | | | |
| b | 0.203 | 0.254 | 0.343 | | | | | |
| b | 0.203 | 0.254 | 0.305 | | | | | |
| c | 0.127 | - | 0.254 | | | | | |
| c | 0.127 | 0.152 | 0.216 | | | | | |
| D | SEE VARIATIONS | | | 4 | | | | |
| E | 7.42 | 7.52 | 7.59 | | | | | |
| e | 0.835 BSC | | | | | | | |
| H | 10.16 | 10.31 | 10.41 | | | | | |
| h | 0.25 | 0.33 | 0.41 | | | | | |
| L | 0.61 | 0.81 | 1.02 | | | | | |
| N | SEE VARIATIONS | | | 6 | | | | |
| X | 2.16 | 2.36 | 2.54 | 10 | | | | |
| α | 0° | 5° | 8° | | | | | |

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