



# 8K × 8 CMOS STATIC RAM

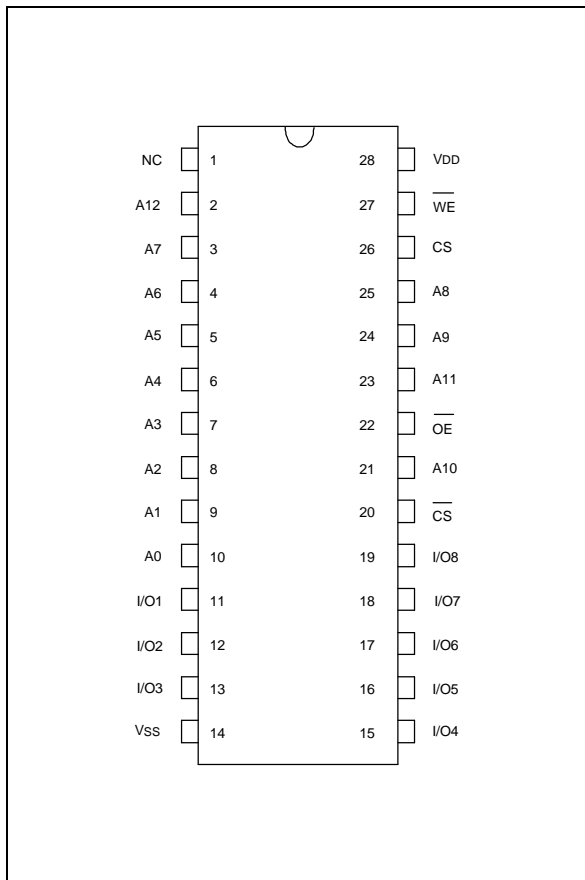
## GENERAL DESCRIPTION

The W2465 is a slow-speed, low-power CMOS static RAM organized as 8192 × 8 bits that operates on a single 5-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

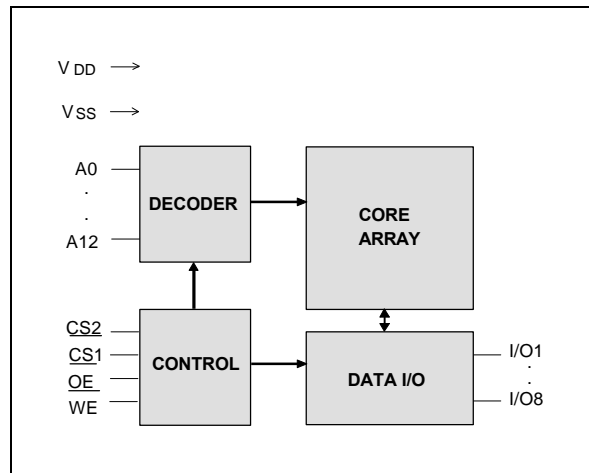
## FEATURES

- Low power consumption:
  - Active: 250 mW (max.)
  - Standby: 100 μW (max.)(LL-version)  
250 μW (max.)(L-version)
- Access time: 70/100 nS (max.)
- Single +5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 2V (min.)
- Available packages: 28-pin 600 mil DIP, 330 mil SOP and 300 mil skinny DIP

## PIN CONFIGURATION



## BLOCK DIAGRAM



## PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A12	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
CS1, CS2	Chip Select Inputs
WE	Write Enable Input
OE	Output Enable Input
VDD	Power Supply
VSS	Ground
NC	No Connection



## TRUTH TABLE

CS1	CS2	OE	WE	MODE	I/O1-I/O8	V <sub>DD</sub> CURRENT
H	X	X	X	Not Selected	High Z	I <sub>SB</sub> , I <sub>SB1</sub>
X	L	X	X	Not Selected	High Z	I <sub>SB</sub> , I <sub>SB1</sub>
L	H	H	H	Output Disable	High Z	I <sub>DD</sub>
L	H	L	H	Read	Data Out	I <sub>DD</sub>
L	H	X	L	Write	Data In	I <sub>DD</sub>

## DC CHARACTERISTICS

### Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to V <sub>SS</sub> Potential	-0.5 to +7.0	V
Input/Output to V <sub>SS</sub> Potential	-0.5 to V <sub>DD</sub> +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

### Operating Characteristics

(V<sub>DD</sub> = 5V ±10%, V<sub>SS</sub> = 0V, T<sub>A</sub> = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Input Low Voltage	V <sub>IL</sub>	-	-0.5	-	+0.8	V	
Input High Voltage	V <sub>IH</sub>	-	+2.2	-	V <sub>DD</sub> +0.5	V	
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>DD</sub>	-2	-	+2	μA	
Output Leakage Current	I <sub>LO</sub>	V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>DD</sub> CS1 = V <sub>IH</sub> (min.) or CS2 = V <sub>IL</sub> (max.) or OE = V <sub>IH</sub> (min.) or WE = V <sub>IL</sub> (max.)	-2	-	+2	μA	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = +4.0 mA	-	-	0.4	V	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0 mA	2.4	-	-	V	
Operating Power Supply Current	I <sub>DD</sub>	CS1 = V <sub>IL</sub> (max.), CS2 = V <sub>IH</sub> (min.) I/O = 0 mA, Cycle = min. Duty = 100%	70	-	-	70	mA
			100	-	-	60	mA
Standby Power Supply Current	I <sub>SB</sub>	CS1 = V <sub>IH</sub> (min.) or CS2 = V <sub>IL</sub> (max.), Cycle = min. Duty = 100%	-	-	3	mA	
	I <sub>SB1</sub>	CS1 ≥ V <sub>DD</sub> -0.2V or CS2 ≤ 0.2V	LL	-	-	20	μA
L			-	-	50	μA	

Note: Typical characteristics are at V<sub>DD</sub> = 5 V, T<sub>A</sub> = 25° C.



**CAPACITANCE**

(V<sub>DD</sub> = 5V, T<sub>A</sub> = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	6	pF
Input/Output Capacitance	C <sub>I/O</sub>	V <sub>OUT</sub> = 0V	8	pF

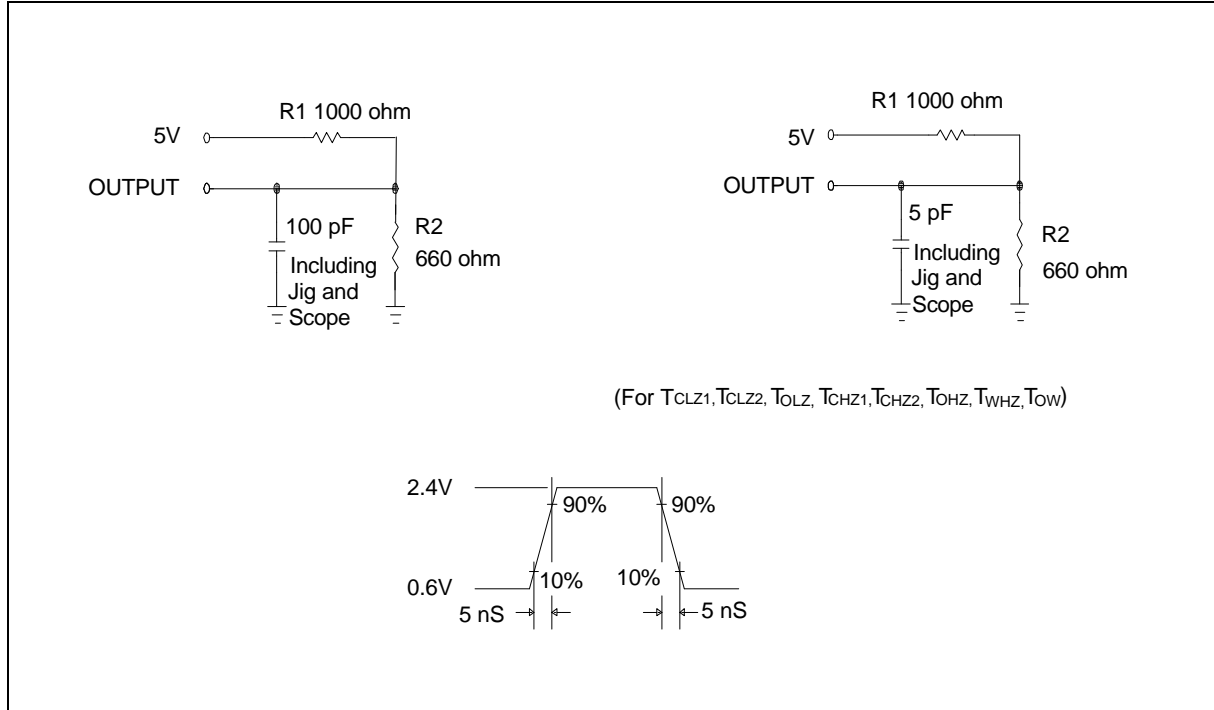
Note: These parameters are sampled but not 100% tested.

**AC CHARACTERISTICS**

**AC Test Conditions**

PARAMETER	CONDITIONS
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	C <sub>L</sub> = 100 pF, I <sub>OH</sub> /I <sub>OL</sub> = -1 mA/4 mA

**AC Test Loads and Waveform**





AC Characteristics, continued

(V<sub>DD</sub> = 5V ±10%, V<sub>SS</sub> = 0V, T<sub>A</sub> = 0 to 70° C)**Read Cycle**

PARAMETER	SYM.	W2465-70		W2465-10		UNIT	
		MIN.	MAX.	MIN.	MAX.		
Read Cycle Time	TRC	70	-	100	-	nS	
Address Access Time	TAA	-	70	-	100	nS	
Chip Select Access Time	$\overline{\text{CS1}}$	TACS1	-	70	-	100	nS
	CS2	TACS2	-	70	-	100	nS
Output Enable to Output Valid	TAOE	-	35	-	50	nS	
Chip Selection to Output in Low Z	$\overline{\text{CS1}}$	TCLZ1*	5	-	10	-	nS
	CS2	TCLZ2*	5	-	10	-	nS
Output Enable to Output in Low Z	TOLZ*	5	-	5	-	nS	
Chip Deselection to Output in High Z	$\overline{\text{CS1}}$	TCHZ1*	-	30	-	35	nS
	CS2	TCHZ2*	-	30	-	35	nS
Output Disable to Output in High Z	TOHZ*	-	30	-	35	nS	
Output Hold from Address Change	TOH	10	-	10	-	nS	

\* These parameters are sampled but not 100% tested.

**Write Cycle**

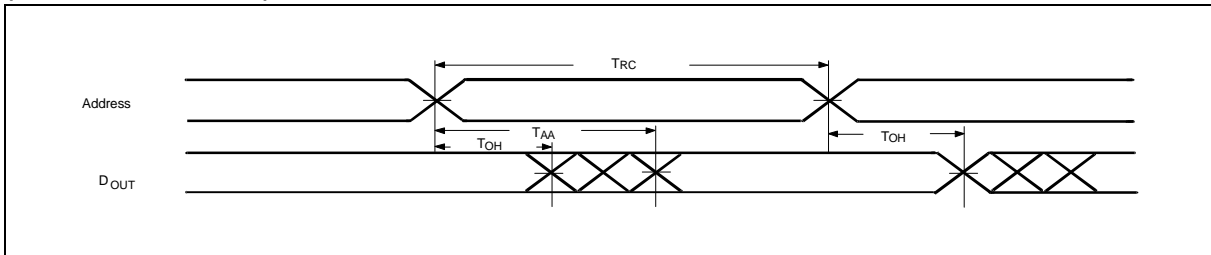
PARAMETER	SYM.	W2465-70		W2465-10		UNIT	
		MIN.	MAX.	MIN.	MAX.		
Write Cycle Time	TWC	70	-	100	-	nS	
Chip Selection to End of Write	$\overline{\text{CS1}}$	TCW1	60	-	80	-	nS
	CS2	TCW2	60	-	80	-	nS
Address Valid to End of Write	TAW	60	-	80	-	nS	
Address Setup Time	TAS	0	-	0	-	nS	
Write Pulse Width	TWP	45	-	60	-	nS	
Write Recovery Time	$\overline{\text{CS1}}, \overline{\text{WE}}$	TWR1	0	-	0	-	nS
	CS2	TWR2	0	-	0	-	nS
Data Valid to End of Write	TDW	30	-	40	-	nS	
Data Hold from End of Write	TDH	0	-	0	-	nS	
Write to Output in High Z	TWHZ*	-	30	-	30	nS	
Output Disable to Output in High Z	TOHZ*	-	30	-	30	nS	
Output Active from End of Write	TOW	0	-	0	-	nS	

\* These parameters are sampled but not 100% tested.

**TIMING WAVEFORMS**

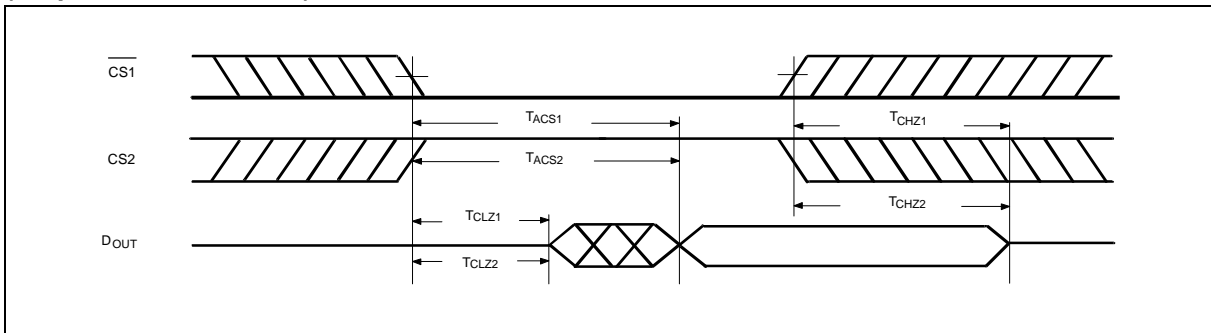
**Read Cycle 1**

(Address Controlled)



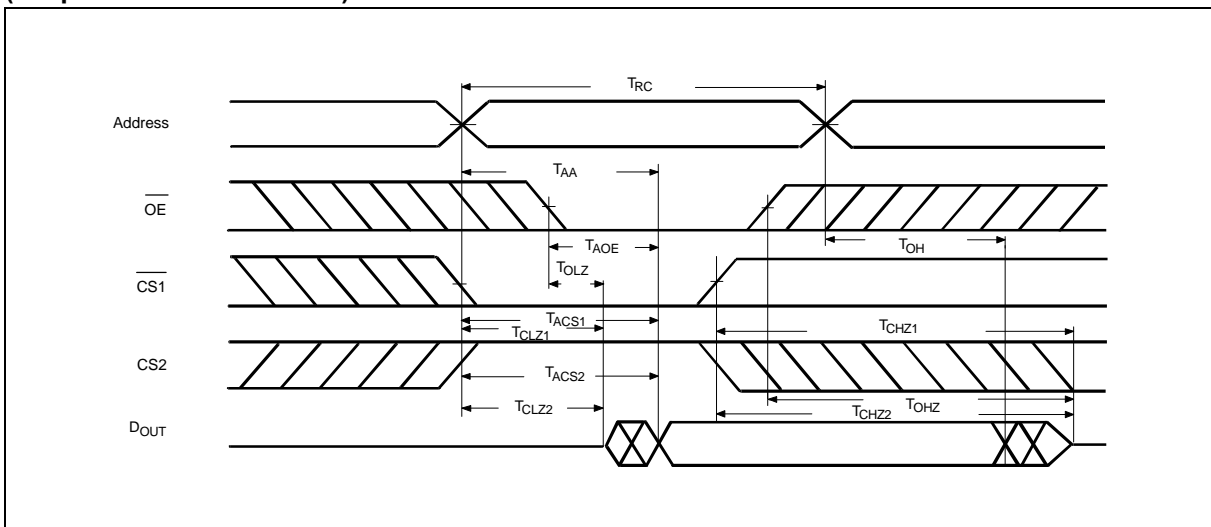
**Read Cycle 2**

(Chip Select Controlled)



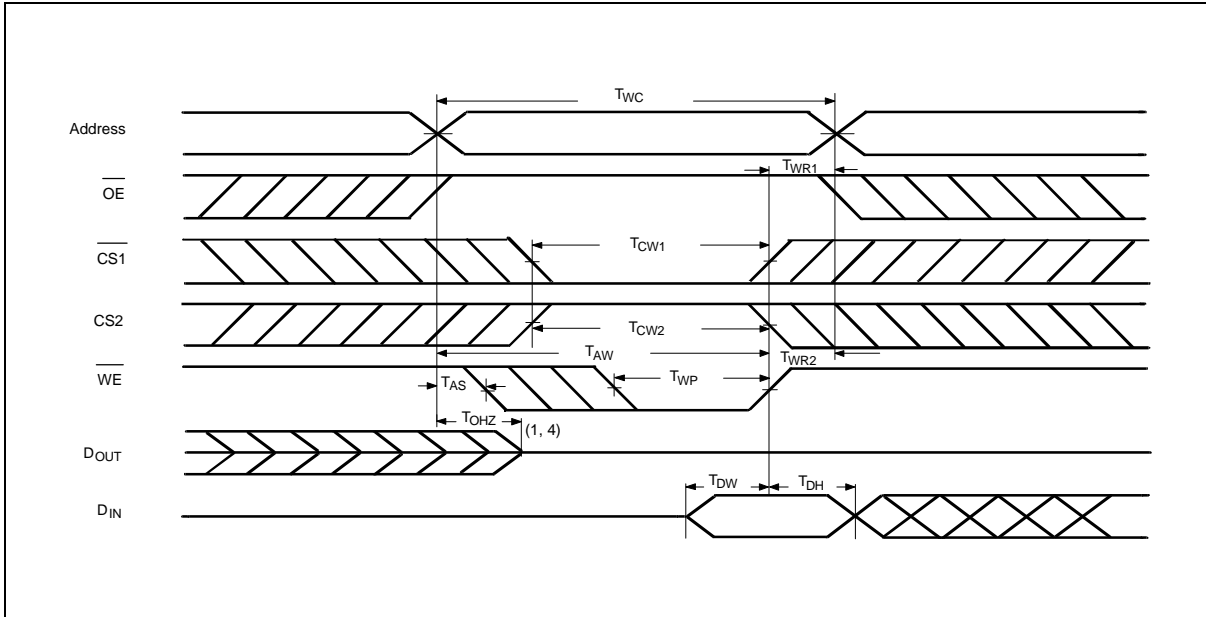
**Read Cycle 3**

(Output Enable Controlled)



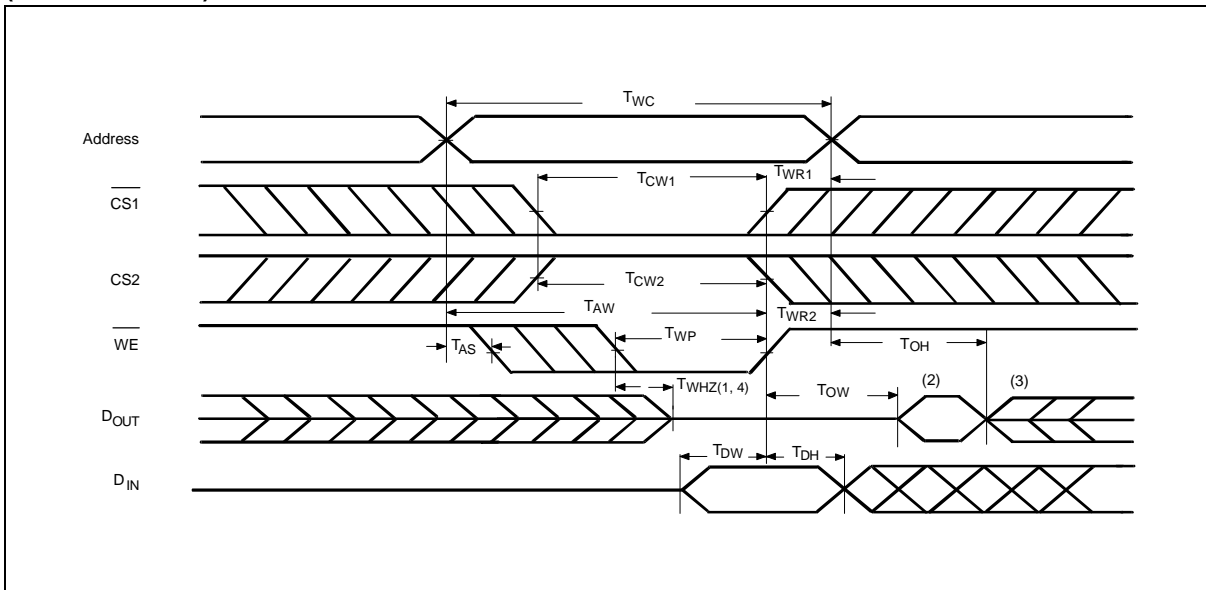
Timing Waveforms, continued

**Write Cycle 1**



**Write Cycle 2**

(OE = V<sub>IL</sub> Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from D<sub>OUT</sub> are the same as the data written to D<sub>IN</sub> during the write cycle.
3. D<sub>OUT</sub> provides the read data for the next address.
4. Transition is measured ±500 mV from steady state with C<sub>L</sub> = 5 pF. This parameter is guaranteed but not 100% tested.



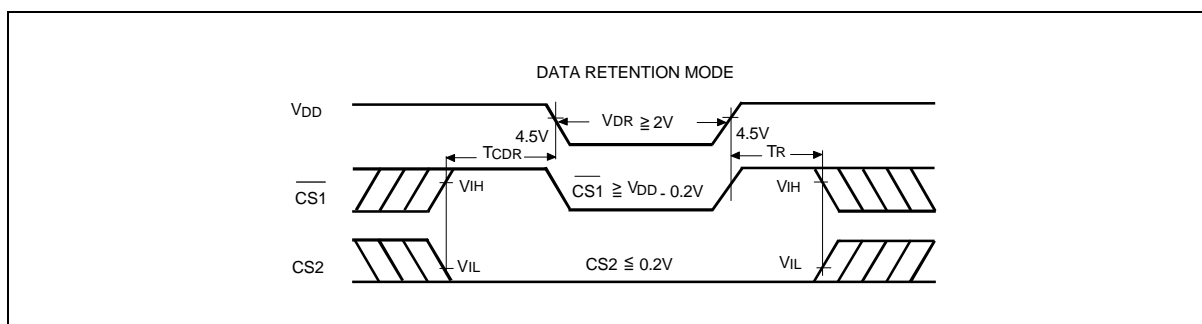
## DATA RETENTION CHARACTERISTICS

(TA = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
VDD for Data Retention	VDR	$\overline{CS1} \geq V_{DD} - 0.2V$ , or $CS2 \leq 0.2V$	2.0	-	-	V	
Data Retention Current	IDDDR	$\overline{CS1} \geq V_{DD} - 0.2V$ , or $CS2 \leq 0.2V$ $V_{DD} = 3V$	LL	-	-	10	$\mu A$
			L	-	-	20	$\mu A$
Chip Deselect to Data Retention Time	TCDR	See data retention waveforms	0	-	-	nS	
Operation Recovery Time	TR		TRC*	-	-	nS	

TRC\* = Read Cycle Time

## DATA RETENTION WAVEFORMS



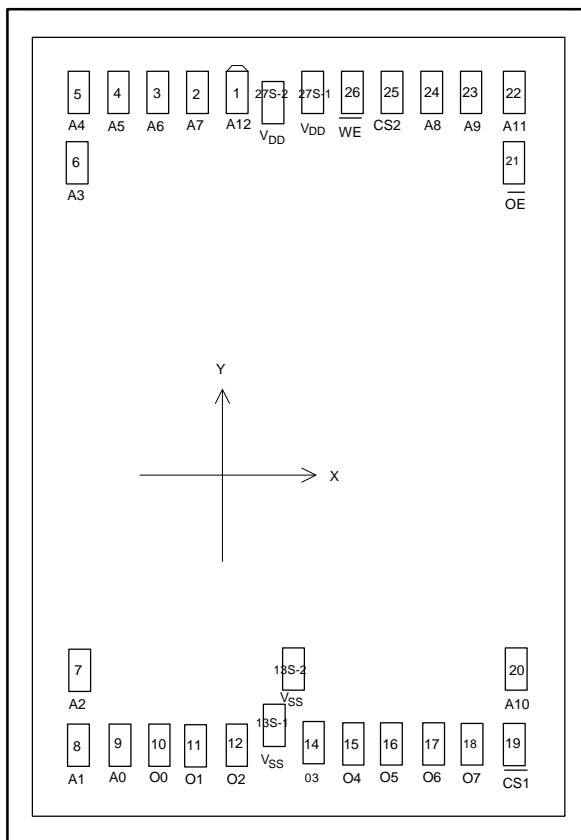
## ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. ( $\mu A$ )	PACKAGE
W2465-70LL	70	70	20	600 mil DIP
W2465-10L	100	60	50	600 mil DIP
W2465S-70LL	70	70	20	330 mil SOP
W2465S-10L	100	60	50	330 mil SOP
W2465K-70LL	70	70	20	300 mil Skinny
W2465K-10L	100	60	50	300 mil Skinny

Notes:

- Winbond reserves the right to make changes to its products without prior notice.
- Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

## BONDING PAD DIAGRAM



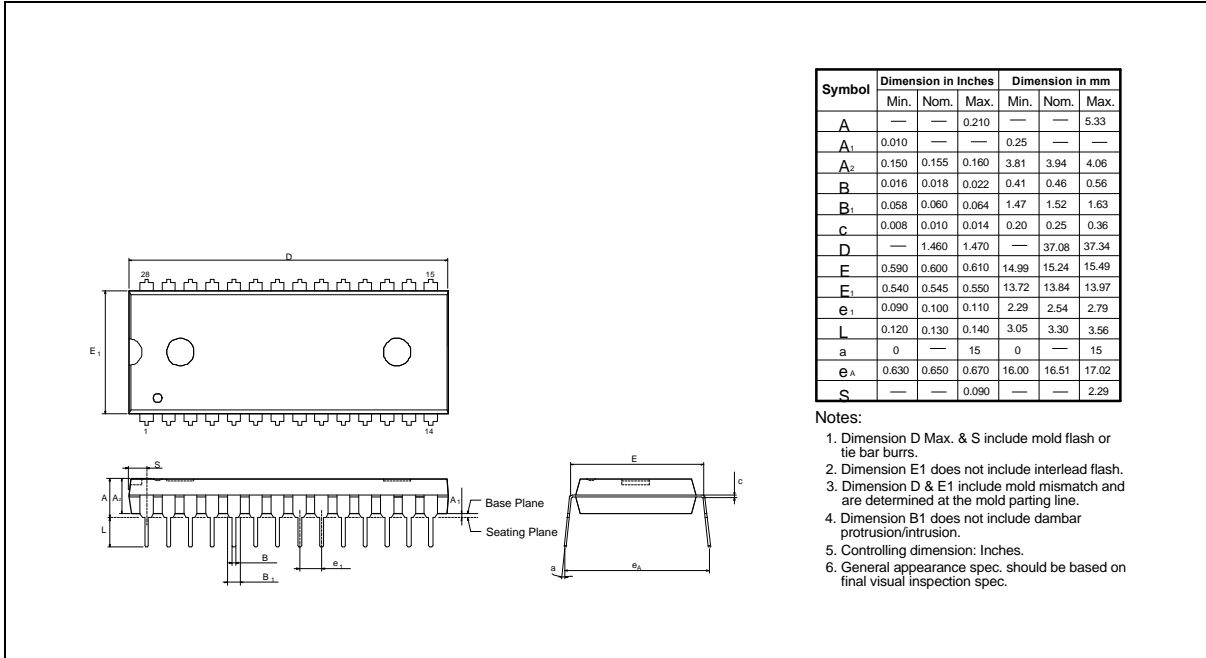
PAD NO.	X	Y
1	-226.95	1526.15
2	-350.95	1526.15
3	-484.10	1526.15
4	-608.10	1526.15
5	-739.75	1526.15
6	-741.75	1315.10
7	-741.75	-1231.85
8	-741.75	-1456.30
9	-610.60	-1456.30
10	-481.50	-1466.30
11	-343.80	-1466.30
12	-206.10	-1466.30
13S-1	-73.00	-1401.10
13S-2	-8.35	-1212.80
14	60.10	-1466.30
15	193.30	-1466.30
16	332.40	-1466.30
17	465.60	-1466.30
18	603.30	-1466.30
19	738.15	-1456.30
20	740.15	-1221.45
21	740.15	1310.80
22	738.15	1526.15
23	606.50	1526.15
24	482.50	1526.15
25	349.35	1526.15
26	225.35	1526.15
27S-1	94.20	1526.15
27S-2	-50.40	1456.10

Note: For bare chip form (C.O.B.) applications, the substrate must be connected to VDD or left floating in the PCB layout.

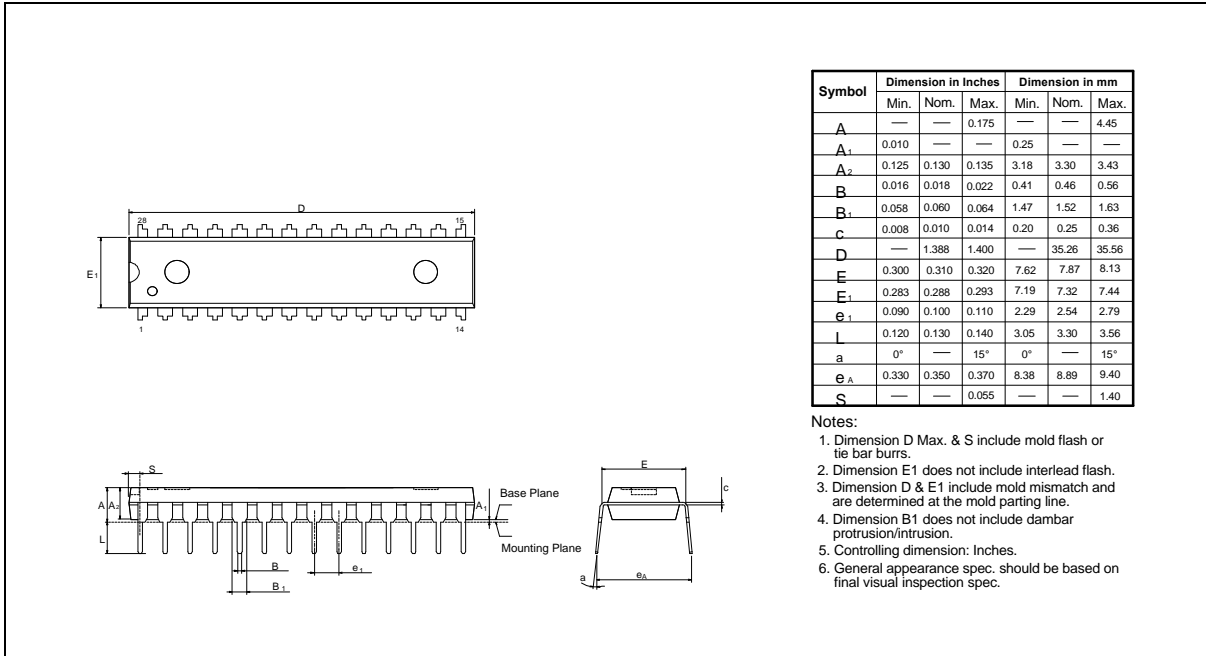


## PACKAGE DIMENSIONS

### 28-pin P-DIP



### 28-pin P-DIP Skinny





Package Dimensions, continued

**28-pin SO Wide Body**

Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.112	—	—	2.85
A <sub>1</sub>	0.004	—	—	0.10	—	—
A <sub>2</sub>	0.093	0.098	0.103	2.36	2.49	2.62
b	0.014	0.016	0.020	0.36	0.41	0.51
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	0.713	0.733	—	18.11	18.62
E	0.326	0.331	0.336	8.28	8.41	8.53
e	0.044	0.050	0.056	1.12	1.27	1.42
H <sub>E</sub>	0.453	0.465	0.477	11.51	11.81	12.12
L	0.028	0.036	0.044	0.71	0.91	1.12
L <sub>E</sub>	0.059	0.067	0.075	1.50	1.70	1.91
S	—	—	0.047	—	—	1.19
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°

**Notes:**

1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension b does not include dambar protrusion/intrusion.
3. Dimension D & E include mold mismatch and determined at the mold parting line.
4. Controlling dimension: Inches.
5. General appearance spec should be based on final visual inspection spec.



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Note: All data and specifications are subject to change without notice.