



512MB – 2x32Mx64 DDR SDRAM UNBUFFERED

FEATURES

- Double-data-rate architecture
- DDR200, DDR266, DDR333 and DDR400
 - JEDEC design specified
- Bi-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency 2,2.5 (clock)
- Programmable Burst Length (2,4,8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input.
- Auto and self refresh
- Serial presence detect
- Dual Rank
- Power supply:
 - $V_{CC} = V_{CCQ} = +2.5V \pm 0.2V$ (100, 133 and 166 MHz)
 - $V_{CC} = V_{CCQ} = +2.6V \pm 0.1V$ (200 MHz)
- Standard 184 pin DIMM package
 - JD3 PCB height: 30.48 (1.20") MAX

DESCRIPTION

The W3EG6462S is a 2x32Mx64 Double Data Rate SDRAM memory module based on 256Mb DDR SDRAM components. The module consists of sixteen 32Mx8 DDR SDRAMs in 66 pin TSOP packages mounted on a 184 pin FR4 substrate.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges and Burst Lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

NOTE: Consult factory for availability of:

- RoHS compliant products
- Vendor source control options
- Industrial temperature option

OPERATING FREQUENCIES

	DDR400 @CL=3	DDR333 @CL=2.5	DDR266 @CL=2.5	DDR266 @CL=2	DDR266 @CL=2.5	DDR200 @CL=2
Clock Speed	200MHz	166MHz	133MHz	133MHz	133MHz	100MHz
CL-tRCD-tRP	3-3-3	2.5-3-3	2-3-3	2-3-3	2.5-3-3	2-2-2



PIN CONFIGURATION

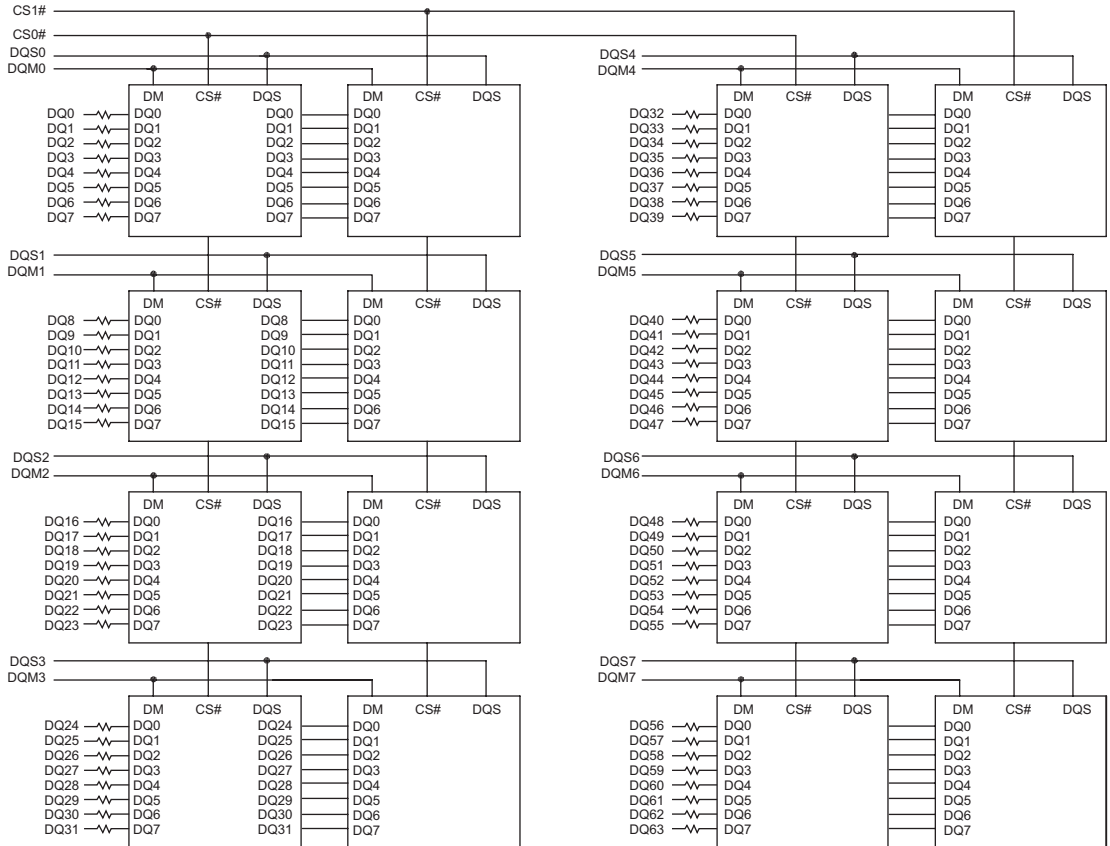
PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VREF	47	NC	93	Vss	139	Vss
2	DQ0	48	A0	94	DQ4	140	NC
3	Vss	49	NC	95	DQ5	141	A10
4	DQ1	50	Vss	96	Vccq	142	NC
5	DQS0	51	NC	97	DQM0	143	Vccq
6	DQ2	52	BA1	98	DQ6	144	NC
7	Vcc	53	DQ32	99	DQ7	145	Vss
8	DQ3	54	Vccq	100	Vss	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	NC	56	DQS4	102	NC	148	Vcc
11	Vss	57	DQ34	103	NC	149	DQM4
12	DQ8	58	Vss	104	Vccq	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	Vss
15	Vccq	61	DQ40	107	DQM1	153	DQ44
16	CK1	62	Vccq	108	Vcc	154	RAS#
17	CK1#	63	WE#	109	DQ14	155	DQ45
18	Vss	64	DQ41	110	DQ15	156	Vccq
19	DQ10	65	CAS#	111	CKE1	157	CS0#
20	DQ11	66	Vss	112	Vccq	158	CS1#
21	CKE0	67	DQS5	113	NC	159	DQM5
22	Vccq	68	DQ42	114	DQ20	160	Vss
23	DQ16	69	DQ43	115	A12	161	DQ46
24	DQ17	70	Vcc	116	Vss	162	DQ47
25	DQS2	71	NC	117	DQ21	163	NC
26	Vss	72	DQ48	118	A11	164	Vccq
27	A9	73	DQ49	119	DQM2	165	DQ52
28	DQ18	74	Vss	120	Vcc	166	DQ53
29	A7	75	CK2#	121	DQ22	167	NC
30	Vccq	76	CK2	122	A8	168	Vcc
31	DQ19	77	Vccq	123	DQ23	169	DQM6
32	A5	78	DQS6	124	Vss	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	Vss	80	DQ51	126	DQ28	172	Vccq
35	DQ25	81	Vss	127	DQ29	173	NC
36	DQS3	82	Vccid	128	Vccq	174	DQ60
37	A4	83	DQ56	129	DQM3	175	DQ61
38	Vcc	84	DQ57	130	A3	176	Vss
39	DQ26	85	Vcc	131	DQ30	177	DQM7
40	DQ27	86	DQS7	132	Vss	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	Vss	88	DQ59	134	NC	180	Vccq
43	A1	89	Vss	135	NC	181	SA0
44	NC	90	WP	136	Vccq	182	SA1
45	NC	91	SDA	137	CK0	183	SA2
46	Vcc	92	SCL	138	CK0#	184	Vccspd

PIN NAMES

A0-A12	Address input (Multiplexed)
BA0-BA1	Bank Select Address
DQ0-DQ63	Data Input/Output
DQS0-DQS7	Data Strobe Input/Output
CK0, CK1, CK2	Clock Input
CK0#, CK1#, CK2#	Clock Input
CKE0, CKE1	Clock Enable input
CS0#, CS1#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DQM0-DQM7	Data in Mask
Vcc	Power Supply
Vccq	Power Supply for DQS
Vss	Ground
VREF	Power Supply for Reference
Vccspd	Serial EEPROM Power Supply
SDA	Serial data I/O
SCL	Serial clock
SA0-SA2	Address in EEPROM
Vccid	Vcc Identification Flag
NC	No Connect

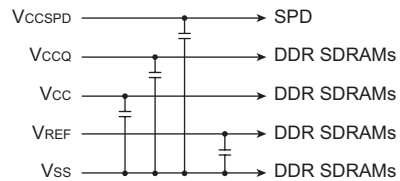
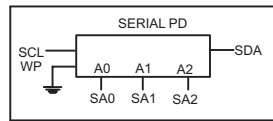


FUNCTIONAL BLOCK DIAGRAM



- RAS# → RAS: DDR SDRAMs
- CAS# → CAS: DDR SDRAMs
- BA0-BA1 → BA0-BA1: DDR SDRAMs
- WE# → WE: DDR SDRAMs
- A0-A12 → A0-A12: DDR SDRAMs
- CKE0 → CKE0: DDR SDRAMs
- CKE1 → CKE1: DDR SDRAMs

CLOCK INPUT	
CK0, CK0#	4 SDRAMs
CK1, CK1#	6 SDRAMs
CK2, CK2#	6 SDRAMs



NOTE: All resistor values are 22 ohms unless otherwise specified.



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 to 3.6	V
Voltage on Vcc supply relative to Vss	V _{CC} , V _{CCQ}	-1.0 to 3.6	V
Storage Temperature	T _{STG}	-55 to +150	°C
Power Dissipation	P _D	16	W
Short Circuit Current	I _{OS}	50	mA

Note:
 Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability

DC CHARACTERISTICS

0°C ≤ T_A ≤ 70°C, V_{CC} = 2.5V ± 0.2V

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	2.3	2.7	V
Supply Voltage	V _{CCQ}	2.3	2.7	V
Reference Voltage	V _{REF}	1.15	1.35	V
Termination Voltage	V _{TT}	1.15	1.35	V
Input High Voltage	V _{IH}	V _{REF} + 0.15	V _{CCQ} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	V _{REF} - 0.15	V
Output High Voltage	V _{OH}	V _{TT} + 0.76	—	V
Output Low Voltage	V _{OL}	—	V _{TT} -0.76	V

CAPACITANCE

T_A = 25°C, f = 1MHz, V_{CC} = 2.5V ±0.2V, V_{REF} = 1.4V ± 200mV

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A12)	C _{IN1}	50	pF
Input Capacitance (RAS#, CAS#, WE#)	C _{IN2}	50	pF
Input Capacitance (CKE0, CKE1)	C _{IN3}	26	pF
Input Capacitance (CK0, CK0#)	C _{IN4}	50	pF
Input Capacitance (CS0#, CS1#)	C _{IN5}	26	pF
Input Capacitance (DQM0-DQM8)	C _{IN6}	13	pF
Input Capacitance (BA0-BA1)	C _{IN7}	50	pF
Data input/output capacitance (DQ0-DQ63)(DQS)	C _{OUT}	13	pF



I_{DD} SPECIFICATIONS AND TEST CONDITIONS

0°C ≤ T_A ≤ 70°C, V_{CCQ} = 2.5V ± 0.2V, V_{CC} = 2.5V ± 0.2V

Includes DDR SDRAM component only

Parameter	Symbol	Conditions	DDR400@ CL=3 Max	DDR333@ CL=2.5-3-3 Max	DDR266@ CL=2 Max	DDR266@ CL=2.5 Max	DDR200@ CL=2 Max	Units
Operating Current	I _{DD0}	One device bank; Active - Precharge; t _{RC} =t _{RC} (MIN); t _{CK} =t _{CK} (MIN); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two cycles.	2200	1960	1800	1800	1800	mA
Operating Current	I _{DD1}	One device bank; Active-Read-Precharge Burst = 2; t _{RC} =t _{RC} (MIN); t _{CK} =t _{CK} (MIN); I _{OUT} = 0mA; Address and control inputs changing once per clock cycle.	2480	2320	2080	2080	2080	mA
Precharge Power-Down Standby Current	I _{DD2P}	All device banks idle; Power-down mode; t _{CK} =t _{CK} (MIN); CKE=(low)	64	64	64	64	64	mA
Idle Standby Current	I _{DD2F}	CS# = High; All device banks idle; t _{CK} =t _{CK} (MIN); CKE = high; Address and other control inputs changing once per clock cycle. V _{IN} = V _{REF} for DQ, DQS and DM.	960	800	720	720	720	mA
Active Power-Down Standby Current	I _{DD3P}	One device bank active; Power-Down mode; t _{CK} (MIN); CKE=(low)	640	480	400	400	400	mA
Active Standby Current	I _{DD3N}	CS# = High; CKE = High; One device bank; Active-Precharge; t _{RC} =t _{RAS} (MAX); t _{CK} =t _{CK} (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.	1120	960	800	800	800	mA
Operating Current	I _{DD4R}	Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; T _{CK} = T _{CK} (MIN); I _{OUT} = 0mA.	2720	2360	2000	2000	2000	mA
Operating Current	I _{DD4W}	Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; t _{CK} =t _{CK} (MIN); DQ, DM and DQS inputs changing once per clock cycle.	2680	2360	2000	2000	2000	mA
Auto Refresh Current	I _{DD5}	t _{RC} = t _{RC} (MIN)	3200	3000	2680	2680	2680	mA
Self Refresh Current	I _{DD6}	CKE ≤ 0.2V	64	64	64	64	64	mA
Operating Current	I _{DD7A}	Four bank interleaving Reads (BL=4) with auto precharge with t _{RC} =t _{RC} (MIN); t _{CK} =t _{CK} (MIN); Address and control inputs change only during Active Read or Write commands.	4880	4240	3600	3600	3600	mA



DETAILED TEST CONDITIONS FOR DDR SDRAM I_{DD1} & I_{DD7A}

I_{DD1} : OPERATING CURRENT : ONE BANK

1. Typical Case : V_{CC}=2.5V, T=25°C
2. Worst Case : V_{CC}=2.7V, T=10°C
3. Only one bank is accessed with t_{RC} (min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. I_{OUT} = 0mA
4. Timing Patterns :
 - DDR200 (100 MHz, CL=2) : t_{CK}=10ns, CL2, BL=4, t_{RCD}=2*t_{CK}, t_{RAS}=5*t_{CK}
Read : A0 N R0 N N P0 N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
 - DDR266 (133MHz, CL=2.5) : t_{CK}=7.5ns, CL=2.5, BL=4, t_{RCD}=3*t_{CK}, t_{RC}=9*t_{CK}, t_{RAS}=5*t_{CK}
Read : A0 N N R0 N P0 N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
 - DDR266 (133MHz, CL=2) : t_{CK}=7.5ns, CL=2, BL=4, t_{RCD}=3*t_{CK}, t_{RC}=9*t_{CK}, t_{RAS}=5*t_{CK}
Read : A0 N N R0 N P0 N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
 - DDR333 (166MHz, CL=2.5) : t_{CK}=6ns, BL=4, t_{RCD}=10*t_{CK}, t_{RAS}=7*t_{CK}
Read : A0 N N R0 N P0 N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
 - DDR400 (200MHz, CL=3) : t_{CK}=5ns, BL=4, t_{RCD}=15*t_{CK}, t_{RAS}=7*t_{CK}
Read : A0 N N R0 N P0 N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst

I_{DD7A} : OPERATING CURRENT : FOUR BANKS

1. Typical Case : V_{CC}=2.5V, T=25°C
2. Worst Case : V_{CC}=2.7V, T=10°C
3. Four banks are being interleaved with t_{RC} (min), Burst Mode, Address and Control inputs on NOP edge are not changing. I_{OUT}=0mA
4. Timing Patterns :
 - DDR200 (100 MHz, CL=2) : t_{CK}=10ns, CL2, BL=4, t_{RRD}=2*t_{CK}, t_{RCD}=3*t_{CK}, Read with Autoprecharge
Read : A0 N A1 R0 A2 R1 A3 R2 A0 R3 A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
 - DDR266 (133MHz, CL=2.5) : t_{CK}=7.5ns, CL=2.5, BL=4, t_{RRD}=3*t_{CK}, t_{RCD}=3*t_{CK}
Read with Autoprecharge
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
 - DDR266 (133MHz, CL=2) : t_{CK}=7.5ns, CL2=2, BL=4, t_{RRD}=2*t_{CK}, t_{RCD}=2*t_{CK}
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
 - DDR333 (166MHz, CL=2.5) : t_{CK}=6ns, BL=4, t_{RRD}=3*t_{CK}, t_{RCD}=3*t_{CK}, Read with Autoprecharge
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
 - DDR400 (200MHz, CL=3) : t_{CK}=5ns, BL=4, t_{RRD}=10*t_{CK}, t_{RCD}=15*t_{CK}, Read with Autoprecharge
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst

Legend:

A = Activate, R = Read, W = Write, P = Precharge, N = NOP

A (0-3) = Activate Bank 0-3

R (0-3) = Read Bank 0-3



**DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND
RECOMMENDED AC OPERATING CONDITIONS**

AC CHARACTERISTICS		403		335		262		263/265		202				
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES	
Access window of DQs from CK/CK#	t _{AC}			-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	-0.75	+0.75	ns		
CK high-level width	t _{CH}			0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t _{CK}	26	
CK low-level width	t _{CL}			0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t _{CK}	26	
Clock cycle time	CL = 3	t _{CK (3)}	5	7.5	6	13	7.5	13	7.5	13	7.5	13	ns	40, 45
	CL = 2.5	t _{CK (2.5)}	6	13	6	13	7.5	13	7.5	13	7.5	13	ns	40, 45
	CL = 2	t _{CK (2)}	7.5	13	7.5	13	7.5/10	13	7.5/10	13	7.5/10	13	ns	40, 45
DQ and DM input hold time relative to DQS	t _{DH}	0.4		0.45		0.5		0.5		0.5		ns	23, 27	
DQ and DM input setup time relative to DQS	t _{DS}	0.4		0.45		0.5		0.5		0.5		ns	23, 27	
DQ and DM input pulse width (for each input)	t _{DIPW}	1.75		1.75		1.75		1.75		1.75		ns	27	
Access window of DQS from CK/CK#	t _{DQSCK}	-0.6		-0.60	+0.60	-0.75	+0.75	-0.75	+0.75	-0.75	+0.75	ns		
DQS input high pulse width	t _{DQSH}	0.35		0.35		0.35		0.35		0.35		t _{CK}		
DQS input low pulse width	t _{DQSL}	0.35		0.35		0.35		0.35		0.35		t _{CK}		
DQS-DQ skew, DQS to last DQ valid, per group, per access	t _{DQSQ}		0.40		0.45		0.5	0.5		0.5		ns	22, 23	
Write command to first DQS latching transition	t _{DQSS}	0.72	1.28	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	t _{CK}		
DQS falling edge to CK rising - setup time	t _{DSS}	0.2		0.2		0.2		0.2		0.2		t _{CK}		
DQS falling edge from CK rising - hold time	t _{DSH}	0.2		0.2		0.2		0.2		0.2		t _{CK}		
Half clock period	t _{HP}	t _{CH} , t _{CL}		t _{CH} , t _{CL}		t _{CH} , t _{CL}		t _{CH} , t _{CL}		t _{CH} , t _{CL}		ns	31	
Data-out high-impedance window from CK/CK#	t _{HZ}		+0.70		+0.70		+0.75		+0.75		+0.75	ns	16, 36	
Data-out low-impedance window from CK/CK#	t _{LZ}	-0.70		-0.70		-0.75		-0.75		-0.75		ns	16, 36	
Address and control input hold time (fast slew rate)	t _{IHF}	0.6		0.75		0.90		.90		.90		ns	12	
Address and control input setup time (fast slew rate)	t _{ISF}	0.6		0.75		0.90		.90		.90		ns	12	
Address and control input hold time (slow slew rate)	t _{IHS}	0.6		0.80		1		1		1		ns	12	



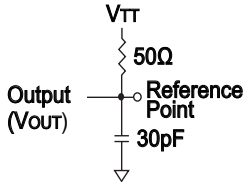
**DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND
RECOMMENDED AC OPERATING CONDITIONS (continued)**

AC CHARACTERISTICS		403		335		262		263/265		202			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Address and control input setup time (slow slew rate)	t _{ISS}	0.6		0.80		1		1		1		ns	12
Address and Control input pulse width (for each input)	t _{IPW}	2.2		2.2		2.2		2.2		2.2		ns	
LOAD MODE REGISTER command cycle time	t _{MRD}	2		12		15		15		15		ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access	t _{QH}	t _{HP} - t _{QHS}		t _{HP} - t _{QHS}		t _{HP} - t _{QHS}		t _{HP} - t _{QHS}		t _{HP} - t _{QHS}		ns	22, 23
Data hold skew factor	t _{QHS}		0.50		0.55		0.75		0.75		0.75	ns	
ACTIVE to PRECHARGE command	t _{RAS}	40	70,000	42	70,000	40	120,000	40	120,000	40	120,000	ns	31, 48
ACTIVE to READ with Auto precharge command	t _{RAP}	15		15		15		20		20		ns	
ACTIVE to ACTIVE/AUTO REFRESH command period	t _{RC}	55		60		60		65		65		ns	
AUTO REFRESH command period	t _{RFC}	70		75		75		75		75		ns	43
ACTIVE to READ or WRITE delay	t _{RCD}	15		15		15		20		20		ns	
PRECHARGE command period	t _{RP}	15		15		15		20		20		ns	
DQS read preamble	t _{RPRE}	0.9		0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	t _{CK}	37
DQS read postamble	t _{RPST}	0.4		0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t _{CK}	37
ACTIVE bank a to ACTIVE bank b command	t _{RRD}	10		12		15		15		15		ns	
DQS write preamble	t _{WPRE}	0.25		0.25		0.25		0.25		0.25		t _{CK}	
DQS write preamble setup time	t _{WPRES}	0		0		0		0		0		ns	18, 19
DQS write postamble	t _{WPST}	0.4		0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t _{CK}	17
Write recovery time	t _{WR}	15		15		15		15		15		ns	
Internal WRITE to READ command delay	t _{WTR}	2		1		1		1		1		t _{CK}	
Data valid output window	na	t _{QH} - t _{DQSQ}		t _{QH} - t _{DQSQ}		t _{QH} - t _{DQSQ}		t _{QH} - t _{DQSQ}		t _{QH} - t _{DQSQ}		ns	22
REFRESH to REFRESH command	t _{REFC}		70.3		70.3		70.3		70.3		70.3	μs	21
Average periodic refresh interval	t _{REFI}		7.8		7.8		7.8		7.8		7.8	μs	21
Terminating voltage delay to V _{CC}	t _{VD}	0		0		0		0		0		ns	
Exit SELF REFRESH to non-READ command	t _{XSNR}	75		75		75		75		75		ns	
Exit SELF REFRESH to READ command	t _{XSRD}	200		200		200		200		200		t _{CK}	



Notes

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:



4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between V_{IL}(AC) and V_{IH}(AC).
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. V_{REF} is expected to equal V_{CCQ}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±2 percent of the DC value. Thus, from V_{CCQ}/2, V_{REF} is allowed ±25mV for DC error and an additional ±25mV for AC noise. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
7. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
8. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time at CL = 2 for 262, and 262, CL = 2.5 for 335 and 265, CL = 3 for 403 with the outputs open.
9. Enables on-chip refresh and address counters.
10. I_{DD} specifications are tested after the device is properly initialized, and is averaged at the defined cycle rate.
11. This parameter is sampled. V_{CC} = +2.5V ±0.2V, V_{CCQ} = +2.5V ±0.2V, V_{REF} = V_{SS}, f = 100 MHz, T_A = 25°C, V_{OUT} (DC) = V_{CCQ}/2, V_{OUT} (peak to peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
12. For slew rates less than 1 V/ns and greater than or equal to 0.5 V/ns. If slew rate is less than 0.5 V/ns, timing must be derated: t_{IS} has an additional 50ps per each 100mV/ns reduction in slew rate from 500mV/ns, while t_{IH} is unaffected. If slew rate exceeds 4.5V/ns, functionality is uncertain.
13. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is V_{REF}.
14. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stabilizes, CKE < 0.3 x V_{CCQ} is recognized as LOW.
15. The output timing reference level, as measured at the timing reference point indicated in Note 3, is V_{TT}.
16. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
17. The intent of the Don't Care state after completion of the postamble is the DQS-driven signal should either be high, low, or high-Z and that any signal transition within the input switching region must follow valid input requirements. That is, if DQS transitions high [above V_{IHDC} (MIN)] then it must not transition low (below V_{IHDC}) prior to t_{BOSSH} (MIN).
18. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
19. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITES were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on t_{BOSS}.
20. MIN (t_{RC} or t_{RFC}) for I_{DD} measurements is the smallest multiple of t_{CK} that meets the minimum absolute value for the respective parameter. t_{RAS} (MAX) for I_{DD} measurements is the largest multiple of t_{CK} that meets the maximum absolute value for t_{RAS}.
21. The refresh period 64ms. This equates to an average refresh rate of 7.8125μs. However, an AUTO REFRESH command must be asserted at least once every 70.3μs; burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.
22. The valid data window is derived by achieving other specifications: t_{HP} (t_{CKI2}), t_{BOSSQ}, and t_{QH} (t_{QH} = t_{HP} - t_{QHS}). The data valid window derates directly proportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55, beyond which functionality is uncertain. Figure 8, Derating Data Valid Window t_{HP} - t_{QHS}, shows derating curves for duty cycles ranging between 50/50 and 45/55.
23. Each byte lane has a corresponding DQS.
24. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period (t_{REF} [MIN]) else CKE is LOW (i.e., during standby).
25. To maintain a valid level, the transitioning edge of the input must:
 - a. Sustain a constant slew rate from the current AC level through to the target AC level, V_{IL} (AC) or V_{IH} (AC).
 - b. Reach at least the target AC level.
 - c. After the AC target level is reached, continue to maintain at least the target DC level, V_{IL} (DC) or V_{IH} (DC).
26. JEDEC specifies CK and CK# input slew rate must be ≥ 1V/ns (2V/ns differentially).
27. DQ and DM input slew rates must not deviate from DQS by more than 10 percent. If the DQ/ DM/DQS slew rate is less than 0.5V/ns, timing must be derated: 50ps must be added to t_{DS} and t_{DH} for each 100mV/ns reduction in slew rate. If slew rate exceeds 4V/ns, functionality is uncertain.
28. V_{CC} must not vary more than 4 percent if CKE is not active while any bank is active.
29. The clock is allowed up to ±150ps of jitter. Each timing parameter is allowed to vary by the same amount.
30. t_{HP} min is the lesser of t_{CL} minimum and t_{CH} minimum actually applied to the device CK and CK# inputs, collectively during bank active.
31. READs and WRITEs with auto precharge are not allowed to be issued until t_{RAS} (MIN) can be satisfied prior to the internal precharge command being issued.
32. Any positive glitch in the nominal voltage must be less than 1/3 of the clock and not more than +400mV or 2.9V, whichever is less. Any negative glitch must be less than 1/3 of the clock cycle and not exceed either 300mV or 2.2V, whichever is more positive. However, the DC average cannot be below 2.3V minimum.



33. The voltage levels used are derived from a minimum V_{CC} level and the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.
34. V_{IH} overshoot: $V_{IH} (MAX) = V_{CCQ} + 1.5V$ for a pulse width $\leq 3ns$ and the pulse width can not be greater than 1/3 of the cycle rate. V_{IL} undershoot: $V_{IL} (MIN) = -1.5V$ for a pulse width $\leq 3ns$ and the pulse width can not be greater than 1/3 of the cycle rate.
35. V_{CC} and V_{CCQ} must track each other.
36. $t_{HZ} (MAX)$ takes precedence over $t_{DQCK} (MAX) + t_{RPST} (MAX)$ condition. $t_{LZ} (MIN)$ will prevail over $t_{DQCK} (MIN) + t_{RPRE} (MAX)$ condition.
37. t_{RPST} end point and t_{RPRE} begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (t_{RPST}), or begins driving (t_{RPRE}).
38. During initialization, V_{CCQ} , V_{TT} , and V_{REF} must be equal to or less than $V_{CC} + 0.3V$. Alternatively, V_{TT} may be 1.35V maximum during power up, even if V_{CC}/V_{CCQ} are 0V, provided a minimum of 42Ω of series resistance is used between the V_{TT} supply and the input pin.
39. For 403, 335, 262, 263 and 265 speed grades, I_{DD3N} is specified to be 35mA per DDR SDRAM at 100 MHz.
40. The current part operates below the slowest JEDEC operating frequency of 83 MHz. As such, future die may not reflect this option.
41. Random addressing changing and 50 percent of data changing at every transfer.
42. Random addressing changing and 100 percent of data changing at every transfer.
43. CKE must be active (high) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until t_{REF} later.
44. I_{DD2N} specifies the DQ, DQS, and DM to be driven to a valid high or low logic level. I_{DD2Q} is similar to I_{DD2F} except I_{DD2Q} specifies the address and control inputs to remain stable. Although I_{DD2F} , I_{DD2N} , and I_{DD2Q} are similar, I_{DD2F} is "worst case."
45. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset. This is followed by 200 clock cycles.
46. Leakage number reflects the worst case leakage possible through the module pin, not what each memory device contributes.
47. When an input signal is HIGH or LOW, it is defined as a steady state logic HIGH or logic LOW.
48. The 403 speed grade will operate with $t_{RAS} (MIN) = 40ns$ and $t_{RAS} (MAX) = 120,000ns$ at any slower frequency.



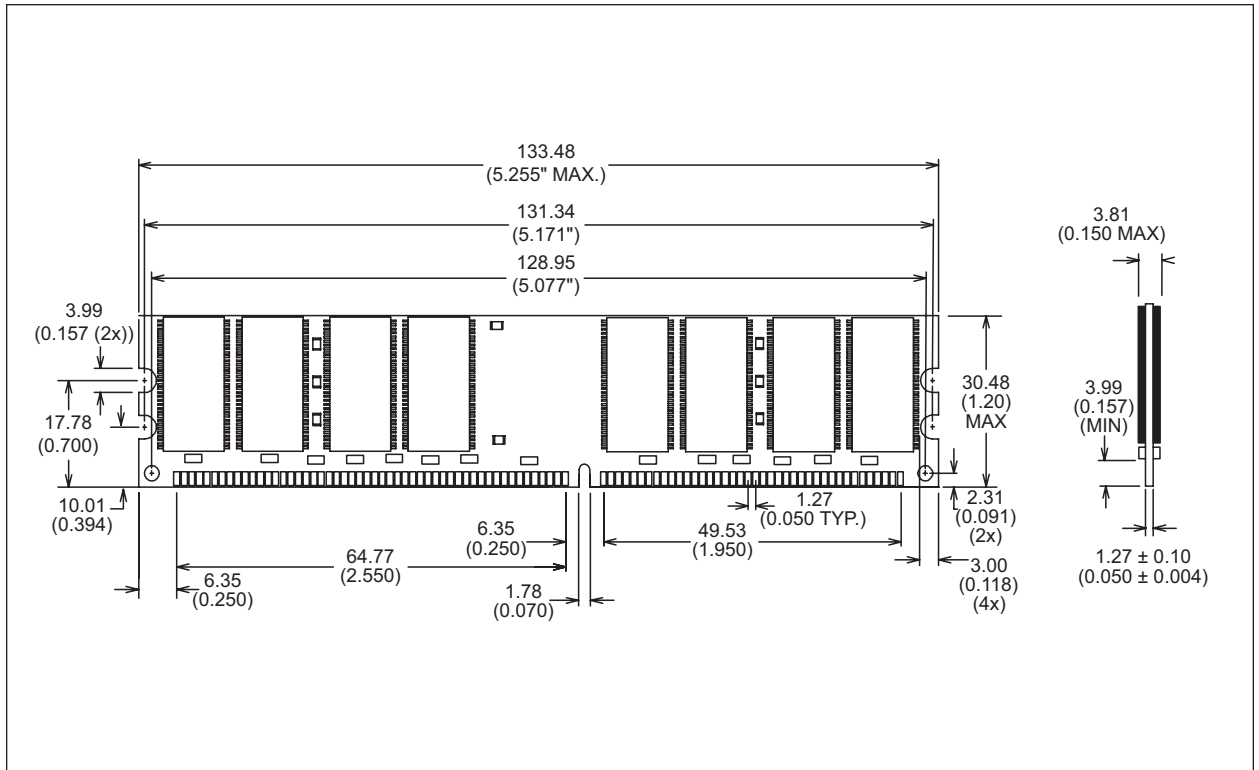
ORDERING INFORMATION FOR JD3

Part Number	Speed	CAS Latency	t _{RC} D	t _{RP}	Height*
W3EG6462S403JD3	200MHz/400Mb/s	3	3	3	30.48 (1.20")
W3EG6462S335JD3	166MHz/333Mb/s	2.5	3	3	30.48 (1.20")
W3EG6462S262JD3	133MHz/266Mb/s	2	2	2	30.48 (1.20")
W3EG6462S263JD3	133MHz/266Mb/s	2	3	3	30.48 (1.20")
W3EG6462S265JD3	133MHz/266Mb/s	2.5	3	3	30.48 (1.20")
W3EG6462S202JD3	100MHz/200Mb/s	2	2	2	30.48 (1.20")

NOTES:

- Consult Factory for availability of RoHS compliant products. (G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR JD3



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)



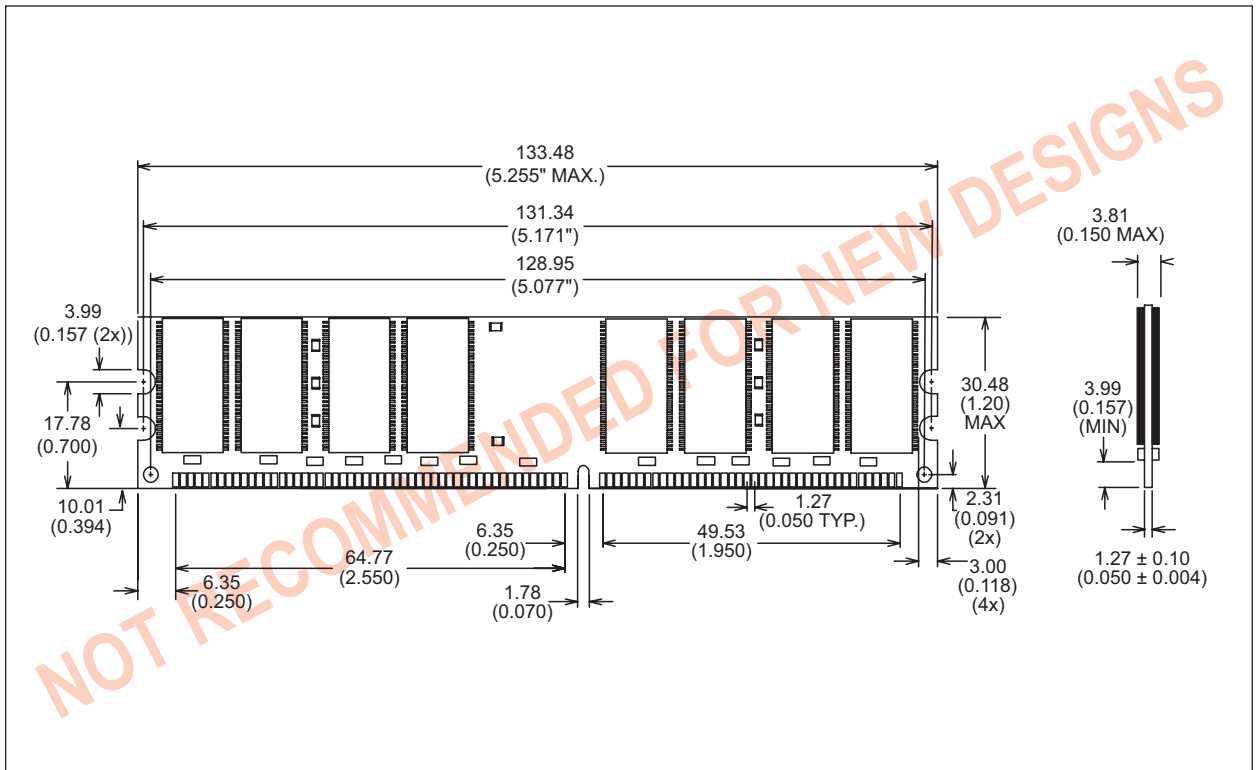
ORDERING INFORMATION FOR D3

Part Number	Speed	CAS Latency	t _{RC} D	t _{RP}	Height*
W3EG6462S403D3	200MHz/400Mb/s	3	3	3	30.48 (1.20")
W3EG6462S335D3	166MHz/333Mb/s	2.5	3	3	30.48 (1.20")
W3EG6462S262D3	133MHz/266Mb/s	2	2	2	30.48 (1.20")
W3EG6462S263D3	133MHz/266Mb/s	2	3	3	30.48 (1.20")
W3EG6462S265D3	133MHz/266Mb/s	2.5	3	3	30.48 (1.20")
W3EG6462S202D3	100MHz/200Mb/s	2	2	2	30.48 (1.20")

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- Consult Factory for availability of RoHS compliant products. (G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR D3



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)



Document Title

512MB – 2x32Mx64, DDR SDRAM UNBUFFERED

Revision History

Rev #	History	Release Date	Status
Rev A	Initial Release	9-20-02	Advanced
Rev 1	1.1 Updated datasheet 1.2 Removed "ED" from part number	5-04	Preliminary
Rev 2	2.1 Added clock speed of 200MHz 2.2 Moved back to Advanced until 200MHz is tested	10-04	Advanced
Rev 3	3.1 Updated module org from 64Mx64 to 2x32M64 3.2 Updated pin configuration 3.3 Added lead-free and RoHS notes 3.4 Added source control notes 3.5 Added industrial temperature note	1-05	Advanced
Rev 4	4.1 Added JEDEC Standard PCB 4.2 D3 "NOT RECOMMENDED FOR NEW DESIGNS"	5-05	Advanced