



## 2GB-256Mx72 DDR SDRAM REGISTERED ECC w/PLL

### FEATURES

- Double-data-rate architecture
- DDR200, DDR266 and DDR333:
  - JEDEC design specifications
- Bi-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency 2,2.5 (clock)
- Programmable Burst Length (2,4,8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input.
- Auto and self refresh
- Serial presence detect
- Power supply:  $V_{CC} = 2.5V \pm 0.20V$
- JEDEC standard 184 pin DIMM package
  - Package height option:
    - JD3: 30.48mm (1.20")
    - AJD3: 28.70mm (1.13")
  - Consult factory for availability of lead-free products.

### DESCRIPTION

The W3EG72256S is a 256Mx72 Double Data Rate SDRAM memory module based on 1Gb DDR SDRAM components. The module consists of eighteen 1Gb DDR SDRAMs in 66 pin TSOP packages mounted on a 184 pin FR4 substrate.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges and Burst Lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

\* This product is under development, is not qualified or characterized and is subject to change without notice.

### OPERATING FREQUENCIES

	DDR333 @CL=2.5	DDR266 @CL=2	DDR266 @CL=2	DDR266 @CL=2.5	DDR200 @CL=2
Clock Speed	166MHz	133MHz	133MHz	133MHz	100MHz
CL-tRCD-tRP	2.5-3-3	2-2-2	2-3-3	2.5-3-3	2-2-2

Advance information: Speed may not be available.



### PIN CONFIGURATION

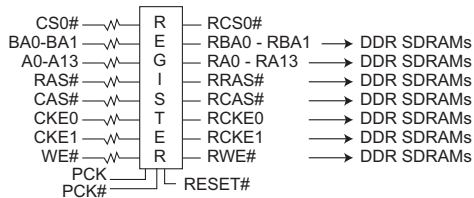
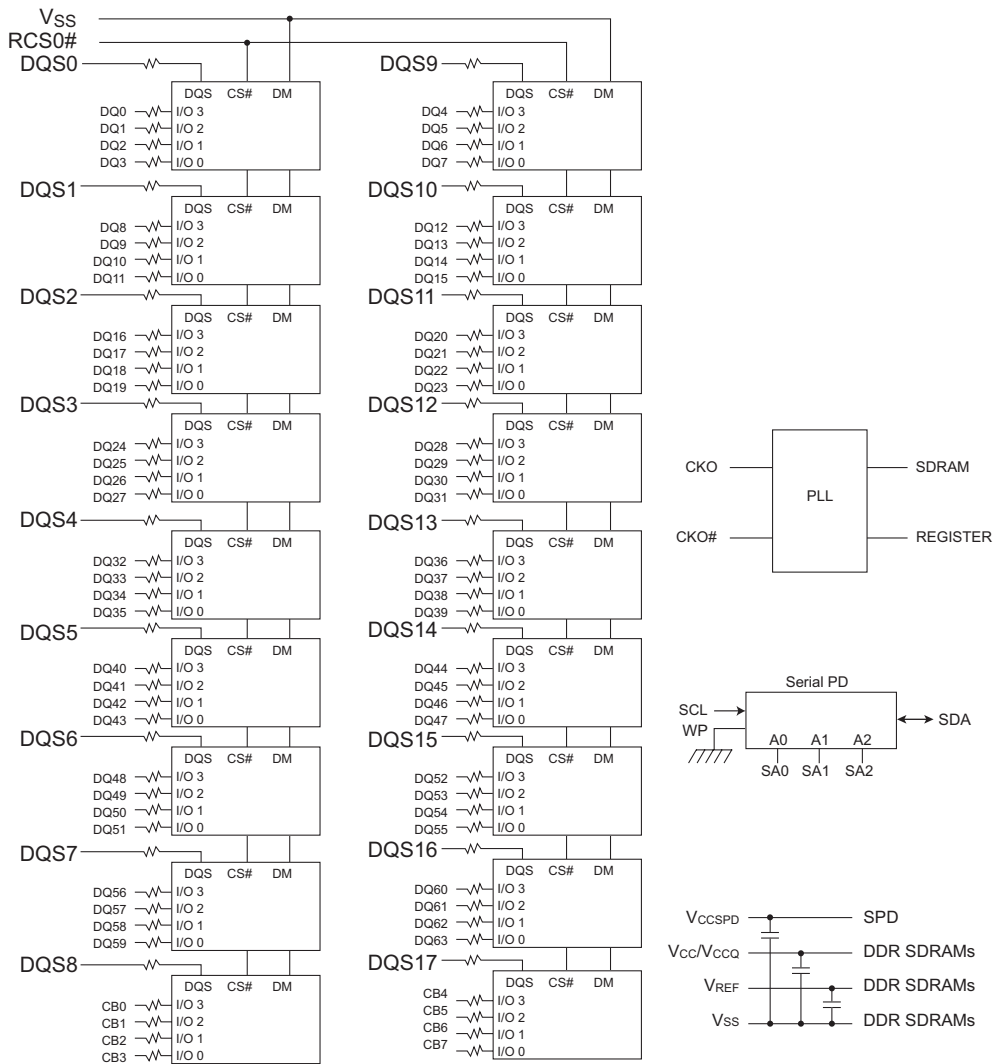
PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VREF	47	DQS8	93	Vss	139	Vss
2	DQ0	48	A0	94	DQ4	140	DQS17
3	Vss	49	CB2	95	DQ5	141	A10
4	DQ1	50	Vss	96	Vccq	142	CB6
5	DQS0	51	CB3	97	DQS9	143	Vccq
6	DQ2	52	BA1	98	DQ6	144	CB7
7	Vcc	53	DQ32	99	DQ7	145	Vss
8	DQ3	54	Vccq	100	Vss	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	RESET#	56	DQS4	102	NC	148	Vcc
11	Vss	57	DQ34	103	NC	149	DQS13
12	DQ8	58	Vss	104	Vccq	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	Vss
15	Vccq	61	DQ40	107	DQS10	153	DQ44
16	NC	62	Vccq	108	Vcc	154	RAS#
17	NC	63	WE#	109	DQ14	155	DQ45
18	Vss	64	DQ41	110	DQ15	156	Vccq
19	DQ10	65	CAS#	111	CKE1	157	CS0#
20	DQ11	66	Vss	112	Vccq	158	NC
21	CKE0	67	DQS5	113	NC	159	DQS14
22	Vccq	68	DQ42	114	DQ20	160	Vss
23	DQ16	69	DQ43	115	A12	161	DQ46
24	DQ17	70	Vcc	116	Vss	162	DQ47
25	DQS2	71	NC	117	DQ21	163	NC
26	Vss	72	DQ48	118	A11	164	Vccq
27	A9	73	DQ49	119	DQS11	165	DQ52
28	DQ18	74	Vss	120	Vcc	166	DQ53
29	A7	75	NC	121	DQ22	167	A13
30	Vccq	76	NC	122	A8	168	Vcc
31	DQ19	77	Vccq	123	DQ23	169	DQS15
32	A5	78	DQS6	124	Vss	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	Vss	80	DQ51	126	DQ28	172	Vccq
35	DQ25	81	Vss	127	DQ29	173	NC
36	DQS3	82	Vccid	128	Vccq	174	DQ60
37	A4	83	DQ56	129	DQS12	175	DQ61
38	Vcc	84	DQ57	130	A3	176	Vss
39	DQ26	85	Vcc	131	DQ30	177	DQS16
40	DQ27	86	DQS7	132	Vss	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	Vss	88	DQ59	134	CB4	180	Vccq
43	A1	89	Vss	135	CB5	181	SA0
44	CB0	90	NC	136	Vccq	182	SA1
45	CB1	91	SDA	137	CK0	183	SA2
46	Vcc	92	SCL	138	CK0#	184	Vccspd

### PIN NAMES

A0-A13	Address input (Multiplexed)
BA0-BA1	Bank Select Address
DQ0-DQ63	Data Input/Output
CB0-CB7	Check bits
DQS0-DQS17	Data Strobe Input/Output
CK0	Clock Input
CK0#	Clock Input
CKE0, CKE1	Clock Enable input
CS0#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
Vcc	Power Supply
Vccq	Power Supply for DQS
Vss	Ground
VREF	Power Supply for Reference
Vccspd	Serial EEPROM Power Supply
SDA	Serial data I/O
SCL	Serial clock
SA0-SA2	Address in EEPROM
Vccid	Vcc Identification Flag
NC	No Connect
RESET#	Reset Enable



## FUNCTIONAL BLOCK DIAGRAM



Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.

NOTE: All resistor values are 22 ohms unless otherwise specified



**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Units
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to 3.6	V
Voltage on Vcc supply relative to Vss	V <sub>CC</sub> , V <sub>CCQ</sub>	-1.0 to 3.6	V
Storage Temperature	T <sub>STG</sub>	-55 to +150	°C
Power Dissipation	P <sub>D</sub>	27	W
Short Circuit Current	I <sub>OS</sub>	50	mA

Note: Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability

**DC CHARACTERISTICS**

0°C ≤ T<sub>A</sub> ≤ 70°C, V<sub>CC</sub> = 2.5V ± 0.2V

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	2.3	2.7	V
Supply Voltage	V <sub>CCQ</sub>	2.3	2.7	V
Reference Voltage	V <sub>REF</sub>	1.15	1.35	V
Termination Voltage	V <sub>TT</sub>	1.15	1.35	V
Input High Voltage	V <sub>IH</sub>	V <sub>REF</sub> + 0.15	V <sub>CCQ</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.3	V <sub>REF</sub> - 0.15	V
Output High Voltage	V <sub>OH</sub>	V <sub>TT</sub> + 0.76	—	V
Output Low Voltage	V <sub>OL</sub>	—	V <sub>TT</sub> -0.76	V

**CAPACITANCE**

T<sub>A</sub> = 25°C. f = 1MHz, V<sub>CC</sub> = 2.5V ± 0.2V

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A13)	C <sub>IN1</sub>	6.25	pF
Input Capacitance (RAS#,CAS#,WE#)	C <sub>IN2</sub>	6.25	pF
Input Capacitance (CKE0)	C <sub>IN3</sub>	6.25	pF
Input Capacitance (CK0#,CK0)	C <sub>IN4</sub>	5.5	pF
Input Capacitance (CS0#)	C <sub>IN5</sub>	6.25	pF
Input Capacitance (DQM0-DQM8)	C <sub>IN6</sub>	13	pF
Input Capacitance (BA0-BA1)	C <sub>IN7</sub>	6.25	pF
Data input/output capacitance (DQ0-DQ63)(DQS)	C <sub>OUT</sub>	13	pF
Data input/output capacitance (CB0-CB7)	C <sub>OUT</sub>	13	pF



**I<sub>DD</sub> SPECIFICATIONS AND TEST CONDITIONS**

0°C ≤ T<sub>A</sub> ≤ 70°C, V<sub>CCQ</sub> = 2.5V ± 0.2V, V<sub>CC</sub> = 2.5V ± 0.2V

Includes DDR SDRAM component only

Parameter	Symbol	Conditions	DDR333@CL=2.5* Max	DDR266@CL=2, 2.5 Max	DDR200@CL=2 Max	Units
Operating Current	I <sub>DD0</sub>	One device bank; Active - Precharge; t <sub>RC</sub> =t <sub>RC</sub> (MIN); t <sub>CK</sub> =t <sub>CK</sub> (MIN); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two cycles.	2880	2610	2610	mA
Operating Current	I <sub>DD1</sub>	One device bank; Active-Read-Precharge Burst = 2; t <sub>RC</sub> =t <sub>RC</sub> (MIN); t <sub>CK</sub> =t <sub>CK</sub> (MIN); I <sub>OUT</sub> = 0mA; Address and control inputs changing once per clock cycle.	3510	3240	3240	mA
Precharge Power-Down Standby Current	I <sub>DD2P</sub>	All device banks idle; Power-down mode; t <sub>CK</sub> =t <sub>CK</sub> (MIN); CKE=(low)	180	180	180	mA
Idle Standby Current	I <sub>DD2F</sub>	CS# = High; All device banks idle; t <sub>CK</sub> =t <sub>CK</sub> (MIN); CKE = high; Address and other control inputs changing once per clock cycle. V <sub>IN</sub> = V <sub>REF</sub> for DQ, DQS and DM.	1170	1080	1080	mA
Active Power-Down Standby Current	I <sub>DD3P</sub>	One device bank active; Power-Down mode; t <sub>CK</sub> (MIN); CKE=(low)	630	540	540	mA
Active Standby Current	I <sub>DD3N</sub>	CS# = High; CKE = High; One device bank; Active-Precharge; t <sub>RC</sub> =t <sub>RAS</sub> (MAX); t <sub>CK</sub> =t <sub>CK</sub> (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.	900	810	810	mA
Operating Current	I <sub>DD4R</sub>	Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; T <sub>CK</sub> = T <sub>CK</sub> (MIN); I <sub>OUT</sub> = 0mA.	3960	3600	3600	mA
Operating Current	I <sub>DD4W</sub>	Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; t <sub>CK</sub> =t <sub>CK</sub> (MIN); DQ, DM and DQS inputs changing once per clock cycle.	4140	3780	3780	mA
Auto Refresh Current	I <sub>DD5</sub>	t <sub>RC</sub> = t <sub>RC</sub> (MIN)	6120	5940	5940	mA
Self Refresh Current	I <sub>DD6</sub>	CKE ≤ 0.2V	162	162	162	mA
Operating Current	I <sub>DD7A</sub>	Four bank interleaving Reads (BL=4) with auto precharge with t <sub>RC</sub> =t <sub>RC</sub> (MIN); t <sub>CK</sub> =t <sub>CK</sub> (MIN); Address and control inputs change only during Active Read or Write commands.	9450	8730	8730	mA



**I<sub>DD</sub> SPECIFICATIONS AND TEST CONDITIONS**

0°C ≤ T<sub>A</sub> ≤ 70°C, V<sub>CCQ</sub> = 2.5V ± 0.2V, V<sub>CC</sub> = 2.5V ± 0.2V

Includes PLL and register power

Parameter	Symbol	Conditions	DDR333@CL=2.5* Max	DDR266@CL=2, 2.5 Max	DDR200@CL=2 Max	Units
Operating Current	I <sub>DD0</sub>	One device bank; Active - Precharge; t <sub>RC</sub> =t <sub>RC</sub> (MIN); t <sub>CK</sub> =t <sub>CK</sub> (MIN); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two cycles.	3155	2885	2885	mA
Operating Current	I <sub>DD1</sub>	One device bank; Active-Read-Precharge Burst = 2; t <sub>RC</sub> =t <sub>RC</sub> (MIN); t <sub>CK</sub> =t <sub>CK</sub> (MIN); I <sub>OUT</sub> = 0mA; Address and control inputs changing once per clock cycle.	3785	3515	3515	mA
Precharge Power-Down Standby Current	I <sub>DD2P</sub>	All device banks idle; Power-down mode; t <sub>CK</sub> =t <sub>CK</sub> (MIN); CKE=(low)	180	180	180	mA
Idle Standby Current	I <sub>DD2F</sub>	CS# = High; All device banks idle; t <sub>CK</sub> =t <sub>CK</sub> (MIN); CKE = high; Address and other control inputs changing once per clock cycle. V <sub>IN</sub> = V <sub>REF</sub> for DQ, DQS and DM.	1480	1390	1390	mA
Active Power-Down Standby Current	I <sub>DD3P</sub>	One device bank active; Power-Down mode; t <sub>CK</sub> (MIN); CKE=(low)	630	540	540	mA
Active Standby Current	I <sub>DD3N</sub>	CS# = High; CKE = High; One device bank; Active-Precharge; t <sub>RC</sub> =t <sub>RAS</sub> (MAX); t <sub>CK</sub> =t <sub>CK</sub> (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.	1210	1120	1120	mA
Operating Current	I <sub>DD4R</sub>	Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; T <sub>CK</sub> = T <sub>CK</sub> (MIN); I <sub>OUT</sub> = 0mA.	4235	3875	3875	mA
Operating Current	I <sub>DD4W</sub>	Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; t <sub>CK</sub> =t <sub>CK</sub> (MIN); DQ, DM and DQS inputs changing once per clock cycle.	4415	4055	4055	mA
Auto Refresh Current	I <sub>DD5</sub>	t <sub>RC</sub> = t <sub>RC</sub> (MIN)	6430	6250	6250	mA
Self Refresh Current	I <sub>DD6</sub>	CKE ≤ 0.2V	472	472	472	mA
Operating Current	I <sub>DD7A</sub>	Four bank interleaving Reads (BL=4) with auto precharge with t <sub>RC</sub> =t <sub>RC</sub> (MIN); t <sub>CK</sub> =t <sub>CK</sub> (MIN); Address and control inputs change only during Active Read or Write commands.	9725	9005	9005	mA



**DETAILED TEST CONDITIONS FOR DDR SDRAM I<sub>DD1</sub> & I<sub>DD7A</sub>**

**I<sub>DD1</sub> : Operating Current : One Bank**

1. Typical Case :  $V_{CC} = 2.5V, T = 25^{\circ}C$
2. Worst Case :  $V_{CC} = 2.7V, T = 10^{\circ}C$
3. Only one bank is accessed with  $t_{RC}$  (min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle.  $I_{OUT} = 0mA$
4. Timing Patterns :
  - DDR200 (100 MHz, CL = 2) :  $t_{CK} = 10ns, CL2, BL=4, t_{RCD} = 2*t_{CK}, t_{RAS} = 5*t_{CK}$   
Read : A0 N R0 N N P0 N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
  - DDR266 (133MHz, CL=2.5) :  $t_{CK} = 7.5ns, CL = 2.5, BL = 4, t_{RCD} = 3*t_{CK}, t_{RC} = 9*t_{CK}, t_{RAS} = 5*t_{CK}$   
Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
  - DDR266 (133MHz, CL = 2) :  $t_{CK} = 7.5ns, CL = 2, BL = 4, t_{RCD} = 3*t_{CK}, t_{RC} = 9*t_{CK}, t_{RAS} = 5*t_{CK}$   
Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
  - DDR333 (166MHz, CL = 2.5) :  $t_{CK} = 6ns, BL = 4, t_{RCD} = 10*t_{CK}, t_{RAS} = 7*t_{CK}$   
Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst

**I<sub>DD7A</sub> : Operating Current: Four Banks**

1. Typical Case :  $V_{CC} = 2.5V, T = 25^{\circ}C$
2. Worst Case :  $V_{CC} = 2.7V, T = 10^{\circ}C$
3. Four banks are being interleaved with  $t_{RC}$  (min), Burst Mode, Address and Control inputs on NOP edge are not changing.  $I_{OUT}=0mA$
4. Timing Patterns :
  - DDR200 (100 MHz, CL = 2) :  $t_{CK} = 10ns, CL2, BL = 4, t_{RRD} = 2*t_{CK}, t_{RCD} = 3*t_{CK}$ , Read with Autoprecharge  
Read : A0 N A1 R0 A2 R1 A3 R2 A0 R3 A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
  - DDR266 (133MHz, CL = 2.5) :  $t_{CK} = 7.5ns, CL = 2.5, BL = 4, t_{RRD} = 3*t_{CK}, t_{RCD} = 3*t_{CK}$   
Read with Autoprecharge  
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
  - DDR266 (133MHz, CL = 2) :  $t_{CK} = 7.5ns, CL2 = 2, BL = 4, t_{RRD} = 2*t_{CK}, t_{RCD} = 2*t_{CK}$   
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
  - DDR333 (166MHz, CL=2.5) :  $t_{CK}=6ns, BL=4, t_{RRD}=3*t_{CK}, t_{RCD}=3*t_{CK}$ , Read with Autoprecharge  
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst

Legend : A = Activate, R = Read, W = Write, P = Precharge, N = NOP

A (0-3) = Activate Bank 0-3

R (0-3) = Read Bank 0-3



**DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND  
RECOMMENDED AC OPERATING CONDITIONS**

0°C ≤ T<sub>A</sub> ≤ +70°C; V<sub>CC</sub> = +2.5V ±0.2V, V<sub>CCQ</sub> = +2.5V ±0.2V

AC Characteristics			335		262/263/265		202			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Units	Notes	
Access window of DQs from CK, CK#	t <sub>AC</sub>	-0.7	+0.7	-0.75	+0.75	-0.8	+0.8	ns		
CK high-level width	t <sub>CH</sub>	0.45	0.55	0.45	0.55	0.45	0.55	t <sub>CK</sub>	16	
CK low-level width	t <sub>CL</sub>	0.45	0.55	0.45	0.55	0.45	0.55	t <sub>CK</sub>	16	
Clock cycle time	CL=2.5 t <sub>CK</sub> (2.5)	6	13	7.5	13	8	13	ns	22	
	CL=2 t <sub>CK</sub> (2)	7.5	13	7.5	13	10	13	ns	22	
DQ and DM input hold time relative to DQS	t <sub>DH</sub>	0.45		0.5		0.6		ns	14,17	
DQ and DM input setup time relative to DQS	t <sub>DS</sub>	0.45		0.5		0.6		ns	14,17	
DQ and DM input pulse width (for each input)	t <sub>DIPW</sub>	1.75		1.75		2		ns	17	
Access window of DQS from CK, CK#	t <sub>DQSK</sub>	-0.60	+0.60	-0.75	+0.75	-0.8	+0.8	ns		
DQS input high pulse width	t <sub>DQSH</sub>	0.35		0.35		0.35		t <sub>CK</sub>		
DQS input low pulse width	t <sub>DQSL</sub>	0.35		0.35		0.35		t <sub>CK</sub>		
DQS-DQ skew, DQS to last DQ valid, per group, per access	t <sub>DQSQ</sub>		0.45		0.5		0.5	ns	13,14	
Write command to first DQS latching transition	t <sub>DQSS</sub>	0.75	1.25	0.75	1.25	0.75	1.25	t <sub>CK</sub>		
DQS falling edge to CK rising - setup time	t <sub>DSS</sub>	0.2		0.2		0.2		t <sub>CK</sub>		
DQS falling edge from CK rising - hold time	t <sub>DSH</sub>	0.2		0.2		0.2		t <sub>CK</sub>		
Half clock period	t <sub>HP</sub>	t <sub>CH</sub> , t <sub>CL</sub>		t <sub>CH</sub> , t <sub>CL</sub>		t <sub>CH</sub> , t <sub>CL</sub>		ns	18	
Data-out high-impedance window from CK, CK#	t <sub>HZ</sub>		+0.70		+0.75		+0.8	ns	8,19	
Data-out low-impedance window from CK, CK#	t <sub>LZ</sub>	-0.70		-0.75		-0.8		ns	8,20	
Address and control input hold time (fast slew rate)	t <sub>HF</sub>	0.75		0.90		1.1		ns	6	
Address and control input set-up time (fast slew rate)	t <sub>HF</sub>	0.75		0.90		1.1		ns	6	
Address and control input hold time (slow slew rate)	t <sub>HS</sub>	0.80		1		1.1		ns	6	
Address and control input setup time (slow slew rate)	t <sub>HS</sub>	0.80		1		1.1		ns	6	
Address and control input pulse width (for each input)	t <sub>IPW</sub>	2.2		2.2		2.2		ns		
LOAD MODE REGISTER command cycle time	t <sub>MRD</sub>	12		15		16		ns		
DQ-DQS hold, DQS to first DQ to go non-valid, per access	t <sub>QH</sub>	t <sub>HP</sub> -t <sub>QHS</sub>		t <sub>HP</sub> -t <sub>QHS</sub>		t <sub>HP</sub> -t <sub>QHS</sub>		ns	13,14	
Data hold skew factor	t <sub>QHS</sub>		0.55		0.75		0.75	ns		
ACTIVE to PRECHARGE command	t <sub>RAS</sub>	42	70,000	40	120,000	40	120,000	ns	15	
ACTIVE to READ with Auto precharge command	t <sub>RAP</sub>	15		15		15		ns		
ACTIVE to ACTIVE/AUTO REFRESH command period	t <sub>RC</sub>	60		65		70		ns		
AUTO REFRESH command period	t <sub>RFC</sub>	75		75		75		ns	21	





**DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND  
RECOMMENDED AC OPERATING CONDITIONS (continued)**

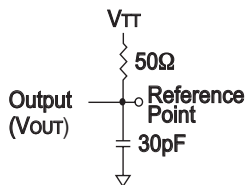
0°C ≤ T<sub>A</sub> ≤ +70°C; V<sub>CC</sub> = +2.5V ±0.2V, V<sub>CCQ</sub> = +2.5V ±0.2V

AC Characteristics		335		262/263/265		202			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Units	Notes
ACTIVE to READ or WRITE delay	t <sub>RC</sub> D	15		15		15		ns	
PRECHARGE command period	t <sub>RP</sub>	15		15		15		ns	
DQS read preamble	t <sub>RP</sub> RE	0.9	1.1	0.9	1.1	0.9	1.1	t <sub>CK</sub>	19
DQS read postamble	t <sub>RP</sub> ST	0.4	0.6	0.4	0.6	0.4	0.6	t <sub>CK</sub>	
ACTIVE bank a to ACTIVE bank b command	t <sub>RR</sub> D	12		15		15		ns	
DQS write preamble	t <sub>WP</sub> RE	0.25		0.25		0.25		t <sub>CK</sub>	
DQS write preamble setup time	t <sub>WP</sub> RES	0		0		0		ns	10,11
DQS write postamble	t <sub>WP</sub> ST	0.4	0.6	0.4	0.6	0.4	0.6	t <sub>CK</sub>	9
Write recovery time	t <sub>WR</sub>	15		15		15		ns	
Internal WRITE to READ command delay	t <sub>W</sub> TR	1		1		1		t <sub>CK</sub>	
Data valid output window	NA	t <sub>QH</sub> -t <sub>basq</sub>		t <sub>QH</sub> -t <sub>basq</sub>		t <sub>QH</sub> -t <sub>basq</sub>		ns	13
REFRESH to REFRESH command interval	t <sub>REF</sub> C		70.3		70.3		70.3	μs	12
Average periodic refresh interval	t <sub>REF</sub> I		7.8		7.8		7.8	μs	12
Terminating voltage delay to V <sub>CC</sub>	t <sub>VT</sub> D	0		0		0		ns	
Exit SELF REFRESH to non-READ command	t <sub>X</sub> SNR	126		127.5		127.5		ns	
Exit SELF REFRESH to READ command	t <sub>X</sub> SRD	200		200		200		t <sub>CK</sub>	



### Notes

1. All voltages referenced to  $V_{SS}$
2. Tests for AC timing,  $I_{DD}$ , and electrical AC and DC characteristics may be conducted at normal reference / supply voltage levels, but the related specifications and device operations are guaranteed for the full voltage range specified.
3. Outputs are measured with equivalent load:



4. AC timing and  $I_{DD}$  tests may use a  $V_{IL}$ -to- $V_{IH}$  swing of up to 1.5V in the test environment, but input timing is still referenced to  $V_{REF}$  (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between  $V_{IL}(AC)$  and  $V_{IH}(AC)$ .
5. The AC and DC input level specifications are defined in the SSTL\_2 standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [high] level).
6. For slew rates less than 1V/ns and greater than or equal to 0.5V/ns. If the slew rate is less than 0.5V/ns, timing must be derated:  $t_{IS}$  has an additional 50ps per each 100mV/ns reduction in slew rate from the 500mV/ns.  $t_{IH}$  has 0ps added, that is, it remains constant. If the slew rate exceeds 4.5V/ns, functionality is uncertain. For 335, slew rates must be greater than or equal to 0.5V/ns.
7. Inputs are not recognized as valid until  $V_{REF}$  stabilizes. Exception: during the period before  $V_{REF}$  stabilizes,  $CKE \leq 0.3 \times V_{CCQ}$  is recognized as LOW.
8.  $t_{HZ}$  and  $t_{LZ}$  transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) and begins driving (LZ).
9. The intent of the "Don't Care" state after completion of the postamble is the DQS-driven signal should either be HIGH, LOW, or high-Z, and that any signal transition within the input switching region must follow valid input requirements. That is, if DQS transitions HIGH (above  $V_{IHDC}$  (MIN)) then it must not transition LOW (below  $V_{IHDC}$ ) prior to  $t_{DQSH}$  (MIN).
10. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
11. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITES were previously in progress on the bus. If a previous WRITE was in progress, DQS could be high during this time, depending on  $t_{DQSS}$ .
12. The refresh period is 64ms. This equates to an average refresh rate of 7.8125 $\mu$ s. However, an AUTO REFRESH command must be asserted at least once every 70.3 $\mu$ s; burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.
13. The valid data window is derived by achieving other specifications -  $t_{HP}$  ( $t_{CK}/2$ ),  $t_{DQSQ}$ , and  $t_{QH}$  ( $t_{QH} = t_{HP} - t_{QHS}$ ). The data valid window derates directly proportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycled variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio. The data valid window derating curves are provided below for duty cycles ranging between 50/50 and 45/55.
14. Referenced to each output group: x4 = DQS with DQ0-DQ3.
15. READs and WRITEs with auto precharge are not allowed to be issued until  $t_{RAS}$  (MIN) can be satisfied prior to the internal precharge command being issued.
16. JEDEC specifies CK and CK# input slew rate must be  $\geq 1V/ns$  (2V/ns differentially).
17. DQ and DM input slew rates must not deviate from DQS by more than 10%. If the DQ/DM/DQS slew rate is less than 0.5V/ns, timing must be derated: 50ps must be added to  $t_{DS}$  and  $t_{DH}$  for each 100mV/ns reduction in slew rate. If slew rates exceed 4V/ns, functionality is uncertain.
18.  $t_{HP}$  min is the lesser of  $t_{CL}$  min and  $t_{CH}$  min actually applied to the device CK and CK# inputs, collectively during bank active.
19.  $t_{HZ}$  (MAX) will prevail over the  $t_{DQSQ}$  (MAX) +  $t_{RPST}$  (MAX) condition.  $t_{LZ}$  (MIN) will prevail over  $t_{DQSQ}$  (MIN) + PRE (MAX) condition.
20. For slew rates greater than 1V/ns the (LZ) transition will start about 310ps earlier.
21. CKE must be active (High) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until  $t_{RFC}$  has been satisfied.
22. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset. This is followed by 200 clock cycles (before READ commands).

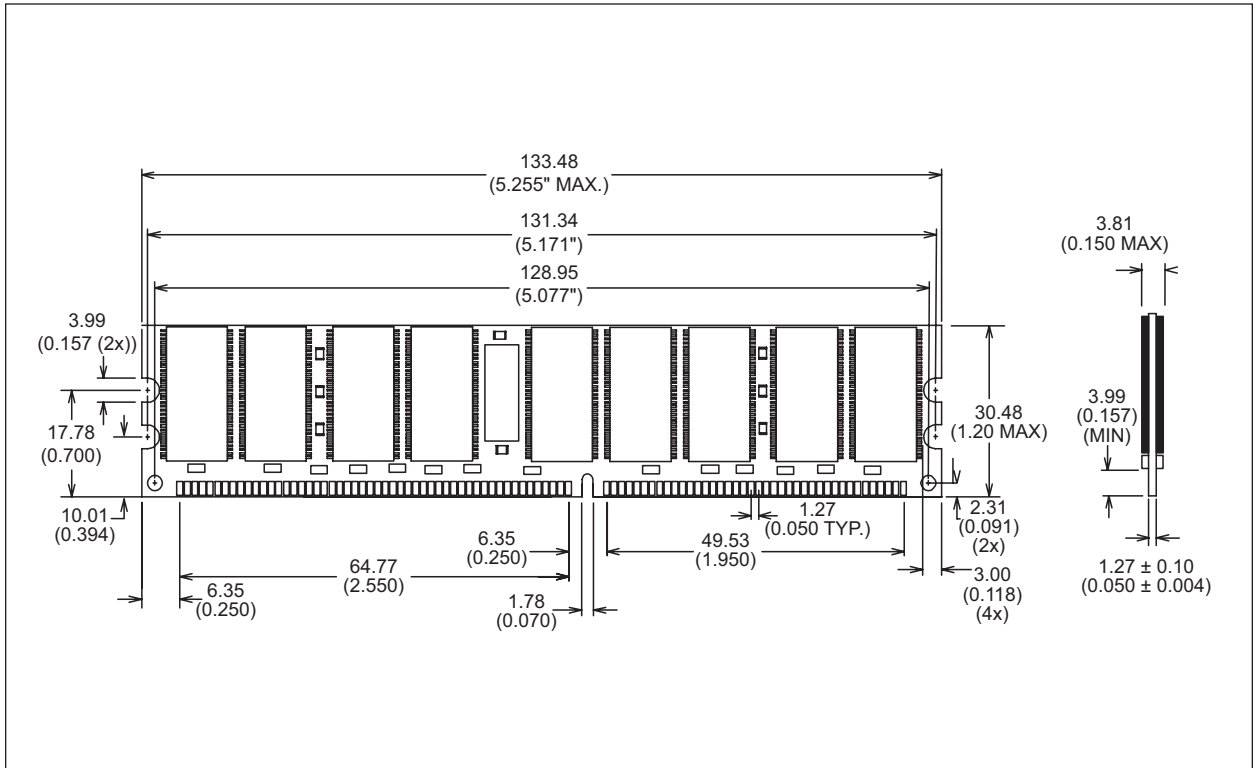


ORDERING INFORMATION FOR JD3

Part Number	Speed	CAS Latency	t <sub>RC</sub> D	t <sub>RP</sub>	Height*
W3EG72256S335JD3	166MHz/133Mb/s	2.5	3	3	30.48 (1.20")
W3EG72256S262JD3	133MHz/266Mb/s	2	2	2	30.48 (1.20")
W3EG72256S263JD3	133MHz/266Mb/s	2	3	3	30.48 (1.20")
W3EG72256S265JD3	133MHz/266Mb/s	2.5	3	3	30.48 (1.20")
W3EG72256S202JD3	100MHz/200Mb/s	2	2	2	30.48 (1.20")

Note: Consult factory for availability of lead-free products. (F = Lead-Free, G = RoHS compliant)  
Vendor Code: M = Micron, S = Samsung

PACKAGE DIMENSIONS FOR JD3



\* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)



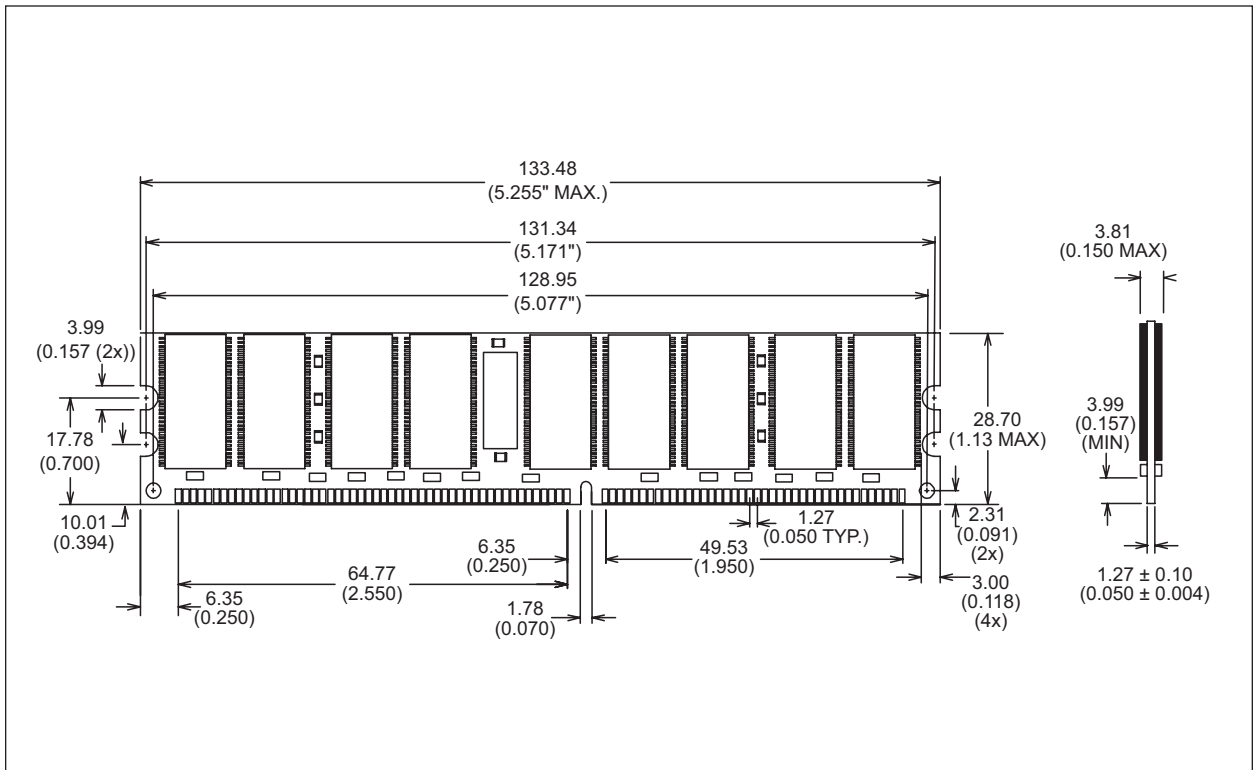
ORDERING INFORMATION FOR AJD3

Part Number	Speed	CAS Latency	trCD	trP	Height*
W3EG72256S335AJD3	166MHz/133Mb/s	2.5	3	3	28.70 (1.13")
W3EG72256S262AJD3	133MHz/266Mb/s	2	2	2	28.70 (1.13")
W3EG72256S263AJD3	133MHz/266Mb/s	2	3	3	28.70 (1.13")
W3EG72256S265AJD3	133MHz/266Mb/s	2.5	3	3	28.70 (1.13")
W3EG72256S202AJD3	100MHz/200Mb/s	2	2	2	28.70 (1.13")

Note: Consult factory for availability of lead-free products. (F = Lead-Free, G = RoHS compliant)

Vendor Code: M = Micron, S = Samsung

PACKAGE DIMENSIONS FOR AJD3

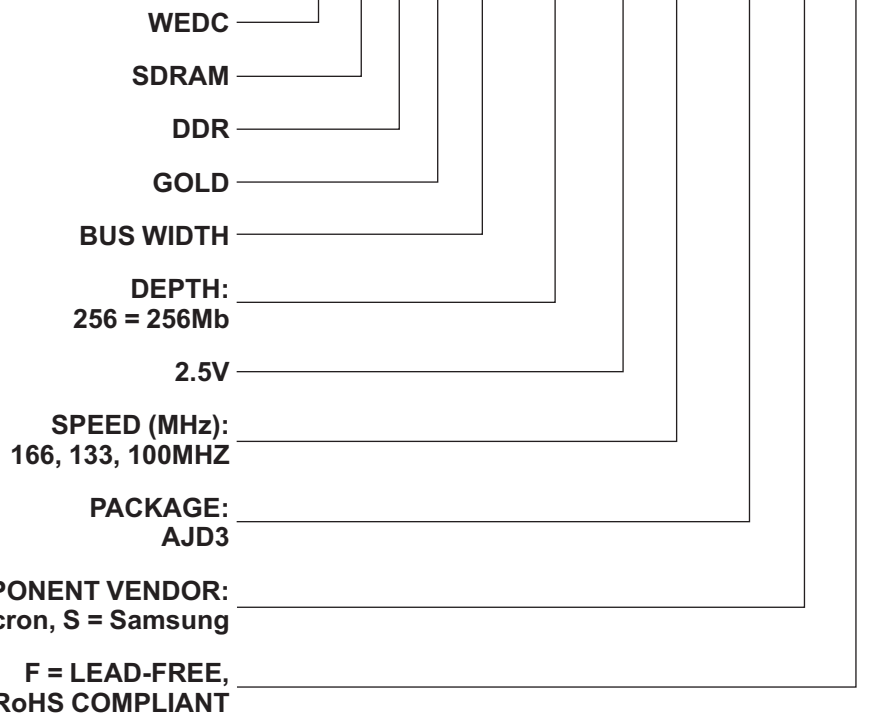


\* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)



**PART NUMBERING GUIDE**

**W 3 E G 72 256M S xxx JD3 x F/G**





## Document Title

2GB - 256Mx72, DDR SDRAM Registered Module, ECC, w/PLL

## Revision History

Rev #	History	Release Date	Status
Rev 0	Initial Release	3-18-02	Advanced
Rev 1	1.1 Added AJD3 package height option 1.2 Removed "ED" from part marking	3-25-04	Preliminary
Rev 2	2.1 Added Lead-Free and RoHS note 2.2 Added vendor code options M = Micron S = Samsung	12-04	Preliminary