STW45NM50

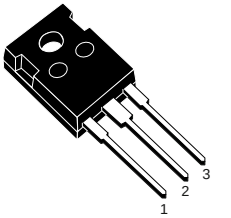
N-CHANNEL 550V @ Tjmax - 0.08Ω - 45A TO-247
MDmesh™ MOSFET

Table 1: General Features

TYPE	V_{DSS} (@Tjmax)	$R_{DS(on)}$	I_D
STW45NM50	550V	< 0.1Ω	45 A

- TYPICAL $R_{DS}(on)$ = 0.08Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE
- TIGHT PROCESS CONTROL AND HIGH MANUFACTURING YIELDS

Figure 1: Package



TO-247

DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

APPLICATIONS

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.

Figure 2: Internal Schematic Diagram

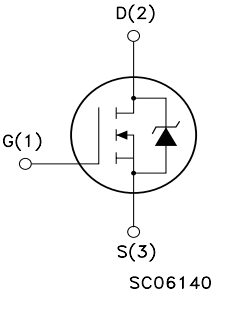


Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STW45NM50	W45NM50	TO-247	TUBE

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source Voltage	±30	V
I_D	Drain Current (continuous) at T_C = 25°C	45	A
I_D	Drain Current (continuous) at T_C = 100°C	28.4	A
I_{DM} (*)	Drain Current (pulsed)	180	A
P_{TOT}	Total Dissipation at T_C = 25°C	417	W
	Derating Factor	2.08	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	15	V/ns
T_{stg}	Storage Temperature	–65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

(*)Pulse width limited by safe operating area
(1)I_{SD} ≤45A, di/dt ≤400A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

Table 4: Thermal Data

Rthj-case	Thermal Resistance Junction-case	Max	0.3	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	30	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		300	°C

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	20	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 35 V)	810	mJ

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)

Table 6: On/Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	500			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			10	µA
		V_{DS} = Max Rating, T_C = 125 °C			100	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ±30 V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V, I_D = 22.5 A		0.08	0.1	Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 7: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (2)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}, I_D = 22.5A$		20		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V$, f = 1 MHz, $V_{GS} = 0$		3700 610 80		pF pF pF
$C_{oss\ eq.}$ (3)	Equivalent Output Capacitance	$V_{GS} = 0V$, $V_{DS} = 0V$ to 400V		325		pF
R_G	Gate Input Resistance	f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		1.7		Ω
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 250V, I_D = 24 A $R_G = 4.7\Omega$ V_{GS} = 10 V (see Figure 14)		40 35		ns ns
$t_{d(off)}$ t_f t_c	Turn-off Delay Time Fall Time Cross-over Time	V_{DD} = 400 V, I_D = 45 A, $R_G = 4.7\Omega$, V_{GS} = 10 V (see Figure 14)		18 23 44		ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 400V, I_D = 45 A, V_{GS} = 10V (see Figure 18)		87 23 42	117	nC nC nC

Table 8: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				45	A
I_{SDM} (3)	Source-drain Current (pulsed)				180	A
V_{SD} (2)	Forward On Voltage	I_{SD} = 45 A, $V_{GS} = 0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 40 A, di/dt = 100A/µs, V_{DD} = 100 V, T_j = 25°C (see Figure 16)		520 7.8 30		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 40 A, di/dt = 100A/µs, V_{DD} = 100 V, T_j = 150°C (see Figure 16)		680 11.2 33		ns µC A

(2)Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

(3)$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Figure 3: Safe Operating Area

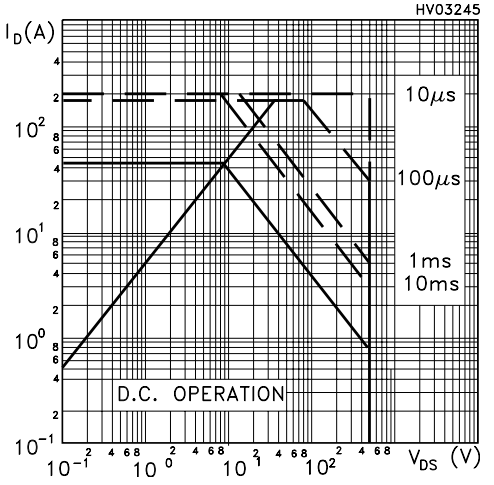


Figure 4: Output Characteristics

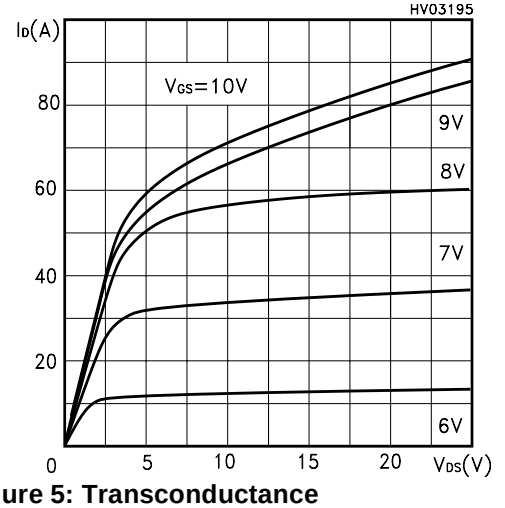


Figure 5: Transconductance

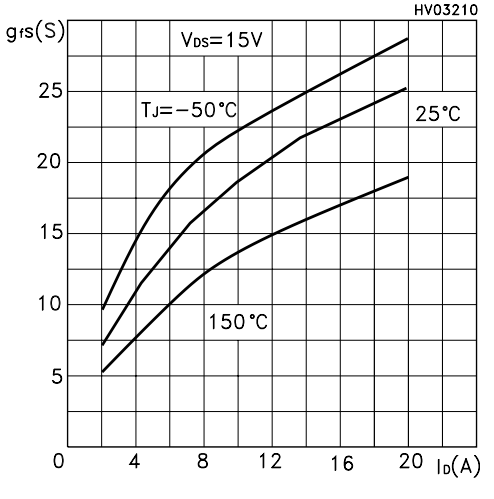


Figure 6: Thermal Impedance

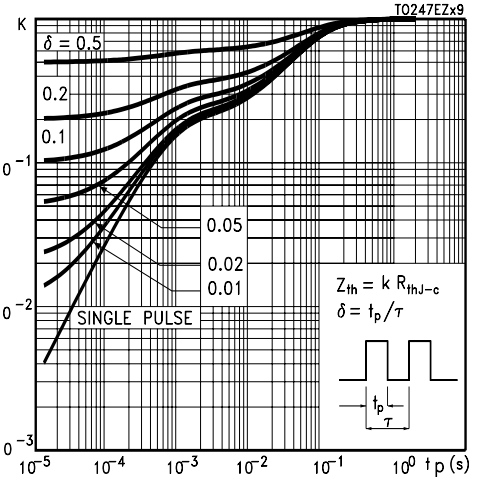


Figure 7: Transfer Characteristics

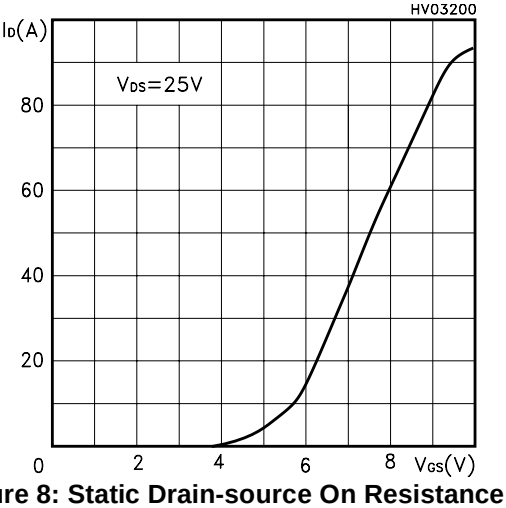


Figure 8: Static Drain-source On Resistance

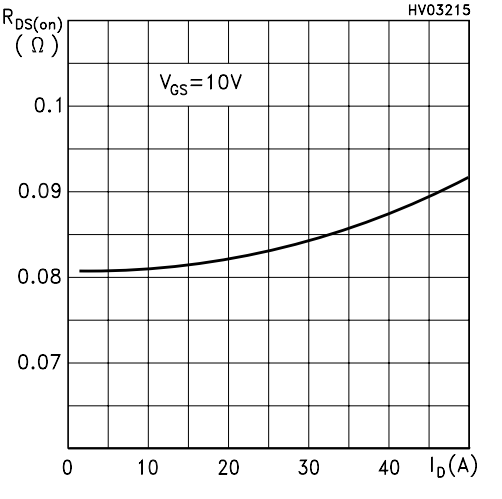


Figure 9: Gate Charge vs Gate-source Voltage

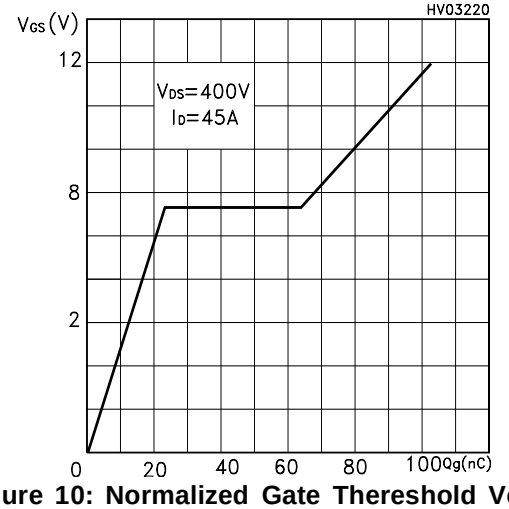


Figure 10: Normalized Gate Thereshold Voltage vs Temperature

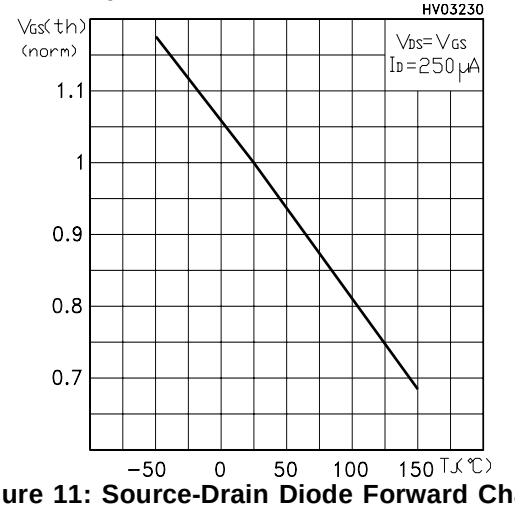


Figure 11: Source-Drain Diode Forward Characteristics

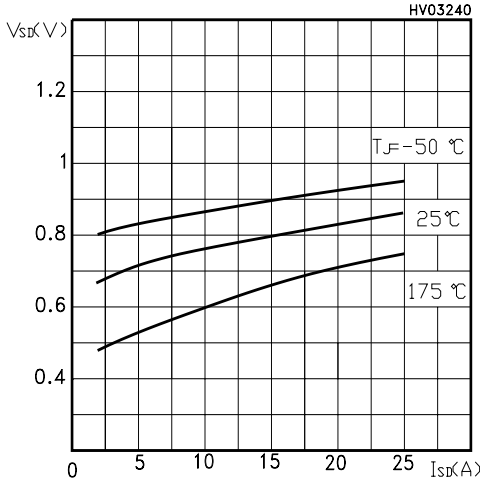


Figure 12: Capacitance Variations

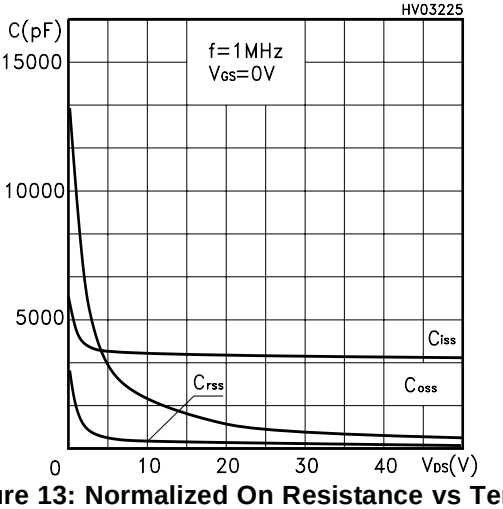


Figure 13: Normalized On Resistance vs Temperature

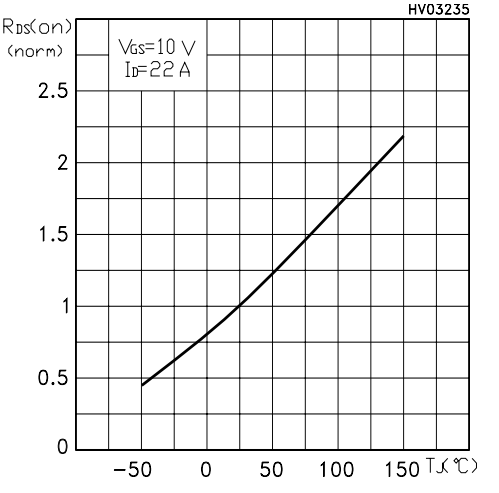


Figure 14: Unclamped Inductive Load Test Circuit

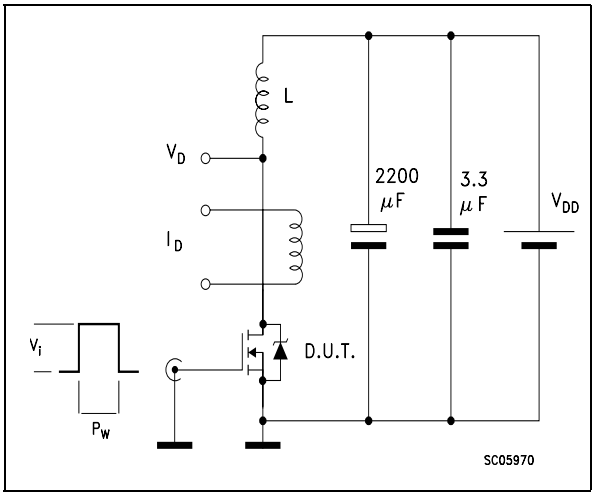


Figure 15: Switching Times Test Circuit For Resistive Load

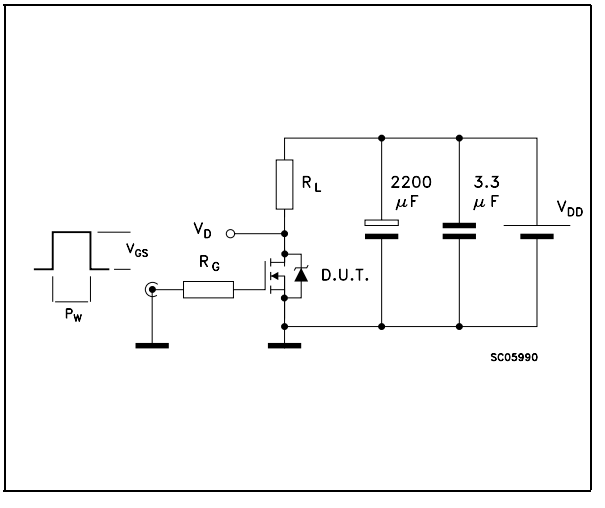


Figure 16: Test Circuit For Inductive Load Switching and Diode Recovery Times

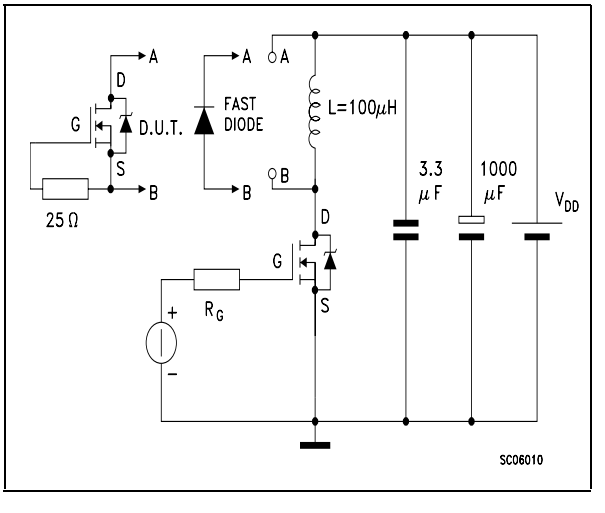


Figure 17: Unclamped Inductive Wafeform

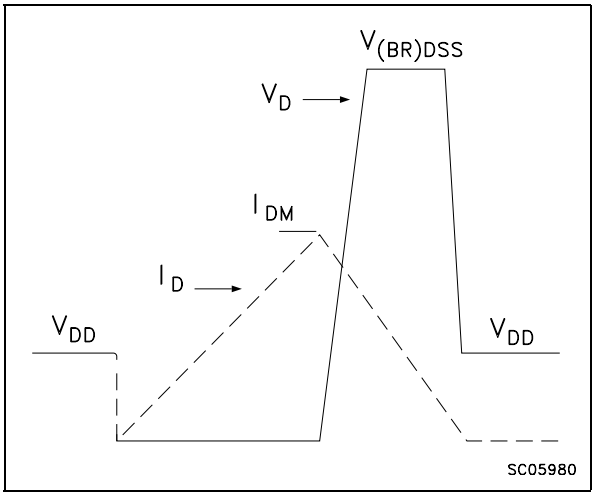
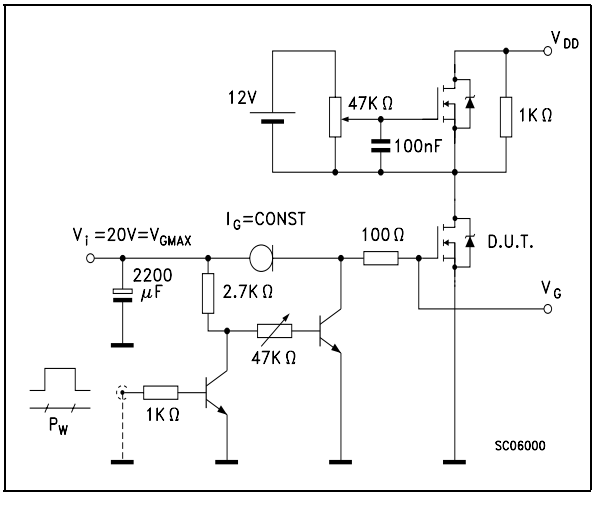


Figure 18: Gate Charge Test Circuit



TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	

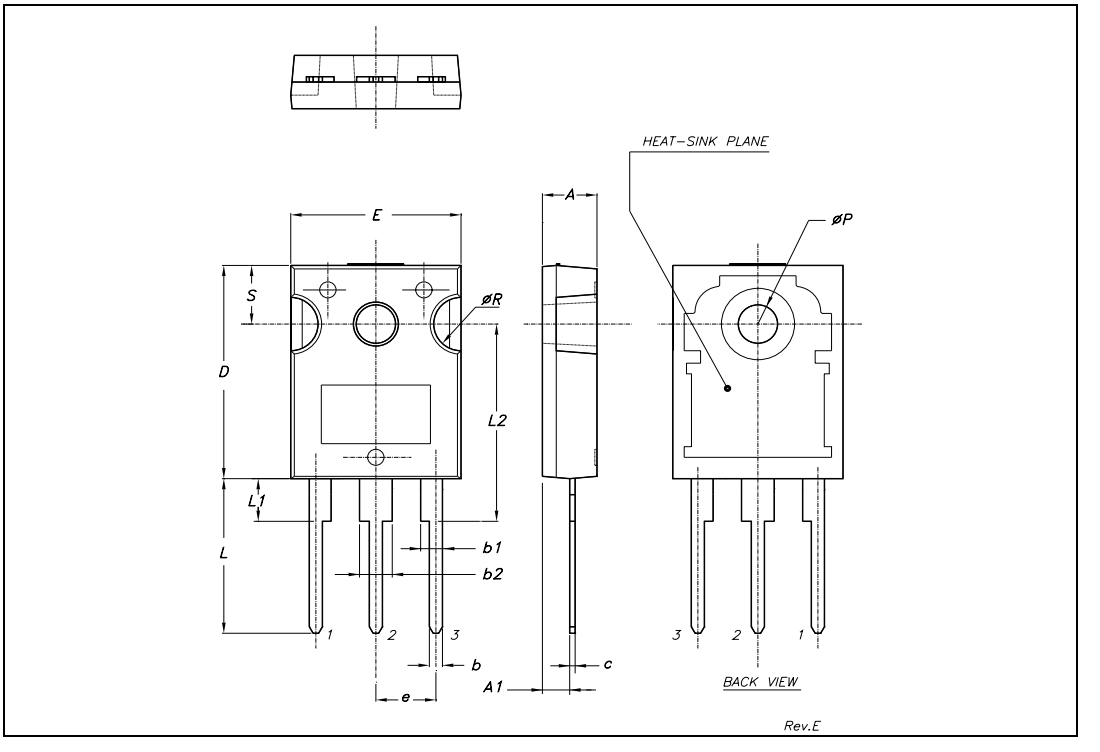


Table 9: Revision History

Date	Revision	Description of Changes
30/Mar/2005	2	Modified value in table 7