W48C20

Audio Subsystem Clock Generator

Features

- **Two independent phase-locked loops**
- **Four independent output frequencies**
- **±250 ps maximum cycle-to-cycle jitter**
- **3 ns rise/fall time (20%-80% V_{DD}).**
- **Options available for a wide range of applications**
- **Supports 3.3V and 5V operation**
- **Low power CMOS design available in:**
  - **8-pin SOIC (Small Outline Integrated Circuit)**

Overview

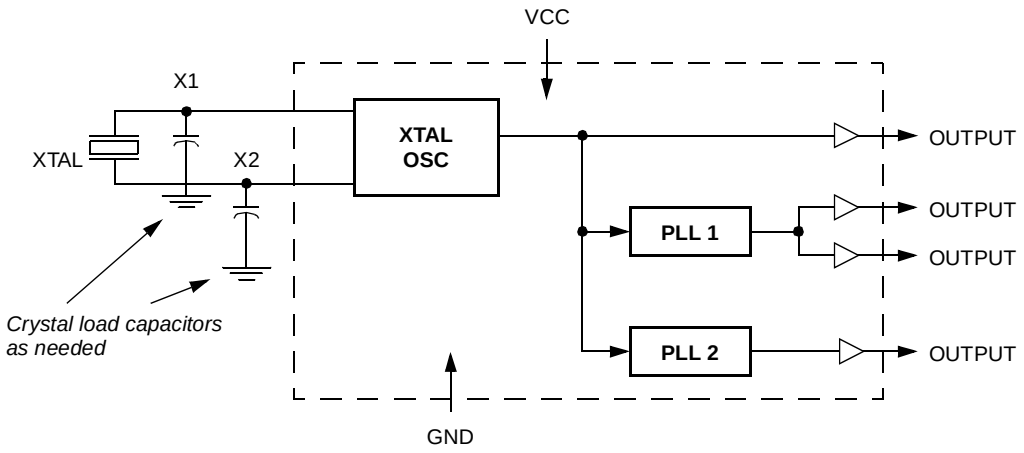
The W48C20 is a general-purpose device that features two phase-locked loops. Through the use of metal masks, the chip can be tailored to a wide variety of applications.

The W48C20 has four clock outputs, each of which is maskable to a different frequency. Because the chip offers four outputs in eight pins, it is suited to applications that require multiple frequencies and have space constraints.

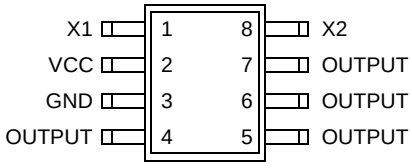
Table 1. Product Selection Guide

Mask	Pin 4	Pin 5	Pin 6	Pin 7	Application
-01A	16.9344	24.576	33.8688	14.318	Audio/Crystal
-08	33.8688	18.432	16.9344	27.00	DVD
-09	40.00	22.50	20.00	25.00	Hard Disk Drives

Functional Block Diagram



Pin Configuration



Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
X1	1	I	Crystal connection or external clock frequency input (14.318 MHz).
VDD	2	P	Power supply connection.
GND	3	P	Ground connection.
OUTPUT	4	O	16.9344-MHZ clock output for stereo codec.
OUTPUT	5	O	24.576-MHz clock output for stereo codec.
OUTPUT	6	O	33.868-MHz clock output for OPL4.
OUTPUT	7	O	14.318-MHz clock buffered output for OPL3 or PCMCIA controller.
X2	8	I	Crystal connection. Leave this pin unconnected when using an external clock.

External Components/Crystal Selection

The W48C20 incorporates a crystal oscillator circuit designed to provide 50% duty cycle over a range of operating conditions, including the addition of external crystal load capacitors to pins X1 and X2. A parallel resonant 14.318-MHz, 12-pF load crystal is recommended. A series-resonant crystal or a parallel resonant crystal specifying a different load can be used, but either will result in frequencies which are slightly different from the ideal (up to 0.06%).

The crystal load capacitance can be increased by adding a capacitor to each of the X1 and X2 pins and ground. This enables the use of a crystal specifying a load greater than 12 pF without changing the output frequency.

Duty cycle is also maintained when using an external clock source (connected to X1, X2 left unconnected) as long as the external clock has good duty cycle. The circuit exhibits about 50% less clock jitter from the 14.318-MHz output when compared to similar devices.

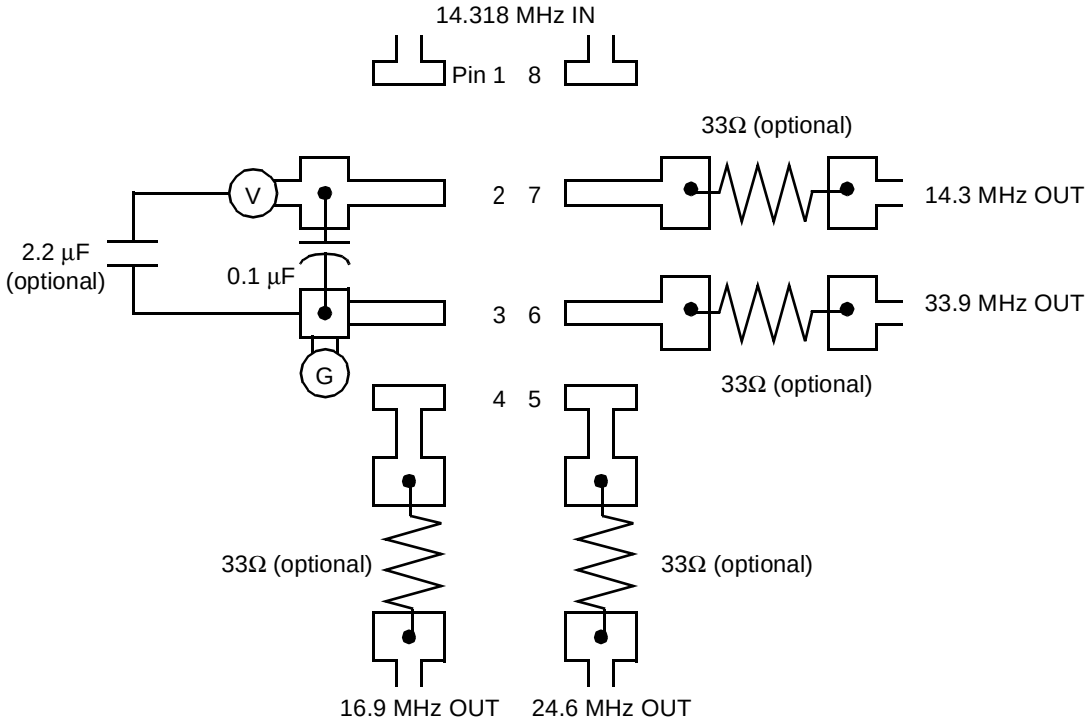


Figure 1. Suggested Layout

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability

Parameter	Description	Rating	Unit
V_{CC}, V_{IN}	Voltage on any Pin with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
T_{SOLD}	Soldering Temperature, Max. 20 seconds	260	°C

Electrical Characteristics at 5.0V

DC Electrical Characteristics: T_A = 0°C to +70°C; V_{CC} = 5V ± 10%

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Operating Voltage		4.5		5.5	V
V_{IH}	Input High Voltage		3.5	2.5		V
V_{IL}	Input Low Voltage			2.5	1.5	V
V_{OH}	Output High Voltage	I_{OH} = 25 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 25 mA			0.4	V
I_{DD}	Operating Supply Current	No Load		18		mA
	Input Capacitance[1]			7		pF
	Actual Mean Frequency versus Target				±0.2	%

AC Characteristics: T_A = 0°C to +70°C; V_{CC} = 5V ± 10%

Parameter	Test Condition/Comments	Min	Typ	Max	Unit
Input Clock Frequency			14.31818		MHz
Input Clock Duty Cycle, 14.318 MHz	Time above 2.5V	20		80	%
Output Clock Rise Time	0.8V to 2.0V			1.5	ns
Output Clock Fall Time	2.0V to 0.8V			1.5	ns
Output Clock Duty Cycle, 24.576 MHz	Time above 1.5V	40	45	60	%
Output Clock Duty Cycle, 16.9344 MHz	Time above 1.5V	45	50	55	%
Output Clock Duty Cycle, 33.868 MHz	Time above 1.5V	45	50	55	%
Output Clock Duty Cycle, 14.318 MHz[2]	Time above 1.5V	45	50	55	%
Absolute Clock Period Jitter, except 14.3	Pins 4, 5, 6 only	–400	200	400	ps
One Sigma Clock Period Jitter, except 14.3	Pins 4, 5, 6 only		60		ps

Notes:

1. If crystal is used as input Crystal Load Capacitance (C_L) = 12 pF.
2. If a clock is used as input, the duty cycle of the 14.318-MHz output will be the same as the input clock.

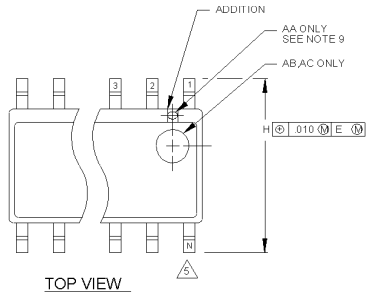
Ordering Information

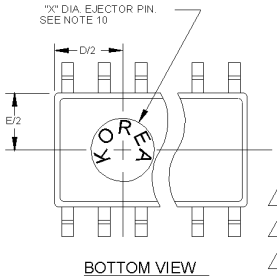
Ordering Code	Freq. Mask Code	Package Name	Package Type
W48C20	01A 08 09	G	8-pin SOIC (150-mil)

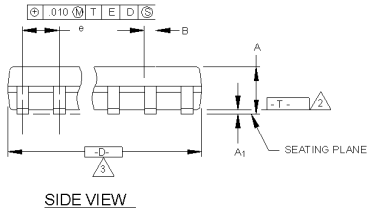
Document #: 38-00879

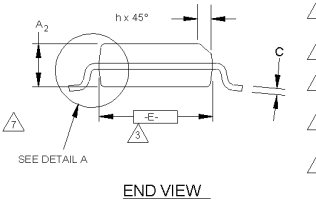
Package Diagram

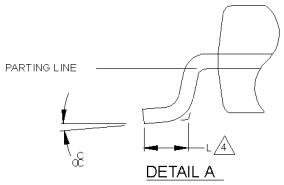
8-Pin Small Outline Integrated Circuit, Narrow (SOIC, 0.150 inch)











NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .015.
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. THE APPEARANCE OF PIN #1 I.D ON THE 8 LD IS OPTIONAL, ROUND TYPE ON SINGLE LEADFRAME AND RECTANGULAR TYPE ON MATRIX LEADFRAME.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPEND ON ASSEMBLY LOCATION.
11. CONTROLLING DIMENSION: INCHES.

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARI-ATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	.061	.064	.068		AA	.189	.194	.196	8
A_1	.004	.006	.0098		AB	.337	.342	.344	14
A_2	.055	.058	.061		AC	.386	.391	.393	16
B	.0138	.016	.0192						
C	.0075	.008	.0098						
D	SEE VARIATIONS			3					
E	.150	.155	.157						
e	.050 BSC								
H	.230	.236	.244						
h	.010	.013	.016						
L	.016	.025	.035						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	.085	.093	.100						

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARI-ATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	1.55	1.63	1.73		AA	4.80	4.93	4.98	8
A_1	0.127	0.15	0.25		AB	8.58	8.69	8.74	14
A_2	1.40	1.47	1.55		AC	9.80	9.93	9.98	16
B	0.35	0.41	0.49						
C	0.19	0.20	0.25						
D	SEE VARIATIONS			3					
E	3.81	3.94	3.99						
e	1.27 BSC								
H	5.84	5.99	6.20						
h	0.25	0.33	0.41						
L	0.41	0.64	0.89						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	2.16	2.36	2.54						