W551CXXX Data Sheet

SERIAL VOICE MEMORY

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1. GENERAL DESCRIPTION

The W551Cxxx series is a serial voice memory IC designed to interface directly with Winbond *PowerSpeech™*, *BandDirector™*, and *ViewTalk™* family ICs to meet the increasing market demand for longer playback duration. The W551Cxxx uses the same three-pin serial interface that Winbond serial flash memory W55Fxx uses, which makes it easier to simulate and verify the memory contents in advance. In addition, the W551Cxxx also provides a "Self-test mode" to verify the voice memory contents easily and quickly, and some members of the W551Cxxx series allow W551Cxxx chips to be “cascaded” to further lengthen playback duration.

W551Cxxx Serial Voice Memory is used to store pre-determined data. The following table shows the part numbers in the W551Cxxx series and their respective memory density.

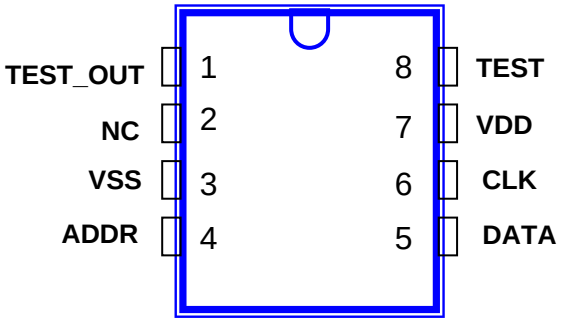
PART #	W551C002	W551C005	W551C010	W551C020	W551C040	W551C060	W551C080
DENSITY	256K bits	512K bits	1M bits	2M bits	4M bits	6M bits	8M bits

PART #	W551C160	W551C240	W551C320
DENSITY	16M bits	24M bits	32M bits

1.1 W551Cxxx Features Description

- Wide range of operating voltages: **2.4 V ~ 5.5 V**
- Operating frequency up to **1 MHz** (@VDD = 2.4 V)
- Versatile operating modes
  Serial read mode
  Serial check-sum output mode (used for manufacturing testing only)
  Fast self-test mode
- Cascading for longer duration applications
- Serial shift-in address bus
- Serial data mode
- Three-pin connection interface: CLK, ADDR, DATA
- Read access time: **500 ns**
- Low power consumption
  Operating current: **5 mA (typ.)**
  Standby current: **2 uA (typ.)**

1.2 W551Cxxx Pad Description



1.2.1 W551C002/005/010/020/040/060/080 Pad Description

PIN NAME	I/O	DESCRIPTION
TEST	I	Internal pull-high. Set TEST low to enable "Self-test" function.
TEST_OUT	O	Indicates the result of self-test process. ”0” indicates a correct result; “1” indicates an incorrect result. At Power-On-Reset, it outputs a logic "1" signal.
ADDR	I	Clock input for shift-in start address; the first rising-edge signal resets the address counter.
DATA	IO	Bi-directional data pin with internal pull-high.
CLK	I	Clock input for data read-out.
VDD	Power	Positive power supply pin.
VSS	Ground	

1.2.2 W551C160/240/320 Pad Description

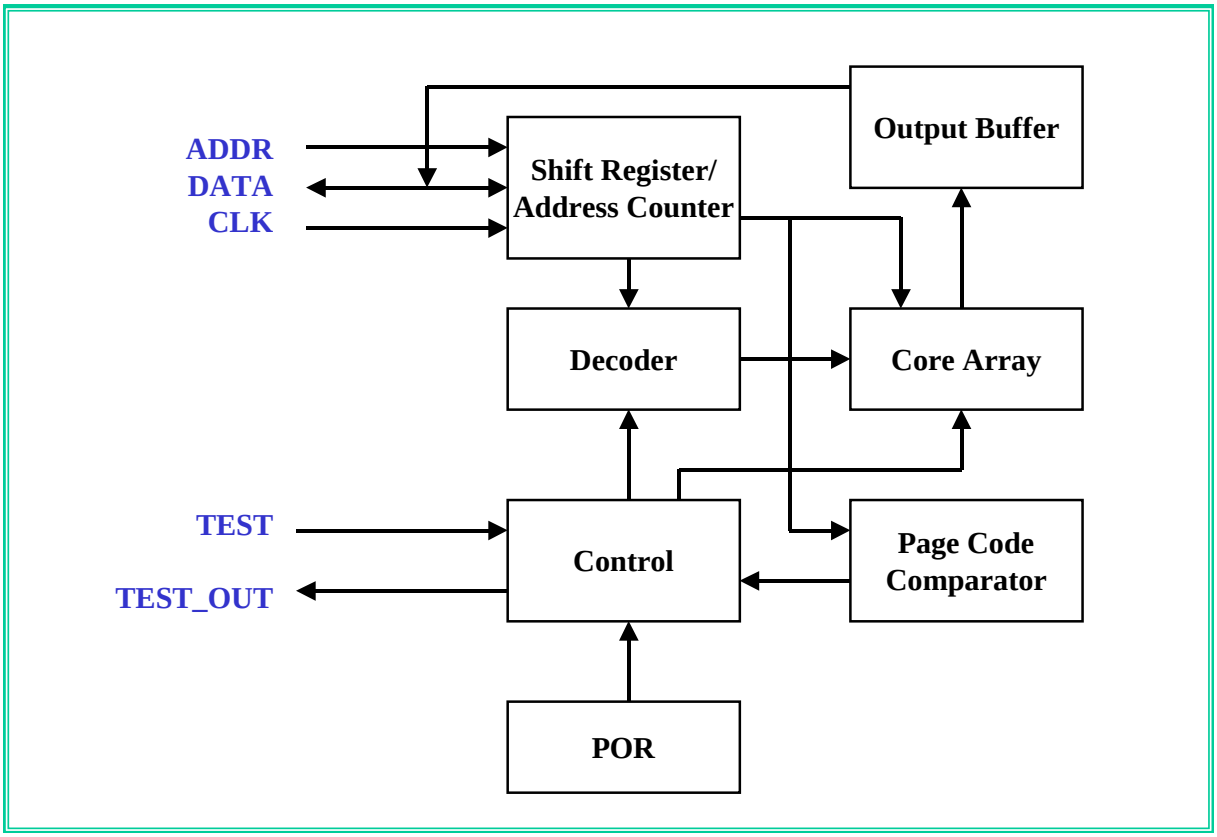
PIN NAME	I/O	DESCRIPTION
TEST	I	Internal pull-high. Set TEST low to enable "Self-test" function.
TEST_OUT	O	Indicates the result of self-test process. “0” indicates a correct result; “1” indicates an incorrect result. At Power-On-Reset, it outputs a logic "1" signal.
ADDR	I	Clock input for shift-in start address; the first rising-edge signal resets the address counter.
BS	I	Memory bank selection (for W551C320 use only; W551C240 TBD): "0": lower 16Mbit, "1": higher 16Mbit.
DATA1	IO	Bi-directional data pin-1 with internal pull-high.
DATA2	IO	Bi-directional data pin-2 with internal pull-high used for cascading address and data through the IC.
/CS	I	Active-low chip enable. Determines whether or not to cascade when in address mode: “0”: DATA2 does not have any cascaded chips appended “1”: DATA2 has cascaded chips appended.
CLK	I	Clock input for data read-out.
VDD	Power	Positive power supply pin.
VSS	Ground	

2. FUNCTION DESCRIPTION

This section provides the system block diagrams, followed by explanations of each mode. Note that serial check-sum output mode is not discussed in these latter sections, as it is only used in manufacturing testing.

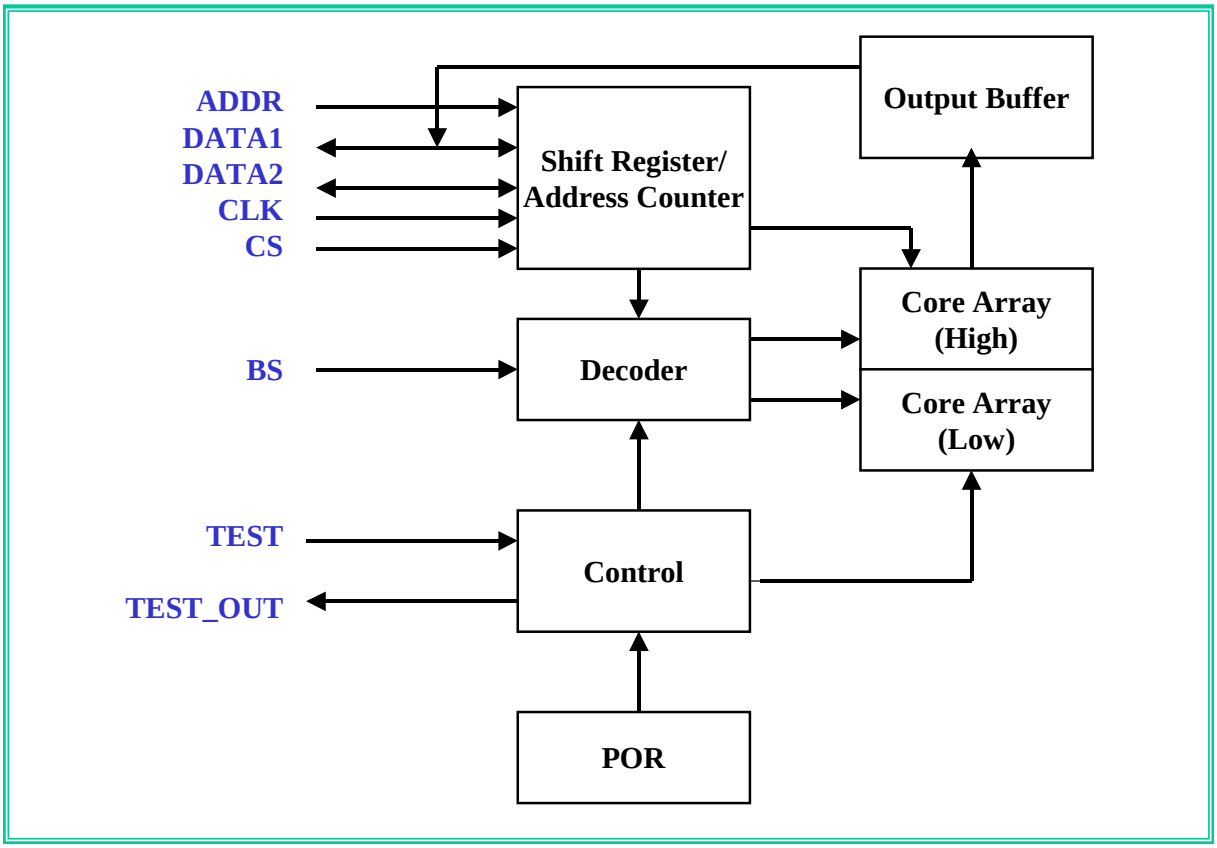
2.1 W551Cxxx System Block Diagram

W551Cxxx BLOCK DIAGRAM



Note: this diagram does not include the W551C160/240/320. That block diagram is shown on the next page.

W551C160/240/320 BLOCK DIAGRAM



2.2 W551Cxxx Serial Read Mode

The default mode is serial read mode.

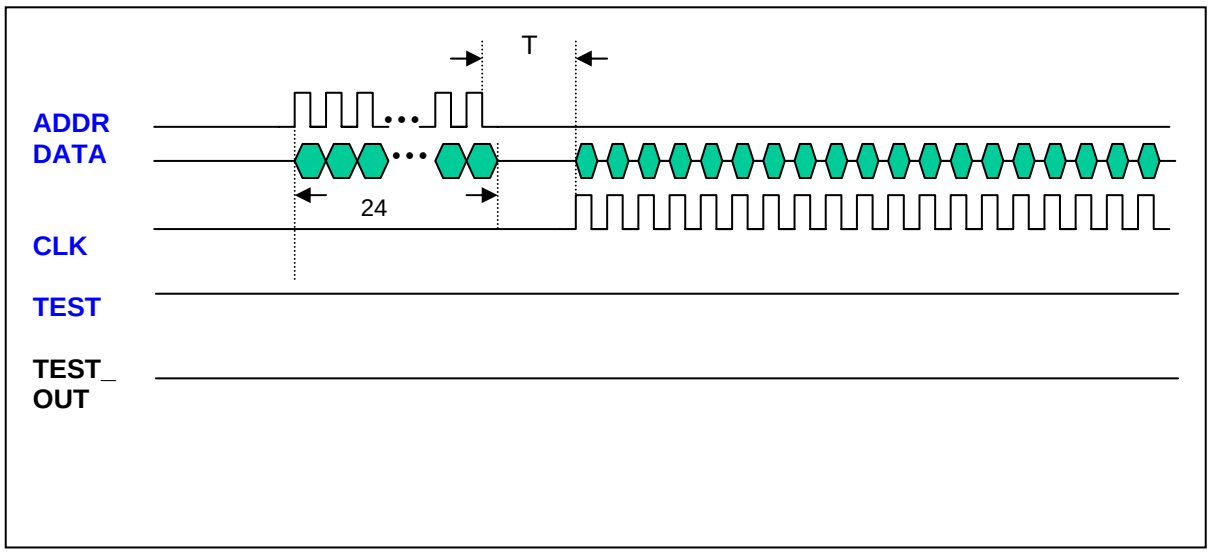
The address is 24 bits long. The MSB x bits are the page code, and the remaining (24 - x) bits are the offset address. The address data is shifted, MSB first, into the address counter by the ADDR clock, and the device is enabled if the page code matches the content of the W551Cxxx page-code cells. The number of bits in the page code varies by part number and is shown below.

PART #	W551C002	W551C005	W551C010	W551C020	W551C040	W551C060	W551C080
DENSITY	256K bits	512K bits	1M bits	2M bits	4M bits	6M bits	8M bits
PAGE CODE	6 bits	5 bits	4 bits	3 bits	2 bits	2 bits	1 bit

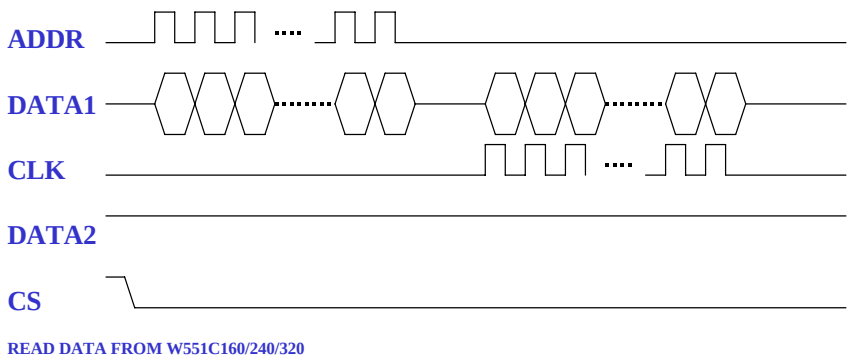
PART #	W551C160	W551C240	W551C320
DENSITY	16M BITS	24M BITS	32M BITS
PAGE CODE	0 BITS	0 BITS	0 BITS

Note: the W551C160/240/320 do not have a page code.

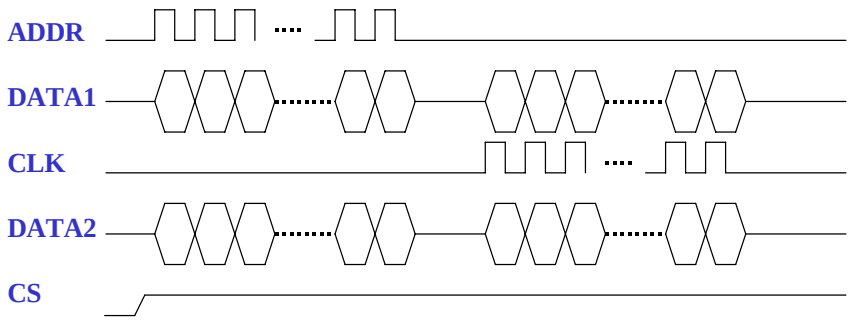
The first rising-edge signal in the ADDR clock resets the address shift registers. Once the address data has been shifted into the address counter (and the page code bit[s] verified), the falling-edge of the CLK clock increments the address counter. As a result, in serial-read mode, the ADDR and CLK clocks should not be active simultaneously. This is illustrated in the timing diagram below.



Serial read-mode also supports cascaded W551Cxxx chips. Cascading allows additional W551Cxxx chips to be connected to a W551C160/240/320 chip and effectively increases the amount of accessible memory. In the connection, all the W551Cxxx chips still share the same ADDR and CLK clock sources, but the data bus is routed through the W551C160/240/320 DATA1 and DATA2 pins. When the /CS pin is low, the W551C160/240/320 ignores any connected chips and responds accordingly on DATA1. When the /CS pin is high, however, the W551C160/240/320 enters cascade mode, and address data and the resulting read-data are passed through the W551C160/240/320. The timing diagrams for the W551C160/240/320 are shown below, and a sample circuit diagram is shown in the **Application Circuits** section.



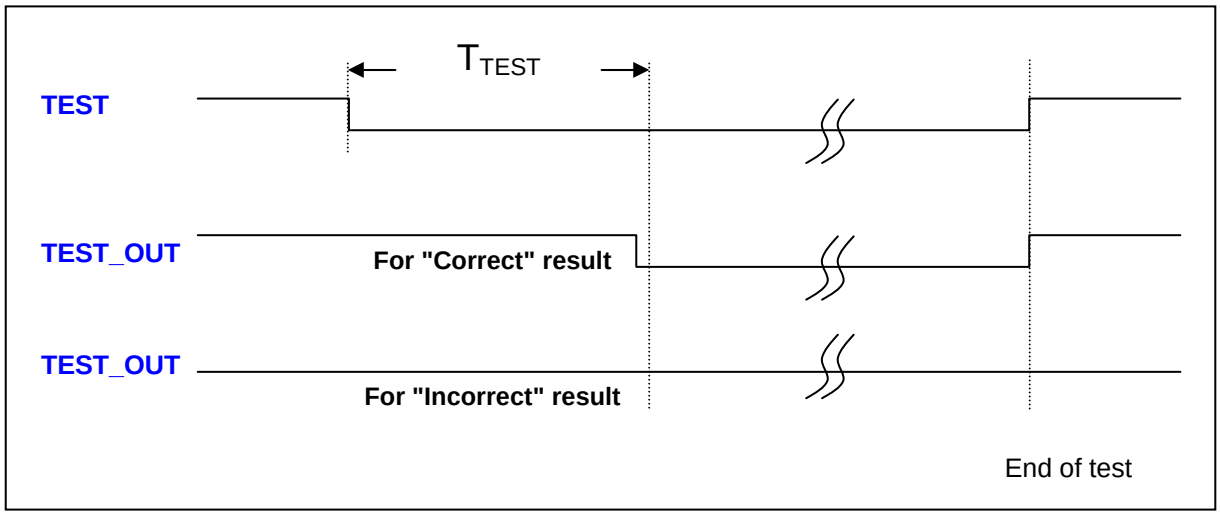
READ DATA FROM W551C160/240/320



READ DATA FROM CASCADE THROUGH W551C160/240/320

2.3 W551Cxxx Self-test Mode

The self-test process starts on any falling edge on the TEST pin. The self-test process accumulates every byte of voice memory in the chip. (The actual number of bytes depends on the part number.) If the accumulated result is 00h, no problem was detected, and a logic **'0'** is output on the TEST_OUT pin. Any other result indicates an error, and a logic **'1'** signal is output on the TEST_OUT pin.



3. ELECTRICAL CHARACTERISTICS

3.1 W551Cxxx Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITION	RATING	UNIT
Operation Temperature	TOPR	-	0 to +70	°C
Storage Temperature	TSTG	-	-65 to +150	°C
Power Supply (VDD-VSS)	VDD-VSS	-	-0.3 to +7.0	V
Input DC Voltage	VDC	All pins	-0.5 to Vcc+1.0	V
Transient Voltage (<20ns)	VTRAN	All pins	-1.0 to Vcc+1.0	V

3.2 W551Cxxx DC Characteristics

VDD = 4.5V, TA = 25° C

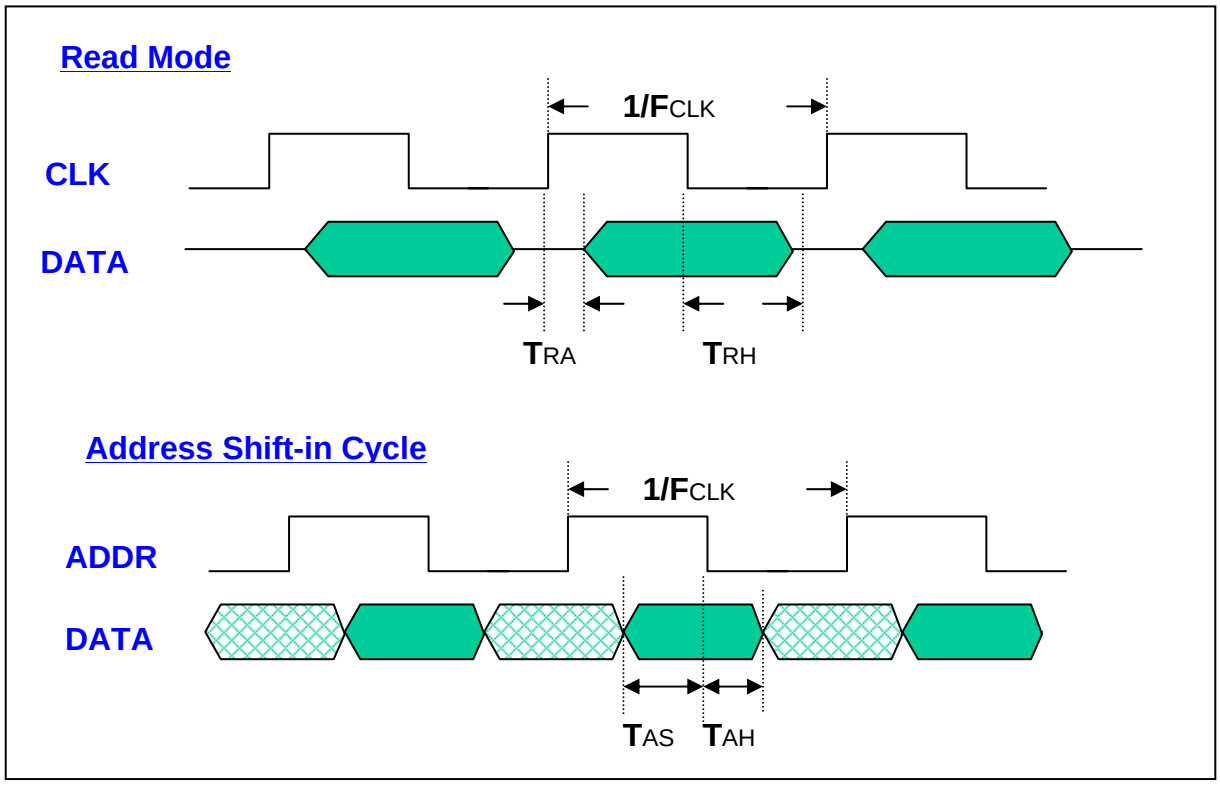
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Operating Voltage	V_{OP}	Normal read mode; F = 1 MHz	2.4	4.5	5.5	V
Operating Current	I_{OP}	In normal read mode, DATA, DATA1, DATA2, TEST & TEST_OUT pins open; f = 1MHz	-	5	10	mA
Standby Current	I_{SB}	All inputs = GND; DATA, DATA1, DATA2, TEST & TEST_OUT pins open	-	1	2 / 4 (W551C320)	uA
Input Leakage Current for DATA, DATA1, DATA2	I_{LI1}	V_{IN} = 0 V	-	-	-4.5	uA
Input Leakage Current for TEST	I_{LI2}	V_{IN} = 4.5 V	22.5	45	90	uA
Input Low Voltage	V_{IL}	All input pins	-0.3	-	0.8	V
Input High Voltage	V_{IH}	All input pins	2.0	-	VDD	V
Output Sink Current	I_{OL}	V_{OL}= 0.5V	2.5	5		mA
Output Drive Current	I_{OH}	V_{OH} = 4.0V	-2.5	-5		mA
ESD capability	V_{ESD}	-	2	-	-	KV

3.3 W551Cxxx AC Characteristics

VDD = 4.5V TA = 25° C

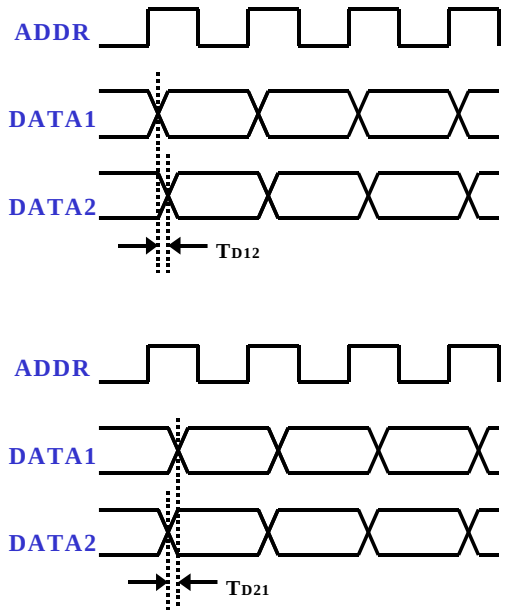
PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Clock frequency of ADDR	FADDR	-	-	-	1	MHz
Clock frequency of CLK	FCR	-	-	-	1	MHz
Interval time between ADDR and CLK	TI	Read mode	1	-	-	uS
Interval between DATA to another pin active	TCFA	-	10	-	-	uS
Data access time	TRA	Read mode	-	-	500	nS
Data setup time	TAS	Address shift-in	250	-	-	nS
Data hold time	TRH	Read mode	0	-	-	nS
	TAH	Address shift-in	10	-	-	nS
Self-test time	T_{TEST}	Self-test mode		500	1300 (W551C320)	mS
Transmission Time of DATA1 to DATA2 DATA2 to DATA1 (VDD = 2.4 V)	TD12 TD21	Cascade mode	35 20			nS
BS Switch Time (Fclk = 1 MHz)	TBS1 TBS2	Read mode	500			nS
CS Switch Time (Fclk = 1 MHz)	TCS1 TCS2	Read mode	500			nS

4. TIMING WAVEFORM

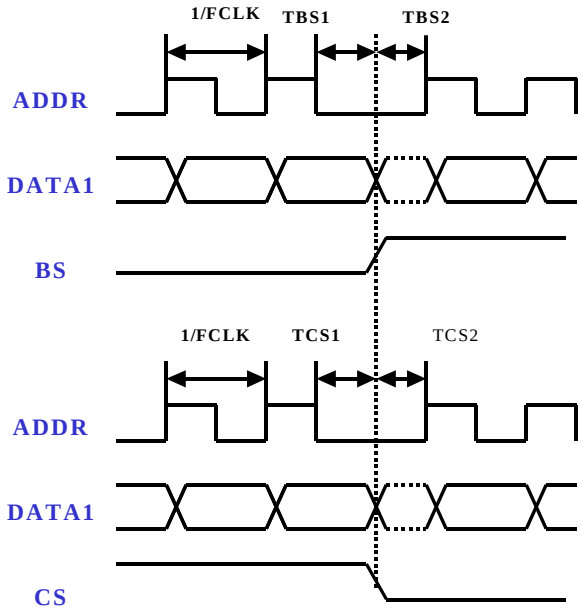


Note: The duty cycle of any clock is 50%.

Cascade Mode

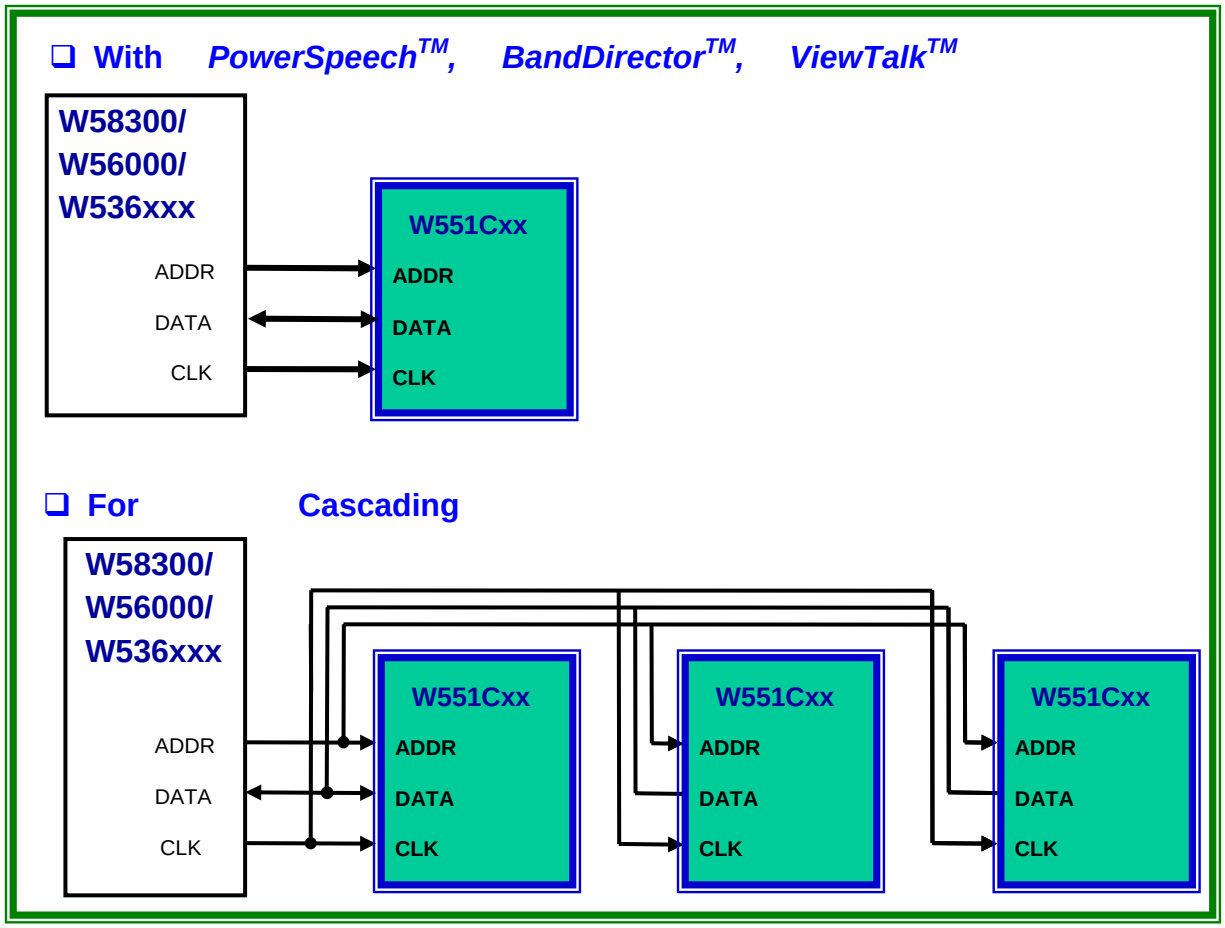


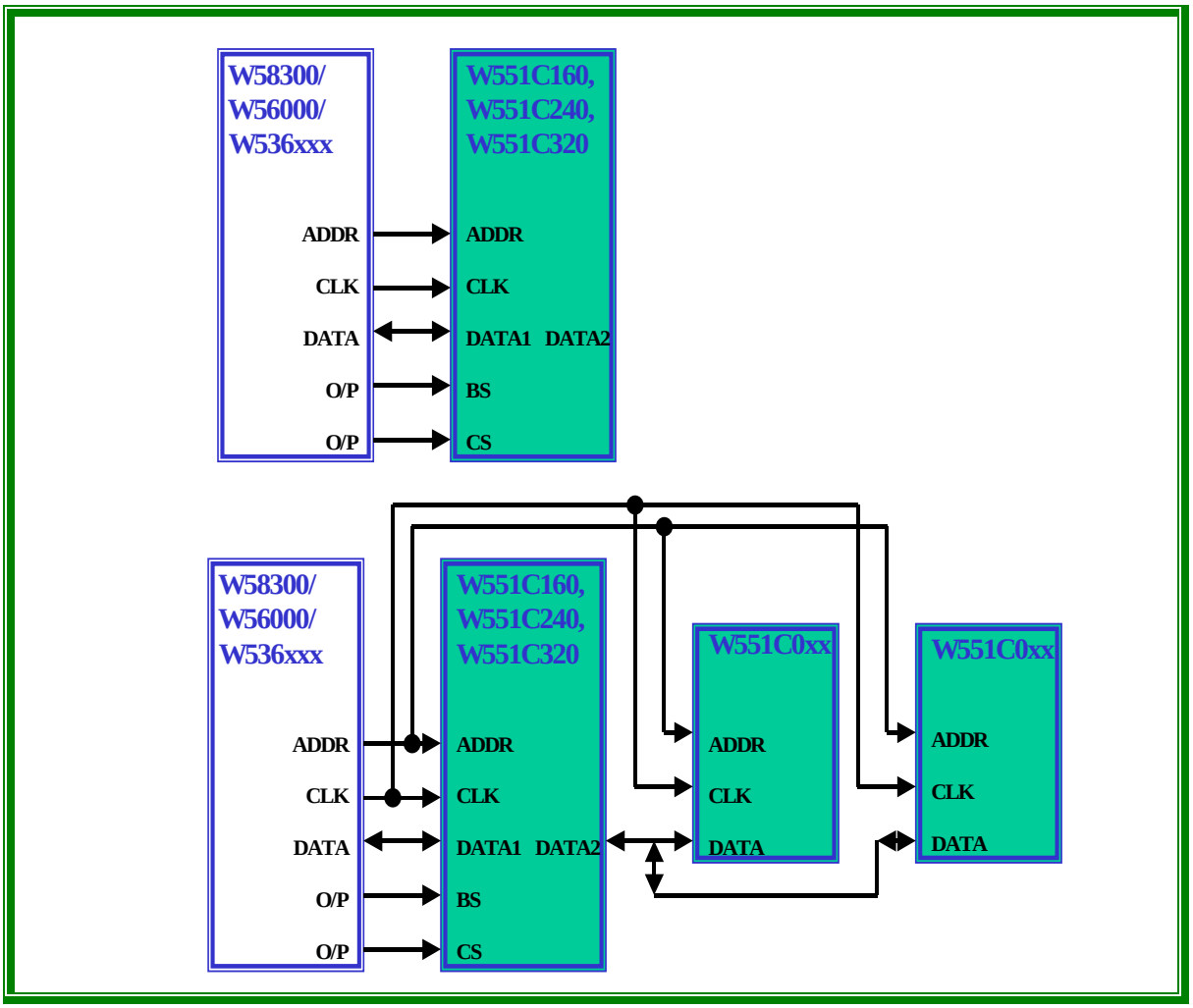
Switch Time



5. APPLICATION CIRCUITS

For reference only:




W58300/
W56000/
W536xxx
ADDR
CLK
DATA
O/P
O/P
W551C160,
W551C240,
W551C320
ADDR
CLK
DATA1 DATA2
BS
CS
W58300/
W56000/
W536xxx
ADDR
CLK
DATA
O/P
O/P
W551C160,
W551C240,
W551C320
ADDR
CLK
DATA1 DATA2
BS
CS
W551C0xx
ADDR
CLK
DATA
W551C0xx
ADDR
CLK
DATA

6. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	JAN. 01, 2001	-	-
A2	MAY 10, 2005	15, 16	REVISED BY BRANT AND ADD IMPORTANT NOTICE
A3	OCT. 3, 2005		Update W551C160, 320 INFORMATION and Page Header.

Winbond Electronics Corp.

Headquarters
No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5665577
http://www.winbond.com.tw/

Taipei Office
9F, No.480, Rueiguang Rd.,
Neihu District, Taipei, 114,
Taiwan, R.O.C.
TEL: 886-2-8177-7168
FAX: 886-2-8751-3579

Winbond Electronics Corporation America
2727 North First Street, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-5441798

Winbond Electronics Corporation Japan
7F Daini-ueno BLDG, 3-7-18
Shinyokohama Kohoku-ku,
Yokohama, 222-0033
TEL: 81-45-4781881
FAX: 81-45-4781800

Winbond Electronics (Shanghai) Ltd.
27F, 2299 Yan An W. Rd. Shanghai,
200336 China
TEL: 86-21-62365999
FAX: 86-21-62365998

Winbond Electronics (H.K.) Ltd.
Unit 9-15, 22F, Millennium City,
No. 378 Kwun Tong Rd.,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064