16-CHANNEL SPEECH+MELODY PROCESSOR (*BandDirector*™ Series)

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1. GENERAL DESCRIPTION

The W567CP260 is a powerful microcontroller (uC) dedicated to speech and melody synthesis applications. With 8Mbit embedded OTP, the help of 8-bit microprocessor, it can synthesize 16-channel speech+melody simultaneously.

The two channels of synthesized speech can be in different kinds of format, for example ADPCM and MDPCM. The W567CP260 can provide 16-channel high-quality ***WinMelody***™ , which can emulate the characteristics of musical instruments, such as piano and violin. The output of speech/melody channels are mixed together through the on-chip digital mixer to produce colorful effects. With these hardware resources, the W567CP260 is very suitable for high-quality and sophisticated scenario applications.

The W567CP260 provides at most 24 bi-directional I/Os, maximum 512 bytes RAM, IR carrier, Serial Interface Management, and 32KHz-Divider for more and more sophisticated applications, such as interactive toys, cartridge toys and final count down function. 3 LED output pins with 256-level control means that numerous combination of RGB colors may result in a versatility of colorful effects. In addition, W567CP260 also provides PWM mode output to save power during playback and Watch Dog Timer to prevent latch-up situation occurring.

W567CP260 is the OTP chip for the W567C series. It covers the correspondent items in the duration of less than 260 seconds and provide only one DAC/PWM (doesn't support W567Cxx6 items)

W567CP260 support items:

Item	**W567C070**	**W567C080**	**W567C100**	**W567C120**	**W567C151**	**W567C171**
Duration	81 sec.	102 sec.	115 sec.	127 sec.	162 sec.	196 sec.
Item	**W567C210**	**W567C260**				
Duration	230 sec.	263 sec.				

Item	**W567J070**	**W567J080**	**W567J100**	**W567J120**	**W567J151**	**W567J171**
Duration	81 sec.	102 sec.	115 sec.	127 sec.	162 sec.	196 sec.
Item	**W567J210**	**W567J260**				
Duration	230 sec.	263 sec.				

Note:

*: The duration time is based on 5-bit MDPCM at 6 KHz sampling rate. The firmware library and timber library have been excluded from user's ROM space for the duration estimation.

2. FEATURES

- Wide range of operating voltage:
  - 8 MHz @ 3.0 volt ~ 5.5 volt
  - 6 MHz @ 2.4 volt ~ 5.5 volt
- Power management:
  - 4 ~ 8 MHz system clocks, with Ring type or crystal type.
  - Stop mode for stopping all IC operations
- Provides up to 24 I/O pins
  - F/W speech synthesis:
    - Multiple format parser that supports

      New 4-bit MDPCM(NM4), 5-bit MDPCM(MDM), 4-bit MDPCM(MD4), 4-bit ADPCM(APM), 8-bit Log PCM(LP8) algorithm can be used
    - Pitch shippable ADPCM for voice changer application
    - Programmable sample rate
- Melody synthesis:
  - 16 melody channels that can emulate characteristics of musical instruments
  - Multi-MIDI simultaneous
  - Multi-MIDI channels dynamic control
  - More MIDI events are supported for colorful melody playback
- Built-in IR carrier generation circuit for simplifying firmware IR application
- Built-in TimerG0 for general purpose applications
- Harmonized synchronization among MIDI, Speech, LED, and Motor
- Build-in 3 LED outputs with 256-level control of brightness.
- Built-in Watch-Dog Timer (WDT) and Low Voltage Reset (LVR)
- Built-in 32KHz crystal oscillator with divider for time-keeping application
- Provide serial interface to access the external memory
  - W55Fxx, W551Cxx
  - SPI flash
- Stereophonic current type digital-to-analog converters (DAC) with 13-bit resolution to drive speaker output
- Stereophonic direct-drive 12-bit PWM output to save power consumption
- Support ***PowerScript***™ for developing codes in easy way
- Full-fledged development system
  - Source-level ICE debugger (Assembly & ***PowerScript***™ format)
  - ***Ultra I/O***™ tool for event synchronization mechanism
  - ICE system with USB port
  - User-friendly GUI environment
- Available package form:
  - COB is essential

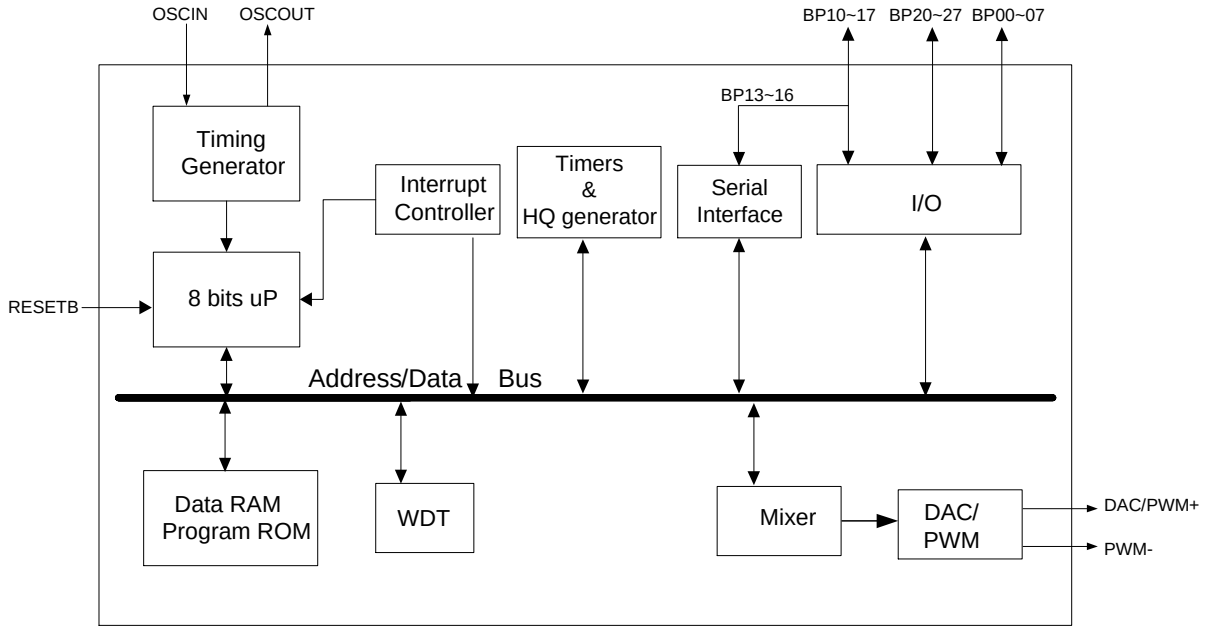
3. PIN DESCRIPTION

PIN NAME	I/O	FUNCTION
/RESET	I	IC reset input, low active.
OSCIN	I	Main-clock oscillation input. When Ring type is used, connects Rosc between OSCIN and VSS to generate the system clock frequency. Reserved one 100pF~200pF capacity to Vdd from OSCin pin to make Ring frequency stability When use X'tal, it is X'tal IN.
OSCOUT	O	Main-clock oscillation output only for X'tal.
X32I	I	32 KHz crystal oscillator with divider for time-keeping application
X32O	Out	32 KHz crystal oscillator with divider for time-keeping application
BP00~BP07	I/O	General input/output pins. When used as output pin, it can be open–drain or CMOS type and it can sink 25mA for high-current applications. When used as input pin, there may have a pull-high option and generate interrupt request to release IC from STOP mode. When BP07 is used as output pin, it can be the IR transmission carrier for IR applications. BP04~BP06 are used as 3 LED outputs with 256-level control. BP00~BP03 share pins to program OTP
BP10~BP17	I/O	General input/output pins. When used as output pin, it can be open–drain or CMOS type. When used as input pin, there may have a pull-high option and generate interrupt request to release IC from STOP mode. When serial interface is enabled, and set memory type as W55F/W551C, BP14~BP16 are used to be an interface with the external memory, W55Fxx or W551Cxxx. If set memory to SPI flash, BP13~BP16 are used to be an interface.
BP20~BP27	I/O	General input/output pins. When used as output pin, it can be open–drain or CMOS type. When used as input pin, there may have a pull-high option and generate interrupt request to release IC from STOP mode.
PWM+/DAC	O	PWM driver positive output or Current type DAC output
PWM-	O	PWM driver negative output
TEST	I	Test input, internally pulled low. Do not connect during normal operation.
VDD	Power	Positive power supply for uP and peripherals. All VDD pins must be bonded out and connect to VDD
VSS	Power	Negative power supply for uP and peripherals.
VDDOSC	Power	Positive power supply for oscillation.
VDDSPK	Power	Positive power supply for speaker driver.
VSSSPK	Power	Negative power supply for speaker driver.
VDD_BP1	Power	Positive power supply for BP1 including serial interface Management (SIM).

PIN NAME	I/O	FUNCTION
CVDD	O	For 3 battery(3.3V~5.5V) application ,add the capacitor 0.1uF to shunts between CVDD and GND as power stability for regulator output. For 2 battery(2.2V~3.6V) application, CVDD will connect to VDD directly.
VPP	High Power	High voltage for embedded OTP programming

Note: As program OTP, the BP00 ~ BP03, VDD, VSS, CVDD, RESETB and VPP pin will be used

4. BLOCK DIAGRAM



5. ITEM VS PIN TABLE

PIN name	CP260 (OTP)	C070/ 080/ 100/ 120	C151/ 171	C210/ 260	Comment
BP00~BP07	V	V	V	V	
BP10~BP17	V	V	V	V	
BP20~BP27	V	V	V	V	
/RESET	V	V	V	V	
TEST	V	V	V	V	
PWM+/DAC	V	V	V	V	
PWM-	V	V	V	V	
OSCIN	V	V	V	V	
OSCOUT	V	V	V	V	Crystal mode
X32I	V	V	V	V	
X32O	V	V	V	V	
VDD	V	V	V	V	
VSS	V	V	V	V	
VDDSPK	V	V	V	V	Support speaker power
VSSSPK	V	V	V	V	
VDD_BP1	V	V	V	V	Support BP10~BP17 including SIM interface power
VDDOSC	V	V	V	V	Support OSCIN/OUT power
VSSOSC	V	V	V	V	
CVDD	V	V	-	V	Regulator out
VDD1			V		Connect to VDD
VPP	V				For OTP writer

6. ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +7.0	V
D.C. Voltage on Any Pin to Ground Potential	-0.3 to V_{DD} +0.3	V
Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

6.2 DC Characteristics

(V_{DD}–V_{SS} = 4.5 V, F_M = 8 MHz, Ta = 25°C, No Load unless otherwise specified)

PARAMETER	SYM.	TEST CONDITIONS	SPEC.			UNIT
			Min.	Typ.	Max.	
Operating Voltage	V_{DD}	F_{SYS} = 6 MHz	2.4	-	5.5	V
		F_{SYS} = 8 MHz	3.0	-	5.5	V
Operating Current	I_{OP1}	No load, F_{SYS} = 6 MHz	-	6	10	mA
Standby Current	I_{SB}	STOP mode	-	--	10	μA
32KHz Crystal current	I_{32K}	F_{OSC} disable, No load, Wake up frequency: 2Hz	-	6	15	μA
Input Low Voltage	V_{IL}	All input pins	V_{SS}	-	0.3 V_{DD}	V
Input High Voltage	V_{IH}	All input pins	0.7 V_{DD}	-	V_{DD}	V
Input Current BP0, BP1, BP2, /RESET	I_{IN1}	V_{IN} = 0V, pulled-high resistor = 500k ohm	-5	-9	-14	μA
Input Current BP0,BP1,BP2, /RESET	I_{IN2}	V_{IN} = 0V, pulled-high resistor = 150k ohm	-15	-30	-45	μA

Output Current (BP0)	I_{OL}	V_{DD} = 3V, V_{OUT} = 0.4V	8	12	-	mA
	I_{OH}	V_{DD} = 3V, V_{OUT} = 2.6V	-4	-6	-	mA
	I_{OL}	V_{DD} = 4.5V, V_{OUT} = 1.0V	-	25	-	mA
	I_{OH}	V_{DD} = 4.5V, V_{OUT} = 3.5V	-	-12	-	mA
Output Current (BP1, BP2)	I_{OL}	V_{DD} = 3V, V_{OUT} = 0.4V	4	8	-	mA
	I_{OH}	V_{DD} = 3V, V_{OUT} = 2.6V	-4	-6	-	mA
	I_{OL}	V_{DD} = 4.5V, V_{OUT} = 1.0V	-	12	-	mA
	I_{OH}	V_{DD} = 4.5V, V_{OUT} = 3.5V	-	-12	-	mA
DAC Full Scale Current	I_{DAC}	V_{DD} = 4.5V, RL = 100Ω	-2.4 -4.0	-3.0 -5.0	-3.6 -6.0	mA
Output Current PWM+ / PWM-	I_{OL1}	RL= 8 Ohm, [PWM+]----[RL]----[PWM-]	+200	-	-	mA
	I_{OH1}		-200	-	-	mA
Pull-high Resistor Test	R_{PL}		75	150	225	KΩ

6.3 AC Characteristics

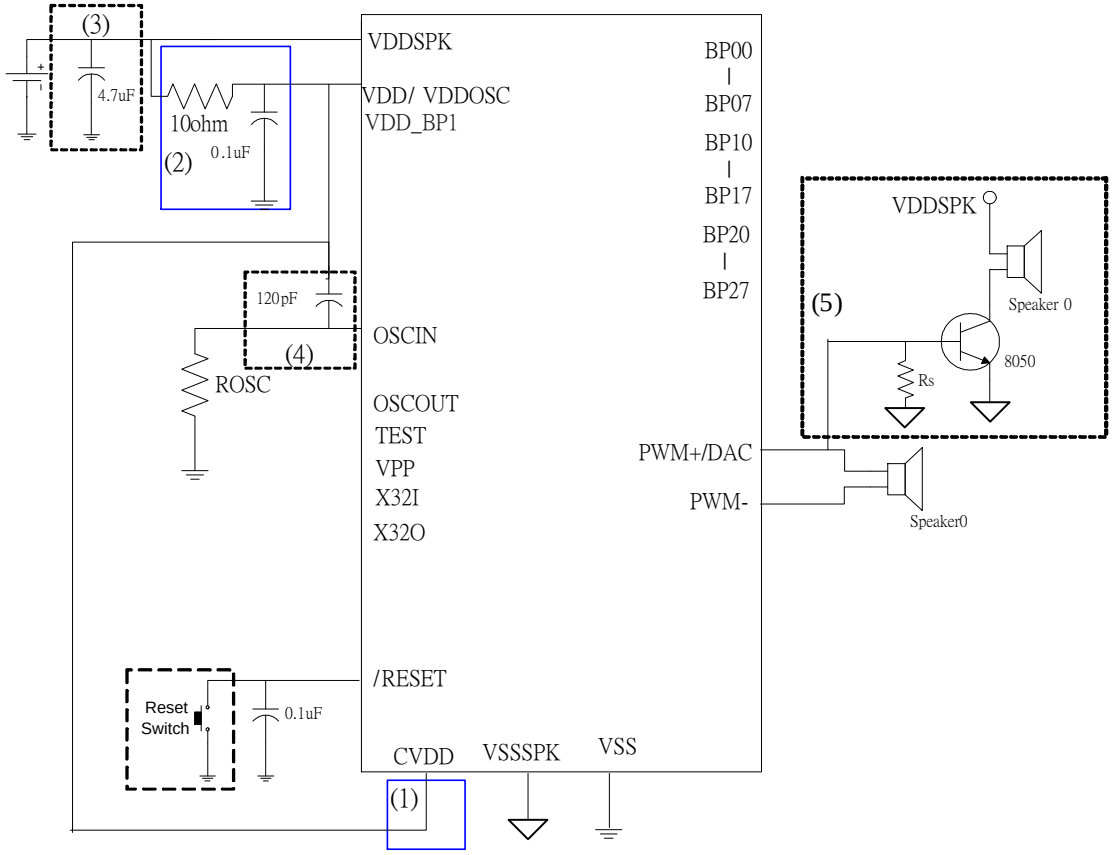
(V_{DD}-V_{SS} = 4.5 V, F_M = 8 MHz, Ta = 25°C; No Load unless otherwise specified)

PARAMETER	SYM.	TEST CONDITIONS	SPEC.			UNIT
			Min.	Typ.	Max.	
Main-Clock	F_M	Ring type, Rosc = TBD Ω	7.2	8	8.8	MHz
		Ring type, Rosc = TBD Ω	5.4	6	6.6	
Main-Clock Wake-up Stable Time	T_{WSM}	Ring type, R = TBD KΩ	-	3	5	mS
Main-Clock Frequency Deviation, Ring type	$\frac{\Delta F}{F}$	$\frac{F_{MAX} - F_{MIN}}{F_{MIN}}$	-	3	7.5	%
Cycle Time	T_{CYC}	CPU clock = 6 MHz	166	-	DC	nS
RESETB Active Width	T_{RES}	After F_{SYS} stable	4	-	-	T_{CYC}

Oscillator resistor for ring oscillation suggested, 300KΩ for 8MHz, 390KΩ for 6MHz and 590KΩ for 4MHz.

7. TYPICAL APPLICATION CIRCUIT

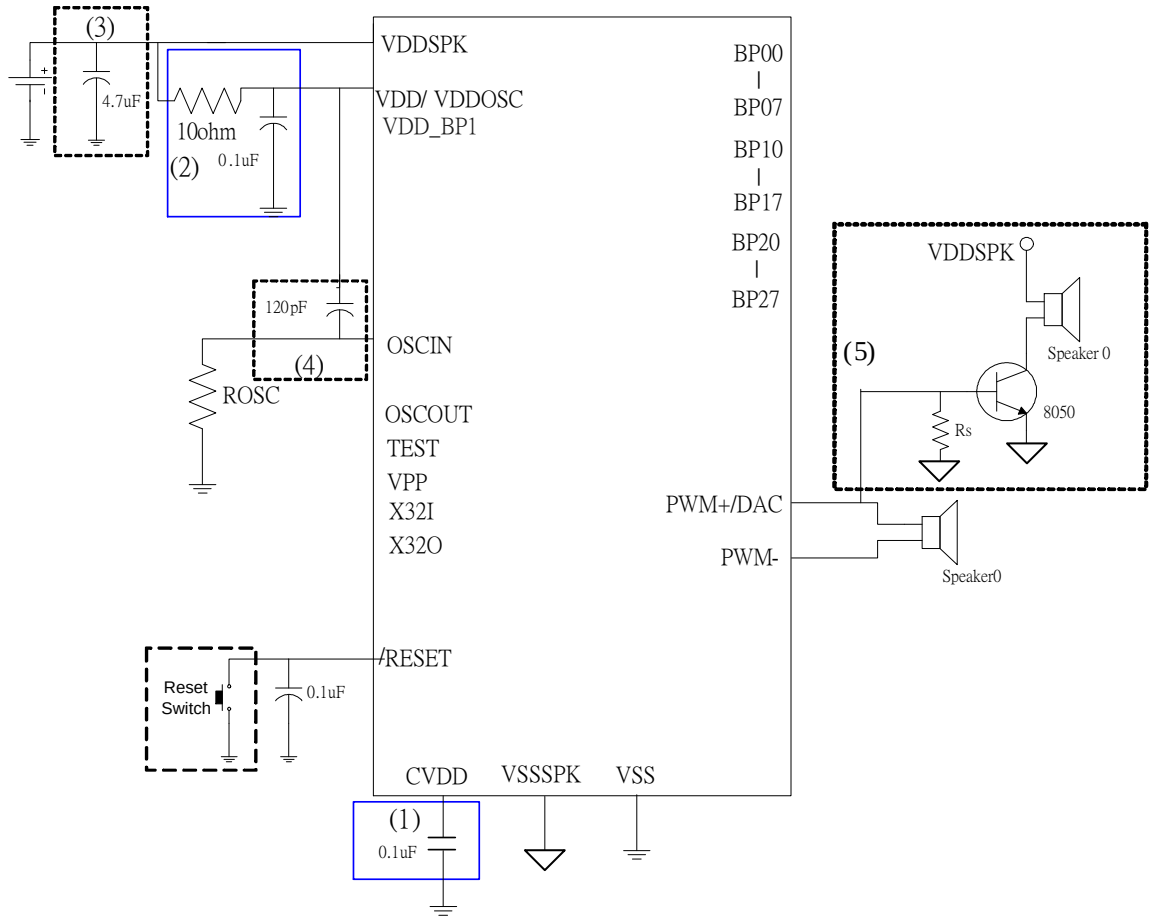
(a) Rosc with 2 Battery



Notes:

1. The block (1): If the project is two-battery application (Voltage 3.6V~2.2V), it is necessary to connect CVDD to VDD.
2. The block (2): The low-pass filter circuit is necessary for VDD stability, in order to avoid VDDSPK noise.
3. The block (3): The capacitor, 4.7uF, shunted between VDD and GND is necessary for power stability. However, the value of capacitor depends on the power loading of the application.
4. The typical value of Rosc is 300 KΩ for 8MHz and 390 KΩ for 6MHz, and the Rosc should be connected to GND (VSS). Please refer to design guide to get typical Rosc value for each part number.
5. The block (4):The capacitor, 120pF, shunted between OSCIN and VDD is optional for Fosc stability, which can prevent noise from happening, because it can block the affection of larger current while playing. However, the value of capacitor depends on the application (100pF~200pF is recommended)
6. The block (5): The Rs value is suggested of 270Ω ~ 1KΩ to limit large DAC output current flowing into transistor.
7. The above application circuit is for reference only. No warranty for mass production.

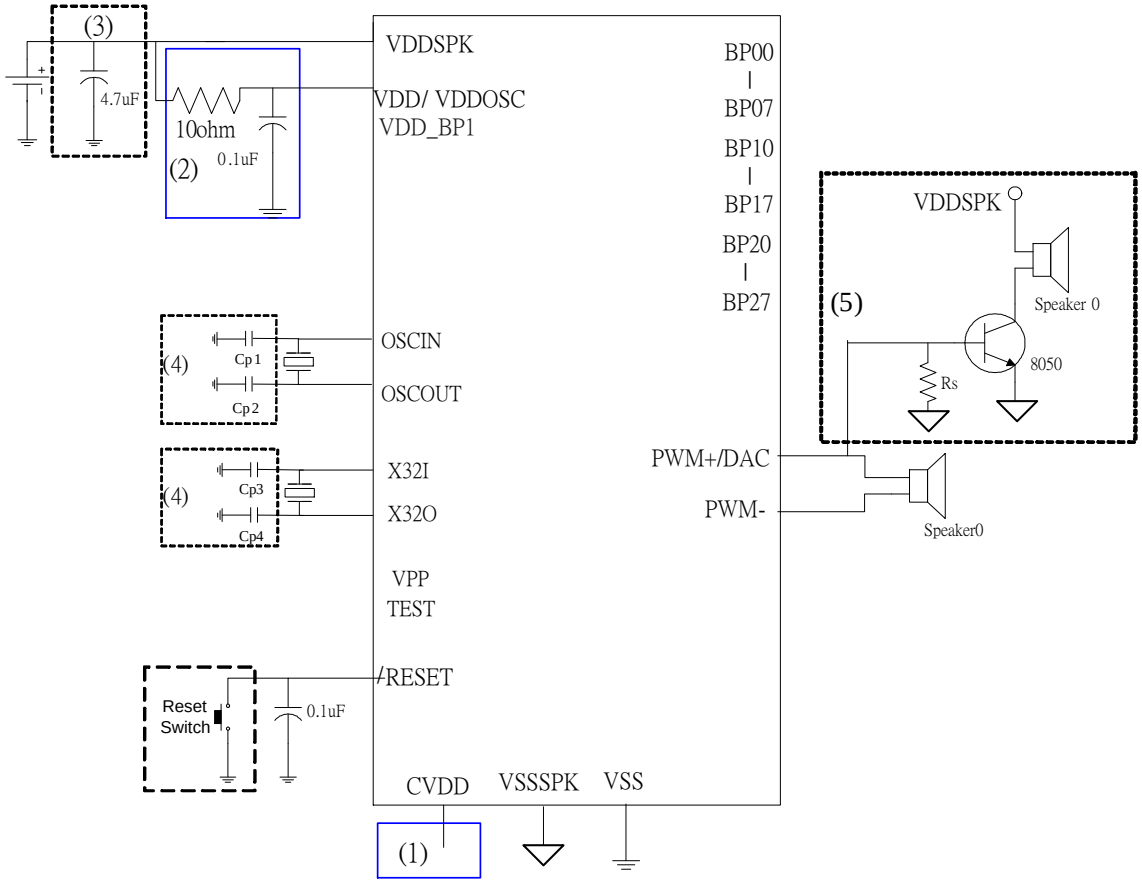
(b) Rosc with 3 Battery



Notes:

1. The block (1): If the project is three-battery application (Voltage 5.5V~3.0V), it is necessary to connect a 0.1uF between CVDD and GND (VSS).
2. The block (2): The low-pass filter circuit is necessary for VDD stability, in order to avoid VDDSPK noise
3. The block (3): The capacitor, 4.7uF, shunted between VDD and GND is necessary for power stability. However, the value of capacitor depends on the power loading of the application.
4. The typical value of Rosc is 300 KΩ for 8MHz and 390 KΩ for 6MHz, and the Rosc should be connected to GND (VSS). Please refer to design guide to get typical Rosc value for each part number.
5. The block (4)The capacitor, 120pF, shunted between OSCIN and VDD is optional for Fosc, which can prevent noise from happening, because it can block the affection of larger current while playing. However, the value of capacitor depends on the application (100pF~200pF is recommended)
6. The block (5): The Rs value is suggested of 270Ω ~ 1KΩ to limit large DAC output current flowing into transistor.
7. The above application circuit is for reference only. No warranty for mass production.

(c) Crystal

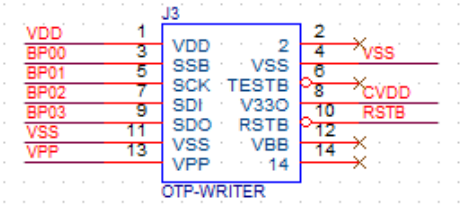


Notes:

1. The block (1): Please refer to (a) and (b) circuits for two-battery or three-battery application.
2. The block (2): The low-pass filter circuit is necessary for VDD stability, in order to avoid VDDSPK noise.
3. The block (3): The capacitor, 4.7uF, shunted between VDD and GND is necessary for power stability. However the value of capacitor depends on the power loading of the application
4. The block (4): Cp1 and Cp2 (15~30pF) are optional for main Crystal, which can be skipped normally.
5. The block (5): The Rs value is suggested of 270Ω ~ 1KΩ to limit large DAC output current flowing into transistor.
6. Cp3 and Cp4 (15~30pF) are optional for 32KHz Crystal, which can be skipped normally.
7. Please connect all VDD pins include VDDOSC/VDD_BP1 to VDD. If with SIM application, the VDD_BP1 pin can connect to different voltage for SPI flash or W551Cxx and the BP10~BP17 also use the same power VDD_BP1.
8. The above application circuit is for reference only. No warranty for mass production.
9. Other application circuits please refer to Design Guide.

(d) Write interface

1. Writer interface pins are BP00~BP03, RESETB, VPP, VSS, VDD and CVDD.
2. Detail application circuit, please refer to NHS-W567CP80 V1.0 user's guide A0.



(e) PCB layout guide

1. The IC substrate should be connected to VSS in PCB layout, but VSSSPK can't connect with IC substrate directly. Both VSS and VSSSPK tie together in battery negative power.
2. Each VDD, VDDOSC, VDD_BP1 and VDDSPK pad must connect to positive power to support stable voltage for individual function work successfully. (Don't let them be floating.)

8. REVISION HISTORY

VERSION	DATE	REASONS FOR CHANGE	PAGE
A1.0	Sep. 2012	Separate from W567Cxxx data sheet Rename from W567CP80 to W567CP260	All

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.