8-CHANNEL SPEECH+MELODY PROCESSOR (*BandDirector*™ Series)

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1. GENERAL DESCRIPTION

The W567Sxxx is a powerful microcontroller (uC) dedicated to speech and melody synthesis applications. With the help of the embedded 8-bit microprocessor & dedicated H/W, the W567Sxxx can synthesize 8-channel speech+melody simultaneously.

The two channels of synthesized speech can be in different kinds of format, for example ADPCM and MDPCM. The W567Sxxx can provide 8-channel high-quality ***WinMelody***^{TM} , which can emulate the characteristics of musical instruments, such as piano and violin. The output of speech/melody channels are mixed together through the on-chip digital mixer to produce colorful effects. The mixer is further processed to drive dual speakers with stereo effects. With these hardware resources, the W567Sxxx is very suitable for high-quality and sophisticated scenario applications.

The W567Sxxx is also capable of transmitting infrared (IR) signals with on-chip carrier generator. As a result, toys can be designed to interact with each other for more play values. A serial interface can be supported as external memory for memory expansion or content-updateable applications.

Besides, the W567Sxxx is equipped with a 4-channel Analog-to-Digital Converter (ADC). With ADC, a toy can respond to environment conditions such as temperature or pressure via sensory devices. Therefore, toys with ADC can behave vividly than ever before.

The W567Sxxx family contains several items with different playback duration as shown below: (@5-bit MDPCM algorithm, 6 KHz sampling rate)

Item	**W567S010**	**W567S015**	**W567S020**	**W567S025**	**W567S030**	**W567S040**
*Duration	14 sec.	18 sec.	27 sec.	31 sec.	35 sec.	52 sec.
Item	**W567S060**	**W567S080**	**W567S100**	**W567S120**	**W567S150**	**W567S170**
Duration	60 sec.	104 sec.	116 sec.	129 sec.	163 sec.	197 sec.
Item	**W567S210**	**W567S260**	**W567S301**	**W567S341**		
Duration	232 sec.	265 sec.	300 sec.	334 sec.		

Note: *: The duration time is based on 5-bit MDPCM at 6 KHz sampling rate. The firmware library and timber library have been xcluded from user's ROM space for the duration estimation.

2. FEATURES

- Wide range of operating voltage:
  - 8 MHz @ 3.6 volt ~ 5.5 volt
  - 4 MHz @ 2.4 volt ~ 5.5 volt
- Power management:
  - 4 ~ 8 MHz system clocks, with Ring type
  - Stop mode for stopping all IC operations
- Provides up to 8 inputs and 24 I/O pins
- Current-type Digital-to-Analog Converter (DAC):
  - (8+2)-bit resolution with programmable output current
  - 2 speaker outputs for stereo applications
- F/W speech synthesis with multiple format support: ADPCM/MDPCM/PCM
- Up to 8 speech synthesis[1] channels at programmable sample rate
- 8 melody channels that can emulate characteristics of musical instruments
- 8-input/10-bit-resolution Mixer can mix the speech and melody signals flexibly
- Dynamic control of the channel assignment to the dual speaker output for stereo effects
- Built-in IR carrier generation circuit for simplifying firmware IR application
- 4-channel ADC interface (W567S301~S341) with maximum 4-KHz sampling rate and 6-bit effective resolution
- Built-in 9 timers for speech/melody synthesis and general purpose applications
- Built-in 10*7 multiplier
- Built-in Watch-Dog Timer (WDT) and Low Voltage Reset (LVR)
- Built-in 32KHz crystal oscillator with divider for time-keeping application in W567S080 ~ S341
- Built-in Serial Interface Manager (SIM) in W567S080 ~ S341
- Support PowerScript for developing codes in easy way
- Full-fledged development system
  - Source-level ICE debugger
  - Event synchronization mechanism
  - Compatible with W566B/C & W588S system
  - User-friendly GUI environment
- Available package form: (COB is essential)
  - W567S010, S015, S020, S025, S030: LQFP48
  - W567S040, S060: QFP64
  - W567S080 ~ S120: LQFP128
  - W567S150 ~ S341: LQFP100

[1] More speech channels are available for 8-bit PCM format in the remaining melody channels. When used as 2-ch MDPCM and 6-ch PCM.

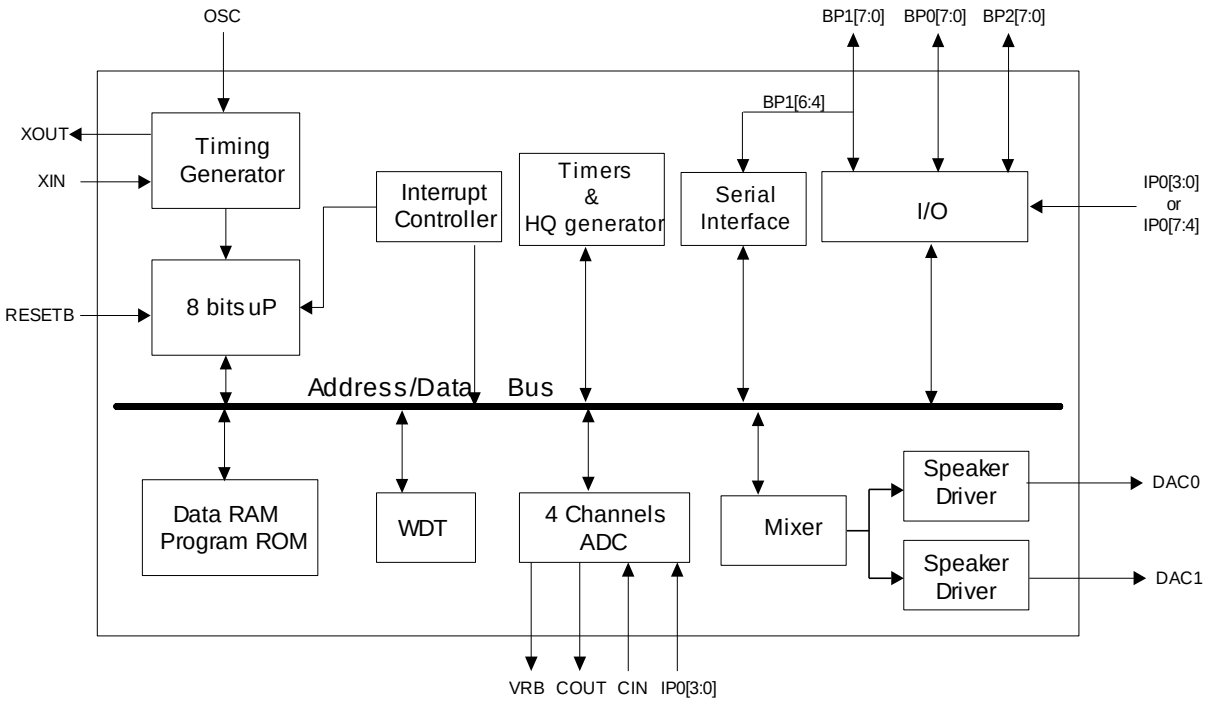
3. PIN DESCRIPTION

PIN NAME	I/O	FUNCTION
RESETB	In	IC reset input, low active.
XIN	In	32 KHz crystal oscillator with divider for time-keeping application
XOUT	Out	32 KHz crystal oscillator with divider for time-keeping application
OSC	In	Main-clock oscillation input. Only Ring type is used. Connect to GND via the oscillation resistor.
IP0[3:0] / IP0[7:4]	In	General input port with pull-high selection. Each 2 input pins can be programmed to generate interrupt request and used to release IC from STOP mode. IP0[3:0] are used as the input of ADC. IP0.0 is the input pin of channel 0 and IP0.3 is the input pin of channel 3, and so on.
BP0[7:0]	I/O	General input/output pins. When used as output pin, it can be open–drain or CMOS type and it can sink 8mA for high-current applications. When used as input pin, there may have a pull-high option and generate interrupt request to release IC from STOP mode. When BP0[7] is used as output pin, it can be the IR transmission carrier for IR applications.
BP1[7:0]	I/O	General input/output pins. When used as output pin, it can be open–drain or CMOS type. When used as input pin, there may have a pull-high option and generate interrupt request to release IC from STOP mode. When serial interface is enabled, BP1[6:4] are used as serial interface pins.
BP2[7:0]	I/O	General input/output pins. When used as output pin, it can be open–drain or CMOS type. When used as input pin, there may have a pull-high option and generate interrupt request to release IC from STOP mode.
[2]VRB	Out	Reference-bottom voltage of ADC. Theoretically, the converted codes 0 ~ 255 will be uniformly distributed between VRB and AVDD. Voltages below VRB will be mapped to code 0.
[2]CIN	In	Capacitor input for ADC.
[2]COUT	Out	Capacitor output for ADC.
[2]AVDD	Out	ADC regulator output voltage.
DAC0	Out	Current type DAC speaker output 0.
DAC1	Out	Current type DAC speaker output 1.
TEST	In	Test input, internally pulled low. Do not connect during normal operation.
V_{DD}	Power	Positive power supply for μP and peripherals.
V_{SS}	Power	Negative power supply for μP and peripherals.
[3]VDDOSC	Power	Positive power supply for oscillation.
[3]VSSOSC	Power	Negative power supply for oscillation.
[2]VDDA	Power	Positive power supply for ADC module.
[2]VSSA	Power	Negative power supply for ADC module.

4. BLOCK DIAGRAM

[2] Only W567S301~S341 provides these pins for ADC application.

[3] In order to get a stable oscillating frequency, W567S080~S341 provides these pins for power supply.


OSC
BP1[7:0]
BP0[7:0]
BP2[7:0]
BP1[6:4]
XOUT
XIN
Timing Generator
Interrupt Controller
Timers & HQ generator
Serial Interface
I/O
IP0[3:0] or IP0[7:4]
RESETB
8 bits uP
Address/Data Bus
Data RAM Program ROM
WDT
4 Channels ADC
Mixer
Speaker Driver
Speaker Driver
DAC0
DAC1
VRB
COUT
CIN
IP0[3:0]

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +7.0	V
D.C. Voltage on Any Pin to Ground Potential	-0.3 to V_{DD} +0.3	V
Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

5.2 D.C. Characteristics

(V_{DD}–V_{SS} = 4.5 V, F_M = 8 MHz, Ta = 25°C, No Load unless otherwise specified)

PARAMETER	SYM.	TEST CONDITIONS	SPEC.			UNIT
			Min.	Typ.	Max.	
Operating Voltage	V_{DD}	F_{SYS} = 4 MHz	2.4	-	5.5	V
		F_{SYS} = 8 MHz	3.6	-	5.5	V
Operating Current	I_{OP}	F_{SYS} = F_M, normal operation	-	15	20	mA
Standby Current	I_{SB}	STOP mode	-	1	2	μA
32KHz Crystal current	I_{32K}	F_{OSC} disable, No load, Wake up frequency: 2Hz	-	6	15	μA
Input Low Voltage	V_{IL}	All input pins	V_{SS}	-	0.3 V_{DD}	V
Input High Voltage	V_{IH}	All input pins	0.7 V_{DD}	-	V_{DD}	V
Output Current (BP0)	I_{OL}	V_{DD} = 4.5V, V_{OUT} = 1.0V	-	25	-	mA
	I_{OH}	V_{DD} = 4.5V, V_{OUT} = 2.6V	-	-12	-	mA
	I_{OL}	V_{DD} = 3V, V_{OUT} = 0.4V	8	12	-	mA
	I_{OH}	V_{DD} = 3V, V_{OUT} = 2.6V	-4	-6	-	mA
Output Low Current	I_{OL}	V_{OUT} = 0.4V, all output pins except BP0	4	-	-	mA
Output High Current	I_{OH}	V_{OUT} = 2.4V, all output pins except BP0	-4	-	-	mA
DAC Full Scale Current	I_{DAC}	V_{DD} = 4.5V, RL = 100Ω	-2.4 -4.0	-3.0 -5.0	-3.6 -6.0	mA
Operation Current of Low Voltage Reset	I_{LVR}	VDD = 4.5V			60	uA
Input current BPn, Reset	I_{IN}	VIN = 0V, pull high resistance = 200K ohm	-15		-45	uA

5.3 A.C. Characteristics

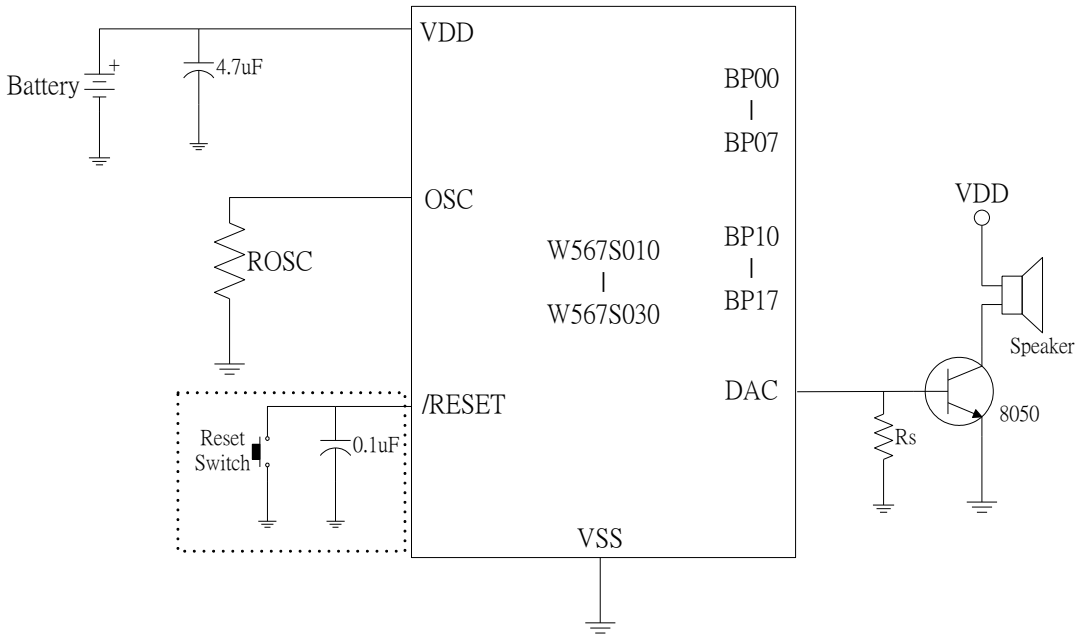
(V_{DD}-V_{SS} = 4.5 V, F_M = 8 MHz, Ta = 25°C; No Load unless otherwise specified)

PARAMETER	SYM.	TEST CONDITIONS	SPEC.			UNIT
			Min.	Typ.	Max.	
Main-Clock	F_M	Ring type, *Rosc = 300 KΩ	3.6	4	4.4	MHz
		Ring type, *Rosc = 150 KΩ	7.2	8	8.8	
Cycle Time	T_{CYC}	F_{SYS} = 8 MHz	125	-	DC	nS
Main-Clock Wake-up Stable Time	T_{WSM}	Ring type, R = 160 KΩ	-	3	5	mS
Main-Clock Frequency Deviation, Ring type	$\frac{\Delta F}{F}$	$\frac{F_{MAX} - F_{MIN}}{F_{MIN}}$	-	3	7.5	%
RESETB Active Width	T_{RES}	After F_{SYS} stable	4	-	-	T_{CYC}

*: Typical ROSC value for each part number should refer to design guide.

6. TYPICAL APPLICATION CIRCUITS

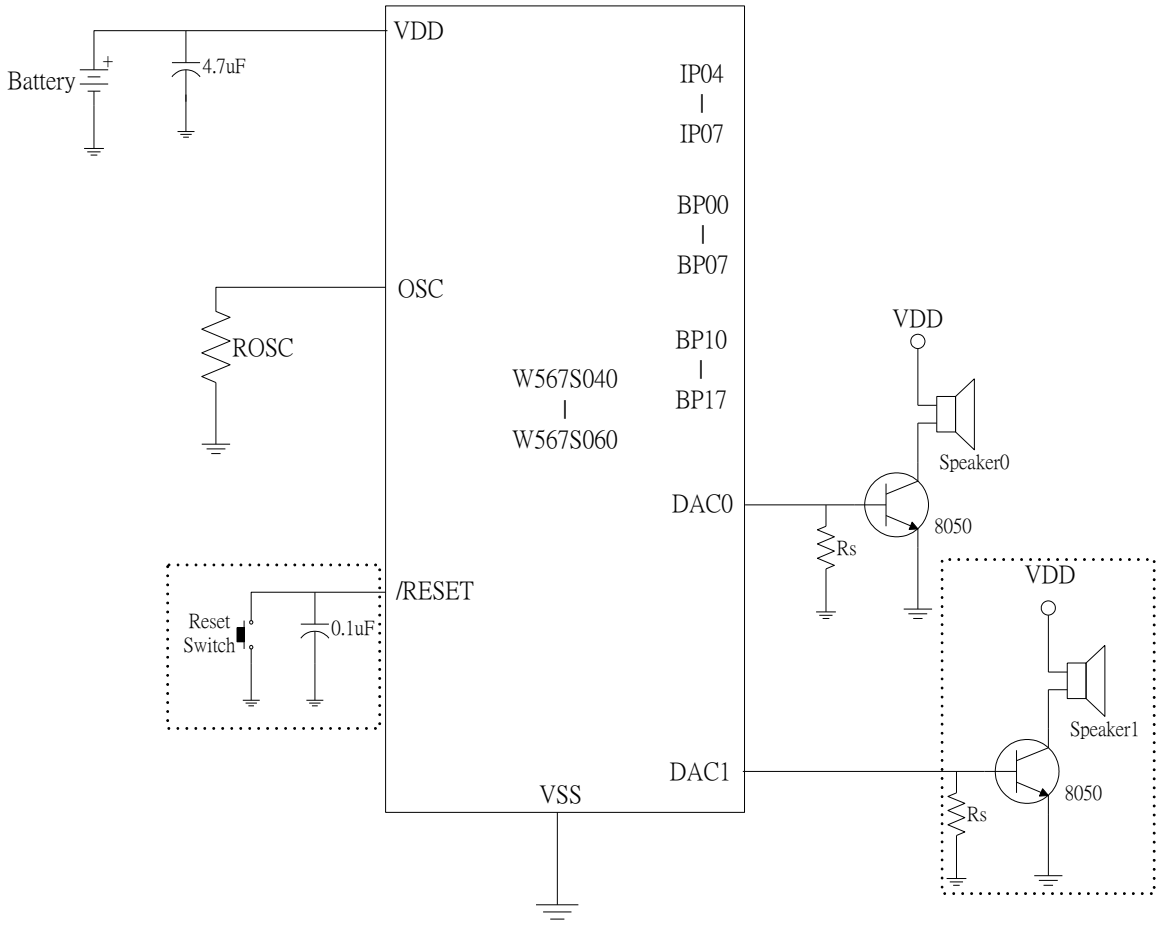
6.1 W567S010~S030



Notes:

1. The typical value of Rosc is 150 KΩ for 8MHz and 300 KΩ for 4MHz and should be connected to GND (V_{SS}).
2. Please refer to design guide to get typical Rosc value for each part number.
3. The Rs value is suggested in 270Ω ~ 1KΩ to limit too large DAC output current flowing into transistor.
4. The capacitor, 4.7μF, shunts between V_{DD} and GND is necessary as power stability. But the value of capacitor is depend on the application.
5. The above application circuits are for reference only. No warranty for mass production.

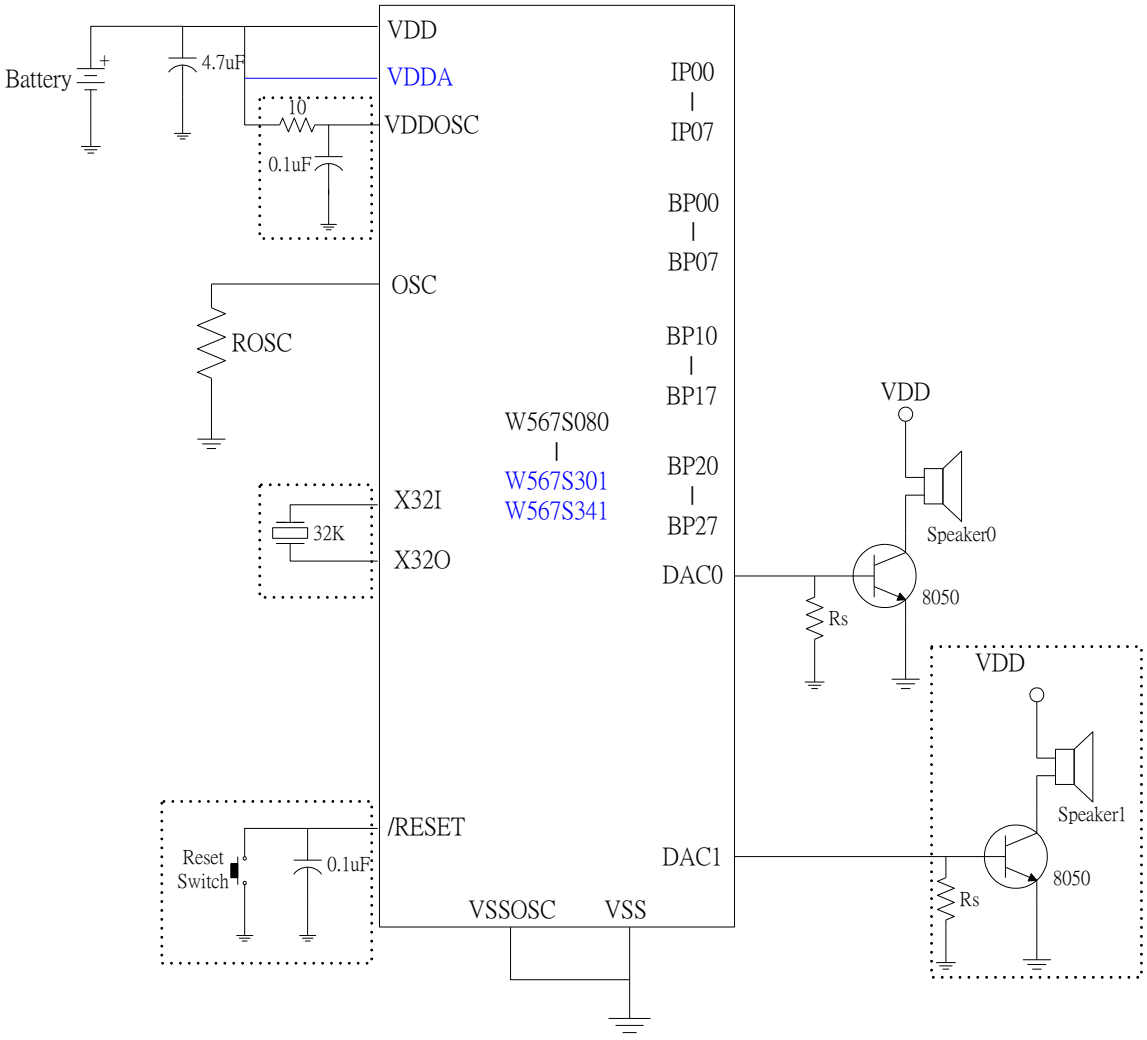
6.2 W567S040~S060



Notes:

1. The typical value of Rosc is 160 KΩ for 8MHz and 330 KΩ for 4MHz and should be connected to GND (V_{SS}).
2. Please refer to design guide to get typical Rosc value for each part number.
3. The Rs value is suggested in 270Ω ~ 1KΩ to limit too large DAC output current flowing into transistor.
4. The capacitor, 4.7uF, shunts between V_{DD} and GND is necessary as power stability. But the value of capacitor is depend on the application.
5. The above application circuits are for reference only. No warranty for mass production.

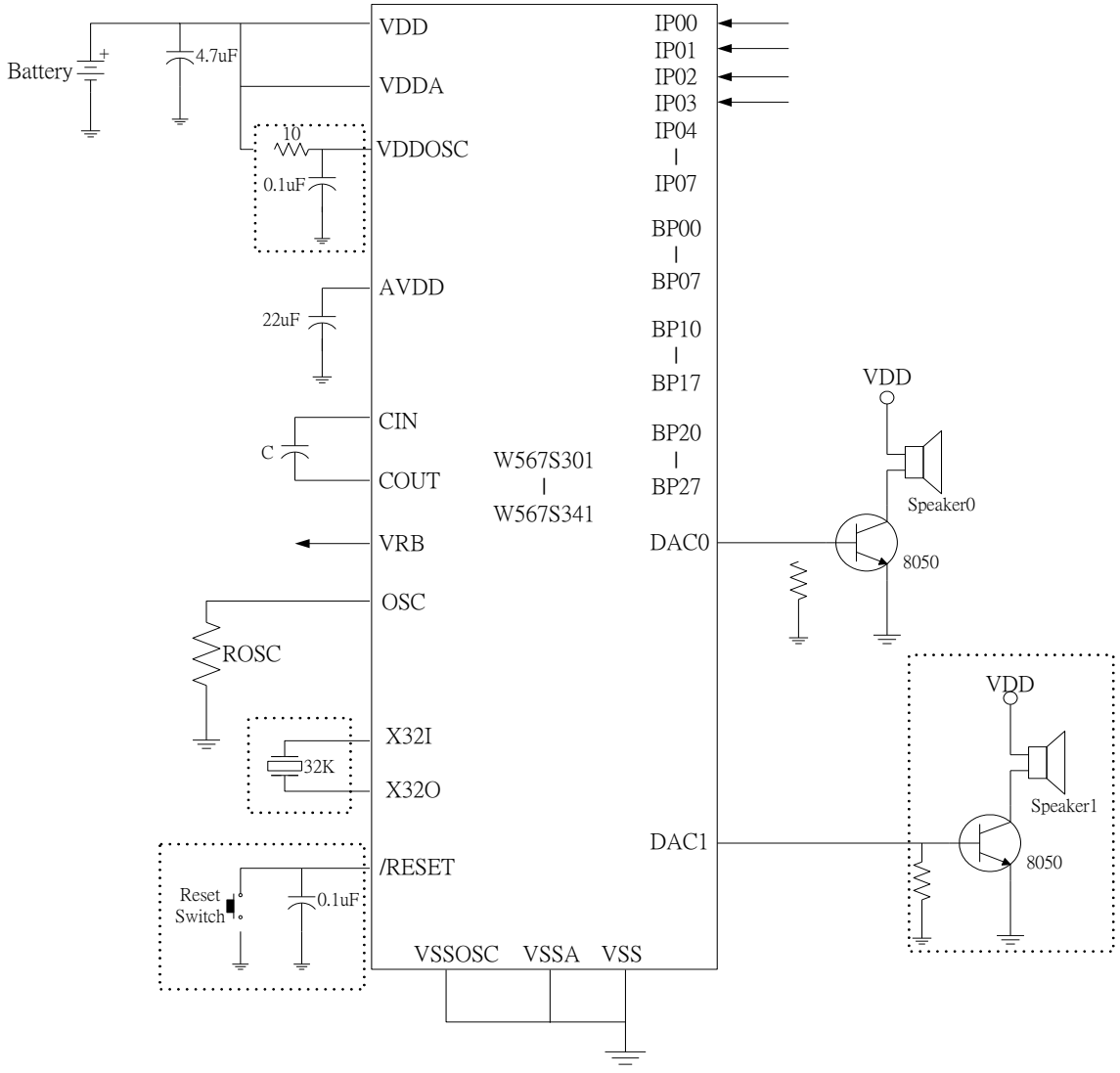
6.3 W567S080~S341



Notes:

1. The typical value of Rosc is 150 KΩ for 8MHz and 300 KΩ for 4MHz and should be connected to GND (V_{SS}).
2. Please refer to design guide to get typical Rosc value for each part number.
3. For W567S080~S341, VSSOSC should be connected to V_{SS}; and VDDOSC should be connected to V_{DD} in PCB layout.
4. Only for W556S301~341, VDDA must be connect to V_{DD} to keep normal standby current.
5. The Rs value is suggested in 270Ω ~ 1KΩ to limit too large DAC output current flowing into transistor.
6. The 10Ω and 0.1μF between V_{DD}, VDDOSC and GND are optional to filter power noise.
7. The capacitor, 4.7μF, shunts between V_{DD} and GND is necessary as power stability. But the value of capacitor is depend on the application.
8. The above application circuits are for reference only. No warranty for mass production.

6.4 W567S301/S341 with ADC Application



Notes:

1. The typical value of Rosc is 150 KΩ for 8MHz and 300 KΩ for 4MHz and should be connected to GND (V_{SS}).
2. Please refer to design guide to get typical Rosc value for each part number.
3. For W567S301~S341, VSSA and VSSOSC should be connected to V_{SS}; and VDDA and VDDOSC should be connected to V_{DD} in PCB layout.
4. For W567S301~S341, VDDA must still be connect to V_{DD} to keep normal standby current, if don't need ADC module application.
5. The Rs value is suggested in 270Ω ~ 1KΩ to limit too large DAC output current flowing into transistor.
6. The 10Ω and 0.1μF between V_{DD}, VDDOSC and GND are optional to filter power noise.
7. The capacitor, 4.7μF, shunts between V_{DD} and GND is necessary as power stability. But the value of capacitor is depend on the application.
8. The above application circuits are for reference only. No warranty for mass production.

7. REVISION HISTORY

VERSION	DATE	REASONS FOR CHANGE
A1.0	Apr 2002	Preliminary release.
A2.0	Jul 2002	W567S020 created. 2 speech channels for entire series. Wording modification.
A3.0	Jul 2002	Modify pin description Modify DC/AC electrical characteristics
A4.0	Oct 2002	Remove SIM out of from W567S040 ~ S060 Define ROSC value in AC ELECTRICAL CHARACTERI
A5.0	Nov 2002	Page 2, provides up to 8 input pins Page 2, available package
A6.0	May 2003	Add a table to show all W567Sxxx duration in page 1 Add ***PowerScript™*** function in feature list Update available package Rename RTC as 32 KHz crystal Update application circuit
A7.0	Sep 2003	Change part number W567S300 as W567S301 Change part number W567S340 as W567S341 Page 3, add Low Voltage Detect (LVD) feature
A8.0	Oct 2003	Update application circuit and notes.
A9.0	Nov 2003	Rename VDD1 to VDDOSC in the Pin Description Update application circuit and notes.
A10.0	Mar 2004	Change the name Low-Voltage-Detect (LVD) to Low-Voltage-Reset (LVR).
A11.0	Jun 2004	Add the operation current of Low-Voltage-Reset.
A12.0	Jug 2005	Revise Features Package form W567S080 ~ S120: LQFP128

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