Winbond Electronics Corp.

8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The W78C33B microcontroller supplies a wider frequency range than most 8-bit microcontrollers on the market. It is functional compatible with the industry standard 80C32 microcontroller series except the one extra 4-bit bit-addressable I/O port (Port 4).

The W78C33B contains four 8-bit bidirectional parallel ports, three 16-bit timer/counters, and a serial port. These peripherals are supported by a six-source, two-level interrupt capability. There are 256 bytes of RAM, and the device supports ROMless operation for application programs.

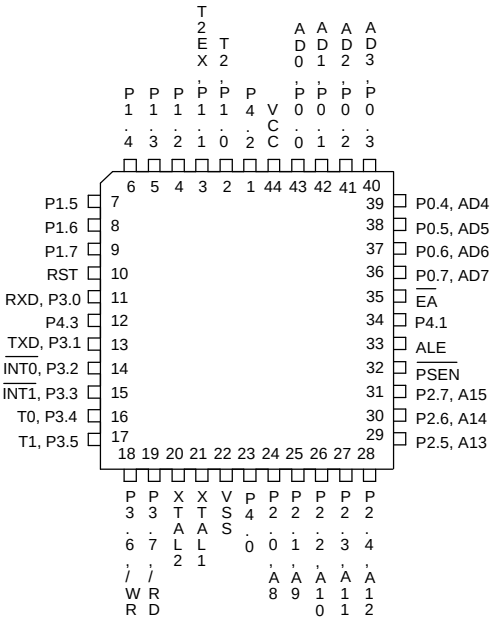
The W78C33B microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor.

FEATURES

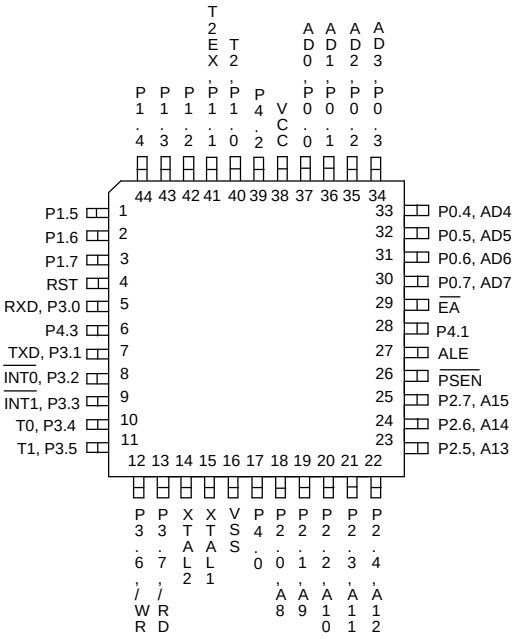
- 8-bit CMOS microcontroller
- Fully static design
- Low standby current at full supply voltage
- DC-40 MHz operation
- 256 bytes of on-chip scratchpad RAM
- ROMless operation
- 64K bytes program memory address space
- 64K bytes data memory address space
- Four 8-bit bidirectional ports
- One extra 4-bit bidirectional port
- Three 16-bit timer/counters
- One full duplex serial port
- Boolean processor
- Six-source, two-level interrupt capability
- Built-in power management
- Packages:
  - PLCC 44: W78C33BP-24/40
  - QFP 44: W78C33BF-24/40
  - TQFP 44: W78C33BM-24/40

PIN CONFIGURATIONS

44-Pin PLCC (W78C33BP)



44-Pin QFP/TQFP (W78C33BF/W78C33BM)



PIN DESCRIPTION

P0.0- P0.7

Port 0, Bits 0 through 7. Port 0 is a bi-directional I/O port. This port also provides a multiplexed low order address/data bus during accesses to external memory.

P1.0- P1.7

Port 1, Bits 0 through 7. Port 1 is a bi-directional I/O port with internal pull-ups. Pins P1.0 and P1.1 also serve as T2 (Timer 2 external input) and T2EX (Timer 2 capture/reload trigger), respectively.

P2.0- P2.7

Port 2, Bits 0 through 7. Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.

P3.0- P3.7

Port 3, Bits 0 through 7. Port 3 is a bi-directional I/O port with internal pull-ups. All bits have alternate functions, which are described below:

PIN	ALTERNATE FUNCTION
P3.0	RXD Serial Receive Data
P3.1	TXD Serial Transmit Data
P3.2	$\overline{INT0}$ External Interrupt 0
P3.3	$\overline{INT1}$ External Interrupt 1
P3.4	T0 Timer 0 Input
P3.5	T1 Timer 1 Input
P3.6	$\overline{WR}$ Data Write Strobe
P3.7	$\overline{RD}$ Data Read Strobe

P4.0- P4.3

Port 4, Bits 0 through 3. Port 4 is a bi-directional I/O port with internal pull-ups.

$\overline{EA}$

External Address Input, active low. This pin forces the processor to execute out of external ROM. This pin should be kept low for all W78C33B operations.

RST

Reset Input, active high. This pin resets the processor. It must be kept high for at least two machine cycles in order to be recognized by the processor.

ALE

Address Latch Enable Output, active high. ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6th of the oscillator frequency. A single ALE pulse is skipped during external data memory accesses. ALE goes to a high state during reset with a weak pull-up.

$\overline{\text{PSEN}}$

Program Store Enable Output, active low. $\overline{\text{PSEN}}$ enables the external ROM onto the Port 0 address/data bus during fetch and MOVC operations. $\overline{\text{PSEN}}$ goes to a high state during reset with a weak pull-up.

XTAL1

Crystal 1. This is the crystal oscillator input. This pin may be driven by an external clock.

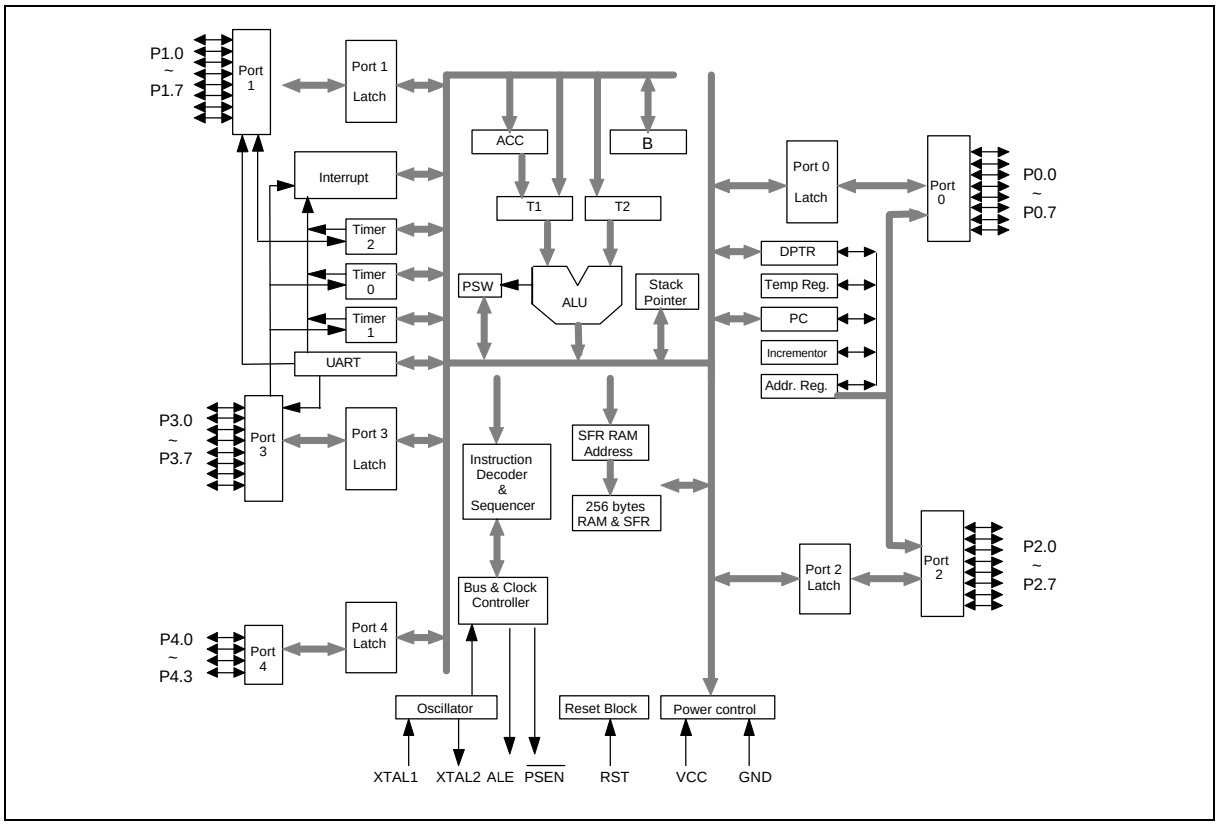
XTAL2

Crystal 2. This is the crystal oscillator output. It is the inversion of XTAL1.

VSS, VCC

Power Supplies. These are the chip ground and positive supplies.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The W78C33B architecture consists of a core controller surrounded by various registers, five general purpose I/O ports, 256 bytes of RAM, three timer/counters, and a serial port. The processor supports 111 different instruction and references both a 64K program address space and a 64K data storage space.

Timers 0, 1, and 2

Timers 0, 1, and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TCON and TMOD registers provide control functions for timers 0, 1. The T2CON register provides control functions for Timer 2. RCAP2H and RCAP2L are used as reload/capture registers for Timer 2.

The operations of Timer 0 and Timer 1 are the same as in the W78C31. Timer 2 is a special feature of the W78C33B: it is a 16-bit timer/counter that is configured and controlled by the T2CON register. Like Timers 0 and 1, Timer 2 can operate as either an external event counter or as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. The clock speed at capture or auto-reload mode is the same as that of Timers 0 and 1.

Clock

The W78C33B is designed to be used with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used. This makes the W78C33B relatively insensitive to duty cycle variations in the clock.

Crystal Oscillator

The W78C33B incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground, and a resistor must also be connected from XTAL1 to XTAL2 to provide a DC bias when the crystal frequency is above 24 MHz.

External Clock

An external clock should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator. As a result, the external clock signal should have an input one level of greater than 3.5 volts.

Power Management

Idle Mode

The idle mode is entered by setting the IDL bit in the PCON register. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

Power-down Mode

When the PD bit of the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks, including the oscillator are stopped. The only way to exit power-down mode is by a reset.

Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running.

An internal trigger circuit in the reset line is used to deglitch the reset line when the W78C33B is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line.

During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

2. PORT4

Another bit-addressable port P4 is also available and only 4 bits (P4<3:0>) can be used. This port address is located at 0D8H with the same function as that of port P1.

```
Example:  P4      REG   0D8H
          MOV     P4, #0AH    ; Output data "A" through P4.0–P4.3.
          MOV     A, P4       ; Read P4 status to Accumulator.
          SETB    P4.0        ; Set bit P4.0
          CLR     P4.1        ; Clear bit P4.1
```

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	V_{CC}–V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{CC} +0.3	V
Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{ST}	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC CHARACTERISTICS

(V_{DD}-V_{SS} = 5V ±10%, T_A = 25°C, Fosc = 20 MHz, unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION		UNIT	TEST CONDITIONS
		MIN.	MAX.		
Operating Voltage	V_{DD}	4.5	5.5	V	
Operating Current	I_{DD}	-	20	mA	No load V_{DD} = 5.5V
Idle Current	I_{IDLE}	-	6	mA	Idle mode V_{DD} = 5.5V
Power Down Current	I_{PWDN}	-	50	µA	Power-down mode V_{DD} = 5.5V
Input Current P1, P2, P3, P4	I_{IN1}	-50	+10	µA	V_{DD} = 5.5V V_{IN} = 0V or V_{DD}
Input Current RST	I_{IN2}	-10	+300	µA	V_{DD} = 5.5V 0 < V_{IN} < V_{DD}
Input Leakage Current P0, $\overline{EA}$	I_{LK}	-10	+10	µA	V_{DD} = 5.5V 0V <V_{IN} < V_{DD}
Logic 1 to 0 Transition Current P1, P2, P3, P4	I_{TL} [*4]	-500	-200	µA	V_{DD} = 5.5V V_{IN} =2.0V
Input Low Voltage P0, P1, P2, P3, P4, $\overline{EA}$	V_{IL1}	0	0.8	V	V_{DD} = 4.5V
Input Low Voltage RST	V_{IL2}	0	0.8	V	V_{DD} = 4.5V
Input Low Voltage XTAL1[*4]	V_{IL3}	0	0.8	V	V_{DD} = 4.5V
Input High Voltage P0, P1, P2, P3, P4, $\overline{EA}$	V_{IH1}	2.4	V_{DD} +0.2	V	V_{DD} = 5.5V
Input High Voltage RST	V_{IH2}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
Input High Voltage XTAL1 [*4]	V_{IH3}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
Output Low Voltage P1, P2, P3, P4	V_{OL1}	-	0.45	V	V_{DD} = 4.5V I_{OL} = +2 mA

DC Characteristics, continued

PARAMETER	SYM.	SPECIFICATION		UNIT	TEST CONDITIONS
		MIN.	MAX.		
Output Low Voltage P0, ALE, $\overline{PSEN}$ [*3]	V_{OL2}	-	0.45	V	V_{DD} = 4.5V I_{OL} = +4mA
Sink Current P1, P2, P3, P4	I_{SK1}	4	8	mA	V_{DD} = 4.5V Vs = 0.45V
Sink Current P0, ALE, $\overline{PSEN}$	I_{SK2}	10	14	mA	V_{DD} = 4.5V Vs = 0.45V
Output High Voltage P1, P2, P3, P4	V_{OH1}	2.4	-	V	V_{DD} = 4.5V I_{OH} = -100 µA
Output High Voltage P0, ALE, $\overline{PSEN}$ [*3]	V_{OH2}	2.4	-	V	V_{DD} = 4.5V I_{OH} = -400 µA
Source Current P1, P2, P3, P4	I_{SR1}	-120	-180	µA	V_{DD} = 4.5V Vs = 2.4V
Source Current P0, ALE, $\overline{PSEN}$	I_{SR2}	-10	-14	mA	V_{DD} = 4.5V Vs = 2.4V

Notes:

*1. RST pin is a Schmitt trigger input. RST has internal pull-low resistors of about 30 KΩ.

*3. P0, ALE and /PSEN are tested in the external access mode.

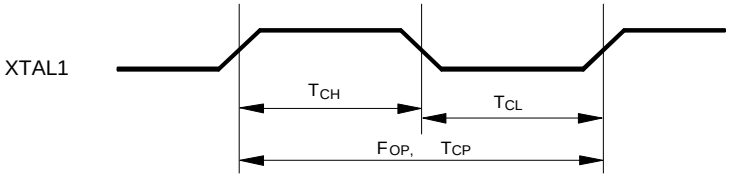
*4. XTAL1 is a CMOS input.

*5. Pins of P1, P2, P3, P4 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} approximates to 2V.

AC CHARACTERISTICS

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (T_{CP}), and actual parts will usually experience less than a ±20 nS variation. The numbers below represent the performance expected from a 1.2 micron CMOS process when using 2 and 4 mA output buffers.

Clock Input Waveform



Continued

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	FOP	0	-	40	MHz	1
Clock Period	TCP	25	-	-	nS	2
Clock High	TCH	10	-	-	nS	3
Clock Low	TCL	10	-	-	nS	3

Notes:

1. The clock may be stopped indefinitely in either state.
2. The TCP specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	TAAS	1 TCP-Δ	-	-	nS	4
Address Hold after ALE Low	TAAH	1 TCP-Δ	-	-	nS	1, 4
ALE Low to $\overline{\text{PSEN}}$ Low	TAPL	1 TCP-Δ	1Tcp	1Tcp+Δ	nS	4
$\overline{\text{PSEN}}$ Low to Data Valid	TPDA	-	-	2 TCP	nS	2
Data Hold after $\overline{\text{PSEN}}$ High	TPDH	0	-	1 TCP	nS	3
Data Float after $\overline{\text{PSEN}}$ High	TPDZ	0	-	1 TCP	nS	
ALE Pulse Width	TALW	2 TCP-Δ	2 TCP	-	nS	4
$\overline{\text{PSEN}}$ Pulse Width	TPSW	3 TCP-Δ	3 TCP	-	nS	4

Notes:

1. P0.0–P0.7, P2.0–P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 TCP.
3. Data have been latched internally prior to $\overline{\text{PSEN}}$ going high.
4. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Data Read Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
ALE Low to $\overline{\text{RD}}$ Low	TDAR	3 TCP-Δ	-	3 TCP+Δ	nS	1, 2
$\overline{\text{RD}}$ Low to Data Valid	TDDA	-	-	4 TCP	nS	1
Data Hold after $\overline{\text{RD}}$ High	TDDH	0	-	2 TCP	nS	
Data Float after $\overline{\text{RD}}$ High	TDDZ	0	-	2 TCP	nS	
$\overline{\text{RD}}$ Pulse Width	TDRD	6 TCP-Δ	6 TCP	-	nS	2

Notes:

1. Data memory access time is 8 TCP.
2. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Data Write Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to $\overline{WR}$ Low	TDAW	3 TCP-Δ	-	3 TCP+Δ	nS
Data Valid to $\overline{WR}$ Low	TDAD	1 TCP-Δ	-	-	nS
Data Hold from $\overline{WR}$ High	TDWD	1 TCP-Δ	-	-	nS
$\overline{WR}$ Pulse Width	TDWR	6 TCP-Δ	6 TCP	-	nS

Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

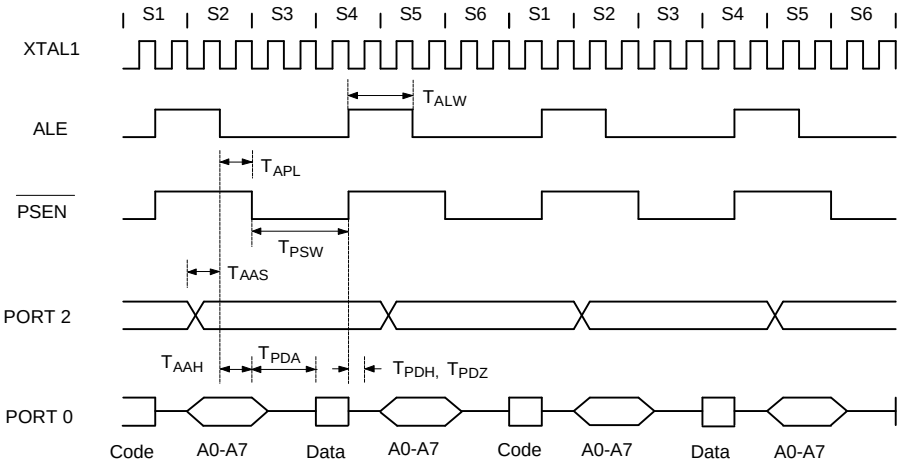
Port Access Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	TPDS	1 TCP	-	-	nS
Port Input Hold from ALE Low	TPDH	0	-	-	nS
Port Output to ALE	TPDA	1 TCP	-	-	nS

Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

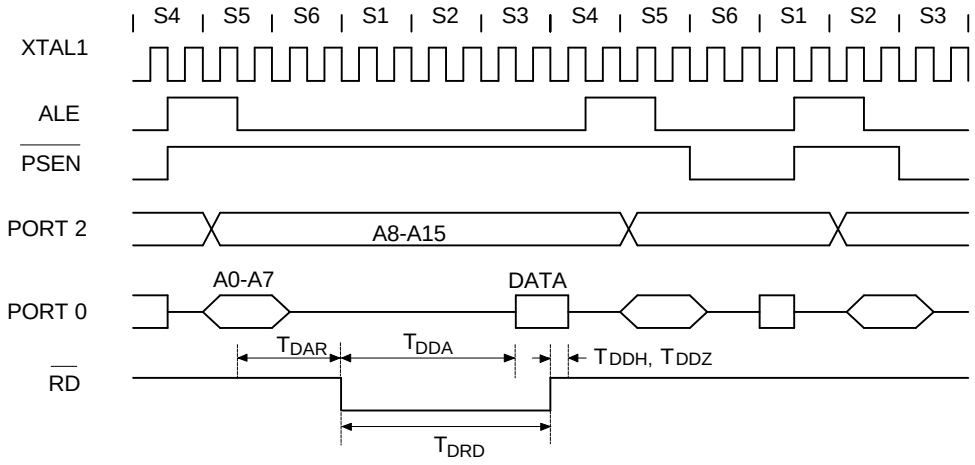
TIMING WAVEFORMS

Program Fetch Cycle

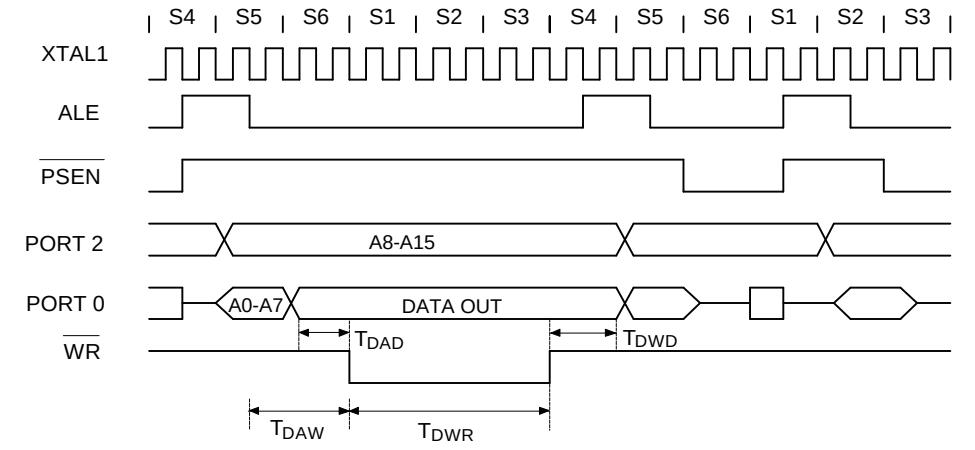


Timing Waveforms, continued

Data Read Cycle

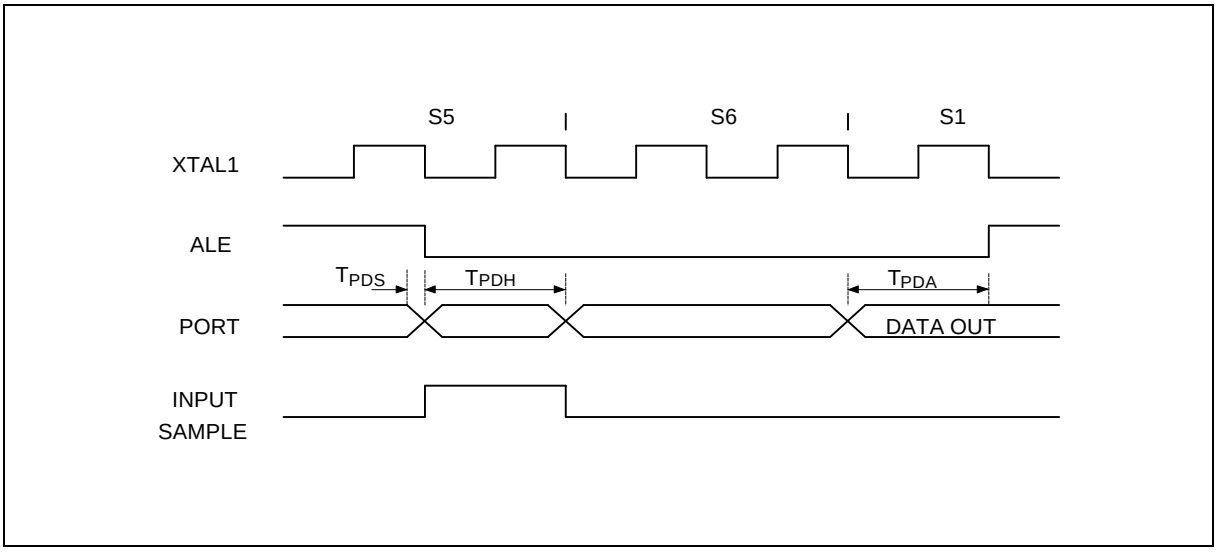


Data Write Cycle



Timing Waveforms, continued

Port Access Cycle



TYPICAL APPLICATION CIRCUIT

Using External Program Memory and Crystal

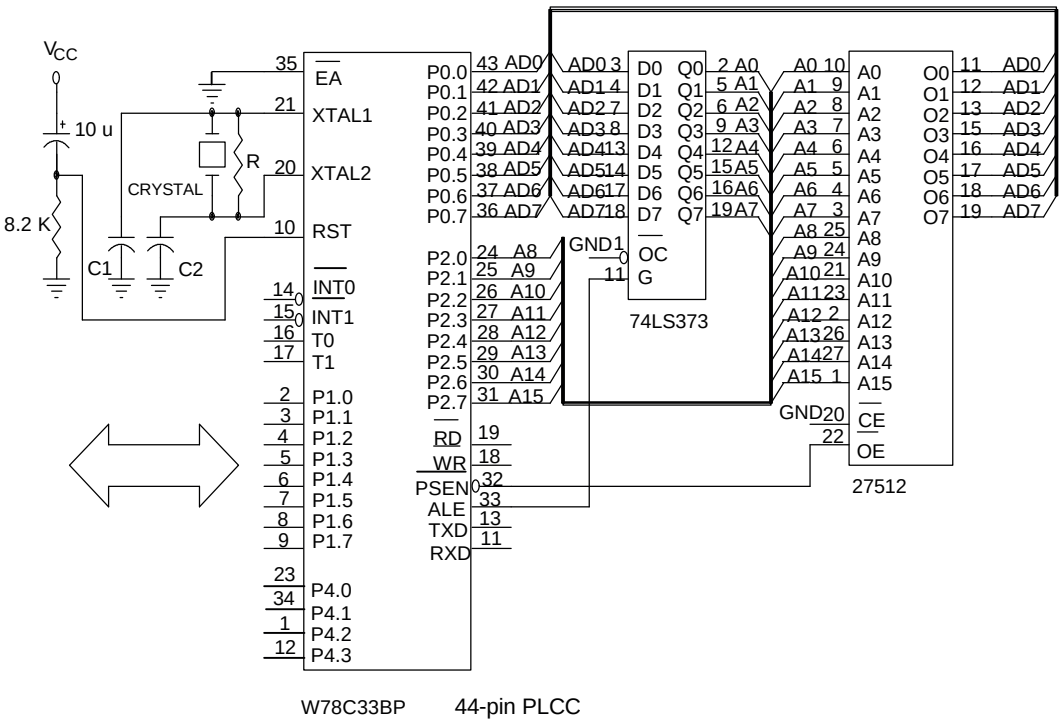


Figure A

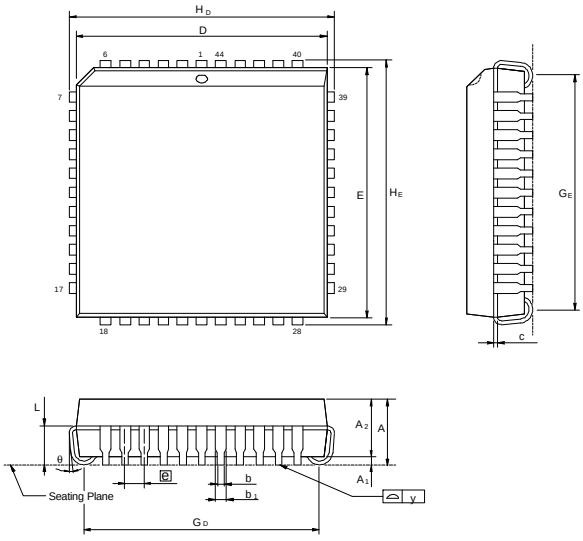
CRYSTAL	C1	C2	R
16 MHz	30P	30P	-
24 MHz	15P	15P	-
33 MHz	10P	10P	6.8K
40 MHz	5P	5P	6.8K

Above table shows the reference values for crystal applications.

Note: C1, C2, R components refer to Figure A.

PACKAGE DIMENSIONS

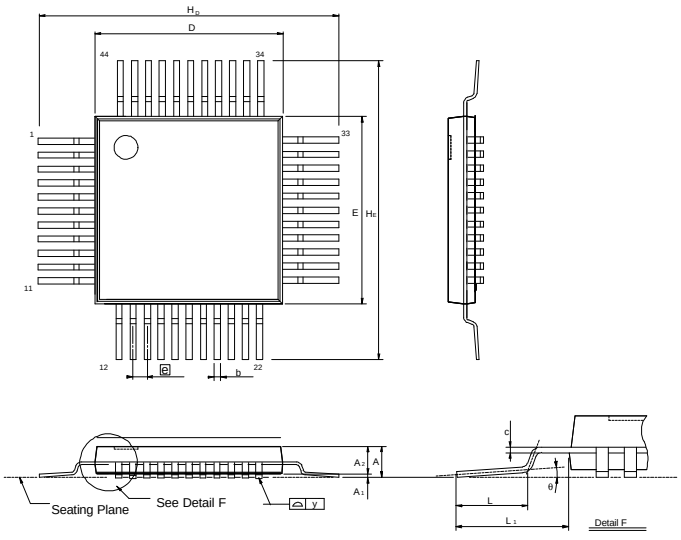
44-pin PLCC



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.699
A_1	0.020	—	—	0.508	—	—
A_2	0.145	0.150	0.155	3.683	3.81	3.937
b_1	0.026	0.028	0.032	0.66	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.296	2.54	2.794
y	—	—	0.004	—	—	0.10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

44-pin QFP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	---	---	---	---
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.510	0.520	0.530	12.95	13.2	13.45
H_E	0.510	0.520	0.530	12.95	13.2	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	0.051	0.063	0.075	1.295	1.6	1.905
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

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