

W78E54C/W78E054C Data Sheet



8-BIT MICROCONTROLLER

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1. GENERAL DESCRIPTION

The W78E054C is an 8-bit microcontroller which can accommodate a wider frequency range with low power consumption. The instruction set for the W78E054C is fully compatible with the standard 8051. The W78E054C contains an 16K bytes Flash EPROM; a 256 bytes RAM; four 8-bit bi-directional and bit-addressable I/O ports; an additional 4-bit I/O port P4; three 16-bit timer/counters; a hardware watchdog timer and a serial port. These peripherals are supported by eight sources two-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W78E054C allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

The W78E054C microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor.

2. FEATURES

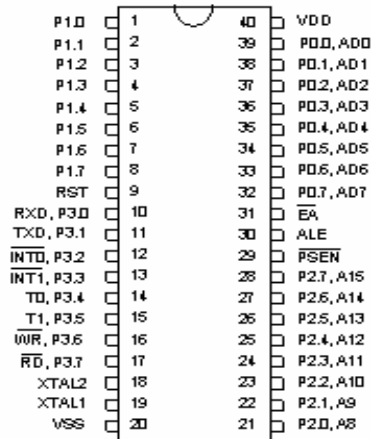
- Fully static design 8-bit CMOS microcontroller
- Wide supply voltage of 4.5V to 5.5V
- 256 bytes of on-chip scratchpad RAM
- 16 KB electrically erasable/programmable Flash EPROM
- 64 KB program memory address space
- 64 KB data memory address space
- Four 8-bit bi-directional ports
- One extra 4-bit bit-addressable I/O port, additional $\overline{\text{INT2}}$ / $\overline{\text{INT3}}$ (available on 44-pin PLCC/QFP package)
- Three 16-bit timer/counters
- One full duplex serial port(UART)
- Watchdog Timer
- Eight sources, two-level interrupt capability
- EMI reduction mode
- Built-in power management
- Code protection mechanism
- Packages:
 - Lead Free (RoHS) DIP 40: W78E054C40DL
 - Lead Free (RoHS) PLCC 44: W78E054C40PL
 - Lead Free (RoHS) PQFP 44: W78E054C40FL

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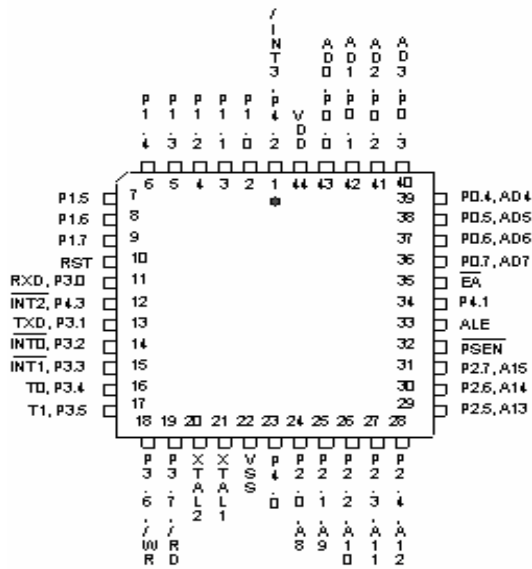


3. PIN CONFIGURATIONS

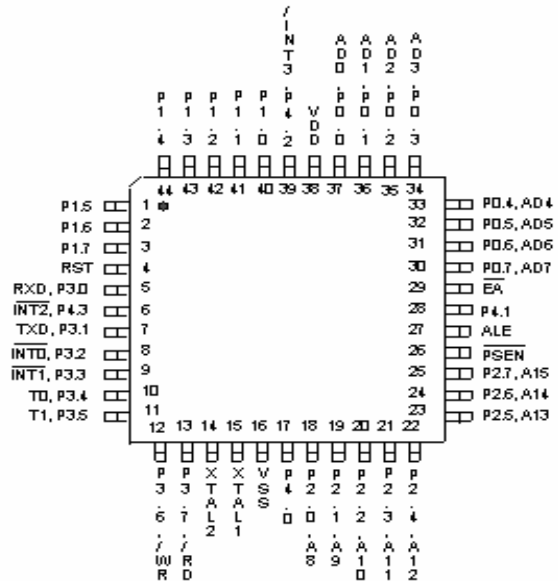
40-Pin DIP



44-Pin PLCC



44-Pin QFP





4. PIN DESCRIPTION

| SYMBOL | DESCRIPTIONS |
|-------------------|---|
| \overline{EA} | EXTERNAL ACCESS ENABLE: This pin forces the processor to execute out of external ROM. It should be kept high to access internal ROM. The ROM address and data will not be presented on the bus if \overline{EA} pin is high and the program counter is within on-chip ROM area. |
| \overline{PSEN} | PROGRAM STORE ENABLE: \overline{PSEN} enables the external ROM data onto the Port 0 address/ data bus during fetch and MOVC operations. When internal ROM access is performed, no \overline{PSEN} strobe signal outputs from this pin. |
| ALE | ADDRESS LATCH ENABLE: ALE is used to enable the address latch that separates the address from the data on Port 0. |
| RST | RESET: A high on this pin for two machine cycles while the oscillator is running resets the device. |
| XTAL1 | CRYSTAL1: This is the crystal oscillator input. This pin may be driven by an external clock. |
| XTAL2 | CRYSTAL2: This is the crystal oscillator output. It is the inversion of XTAL1. |
| VSS | GROUND: Ground potential |
| VDD | POWER SUPPLY: Supply voltage for operation. |
| P0.0–P0.7 | PORT 0: Port 0 is a bi-directional I/O port which also provides a multiplexed low order address/data bus during accesses to external memory. The Port 0 is also an open-drain port and external pull-ups need to be connected while in programming. |
| P1.0–P1.7 | PORT 1: Port 1 is a bi-directional I/O port with internal pull-ups. The bits have alternate functions which are described below: T2(P1.0): Timer/Counter 2 external count input T2EX(P1.1): Timer/Counter 2 Reload/Capture control |
| P2.0–P2.7 | PORT 2: Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory. |
| P3.0–P3.7 | PORT 3: Port 3 is a bi-directional I/O port with internal pull-ups. All bits have alternate functions, which are described below: RXD(P3.0) : Serial Port receiver input TXD(P3.1) : Serial Port transmitter output $\overline{INT0}$ (P3.2) : External Interrupt 0 $\overline{INT1}$ (P3.3) : External Interrupt 1 T0(P3.4) : Timer 0 External Input T1(P3.5) : Timer 1 External Input \overline{WR} (P3.6) : External Data Memory Write Strobe \overline{RD} (P3.7) : External Data Memory Read Strobe |
| P4.0–P4.3 | PORT 4: Another bit-addressable bidirectional I/O port P4. P4.3 and P4.2 are alternative function pins. It can be used as general I/O port or external interrupt input sources ($\overline{INT2}$ / $\overline{INT3}$). |



5. FUNCTIONAL DESCRIPTION

The W78E054C architecture consists of a core controller surrounded by various registers, five general purpose I/O ports, 256 bytes of RAM, three timer/counters, and a serial port. The processor supports 111 different opcodes and references both a 64K program address space and a 64K data storage space.

5.1 Timers 0, 1, and 2

Timers 0, 1, and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TCON and TMOD registers provide control functions for timers 0 and 1. The T2CON register provides control functions for Timer 2. RCAP2H and RCAP2L are used as reload/capture registers for Timer 2.

The operations of Timer 0 and Timer 1 are the same as in the W78C51. Timer 2 is a special feature of the W78E054C: it is a 16-bit timer/counter that is configured and controlled by the T2CON register. Like Timers 0 and 1, Timer 2 can operate as either an external event counter or as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. The clock speed at capture or auto-reload mode is the same as that of Timers 0 and 1.

5.2 New Defined Peripheral

In order to be more suitable for I/O, an extra 4-bit bit-addressable port P4 and two external interrupt $\overline{INT2}$, $\overline{INT3}$ has been added to either the PLCC or QFP 44-pin package. And description follows:

5.2.1 $\overline{INT2}/\overline{INT3}$

Two additional external interrupts, $\overline{INT2}$ and $\overline{INT3}$, whose functions are similar to those of external interrupt 0 and 1 in the standard 80C52. The functions/status of these interrupts are determined/shown by the bits in the XICON (External Interrupt Control) register. The XICON register is bit-addressable but is not a standard register in the standard 80C52. Its address is at 0C0H. To set/clear bits in the XICON register, one can use the "SETB (/CLR) bit" instruction. For example, "SETB 0C2H" sets the EX2 bit of XICON.

XICON - external interrupt control (C0H)

| | | | | | | | |
|-----|-----|-----|-----|-----|-----|-----|-----|
| PX3 | EX3 | IE3 | IT3 | PX2 | EX2 | IE2 | IT2 |
|-----|-----|-----|-----|-----|-----|-----|-----|

PX3: External interrupt 3 priority high if set

EX3: External interrupt 3 enable if set

IE3: If IT3 = 1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced

IT3: External interrupt 3 is falling-edge/low-level triggered when this bit is set/cleared by software

PX2: External interrupt 2 priority high if set

EX2: External interrupt 2 enable if set

IE2: If IT2 = 1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced

IT2: External interrupt 2 is falling-edge/low-level triggered when this bit is set/cleared by software



Eight-source interrupt information

| INTERRUPT SOURCE | VECTOR ADDRESS | POLLING SEQUENCE WITHIN PRIORITY LEVEL | ENABLE REQUIRED SETTINGS | INTERRUPT TYPE EDGE/LEVEL |
|----------------------|----------------|--|--------------------------|---------------------------|
| External Interrupt 0 | 03H | 0 (highest) | IE.0 | TCON.0 |
| Timer/Counter 0 | 0BH | 1 | IE.1 | - |
| External Interrupt 1 | 13H | 2 | IE.2 | TCON.2 |
| Timer/Counter 1 | 1BH | 3 | IE.3 | - |
| Serial Port | 23H | 4 | IE.4 | - |
| Timer/Counter 2 | 2BH | 5 | IE.5 | - |
| External Interrupt 2 | 33H | 6 | XICON.2 | XICON.0 |
| External Interrupt 3 | 3BH | 7 (lowest) | XICON.6 | XICON.3 |

5.2.2 PORT4

Another bit-addressable port P4 is also available and only 4 bits (P4<3:0>) can be used. This port address is located at 0D8H with the same function as that of port P1, except the P4.3 and P4.2 are alternative function pins. It can be used as general I/O pins or external interrupt input sources ($\overline{\text{INT2}}$, $\overline{\text{INT3}}$).

Example:

```

P4      REG  0D8H
MOV     P4, #0AH    ; Output data "A" through P4.0–P4.3.
MOV     A, P4       ; Read P4 status to Accumulator.
SETB   P4.0        ; Set bit P4.0
CLR    P4.1        ; Clear bit P4.1

```

5.2.3 Reduce EMI Emission

Because of on-chip Flash EPROM, when a program is running in internal ROM space, the ALE will be unused. The transition of ALE will cause noise, so it can be turned off to reduce the EMI emission if it is useless. Turning off the ALE signal transition only requires setting the bit 0 of the AUXR SFR, which is located at 08Eh. When ALE is turned off, it will be reactivated when the program accesses external ROM/RAM data or jumps to execute an external ROM code. The ALE signal will turn off again after it has been completely accessed or the program returns to internal ROM code space. The AO bit in the AUXR register, when set, disables the ALE output. In order to reduce EMI emission from oscillation circuitry, W78E054C allows user to diminish the gain of on-chip oscillator amplifiers by using programmer to clear the B7 bit of security register. Once B7 is set to 0, a half of gain will be decreased. Care must be taken if user attempts to diminish the gain of oscillator amplifier, reducing a half of gain may affect the external crystal operating improperly at high frequency above 24 MHz. The value of R and C1, C2 may need some adjustment while running at lower gain.



*****AUXR - Auxiliary register (8EH)**

| | | | | | | | |
|---|---|---|---|---|---|---|----|
| - | - | - | - | - | - | - | AO |
|---|---|---|---|---|---|---|----|

AO: Turn off ALE output.

5.3 Power-off Flag

*****PCON - Power control (87H)**

| | | | | | | | |
|---|---|---|-----|-----|-----|----|-----|
| - | - | - | POF | GF1 | GF0 | PD | IDL |
|---|---|---|-----|-----|-----|----|-----|

POF: Power off flag. Bit is set by hardware when power on reset. It can be cleared by software to determine chip reset is a warm boot or cold boot.

GF1, GF0: These two bits are general-purpose flag bits for the user.

PD: Power down mode bit. Set it to enter power down mode.

IDL: Idle mode bit. Set it to enter idle mode.

The power-off flag is located at PCON.4. This bit is set when VDD has been applied to the part. It can be used to determine if a reset is a warm boot or a cold boot if it is subsequently reset by software.

5.4 Watchdog Timer

The Watchdog timer is a free-running timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs, a system reset can also be caused if it is enabled. The main use of the Watchdog timer is as a system monitor. This is important in real-time control applications. In case of power glitches or electromagnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. The watchdog time-out selection will result in different time-out values depending on the clock speed. The Watchdog timer will be disabled on reset. In general, software should restart the Watchdog timer to put it into a known state. The control bits that support the Watchdog timer are discussed below.

Watchdog Timer Control Register

| | | | | | | | | |
|------|-----|------|------|---|---|-----|-----|-----|
| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | ENW | CLRW | WIDL | - | - | PS2 | PS1 | PS0 |

Mnemonic: WDTC

Address: 8FH

ENW : Enable watch-dog if set.

CLRW : Clear watch-dog timer and prescaler if set. This flag will be cleared automatically

WIDL : If this bit is set, watch-dog is enabled under IDLE mode. If cleared, watch-dog is disabled under IDLE mode. Default is cleared.

PS2, PS1, PS0: Watch-dog prescaler timer select. Prescaler is selected when set PS2~0 as follows:

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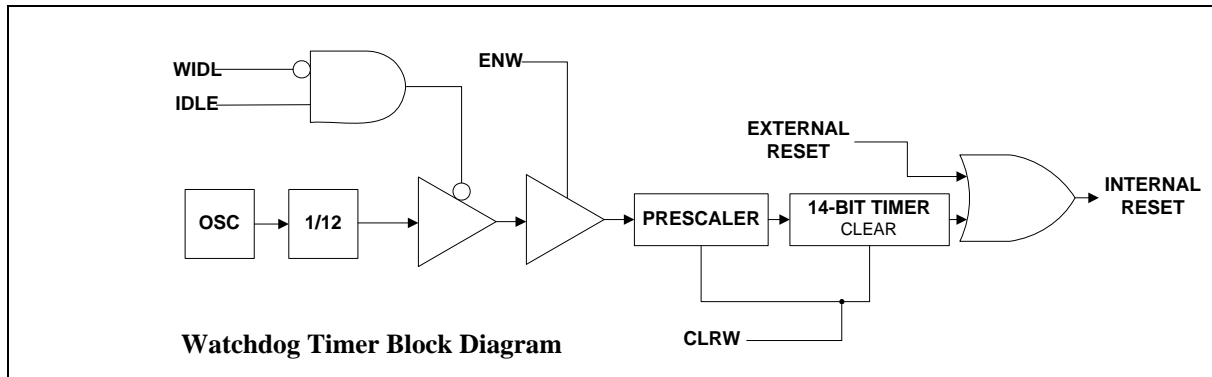


| PS2 PS1 PS0 | PRESCALER SELECT |
|-------------|------------------|
| 0 0 0 | 2 |
| 0 0 1 | 4 |
| 0 1 0 | 8 |
| 0 1 1 | 16 |
| 1 0 0 | 32 |
| 1 0 1 | 64 |
| 1 1 0 | 128 |
| 1 1 1 | 256 |

The time-out period is obtained using the following equation:

$$\frac{1}{\text{OSC}} \times 2^{14} \times \text{PRESCALER} \times 1000 \times 12 \text{ mS}$$

Before Watchdog time-out occurs, the program must clear the 14-bit timer by writing 1 to WDTC.6 (CLRW). After 1 is written to this bit, the 14-bit timer, prescaler and this bit will be reset on the next instruction cycle. The Watchdog timer is cleared on reset.



Typical Watch-Dog time-out period when OSC = 20 MHz

| PS2 PS1 PS0 | WATCHDOG TIME-OUT PERIOD |
|-------------|--------------------------|
| 0 0 0 | 19.66 mS |
| 0 0 1 | 39.32 mS |
| 0 1 0 | 78.64 mS |
| 0 1 1 | 157.28 mS |
| 1 0 0 | 314.57 mS |
| 1 0 1 | 629.14 mS |
| 1 1 0 | 1.25 S |
| 1 1 1 | 2.50 S |



5.5 Clock

The W78E054C is designed to be used with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used. This makes the W78E054C relatively insensitive to duty cycle variations in the clock. The W78E054C incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground. An external clock source should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator.

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5.6 Power Management

Idle Mode

The idle mode is entered by setting the IDL bit in the PCON register. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

Power-down Mode

When the PD bit of the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks are stopped, including the oscillator. The only way to exit power-down mode is by a reset.

5.7 Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running. An internal trigger circuit in the reset line is used to deglitch the reset line when the W78E054C is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line.

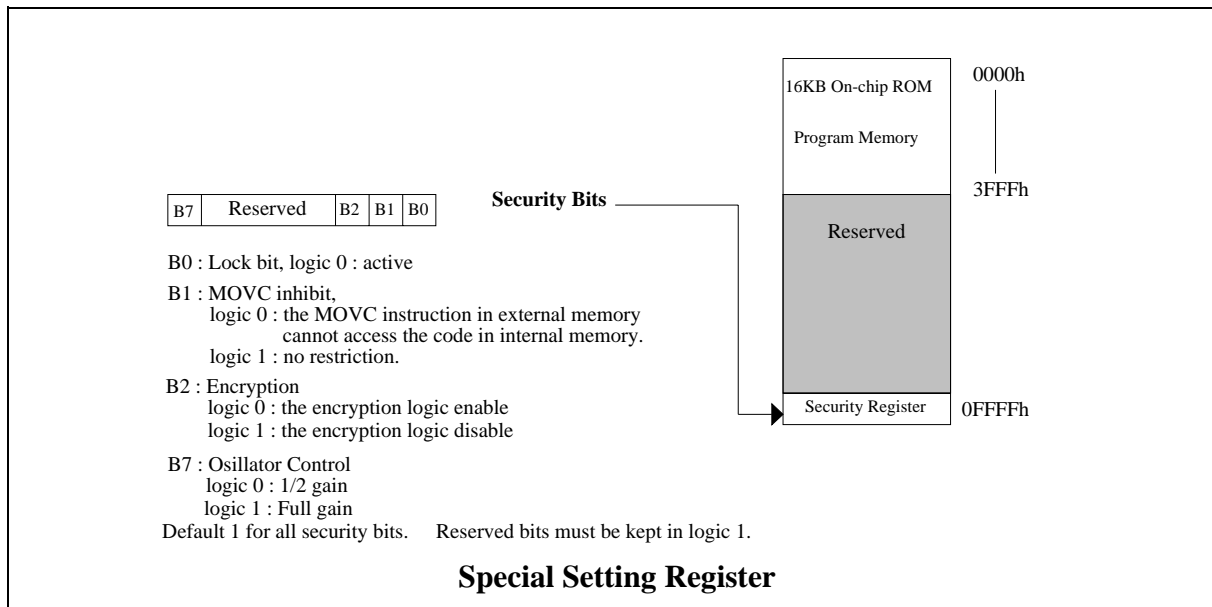
During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.



6. SECURITY BITS

During the on-chip Flash EPROM operation mode, the Flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of Flash EPROM and those operations on it are described below.

The W78E054C has a Security Register which can not be accessed in normal mode. These registers can only be accessed from the Flash EPROM operation mode. Those bits of the Security Register can not be changed once they have been programmed from high to low. They can only be reset through erase-all operation. The Security Register is addressed in the Flash EPROM operation mode by address #0FFFFh.



6.1 Lock Bit

This bit is used to protect the customer's program code in the W78E054C. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the Flash EPROM data and Special Setting Register can not be accessed again.



6.2 MOV C Inhibit

This bit is used to restrict the accessible region of the MOV C instruction. It can prevent the MOV C instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOV C instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOV C instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOV C instruction.

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6.3 Encryption

This bit is used to enable/disable the encryption logic for code protection. Once encryption feature is enabled, the data presented on port 0 will be encoded via encryption logic. Only whole chip erase will reset this bit.



7. ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|-----------------------|---------|----------|----------|------|
| DC Power Supply | VDD-VSS | -0.3 | +7.0 | V |
| Input Voltage | VIN | VSS -0.3 | VDD +0.3 | V |
| Operating Temperature | TA | 0 | 70 | °C |
| Storage Temperature | TST | -55 | +150 | °C |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

7.2 D.C. Characteristics

(VCC-VSS = 5V ±10%, TA = 25° C, unless otherwise specified.)

| PARAMETER | SYMBOL | TEST CONDITIONS | PECIFICATION | | UNIT |
|--|--------|---------------------------------|--------------|------|------|
| | | | MIN. | MAX. | |
| Operating Voltage | VDD | - | 4.5 | 5.5 | V |
| Operating Current | IDD | No load, VDD = 5.5V, RST = 1 | - | 20 | mA |
| Idle Current | IIDLE | Idle mode VDD = 5.5V | - | 6 | mA |
| Power Down Current | IPWDN | Power-down mode VDD = 5.5V | - | 50 | μA |
| Input Current P1, P2, P3, P4 | IIN1 | VDD = 5.5V VIN = 0V or VDD | -50 | +10 | μA |
| Logical 1-to-0 Transition Current P1, P2, P3 (*1), P4 | ITL | VDD = 5.5V VIN = 2.0V (*1) | -550 | - | μA |
| Input Current RST (*2) | IIN2 | VDD = 5.5V VIN = VDD | -10 | +300 | μA |
| Input Leakage Current P0, EA | ILK | VDD = 5.5V 0V < VIN < VDD | -10 | +10 | μA |
| Output Low Voltage P1, P2, P3, P4 | VOL1 | VDD = 4.5V IOL1 = +2 mA | - | 0.45 | V |
| Output Low Voltage ALE, PSEN, P0 (*3) | VOL2 | VDD = 4.5V IOL2 = +4 mA | - | 0.45 | V |
| Output High Voltage P1, P2, P3, P4 | VOH1 | VDD = 4.5V IOH1 = -100 μA | 2.4 | - | V |

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DC Characteristics, continued

| PARAMETER | SYMBOL | TEST CONDITIONS | PECIFICATION | | UNIT |
|--|------------------|---|-------------------------|-------------------------|---------|
| | | | MIN. | MAX. | |
| Output High Voltage ALE, $\overline{\text{PSEN}}$, P0 (*3) | V _{OH2} | V _{DD} = 4.5V I _{OH2} = -400 μ A | 2.4 | - | V |
| Input Low Voltage (Except RST) | V _{IL1} | V _{DD} = 4.5V | 0 | 0.8 | V |
| Input Low Voltage RST (*4) | V _{IL2} | V _{DD} = 4.5V | 0 | 0.8 | V |
| Input Low Voltage XTAL1 (*4) | V _{IL3} | V _{DD} = 4.5V | 0 | 0.8 | V |
| Input High Voltage (Except RST) | V _{IH1} | V _{DD} = 4.5V | 2.4 | V _{DD} +0.2 | V |
| Sink Current P1, P2, P3, P4 | I _{SK1} | V _{DD} = 4.5V V _s = 0.45V | 4 | 12 | mA |
| Input High Voltage RST (*4) | V _{IH2} | V _{DD} = 4.5V | 0.67 V _{DD} | V _{DD} +0.2 | V |
| Input High Voltage XTAL1 (*4) | V _{IH3} | V _{DD} = 4.5V | 0.67 V _{DD} | V _{DD} +0.2 | V |
| Sink Current P0, ALE, $\overline{\text{PSEN}}$ (*3) | I _{SK2} | V _{DD} = 4.5V V _s = 0.45V | 8 | 16 | mA |
| Source Current P1, P2, P3, P4 | I _{SR1} | V _{DD} = 4.5V V _s = 2.4V | -100 | -250 | μ A |
| Source Current P0, ALE, $\overline{\text{PSEN}}$ (*3) | I _{SR2} | V _{DD} = 4.5V V _s = 2.4V | -8 | -14 | mA |

Notes:

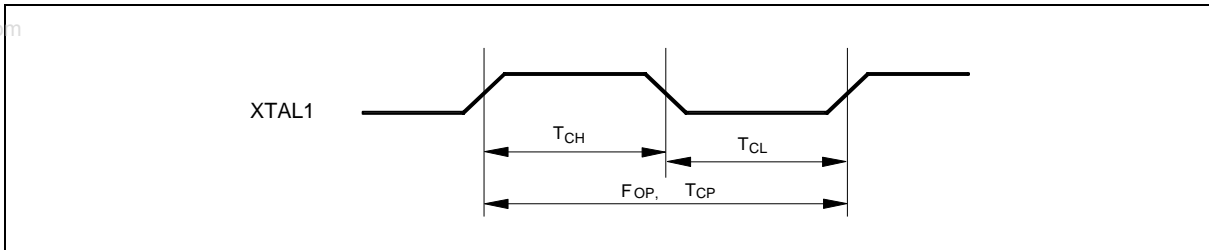
- *1. Pins P1, P2 and P3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
- *2. RST pin has an internal pull-down resistor.
- *3. P0, ALE, $\overline{\text{PSEN}}$ are in the external access memory mode.
- *4. XTAL1 is a CMOS input and RST is a Schmitt trigger input.



7.3 A.C. Characteristics

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (TCP), and actual parts will usually experience less than a ± 20 nS variation. The numbers below represent the performance expected from a 0.6micron CMOS process when using 2 and 4 mA output buffers.

7.3.1 Clock Input Waveform



| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT | NOTES |
|-----------------|--------|------|------|------|------|-------|
| Operating Speed | FOP | 0 | - | 40 | MHz | 1 |
| Clock Period | TCP | 25 | - | - | nS | 2 |
| Clock High | TCH | 10 | - | - | nS | 3 |
| Clock Low | TCL | 10 | - | - | nS | 3 |

Notes:

1. The clock may be stopped indefinitely in either state.
2. The T_{CP} specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

7.3.2 Program Fetch Cycle

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT | NOTES |
|--|--------|-----------|-------|-------|------|-------|
| Address Valid to ALE Low | TAAS | 1 TCP - Δ | - | - | nS | 4 |
| Address Hold from ALE Low | TAAH | 1 TCP - Δ | - | - | nS | 1, 4 |
| ALE Low to $\overline{\text{PSEN}}$ Low | TAPL | 1 TCP - Δ | - | - | nS | 4 |
| $\overline{\text{PSEN}}$ Low to Data Valid | TPDA | - | - | 2 TCP | nS | 2 |
| Data Hold after $\overline{\text{PSEN}}$ High | TPDH | 0 | - | 1 TCP | nS | 3 |
| Data Float after $\overline{\text{PSEN}}$ High | TPDZ | 0 | - | 1 TCP | nS | |
| ALE Pulse Width | TALW | 2 TCP - Δ | 2 TCP | - | nS | 4 |
| $\overline{\text{PSEN}}$ Pulse Width | TPSW | 3 TCP - Δ | 3 TCP | - | nS | 4 |

Notes:

1. P0.0–P0.7, P2.0–P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 TCP.
3. Data have been latched internally prior to $\overline{\text{PSEN}}$ going high.
4. "Δ" (due to buffer driving delay and wire loading) is 20 nS.



7.3.3 Data Read Cycle

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT | NOTES |
|--------------------------------------|------------------|-------------------------------|--------------------|-------------------------------|------|-------|
| ALE Low to \overline{RD} Low | T _{DAR} | 3 T _C P - Δ | - | 3 T _C P + Δ | nS | 1, 2 |
| \overline{RD} Low to Data Valid | T _{DDA} | - | - | 4 T _C P | nS | 1 |
| Data Hold from \overline{RD} High | T _{DDH} | 0 | - | 2 T _C P | nS | |
| Data Float from \overline{RD} High | T _{DDZ} | 0 | - | 2 T _C P | nS | |
| \overline{RD} Pulse Width | T _{DRD} | 6 T _C P - Δ | 6 T _C P | - | nS | 2 |

Notes:

1. Data memory access time is 8 T_CP.
2. " Δ " (due to buffer driving delay and wire loading) is 20 nS.

7.3.4 Data Write Cycle

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|-------------------------------------|------------------|-------------------------------|--------------------|-------------------------------|------|
| ALE Low to \overline{WR} Low | T _{DAW} | 3 T _C P - Δ | - | 3 T _C P + Δ | nS |
| Data Valid to \overline{WR} Low | T _{DAD} | 1 T _C P - Δ | - | - | nS |
| Data Hold from \overline{WR} High | T _{DWD} | 1 T _C P - Δ | - | - | nS |
| \overline{WR} Pulse Width | T _{DWR} | 6 T _C P - Δ | 6 T _C P | - | nS |

Note: " Δ " (due to buffer driving delay and wire loading) is 20 nS.

7.3.5 Port Access Cycle

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|------------------------------|-------------------|--------------------|------|------|------|
| Port Input Setup to ALE Low | T _{PD} S | 1 T _C P | - | - | nS |
| Port Input Hold from ALE Low | T _{PD} H | 0 | - | - | nS |
| Port Output to ALE | T _{PD} A | 1 T _C P | - | - | nS |

Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

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7.3.6 Program Operation

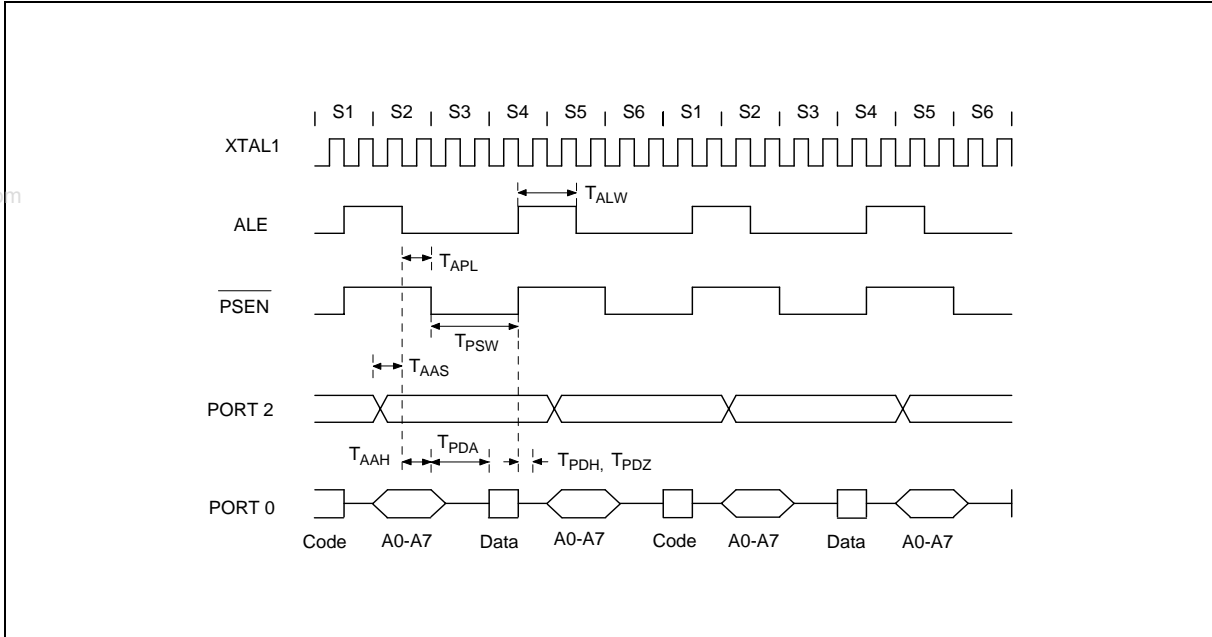
| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|--|--------|------|------|------|---------------|
| VPP Setup Time | TVPS | 2.0 | - | - | μS |
| Data Setup Time | TDS | 2.0 | - | - | μS |
| Data Hold Time | TDH | 2.0 | - | - | μS |
| Address Setup Time | TAS | 2.0 | - | - | μS |
| Address Hold Time | TAH | 0 | - | - | μS |
| $\overline{\text{CE}}$ Program Pulse Width for Program Operation | TPWP | 290 | 300 | 310 | μS |
| OCTRL Setup Time | TOCS | 2.0 | - | - | μS |
| OCTRL Hold Time | TOCH | 2.0 | - | - | μS |
| $\overline{\text{OE}}$ Setup Time | TOES | 2.0 | - | - | μS |
| $\overline{\text{OE}}$ High to Output Float | TDFP | 0 | - | 130 | nS |
| Data Valid from $\overline{\text{OE}}$ | TOEV | - | - | 150 | nS |

Note: Flash data can be accessed only in flash mode. The RST pin must pull in V_{IH} status, the ALE pin must pull in V_{IL} status, and the $\overline{\text{PSEN}}$ pin must pull in V_{IH} status.

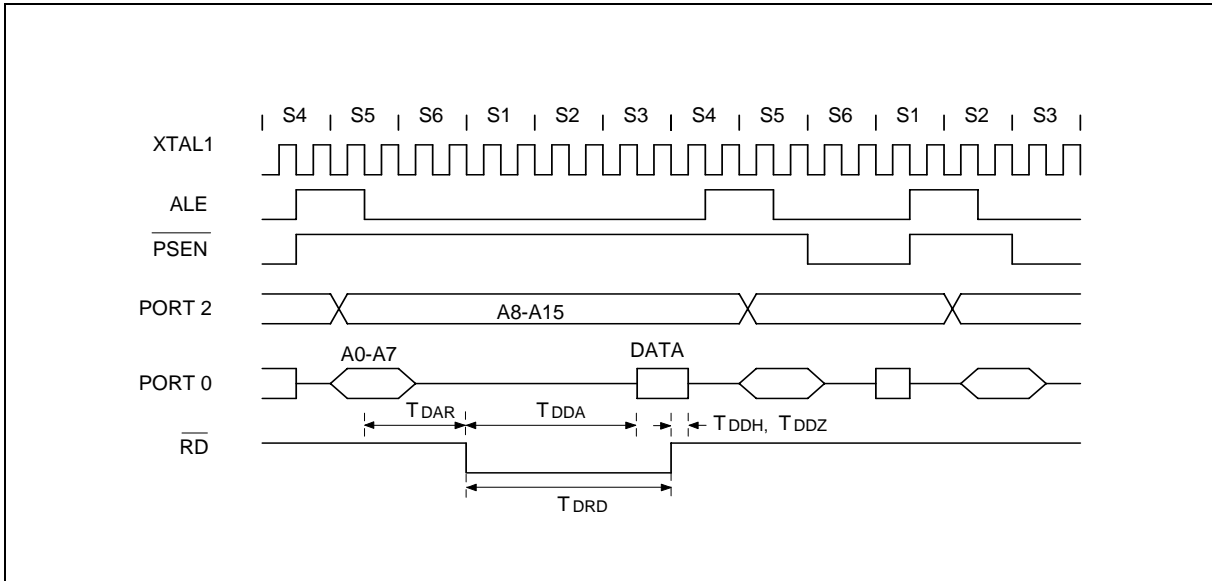


8. TIMING WAVEFORMS

8.1 Program Fetch Cycle



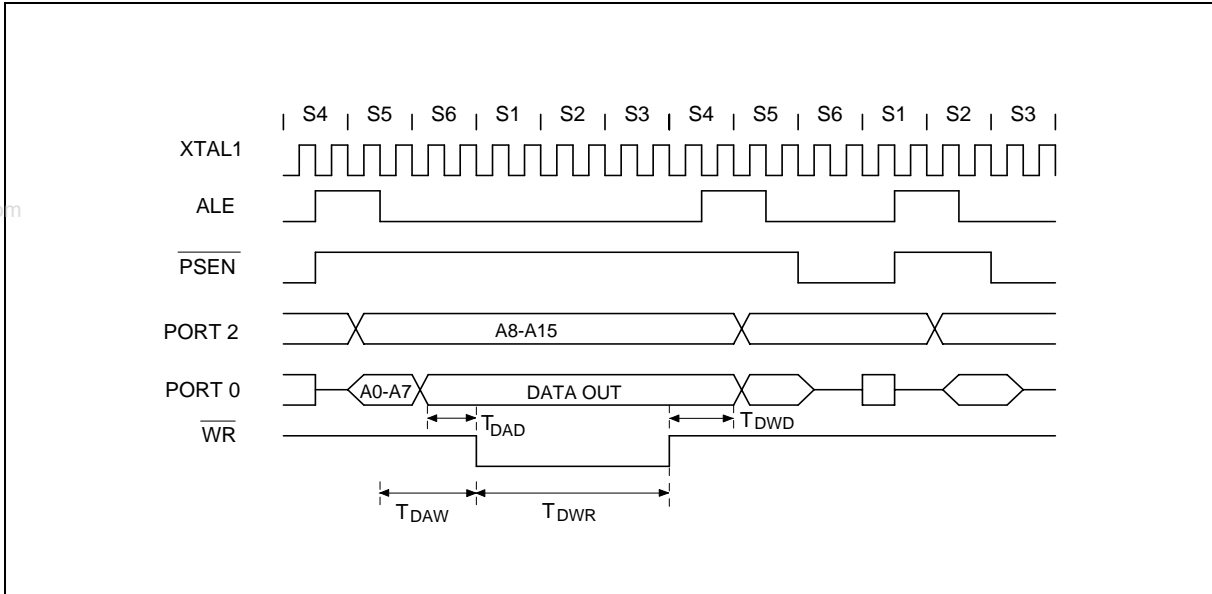
8.2 Data Read Cycle



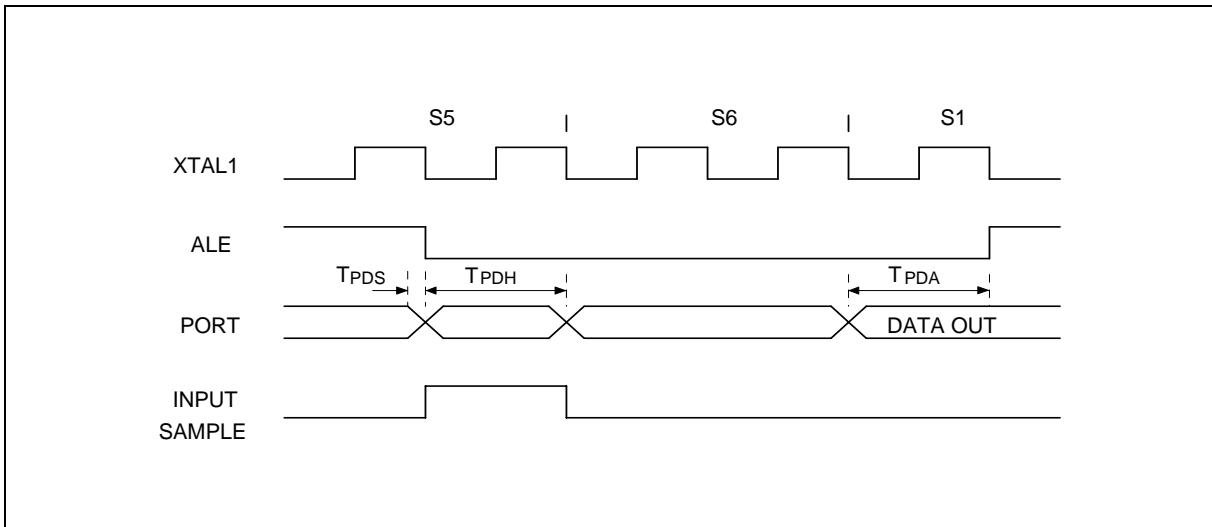


Timing Waveforms, continued

8.3 Data Write Cycle



8.4 Port Access Cycle





9. TYPICAL APPLICATION CIRCUITS

9.1 Expanded External Program Memory and Crystal

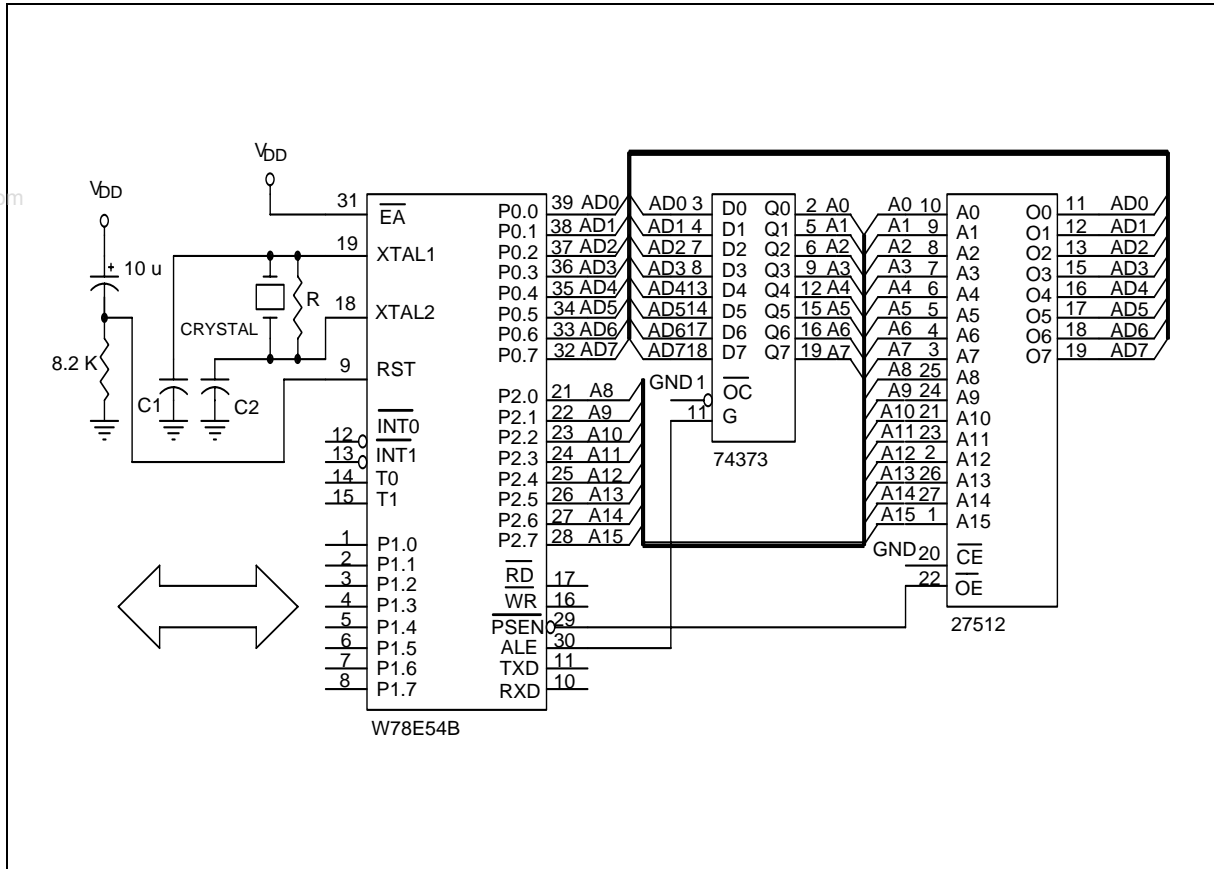


Figure A

| CRYSTAL | C1 | C2 | R |
|---------|-----|-----|------|
| 16 MHz | 30P | 30P | - |
| 24 MHz | 15P | 15P | - |
| 33 MHz | 10P | 10P | 6.8K |
| 40 MHz | 5P | 5P | 4.7K |

Above table shows the reference values for crystal applications (full gain).

Note: C1, C2, R components refer to Figure A.



Typical Application Circuits, continued

9.2 Expanded External Data Memory and Oscillator

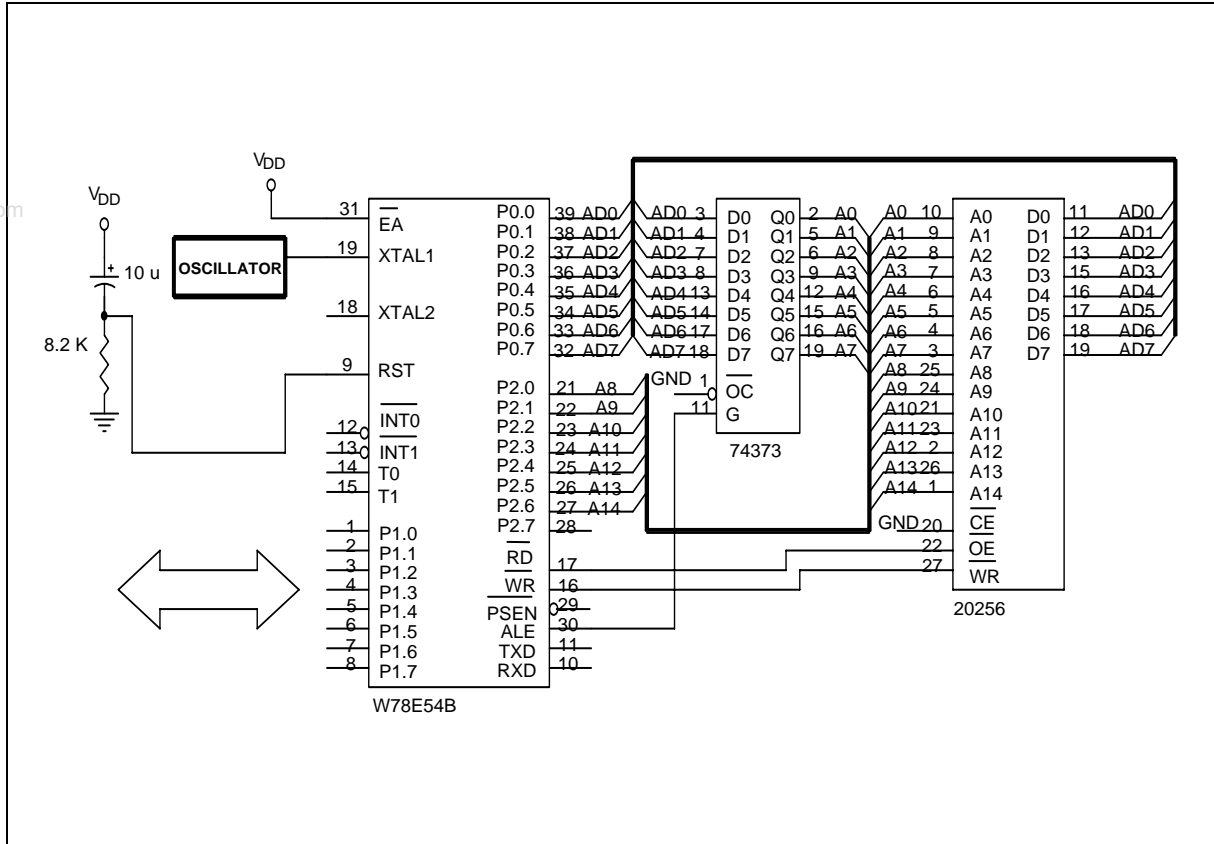


Figure B

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10. PACKAGE DIMENSIONS

10.1 40-pin DIP

| Symbol | Dimension in inch | | | Dimension in mm | | |
|----------------|-------------------|-------|-------|-----------------|-------|--------|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| A | — | — | 0.210 | — | — | 5.334 |
| A ₁ | 0.010 | — | — | 0.254 | — | — |
| A ₂ | 0.150 | 0.155 | 0.160 | 3.81 | 3.937 | 4.064 |
| B | 0.016 | 0.018 | 0.022 | 0.406 | 0.457 | 0.559 |
| B ₁ | 0.048 | 0.050 | 0.054 | 1.219 | 1.27 | 1.372 |
| C | 0.008 | 0.010 | 0.014 | 0.203 | 0.254 | 0.356 |
| D | — | 2.055 | 2.070 | — | 52.20 | 52.58 |
| E | 0.590 | 0.600 | 0.610 | 14.986 | 15.24 | 15.494 |
| E ₁ | 0.540 | 0.545 | 0.550 | 13.72 | 13.84 | 13.97 |
| e ₁ | 0.090 | 0.100 | 0.110 | 2.286 | 2.54 | 2.794 |
| L | 0.120 | 0.130 | 0.140 | 3.048 | 3.302 | 3.556 |
| a | 0 | — | 15 | 0 | — | 15 |
| e _A | 0.630 | 0.650 | 0.670 | 16.00 | 16.51 | 17.01 |
| S | — | — | 0.090 | — | — | 2.286 |

Notes:

- Dimension D Max. & S include mold flash or tie bar burrs.
- Dimension E₁ does not include interlead flash.
- Dimension D & E₁ include mold mismatch and are determined at the mold parting line.
- Dimension B₁ does not include dambar protrusion/intrusion.
- Controlling dimension: inches.
- General appearance spec. should be based on final visual inspection spec.

10.2 44-pin PLCC

| Symbol | Dimension in inch | | | Dimension in mm | | |
|----------------|-------------------|-------|-------|-----------------|-------|-------|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| A | — | — | 0.185 | — | — | 4.699 |
| A ₁ | 0.020 | — | — | 0.508 | — | — |
| A ₂ | 0.145 | 0.150 | 0.155 | 3.683 | 3.81 | 3.937 |
| b ₁ | 0.026 | 0.028 | 0.032 | 0.66 | 0.711 | 0.813 |
| b | 0.016 | 0.018 | 0.022 | 0.406 | 0.457 | 0.559 |
| c | 0.008 | 0.010 | 0.014 | 0.203 | 0.254 | 0.356 |
| D | 0.648 | 0.653 | 0.658 | 16.46 | 16.59 | 16.71 |
| E | 0.648 | 0.653 | 0.658 | 16.46 | 16.59 | 16.71 |
| ⓐ | 0.050 | BSC | — | 1.27 | BSC | — |
| G _D | 0.590 | 0.610 | 0.630 | 14.99 | 15.49 | 16.00 |
| G _E | 0.590 | 0.610 | 0.630 | 14.99 | 15.49 | 16.00 |
| H _D | 0.680 | 0.690 | 0.700 | 17.27 | 17.53 | 17.78 |
| H _E | 0.680 | 0.690 | 0.700 | 17.27 | 17.53 | 17.78 |
| L | 0.090 | 0.100 | 0.110 | 2.296 | 2.54 | 2.794 |
| y | — | — | 0.004 | — | — | 0.10 |

Notes:

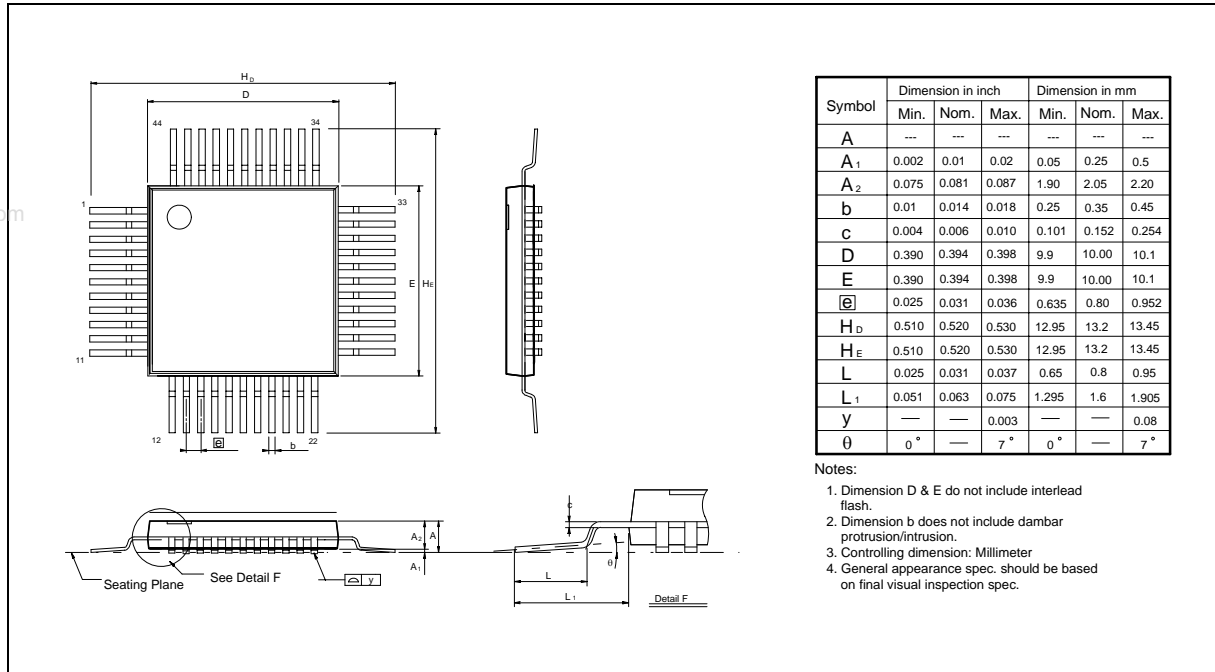
- Dimension D & E do not include interlead flash.
- Dimension b₁ does not include dambar protrusion/intrusion.
- Controlling dimension: inches.
- General appearance spec. should be based on final visual inspection spec.

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Package Dimensions, continued

10.3 44-pin PQFP



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11. REVISION HISTORY

| VERSION | DATE | PAGE | DESCRIPTION |
|---------|-----------------|------|----------------------------|
| A1 | Nov. 26, 2004 | - | Formerly issued |
| A2 | April 20, 2005 | 24 | Add Important Notice |
| A3 | May 17, 2005 | 3 | Add Lead Free (RoHS) parts |
| A4 | October 3, 2006 | | Remove block diagram |
| | | 3 | Remove all Leaded parts |

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