Winbond

W82C476
W82C478
Graphics Color Palette

■ DISTINCTIVE CHARACTERISTICS

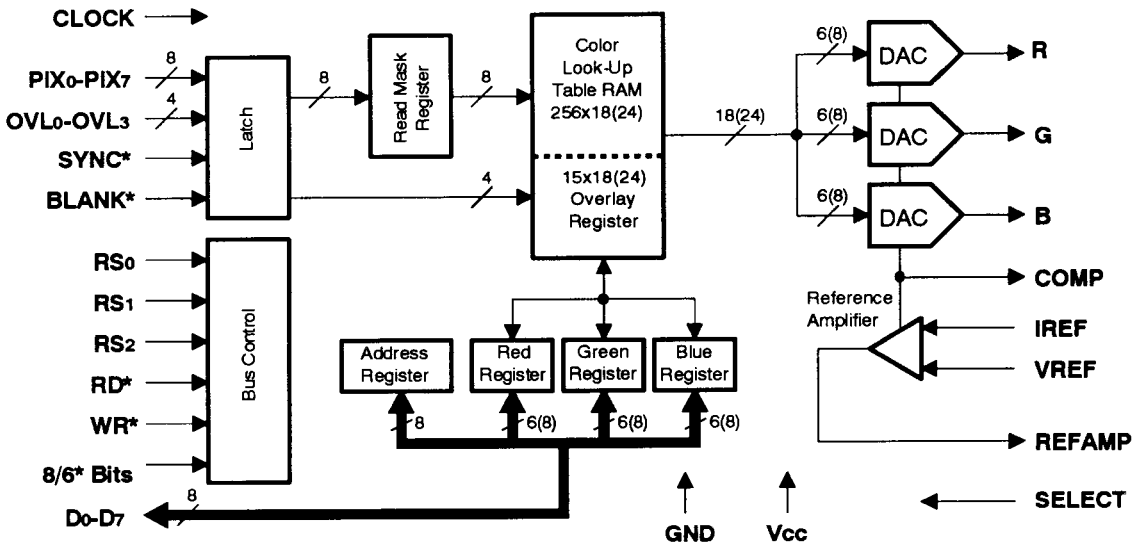
- Functionally compatible with Bt476 and Bt478
- Fast settling time and low glitch outputs for visually clean displays
- Fast 0-wait state microprocessor (MPU) interface
- Glitchless "SNOW FREE" access to palette by MPU
- Triple 6-bit (8-bit) DAC display outputs
- 256x18(24) Palette displays 256 colors of 256K(16M)
- 66 MHz, 80 MHz and 100 MHz versions available

■ TARGET APPLICATIONS

☞ VGA, SuperVGA, PS/2®, 8514/a® and Macintosh® compatible video display adapters with resolutions up to and above 1024x768 pixels non-interlaced.

☞ Low and Medium-end Personal Computers, Graphics Work-stations, and XWindows terminals .

■ BLOCK DIAGRAM



■ GENERAL DESCRIPTION

The W82C476/478 CMOS Color Palettes are generally used in VGA, SuperVGA, and 8514/a-compatible display adapter products. With the high-speed versions available from Winbond, monitor resolutions up to 1024x768 and above may be supported, with interlaced and non-interlaced refresh rates. EGA, CGA and other Personal Computer display modes may also be supported with the W82C476/478 using the palette or overlay features.

The W82C476 has triple 6-bit video DAC outputs, while the W82C478 has selectable 6- or 8-bit DAC outputs for higher color resolving capability. With the 256x18(24) look-up-table RAM on the W82C476(478), Windowing software and display adapters may display 256 simultaneous colors from a selection of 262,143(16.8M) colors. The overlay registers, 15x18(24) may be used for cursor, text overlay, or sprite support, and provide an additional 15 simultaneous colors.

Publication #	Revision	Ammendment
91476	A	/0

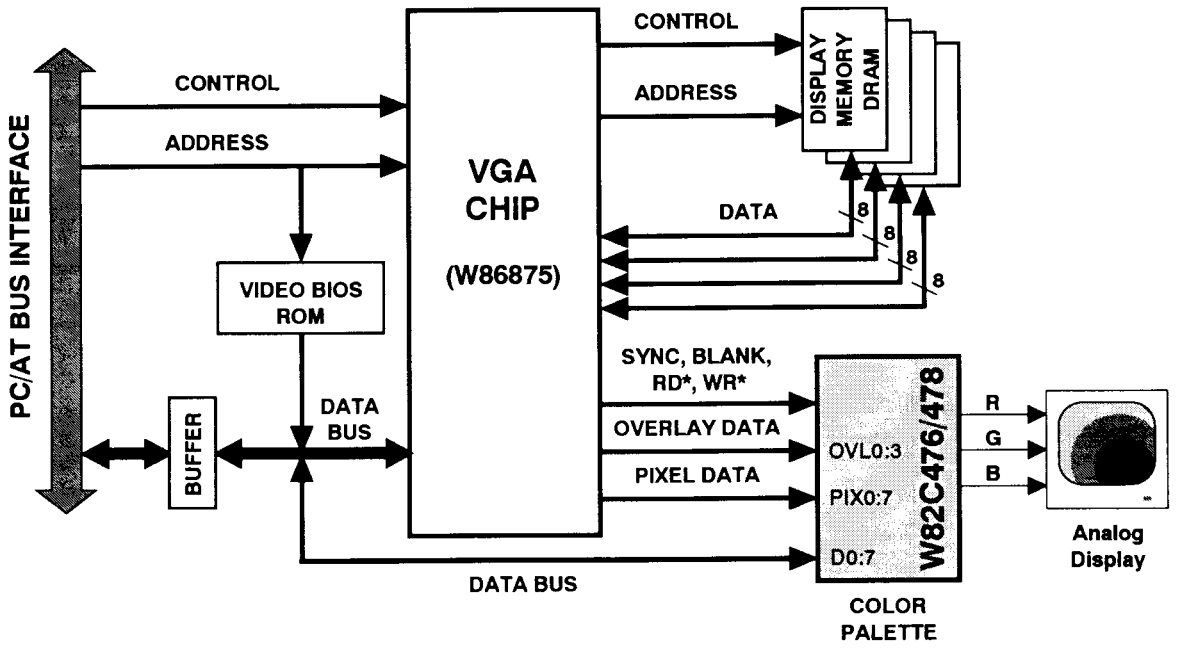
Publication Release Date: August 1991

■ GENERAL DESCRIPTION (CONTINUED)

Available in versions with pixel rates as high as 80 and 100MHz, the W82C476/478 incorporates special proprietary circuitry to minimize output glitch energy, to minimize the DAC output settling time, and to reduce output-to-output skew. The result is a visually "crisper" and "cleaner" display on the monitor, especially at high pixel rates.

A fast microprocessor interface on the W82C476/478 allows for zero-Wait State interfacing to '386 and '486 microprocessors; this minimizes the interface circuitry, and speeds up accessing to the color palettes during palette updates. A unique "**SNOW FREE**" feature minimizes corruption of the DAC outputs during simultaneous access to the palette RAM by the microprocessor and display hardware during screen refresh. Without this feature, a normal color palette would display "snow" or "hash" on the monitor during palette updates.

The W82C476 and W82C478 outputs may drive video monitors **without external buffers**, and the outputs are compatible with RS343A (into a doubly-terminated 75Ω load), and RS170 (into a singly-terminated 75Ω load). The W82C476 and W82C478 have programmable pedestals (0 or 7.5 IRE), and can operate with external current or voltage references.



■ FIGURE 1. EXAMPLE SYSTEM APPLICATION DIAGRAM

■ FUNCTIONAL DESCRIPTION

The W82C476/478 Color Palettes provide for the easy implementation of the color-mapping and analog circuitry required in Personal Computer (PC) and Workstation designs, with screen resolutions as high as 1024x768 pixels or greater. **FIGURE 1** shows an example PC display subsystem using the W82C476/478.

The look-up-table RAM translates the 8-bit pixel data from the video frame buffer into three programmable color values for the Red, Green, and Blue DAC outputs. These RS343A/RS170-compatible outputs are used to drive the RGB signals to the monitor.

The functionality of the W82C476/478 may be divided into three sections: the **MICROPROCESSOR INTERFACE**, **DISPLAY MEMORY INTERFACE**, and the **VIDEO INTERFACE**.

■ MICROPROCESSOR INTERFACE

The W82C476/478 has a general-purpose microprocessor bus interface which can easily connect to 8-, 16-, or 32-bit microprocessors through the 8-bit data bus and control signals. The microprocessor interface is used to read and write to the 256 color **Look-Up-Table (LUT)** RAM locations, the 15 **Overlay Registers (OLR)**, the pixel Mask Register, and the Address Register. With the incorporation of a proprietary fast bus interface and special on-board logic, a microprocessor may access the W82C476/478 in a **single cycle** at up to 20MHz (50ns per read/write cycle). This fast bus operation allows for zero-wait-state interfacing to fast microprocessors, especially when placing the W82C476/478 directly on the CPU motherboard.

Read/Write access to the microprocessor interface of the W82C476/478 may be totally asynchronous to the pixel clock. Read and Write operations to the LUT RAM or overlay registers do not need to be synchronized to the pixel clock, and these operations complete in a cycle. Because of on-board proprietary arbitration logic, the W82C476/478 has "**SNOW FREE**" operation during microprocessor access: since both the microprocessor and normal operation of the display refresh may try to access the LUT RAM at the same time, the W82C476/478 internally arbitrates these accesses, and stabilizes the DAC outputs during microprocessor accesses, resulting in a cleaner, noise-free display during LUT updates. "**SNOW FREE**" Operation is explained in a later section ("**VIDEO INTERFACE**").

The microprocessor interface operation is controlled by the RS_0-RS_2 control inputs, and the RD*, WR* Read/Write control inputs. The RD* signal serves as the control signal for Read operations, and the WR* signal controls Write operations. For either Read or Write cases, the falling edge of RD* or WR* begins the operations. To Read or Write to a register on the W82C476/478, only one RD* or WR* cycle is required, with no wait cycles required between subsequent accesses.

To read or write to the LUT RAM or OLR at a specific location, the Address Register must be loaded (written to) first as an address pointer, and then the data is read from or written to the LUT or OLR location. Operation of the Address Register and its contents is described below, and in **TABLE 3**.

The RS_0-RS_2 inputs are sampled at the beginning of a Read or Write cycle, and these signals determine the destination of the operation to be performed, as shown in **TABLE 1**.

RS_2	RS_1	RS_0	OPERATION
0	0	0	Address Pointer Register, LUT* RAM Write-Mode
0	1	1	Address Pointer Register, LUT RAM Read-Mode
0	0	1	Color Palette RAM LUT
0	1	0	Pixel Read Mask Register
1	0	0	Address Pointer Register, Overlay Write-Mode
1	1	1	Address Pointer Register, Overlay Read-Mode
1	0	1	Overlay Registers
1	1	0	Reserved

Note: LUT: "Look-Up-Table RAM"

■ **TABLE 1. RS_0-RS_2 DECODING**

READING COLOR LUT OR OLR DATA

In order to begin reading from any location of the 256-entry LUT RAM or Overlay Registers, an 8-bit address pointer for the desired location must first be loaded into the Address Register. This is performed by setting the RS_0-RS_2 inputs to the proper value indicated in **TABLE 1** to select the appropriate Address Register mode (Overlay Read-Mode or LUT Address Register Read-Mode). Next, the microprocessor reads three consecutive times (each time selecting the RS_0-RS_2 values to select the Color Palette RAM LUT or Overlay Registers): once each for reading the Red, Green, and Blue values in the LUT or Overlay Register location.

When the third and final Read cycle is completed, the selected Address Register is auto-incremented to point to the next location in the LUT RAM (or Overlay Register). The microprocessor may then read from this **next** location by performing three consecutive reads for Red, Green, and Blue, or may set a new Address location through the proper Address register, repeating the process above. **TABLE 2** shows the detailed operation of the various control signals during Read/Write accesses.

WRITING COLOR LUT OR OLR DATA

Writing to any location of the 256-entry LUT RAM or Overlay Registers begins by first loading an 8-bit address pointer for the desired destination location into the proper Address Register. This is performed by setting the RS_0-RS_2 inputs to the proper value indicated in **TABLE 1** to select the appropriate Address Register mode (Overlay Write-Mode or LUT Address Register Write-Mode). The microprocessor then writes three consecutive times (each time selecting the RS_0-RS_2 values to select the Color Palette RAM LUT or Overlay Registers): once each for writing the Red, Green, and Blue values in the LUT or Overlay Register location.

When the third and final Write cycle is completed, the Red, Green, and Blue values are internally concatenated into an 18-bit word (24-bit on the W82C478), and stored into the appropriate LUT or Overlay Register location. The selected Address Register is then auto-incremented to point to the next location in the LUT RAM (or Overlay Register). The microprocessor may then write to this **next** location by again performing three consecutive writes for Red, Green and Blue, or may set a new Address location through the proper Address register, repeating the process above. **TABLE 2** shows the operation of the various control signals during Read/Write accesses.

RD*	WR*	RS_2	RS_1	RS_0	$AR_{A,B}$	FUNCTION	OPERATION
						LOOK-UP-TABLE WRITE SEQUENCE:	
1	↓	0	0	0	XX	❶ Write Address Register	D(7:0) → AR(7:0); 0 → ARa,b
1	↓	0	0	1	00	❷ Write Red value	D(7:0) → Red_reg(7:0); INC(ARa,b)
1	↓	0	0	1	01	❸ Write Green value	D(7:0) → Green_reg(7:0); INC(ARa,b)
1	↓	0	0	1	10	❹ Write Blue value Write Color LUT * (internal operation)	D(7:0) → Blue_reg(7:0); 0 → ARa,b Red_reg(7:0) → R(7:0); Green_reg(7:0) → G(7:0); Blue-reg(7:0) → B(7:0); INC(AR(7:0))
						OVERLAY REGISTER WRITE SEQUENCE:	
1	↓	1	0	0	XX	❶ Write Address Register	D(7:0) → AR(7:0); 0 → ARa,b
1	↓	1	0	1	00	❷ Write Red value	D(7:0) → Red_reg(7:0); INC(ARa,b)
1	↓	1	0	1	01	❸ Write Green value	D(7:0) → Green_reg(7:0); INC(ARa, b)
1	↓	1	0	1	10	❹ Write Blue value Write Overlay * (internal operation)	D(7:0) → Blue_reg(7:0); 0 → ARa, b Red_reg(7:0) → R(7:0); Green_reg(7:0) → G(7:0); Blue-reg(7:0) → B(7:0); INC(AR(7:0))
						LOOK-UP-TABLE READ SEQUENCE:	
1	↓	0	1	1	XX	❶ Read Address Register	D(7:0) → AR(7:0); 0 → ARa,b
↓	1	0	0	1	00	❷ Read Red value	Red_reg(7:0) → D(7:0); INC(ARa,b)
↓	1	0	0	1	01	❸ Read Green value	Green_reg(7:0) → D(7:0); INC(ARa, b)
↓	1	0	0	1	10	❹ Read Blue value	Blue_reg(7:0) → D(7:0); 0 → ARa, b; INC(AR(7:0))
						OVERLAY REGISTER READ SEQUENCE:	
1	↓	1	1	1	XX	❶ Read Address Register	D(7:0) → AR(7:0); 0 → ARa,b
↓	1	1	0	1	00	❷ Read Red value	Red_reg(7:0) → D(7:0); INC(ARa, b)
↓	1	1	0	1	01	❸ Read Green value	Green_reg(7:0) → D(7:0); INC(ARa, b)
↓	1	1	0	1	10	❹ Read Blue value	Blue_reg(7:0) → D(7:0); 0 → ARa, b; INC(AR(7:0))

Note: ARa,b refers to internal register pointers to the Red, Green, and Blue color values at a LUT or OLR location. Please refer to timing diagrams for edge and timing information on RD and WR*. The internal concatenation of the three 6(8)-bit values, R(7:0), G(7:0), B(7:0) refers to the 18(24-bit) word pointed to by the address register (AR).*

■ **TABLE 2. W82C476/478 READ/WRITE ACCESS**

ADDITIONAL MICROPROCESSOR INTERFACE INFORMATION

For read/write operations to the W82C476 RAM LUT and Overlay Registers, and Mask Registers, the 6-bit color data from the microprocessor is contained in the six LSB's (D_5-D_0) of the data bus. On the W82C478, when the 8/6* pin is set LOW (for 6-bit operation), the data also occupies the 6 LSB positions of the data bus. Bits D_6 and D_7 are ignored during write cycles in these two 6-bit cases, and are set to 0 during a read cycle.

As discussed above, the W82C476/478 uses an Address Register to address the LUT and Overlay Register locations. **Table 3** shows detailed operation of the Address Register bits; during access to the Overlay Registers, only the lower four bits of the Address Register are used. In order to track the three consecutive Red, Green, and Blue Read/Write cycles required for a LUT or Overlay Register Read/Write operation, an internal modulo-3 address counter (ARa,b) auto-increments after each read/write access to the LUT or Overlay Register. This internal counter is internally

decoded to point to the proper Red, Green, or Blue value when reading and writing, and is reset to zero (pointing to the Red value) after a write to the Address Register.

Following a full read/write sequence to LUT location $FF (after the Blue value read/write), the Address Register is auto-incremented and set to $00. When accessing the Overlay Register (OLR) location $F, the Address Register is auto-incremented, logically wrapping around to $0.

AR(7:0) CONTENTS	RS_2	RS_1	RS_0	FUNCTION
$00..$FF	0	0	1	Color LUT locations $00..$FF ARa,b = 00 → Red value ARa,b = 01 → Green value ARa,b = 10 → Blue value
XXXX0000b	1	0	1	Reserved
XXXX0001b	1	0	1	Overlay Register 1
XXXX0010b	1	0	1	Overlay Register 2
XXXX0011b	1	0	1	Overlay Register 3
•	•	•	•	•
•	•	•	•	•
XXXX1111b	1	0	1	Overlay Register 15

■ **TABLE 3. ADDRESS REGISTER VALUES**

■ DISPLAY MEMORY INTERFACE

In a typical system configuration (see **FIGURE 1**), the color palette is located in the path from the pixel display memory to the display monitor. On the W82C476/478, the pixel color inputs from the video display memory, PIX_0-PIX_7, and OVL_0-OVL_3, are used as addresses to the 256 locations of the Look-Up-Table RAM and the 15 Overlay Registers, respectively. These inputs are sampled on the rising edge of the pixel CLK input and are used by the color palette look-up tables to select a pixel color.

With the W82C476/478, the microprocessor has a method to rapidly alter the appearance of one or more colors on the display by using the pixel masking scheme. With a single write access to load the 8-bit Pixel Read Mask Register, the microprocessor can store a color masking value. With this value, the address to the LUT RAM is modified for each pixel: the PIX_0-PIX_7 inputs are logically ANDed with the contents of this register, and the resulting modified address is used to address the LUT RAM.

When the OVL_0-OVL_3 inputs are set to 0000b, the PIX_0-PIX_7 inputs (after any modification by the Pixel Read Mask Register) are used to address the LUT RAM, whose contents drive the video DACs. If a non-zero value is given for the OVL_0-OVL_3 inputs, the DACs are driven by the contents of the addressed Overlay Registers. **TABLE 4** illustrates this operation. In this manner, using the OVL_0-OVL_3 inputs, a display system can easily implement cursors, overlay text, grids, and other overlays.

OVL_0-OVL_3	PIX_0-PIX_7	COLOR SOURCE LOCATION SELECTED FOR OUTPUT TO DACS
$0	$00	Color LUT RAM Location $00
$0	$01	Color LUT RAM Location $01
•	•	•
•	•	•
$0	$FF	Color LUT RAM Location $FF
$1	$XX	Overlay Register Location 1
•	•	•
•	•	•
$F	$XX	Overlay Register Location 15

■ TABLE 4. PIXEL AND OVERLAY INPUT FUNCTIONS

The total pipeline delay times from the digital Display inputs (PIX_0-PIX_7, OVL_0-OVL_3, SYNC*, and BLANK*) to the analog video outputs (R, G, B) is four pixel CLK clock cycles.

■ VIDEO INTERFACE

For each cycle of the pixel clock (CLK), using the modified address formed from the PIX_0-PIX_7 and OVL_0-OVL_3 pixel inputs, a 24-bit word is read from either the LUT RAM or the Overlay Registers (an 18-bit word is read for the W82C476, or the W82C478 when the 8/6* input is LOW). This word value is split into three 8-bit (or 6-bit) values and converted by the three DACs into RS343A analog format.

Note that on the W82C478, when operating in 6-bit mode (8/6* set to LOW), the full-scale output current will be about 1.5% lower than when in 8-bit mode with the same R_{set} value. This is due to the loss of 2 LSB's, which are set to 0 in the 8-bit DAC outputs in 6-bit mode. One way to compensate for this is to alter the R_{set} value, or adjust the voltage reference value to adjust the full-scale output.

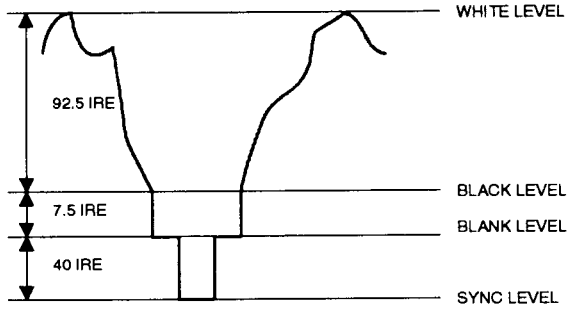
The SYNC* and BLANK* inputs are sampled on the rising edge of CLK, and condition the RGB analog output as shown in **TABLE 5** by adding weighted currents to the outputs as shown in **FIGURE 2** and **FIGURE 3**. The SYNC* and BLANK* signals are internally delayed by four pixel CLK periods, to compensate for the pipeline delay of the video stream, before conditioning the DAC outputs.

The SELECT input specifies the blanking pedestal to be used by the RGB outputs. For SELECT = logical ZERO, the blanking pedestal is 0.0 IRE; for SELECT = logical ONE, the blanking pedestal is 7.5 IRE. The W82C476/478 outputs are designed to individually drive doubly-terminated 75Ω coaxial cables to the video display monitor, with AC coupling.

SNOW FREE FEATURE OPERATION

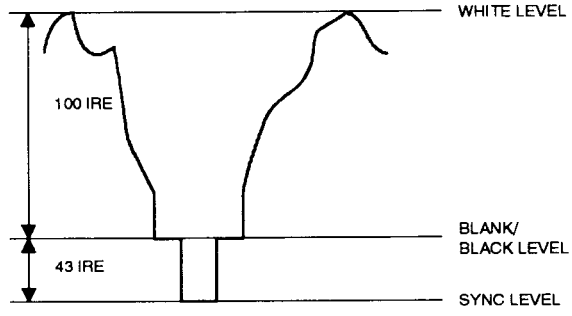
When the microprocessor reads or writes to the color Look-Up-Tables or Overlay Registers during non-blanking periods, there may be a conflict with the simultaneous access of the LUT/OLR contents through the normal operation of the PIX_0-PIX_7/OVL_0-OVL_3 inputs. In other RAMDAC™ devices, this conflict can cause "hash" or "noise" to display on the screen. On the W82C476/478, a "**SNOW FREE**" feature stabilizes the DAC outputs during the microprocessor access to eliminate this visual noise. Specifically, the output of the DAC remains the same value as the last pixel value before the read/write operation began. This value remains on the output until the next pixel CLK after the Read/Write operation is completed.

W82C478 WITHOUT SYNC		W82C478 WITH SYNC	
mA	V	mA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.000	0.000	7.62	0.286
		0.000	0.000



■ **FIGURE 2. COMPOSITE VIDEO OUTPUT SIGNALS (SELECT = V_{CC})**

W82C476 OR 'C478 WITHOUT SYNC		W82C478 WITH SYNC	
mA	V	mA	V
17.62	0.660	25.24	0.950
0.000	0.000	7.62	0.286
0.000	0.000	0.000	0.000



■ **FIGURE 3. COMPOSITE VIDEO OUTPUT SIGNALS (SELECT = GND)**

				SELECT = V_{CC}	SELECT = GND	
DESCRIPTION	SYNC*	BLANK*	DAC INPUT	I_{OUT} (mA)	I_{OUT} (mA) W82C476	I_{OUT} (mA) W82C478
WHITE	1	1	$FF	26.67	17.62	25.24
DATA	1	1	$FE..$01	data + 9.05	data	data + 7.62
DATA-SYNC	0	1	$FE..$01	data + 1.44	data	data
BLACK	1	1	$00	9.05	0	7.62
BLANK	1	0	$XX	7.62	0	7.62
BLACK-SYNC	0	1	$00	1.44	0	0
SYNC	0	0	$XX	0	0	0

Note: Typical full scale Green output (G) = 26.67mA. External voltage or current reference and R_{set} adjusted for 26.7mA full scale output. Typical V_{REF} = 1.235V, R_{SET} = 147Ω. 75Ω doubly-terminated load. Note that full-scale output may vary up to 1.5% lower on the W82C476 and W82C478 in 6-bit mode, due to not implementing 2LSB's (see ***VIDEO INTERFACE*** *for details).*

■ **TABLE 5. COMPOSITE VIDEO OUTPUT TRUTH TABLE**

■ PIN DESCRIPTION (SORTED BY FUNCTION)

■ MICROPROCESSOR INTERFACE SECTION

D_0-D_7 **Data and address bus (TTL Compatible Bi-directional)**
The 8-bit data bus used to read and load the internal control registers, Color Look-up Table, and Overlay Registers. Bit D_0 is the LSB.

RD* **Read Control Input (TTL Compatible Input)**
An active low on the RD* input initiates a read of the data from the color LUT or registers. RS_0-RS_2 are sampled and latched on the falling edge of RD*.

WR* **Write Control Input (TTL Compatible Input)**
An active low on the WR* input initiates a write of the data from the data bus to the color LUT or registers. RS_0-RS_2 are sampled and latched on the falling edge of WR*, and D_0-D_7 are sampled on the rising edge of WR*.

RS_0-RS_2 **Register Select Inputs (TTL Compatible Inputs)**
RS_0-RS_2 select the destination (Color LUT or any internal register) during a read or write cycle by the microprocessor. The value of RS_0-RS_2 determines the action performed by the read or write, as indicated in Tables 1, and 3.

8/6* **8-bit/6-bit Select Input (TTL Compatible Input, Internal Pull-up Resistor)**
For the W82C478, the 8/6* pin controls whether 8-bits (logical ONE) or 6-bits (logical ZERO) from the data bus are used during microprocessor read and write cycles to the color LUT or Overlay Registers. In 8-bit operation, D_7 is the MSB, while in 6-bit operation, D_5 is the MSB. D_6 and D_7 are set to 00b in a 6-bit read cycle, and are ignored during a 6-bit write cycle. This pin should be connected to GND on the W82C476.

■ TIMING SECTION

CLK **Pixel Clock (TTL Compatible Input)**
The pixel clock of the system. The rising edge of CLK latches the SYNC*, BLANK*, PIX_0-PIX_7, and OVL_0-OVL_3 inputs. The CLK input should be driven by a dedicated TTL buffer for maximum noise immunity and stability.

BLANK* **Video Composite Blank (TTL Compatible Input)**
When active, the BLANK* input forces the R, G, B video outputs to the appropriate blanking levels, overriding the pixel (PIX_0-PIX_7) and Overlay (OVL_0-OVL_3) inputs, per **TABLE 5**. Video monitors require blanking during horizontal and vertical retrace. Blank* is sampled and latched on the rising edge of CLK.

SYNC* **Video Sync (TTL Compatible Input)**
When active, the SYNC* input forces the R, G, and B video output current sources off, to provide SYNC pulses to the video monitor, per **TABLE 5**. SYNC* should only be asserted during the blanking interval, since SYNC* does not override any other input or control pin. This pin should be tied to an inactive level (logical ONE) if generation of SYNC information is not needed on the analog outputs.

■ DISPLAY MEMORY INTERFACE SECTION

PIX_0-PIX_7 **Pixel Color Data (TTL Compatible Input)**
The 8 PIX_0-PIX_7 inputs are used as addresses to select the pixel color information from one of 256 locations in the Color Palette look-up-table (LUT) RAM. The PIX_0-PIX_7 values are latched on each rising edge of the pixel CLK. PIX_0 is the LSB. All unused PIX_0-PIX_7 inputs should be grounded.

OVL_0-OVL_3 **Overlay Data (TTL Compatible Input)**
The four OVL_0-OVL_3 inputs are used to determine the overlay function, and to select which Overlay Register is used in providing the color output information, as indicated in **TABLE 4**. When the overlay palette is used (by activating the OVL_0-OVL_3 inputs), the pixel inputs, PIX0-PIX7 are ignored, and the Overlay Registers are used to drive the DACs through the OLR values. The LSB is OVL_0. The OVL_0-OVL_3 inputs are latched on the rising edge of each pixel CLK cycle. Any unused OVL_0-OVL_3 inputs should be grounded.

■ VIDEO OUTPUT SECTION

R, G, B *(Three Signals)* **Red, Green, Blue individual video outputs (Analog outputs)**
The three pins, R, G, B are for the three analog outputs of the three video DACs, each capable of driving a doubly-terminated 75Ω RS343A cable, or a singly-terminated 75Ω RS170 cable. All outputs have video synch outputs, and are stabilized for glitchless operation during microprocessor access to the internal registers and color palette RAM.

I_{REF} **Current Reference, Full Scale Adjust Control (Analog Input)**
The W82C476/478 references for the DACs may be implemented in one of two ways, depending on the connections to this pin: **VOLTAGE REFERENCE** mode, or **CURRENT REFERENCE** mode.

■ EXTERNAL VOLTAGE REFERENCE MODE:

A resistor, R_{set} should be connected from this pin to GND when an external voltage reference is used. The R_{set} resistor controls the magnitude of the full scale video signal according to the following formula:

$$R_{set(\Omega)} = K * 1{,}000 * V_{REF(Volts)} / I_{OUT(mA)}$$

The table below defines the K and recommended R_{set} values for doubly-terminated 75Ω loads:

	MODE	PEDESTAL	K
W82C478	6-bit	7.5 IRE	3.170
	8-bit	7.5 IRE	3.195
	6-bit	0 IRE	3.000
	8-bit	0 IRE	3.025
W82C476	(6-bit)	0 IRE	2.100

■ EXTERNAL CURRENT REFERENCE MODE:

If an external current reference is used, the output current (I_{OUT}) on each R, G, B video output is determined by the relationship:

$$I_{REF(mA)} = I_{OUT(mA)}/K$$

V_{REF} **Voltage Reference (Analog Input)**
When using the W82C476/478 with an external voltage reference, a stable 1.235V (typical) reference voltage should be supplied on this pin as a reference for the video DACs. A 0.1μF decoupling capacitor should always be connected between the V_{REF} pin and V_{CC}, with short leads and in close proximity to the device pins. If the W82C476/478 is used with an external current reference, this pin should be left floating, except for the bypass capacitor.

REFAMP **Reference Amplifier Output (Analog Output)**
When using an **external voltage reference**, this pin should be connected to the COMP pin. The REFAMP pin should be left floating if an **external current reference** is used.

COMP **Compensation capacitor pin (Analog Input)**
A 0.1μF ceramic capacitor should be connected between this pin and V_{CC}. When an external **voltage reference** is used, this pin should be connected to the REFAMP pin. When using an external **current reference**, this pin should be connected to I_{REF}.

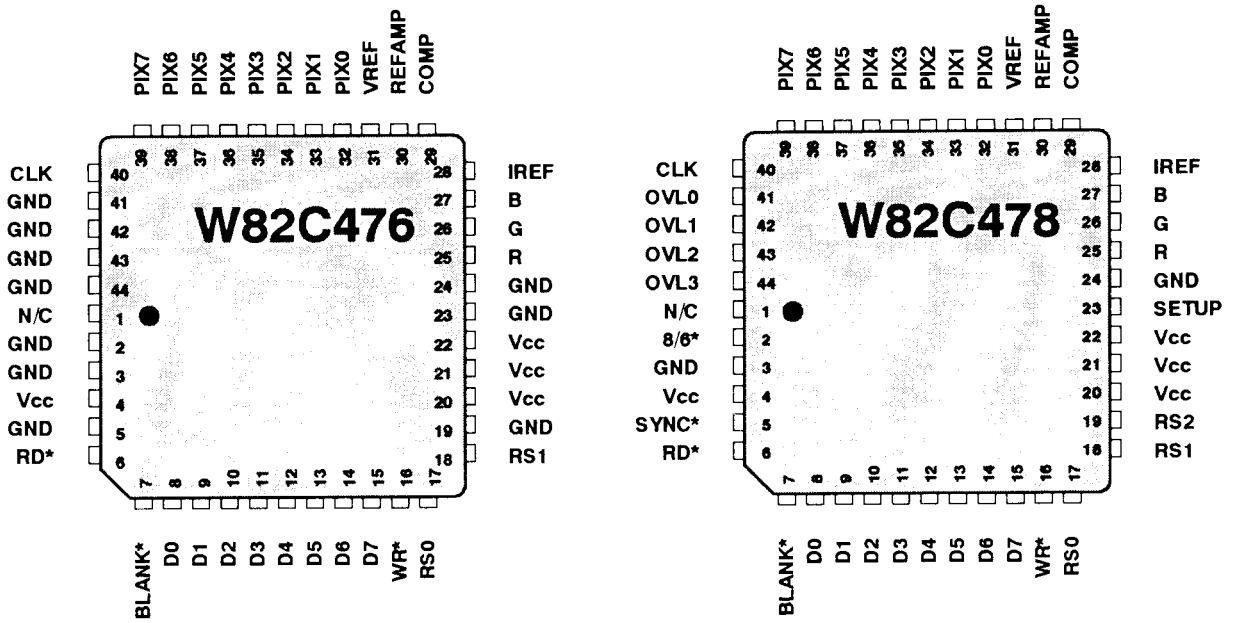
SELECT **Select control pin (TTL compatible input)**
The SELECT pin selects a blanking pedestal of either 0 IRE (SELECT = GND), or 7.5 IRE (SELECT = V_{CC}).

■ POWER SUPPLY SECTION

V_{CC} **Analog +5 Volt power supply**
All Vcc pins should be connected to +5V.

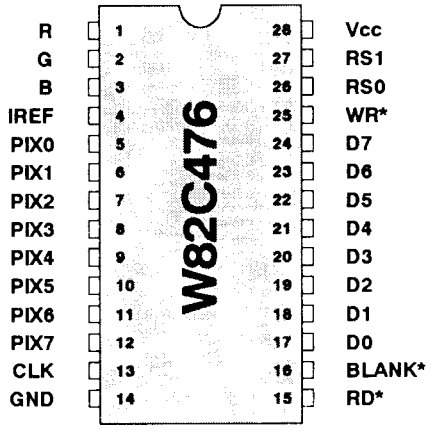
GND **Analog Ground voltage supply**
All GND pins should be connected to Ground.

■ PACKAGE DIAGRAMS



NOTE: Pin 1 is marked for orientation.
N/C pins may be left unconnected without affecting operation of the W82C476/478.

■ 44-PIN J-LEAD PLASTIC (PLCC)
TOP VIEW



■ 28-PIN DIP (PDIP)

■ ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... -65 to +150°C
Ambient Operating Temperature ..... -55 to +125°C
Junction Temperature ..... +150°C
Supply Voltage Measured to Ground ..... -0.5 to +7.0V
Voltage on any I/O pin ..... GND-0.5V to V_{CC}+0.5V
Analog Output Short Circuit to V_{CC} or GND Duration ..... Indefinite
Soldering Temperature (5 sec, 1/4" from pin) ..... 260°C
Vapor Phase Soldering (1 minute) ..... 220°C

*Stresses above those listed in **ABSOLUTE MAXIMUM RATINGS** may cause permanent device damage. Functionality at or above these specification limits is not implied. Exposure to absolute maximum ratings for prolonged periods may affect device reliability.*

■ RECOMMENDED OPERATING RANGE

Ambient Operating Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC})
For 66, 80, 100MHz devices ..... +4.75 to +5.25V
For 35, 50MHz devices ..... +4.5 to +5.5V
Reference Voltage (V_{REF})
(Voltage Reference Configuration) ..... +1.14 to 1.26V
Current Reference (I_{REF})
(Current Reference Configuration) ..... -3 to -10mA
Standard RS343A **typical** -8.39mA
PS/2 Compatible **typical** -8.88mA
Output Load 37.5Ω

Recommended Operating Ranges defines the limits between which the functionality of the device is guaranteed

■ DC CHARACTERISTICS OVER OPERATING RANGE

PARAMETER SYMBOL	PARAMETER DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS						
V_{IH}	Input High Voltage		2.0		Vcc+0.5	V
V_{IL}	Input Low Voltage		GND-0.5		0.8	V
I_{IH}	Input High Current	V_{in} = 2.4V			1	µA
I_{IL}	Input Low Current	V_{in} = 0.4V			-1	µA
C_{IN}	Input Capacitance	f=1MHz; V_{in} = 2.4V			7	pF
DIGITAL OUTPUTS						
V_{OH}	Output High Voltage	I_{OH} = - 400µA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 3.2mA			0.4	V
I_{OZ}	3-State Output				50	µA
C_{OUT}	Output Capacitance				7	pF

■ DC CHARACTERISTICS OVER OPERATING RANGE (CONTINUED)

PARAMETER SYMBOL	PARAMETER DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG OUTPUTS						
Resolution:	Each DAC, W82C476(478)		6(8)	6(8)	6(8)	Bits
Accuracy, each DAC:						
LIN_i	Integral Linearity Error, W82C476(478)				±1/2 (1)	LSB
LIN_d	Differential Linearity Error				±1/2 (1)	LSB
	Gray Scale Error				±5	% Gray
	Monotonicity: ***Guaranteed***					
	Coding					Binary
	LSB Size					
	W82C476			279.68		µA
	W82C478	*8/6* = ONE*		69.1		µA
	DAC-to-DAC Matching			2	5	%
V_{OC}	Output Compliance		-1.0		+1.5	V
I_{VREF}	Voltage Reference Input Current			10		µA
R_{out}	Output Impedance			10		KΩ
C_{out}	Output Capacitance	*f=1MHz;* *I_{OUT} = 0mA*			30	pF
PSSR	Power Supply Rejection	*f=1KHz;* *COMP = 0.1µF*			0.5	%/%ΔV_{CC}
VIDEO OUTPUT LEVELS - RS343A COMPATIBILITY						
	Output Current					
	White Level Relative to BLANK		17.69	19.05	20.40*	mA
	White Level Relative to BLACK		16.74	17.62	18.50*	mA
	Black Level Relative to BLANK:					
	- W82C478	*SELECT = 1*	0.95	1.44	1.90	mA
		SELECT = 0	0	5	50	µA
	- W82C476		0	0	0	µA
	Blank Level:					
	- W82C478		6.29	7.62	8.96	mA
	- W82C476		0	5	50	µA
	Sync Level (W82C478 only)		0	5	50	µA

NOTE:* ***Test Conditions* *to generate RS343A standard video signals (unless other wise specified):* RECOMMENDED OPERATING CONDITIONS *using external voltage reference with R_{set} = 147Ω , V_{REF} = 1.235V, SETUP = V_{CC}, 8/6* = ONE. For 28-pin DIP version of W82C476, I_{REF} = -8.39mA. Since the above parameters are guaranteed over the full range, temperature coefficients are not specified or required.*

Full-scale output levels in 6-bit DAC mode are approximately 1.5% lower than 8-bit full scale output level, due to 2 fewer LSB's (See ***VIDEO INTERFACE*** *section).*

■ AC SWITCHING CHARACTERISTICS

PARAM. #	SYMBOL NAME	PARAMETER DESCRIPTION	100 MHZ MIN	100 MHZ TYP	100 MHZ MAX	80 MHZ MIN	80 MHZ TYP	80 MHZ MAX	UNITS
	F_{max}	**Clock Rate**			**100**			**80**	MHz
1	t_S	RS_0-RS_2 Setup Time	10			10			ns
2	t_H	RS_0-RS_2 Hold Time	10			10			ns
3	t_P	RD* Asserted to Data Bus Driven	5			5			ns
4	t_P	RD* Asserted to Data Valid			40			40	ns
5	t_P	RD* Negated to Data Bus Tri-Stated			20			20	ns
(5)		Read Data Hold Time	5			5			ns
6	t_S	Write Data Setup Time	10			10			ns
7	t_H	Write Data Hold Time	10			10			ns
8	t_W	RD*, WR* Pulse Width Low	50			50			ns
9	t_W	RD*, WR* Pulse Width High	50			50			ns
10	t_S	Pixel and Overlay Setup Time	3			3			ns
11	t_H	Pixel and Overlay Hold Time	3			3			ns
12	t_{CYC}	Clock Cycle Time	10			12.5			ns
13	t_W	Clock Pulse Width High	3			4			ns
14	t_W	Clock Pulse Width Low	3			4			ns
15	t_P	Analog Output Delay			30			30	ns
16	t_R, t_F	Analog Output Rise/Fall Time (Note1)		3			3		ns
17	t_S	Analog Output Settling Time (Note1)		10			13		ns
		Clock and Data Feedthrough		-30			-30		dB
		Glitch Impulse (Note1)		75			75		pV-sec
		DAC to DAC Crosstalk		-23			-23		dB
		Analog Output Skew			2			2	ns
		Pipeline Delay	4	4	4	4	4	4	Clocks
	I_{CC}	V_{CC} Supply Current (Note3)		180	220		180	220	mA

Test Conditions: *See next Page.*

Notes: *See Next Page*

■ AC SWITCHING CHARACTERISTICS (CONTINUED)

PARAM. #	SYMBOL NAME	PARAMETER DESCRIPTION	66 MHZ MIN	TYP	MAX	UNITS
	F_{max}	**Clock Rate**			66	MHz
1	t_S	RS_0-RS_2 Setup Time	10			ns
2	t_H	RS_0-RS_2 Hold Time	10			ns
3	t_P	RD* Asserted to Data Bus Driven	5			ns
4	t_P	RD* Asserted to Data Valid			40	ns
5	t_P	RD* Negated to Data Bus Tri-Stated			20	ns
(5)		Read Data Hold Time	5			ns
6	t_S	Write Data Setup Time	10			ns
7	t_H	Write Data Hold Time	10			ns
8	t_W	RD*, WR* Pulse Width Low	50			ns
9	t_W	RD*, WR* Pulse Width High	50			ns
10	t_S	Pixel and Overlay Setup Time	3			ns
11	t_H	Pixel and Overlay Hold Time	3			ns
12	t_{CYC}	Clock Cycle Time	15.15			ns
13	t_W	Clock Pulse Width High	5			ns
14	t_W	Clock Pulse Width Low	5			ns
15	t_P	Analog Output Delay			30	ns
16	t_R, t_F	Analog Output Rise/Fall Time (Note1)		3		ns
17	t_S	Analog Output Settling Time (Note1)		10		ns
		Clock and Data Feedthrough		-30		dB
		Glitch Impulse (Note1)		75		pV-sec
		DAC to DAC Crosstalk		-23		dB
		Analog Output Skew			2	ns
		Pipeline Delay	4	4	4	Clocks
	I_{CC}	V_{CC} Supply Current (Note3)		180	220	mA

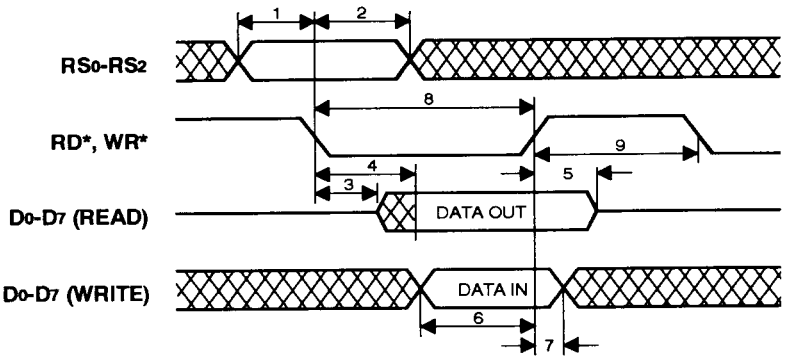
Test Conditions:

RECOMMENDED OPERATING CONDITIONS *unless otherwise specified.*
External voltage reference.
R_{set} = 147Ω, V_{REF} = 1.235V, SELECT = V_{CC}, 8/6 = ONE.*
(28PDIP W82C476: I_{REF} = -8.39mA)
TTL Input Level: 0 to 3V with t_R, t_F (10-90%) <= 3ns.
Analog Output Load <= 10pF, D_0-D_7 Output Load <= 50pF.

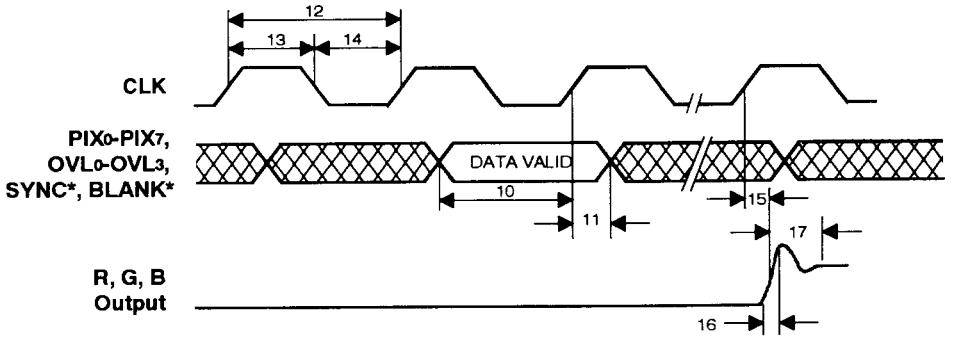
Notes:

1. *Clock and Data Feedthrough are not included.*
2. *Included Clock and data Feedthrough, -3dB bandwidth = 2x Clock Frequency.*
3. *Measured at maximum f_{clk};*
   I_{CC}(max): V_{CC} = 5.25V, T_A = 0^0C.
   I_{CC}(typ): V_{CC} = 5.00V, T_A = $+25^0$C.

■ AC WAVEFORMS

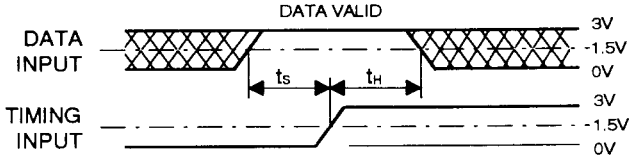


■ FIGURE 4. MPU READ/WRITE TIMING



Notes: *Output delay is measured from the 50% point of the rising edge of CLK, to the 50% point of the measured signals' full scale transition. Settling time is measured from the 50% point of the output full-scale transition, to the point where output remains within ±1 LSB(W82C478) or ±1/2 LSB (W82C476). Output rise/fall time is measured between the 10% and 90% points of the full-scale transition.*

■ FIGURE 5. VIDEO INPUT/OUTPUT TIMING



Notes: *Diagram is shown for HIGH data value only. Output transition may be opposite sense. Cross-hatched areas are "Don't Care" conditions.*

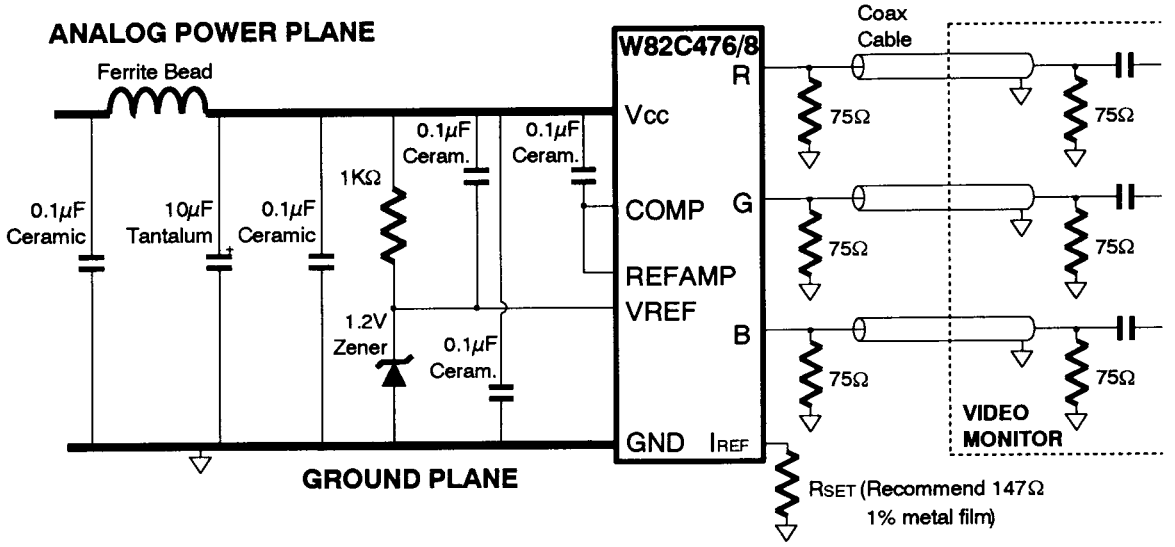
■ FIGURE 6. SWITCHING TEST WAVEFORM

■ ORDERING INFORMATION

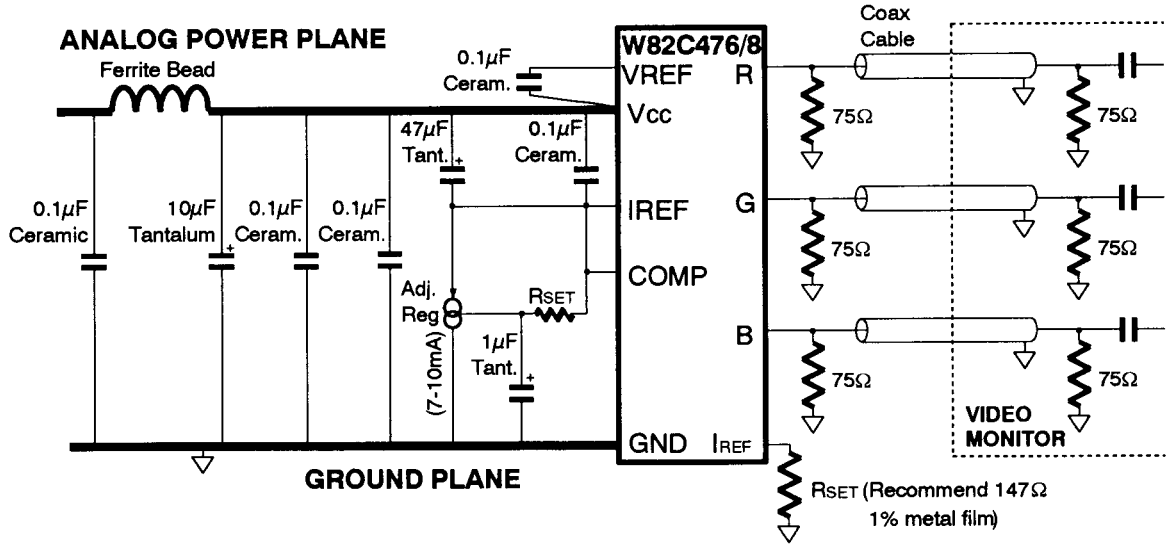
DEVICE PART NUMBER	SPEED	COLOR PALETTE SIZE	OVERLAY PALETTE	SYNC SIGNAL GENERATION	PACKAGE
W82C476P-66	66 MHz	256 x 18	none	no	44-pin PLCC, J-Lead
W82C467P-80	80 MHz	256 x 18	none	no	44-pin PLCC, J-Lead
W82C476-66	66 MHz	256 x 18	none	no	28-pin, 600mil Plastic DIP
W82C476-80	80 MHz	256 x 18	none	no	28-pin, 600mil Plastic DIP
W82C478P-66	66 MHz	256 x 24	15 x 24	yes	44-pin PLCC, J-Lead
W82C468P-80	80 MHz	256 x 24	15 x 24	yes	44-pin PLCC, J-Lead
W82C478P-100	100 MHz	256 x 24	15 x 24	yes	44-pin PLCC, J-Lead

Note: ALL DEVICES ABOVE ARE COMMERCIAL AMBIENT TEMPERATURE RANGE, 0°C to +70°C.

■ CIRCUIT CONNECTION RECOMMENDATIONS



■ FIGURE 7. EXAMPLE APPLICATION CIRCUIT, VOLTAGE REFERENCE MODE



■ FIGURE 8. EXAMPLE APPLICATION CIRCUIT, CURRENT REFERENCE MODE

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