Winbond Electronics Corp.

150MHZ CLOCK FOR WHITNEY CHIPSET

1.0 GENERAL DESCRIPTION

The W83194AR-W is a Clock Synthesizer for Intel Whitney chipset. W83194AR-W provides all clocks required for high-speed RISC or CISC microprocessor and also provides 64 different frequencies of CPU, SDRAM, PCI, 3V66, IOAPIC clocks frequency setting. All clocks are externally selectable with smooth transitions.

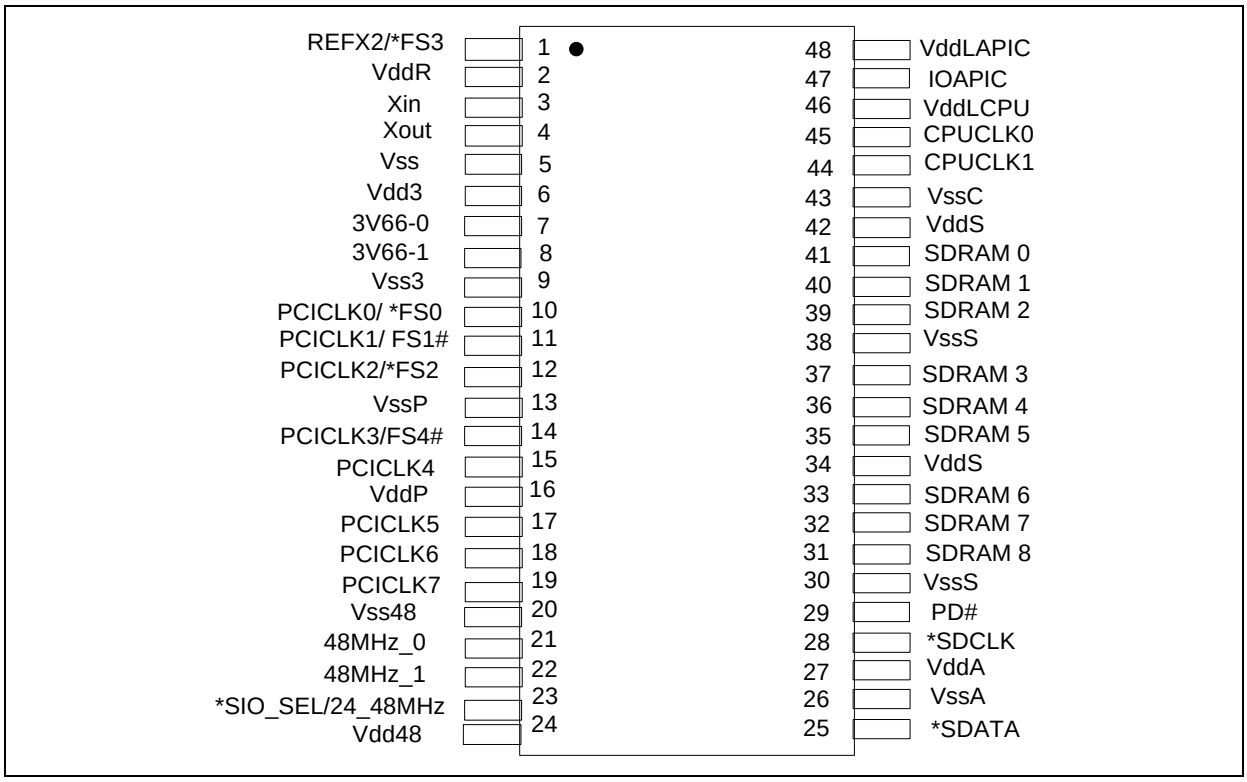
The W83194AR-W provides I^2C serial bus interface to program the registers to enable or disable each clock outputs and provides 0.5% and 0.75% center type spread spectrum to reduce EMI.

The W83194AR-W accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. High drive PCI and SDRAM CLOCK outputs typically provide greater than 1 V /ns slew rate into 30 pF loads. CPU CLOCK outputs typically provide better than 1 V /ns slew rate into 20 pF loads as maintaining 50¡Ó 5% duty cycle. The fixed frequency outputs as REF, 24MHz, and 48 MHz provide better than 0.5V /ns slew rate.

2.0 PRODUCT FEATURES

- 2 CPU clocks
- 9 SDRAM clocks for 2 DIMMs
- 8 PCI synchronous clocks.
- Optional single or mixed supply:
  (VddR = VddP=VddS = Vdd48 = Vdd3 = 3.3V, VddA=VddC=2.5V)
- Skew form CPU to PCI clock -1 to 4 ns, center 2.6 ns
- Smooth frequency switch with selections from 66.8 to 150MHz
- I^2C 2-Wire serial interface and I^2C read back
- 0.5% and 0.75% center type spread spectrum
- Programmable registers to enable/stop each output and select modes
  (mode as Tri-state or Normal)
- Two 48 MHz pins for USB
- 24 MHz for super I/O
- 48-pin SSOP package

3.0 PIN CONFIGURATION



4.0 PIN DESCRIPTION

IN - Input

OUT - Output

I/O - Bi-directional Pin

- Active Low

* - Internal 250kΩ pull-up

4.1 Crystal I/O

SYMBOL	PIN	I/O	FUNCTION
Xin	3	IN	Crystal input with internal loading capacitors and feedback resistors.
Xout	4	OUT	Crystal output at 14.318MHz nominally.

4.2 CPU, SDRAM, PCI, IOAPIC Clock Outputs

SYMBOL	PIN	I/O	FUNCTION
CPUCLK [0:1]	45,44	OUT	Low skew (< 250ps) clock outputs for host frequencies such as CPU and Chipset.
PD#	29	IN	Power Down mode when driven low.
IOAPIC	47	OUT	Clock outputs synchronous with PCI clock and powered by VddA.
SDRAM [0:8]	41,40, 39,37,36,35,33 ,32,31	OUT	SDRAM clock outputs.
PCICLK0/ *FS0	10	I/O	3.3V 33MHz PCI clock during normal operation. Latched input for FS0 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
PCICLK1/ FS1#	11	I/O	Low skew (< 250ps) PCI clock outputs. Latched input for FS1 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
PCICLK2/ *FS2	12	I/O	Low skew (< 250ps) PCI clock outputs. Latched input for FS2 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
PCICLK3/ FS4#	14	I/O	Low skew (< 250ps) PCI clock outputs. Latched input for FS4 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
PCICLK [4:7]	15,17,18,19	OUT	Low skew (< 250ps) PCI clock outputs.
3V66 [0:1]	7,8	OUT	3.3V output clocks for the chipset.

4.3 I²C Control Interface

SYMBOL	PIN	I/O	FUNCTION
*SDATA	25	I/O	Serial data of I²C 2-wire control interface with internal pull-up resistor.
*SDCLK	28	IN	Serial clock of I²C 2-wire control interface with internal pull-up resistor.

4.4 Fixed Frequency Outputs

SYMBOL	PIN	I/O	FUNCTION
REFX2 / *FS3	3	I/O	14.318MHz reference clock. This REF output is the stronger buffer for ISA bus loads. Halt PCICLK(0:4) clocks at logic 0 level, when input low (In mobile mode. MODE=0)
*SIO_SEL/24_48MHz	23	I/O	24MHz or 48MHz output clock. Latched input for SIO_SEL at initial power up for the output frequency of 24MHz(HIGH) and 48MHz(LOW) clocks.
48MHz [0:1]	21,22	I/O	48MHz output for USB during normal operation.

4.5 Power Pins

SYMBOL	PIN	FUNCTION
VddL	48	Power supply for CPU & IOAPIC, 2.5V or 3.3V.
Vdd48	24	Power supply for 48MHz output,3.3V.
Vdd3	6	Power supply for 3V_66 output, 3.3V.
VddP	16	Power supply for PCICLK, 3.3V.
VddR	2	Power supply for REFX2, 3.3V.
VddS	42,34	Power supply for SDRAM[0:8], nominal 3.3V.
VddA	27	Power for I2C CLK and DATA.
Vss	5,9,13,20,26,30,38, 43	Circuit Ground.

5.0 FREQUENCY SELECTION BY HARDWARE

FS4	FS3	FS2	FS1	FS0	CPU (MHz)	SDRAM (MHz)	3V66(MHz)	PCI (Mhz) = 3V66/2	IOAPIC (Mhz) = PCI/2
0	0	0	0	0	83.3	125	83	41.7	20.85
0	0	0	0	1	90	90	60	30	15
0	0	0	1	0	75	113	75	37.7	18.85
0	0	0	1	1	150	150	75	37.5	18.75
0	0	1	0	0	138	138	69	34.6	17.3
0	**0**	**1**	**0**	**1**	**95.25**	**95.25**	**63.5**	**31.75**	**15.88**
0	0	1	1	0	**129**	**129**	**86**	**43**	**21.5**
0	0	1	1	1	124	124	83	41.4	20.7
0	1	0	0	0	119	119	80	39.8	19.9
0	1	0	0	1	114	114	76	38	19
0	1	0	1	0	110	110	73.3	36.7	18.35
0	1	0	1	1	105	105	70	35	17.5
0	**1**	**1**	**0**	**0**	**66.8**	**100.2**	**66.8**	**33.4**	**16.7**
0	**1**	**1**	**0**	**1**	**100.2**	**100.2**	**66.8**	**33.3**	**16.7**
0	**1**	**1**	**1**	**0**	**133.6**	**100.2**	**66.7**	**33.6**	**16.8**
0	**1**	**1**	**1**	**1**	**133.3**	**133.3**	**66.7**	**33.3**	**16.7**
1	0	0	0	0	**125**	**125**	**83.33**	**41.67**	**20.83**
1	0	0	0	1	**127**	**127**	**84.67**	**42.34**	**21.17**
1	0	0	1	0	**130**	**130**	**86.67**	**43.33**	**21.67**
1	0	0	1	1	72	108	72	36.1	18.05
1	0	1	0	0	140	140	70	35.1	17.55
1	0	1	0	1	136	136	68	33.9	16.95
1	**0**	**1**	**1**	**0**	**145**	**145**	**73**	**36.3**	**18.15**
1	**0**	**1**	**1**	**1**	**155**	**155**	**78**	**38.8**	**19.4**
1	1	0	0	0	121	121	81	40.5	20.25
1	1	0	0	1	117	117	78	38.9	19.45
1	1	0	1	0	112	112	75	37.3	18.65
1	1	0	1	1	107	107	71	35.7	17.85
1	**1**	**1**	**0**	**0**	**66.8**	**100.2**	**66.8**	**33.4**	**16.7**
1	**1**	**1**	**0**	**1**	**100.2**	**100.2**	**66.8**	**33.4**	**16.7**
1	**1**	**1**	**1**	**0**	**100.9**	**100.9**	**67.3**	**33.6**	**16.8**
1	**1**	**1**	**1**	**1**	**133.6**	**133.6**	**66.7**	**33.3**	**16.7**

6.0 SERIAL CONTROL 0REGISTERS

The Pin column lists the affected pin number and the @PowerUp column gives the state at true power up. Registers are set to the values shown only on true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the below described sequence (Register 0, Register 1, Register 2, ...) will be valid and acknowledged.

Frequency Table Setting by I2C (SEL5 ~ SEL0)

SEL5	SEL4	SEL3	SEL2	SEL1	SEL0	CPU (MHz)	SDRAM (MHz)	3V66 (MHz)	PCI (MHz)	IOAPIC (MHz)
0	**0**	0	0	0	0	83.3	125	83	41.7	20.85
0	**0**	0	0	0	1	90	90	60	30	15
0	**0**	0	0	1	0	75	113	75	37.7	18.85
0	**0**	0	0	1	1	150	150	75	37.5	18.75
0	**0**	0	1	0	0	138	138	69	34.6	17.3
0	**0**	**0**	**1**	**0**	**1**	**95.25**	**95.25**	**63.5**	**31.75**	**15.88**
0	**0**	0	1	1	0	**129**	**129**	**86**	**43**	**21.5**
0	**0**	0	1	1	1	124	124	83	41.4	20.7
0	**0**	1	0	0	0	119	119	80	39.8	19.9
0	**0**	1	0	0	1	114	114	76	38	19
0	**0**	1	0	1	0	110	110	73.3	36.7	18.35
0	**0**	1	0	1	1	105	105	70	35	17.5
0	**0**	**1**	**1**	**0**	**0**	**66.8**	**100.2**	**66.8**	**33.4**	**16.7**
0	**0**	**1**	**1**	**0**	**1**	**100.2**	**100.2**	**66.8**	**33.3**	**16.7**
0	**0**	**1**	**1**	**1**	**0**	**133.6**	**100.2**	**66.7**	**33.6**	**16.8**
0	**0**	**1**	**1**	**1**	**1**	**133.3**	**133.3**	**66.7**	**33.3**	**16.7**
0	**1**	0	0	0	0	**125**	**125**	**83.33**	**41.67**	**20.83**
0	**1**	0	0	0	1	**127**	**127**	**84.67**	**42.34**	**21.17**
0	**1**	0	0	1	0	**130**	**130**	**86.67**	**43.33**	**21.67**
0	**1**	0	0	1	1	72	108	72	36.1	18.05
0	**1**	0	1	0	0	140	140	70	35.1	17.55
0	**1**	0	1	0	1	136	136	68	33.9	16.95
0	**1**	**0**	**1**	**1**	**0**	**145**	**145**	**73**	**36.3**	**18.15**
0	**1**	**0**	**1**	**1**	**1**	**155**	**155**	**78**	**38.8**	**19.4**
0	**1**	1	0	0	0	121	121	81	40.5	20.25
0	**1**	1	0	0	1	117	117	78	38.9	19.45
0	**1**	1	0	1	0	112	112	75	37.3	18.65
0	**1**	1	0	1	1	107	107	71	35.7	17.85
0	**1**	**1**	**1**	**0**	**0**	**66.8**	**100.2**	**66.8**	**33.4**	**16.7**
0	**1**	**1**	**1**	**0**	**1**	**100.2**	**100.2**	**66.8**	**33.4**	**16.7**
0	**1**	**1**	**1**	**1**	**0**	**100.9**	**100.9**	**67.3**	**33.6**	**16.8**
0	**1**	**1**	**1**	**1**	**1**	**133.3**	**133.3**	**66.7**	**33.3**	**16.7**

SEL5	SEL4	SEL3	SEL2	SEL1	SEL0	CPU (MHz)	SDRAM (MHz)	3V66 (MHz)	PCI (MHz)	IOAPIC (MHz)
1	0	0	0	0	0	141	141	70.5	35.25	17.63
1	0	0	0	0	1	143	143	71.5	35.75	17.88
1	0	0	0	1	0	145	145	72.5	36.25	18.13
1	0	0	0	1	1	146	146	73	36.5	18.25
1	0	0	1	0	0	147	147	73.5	36.75	18.38
1	0	0	1	0	1	148	148	74	37	18.5
1	0	0	1	1	0	149	149	74.5	37.25	18.63
1	0	0	1	1	1	151	151	75.5	37.75	18.88
1	0	1	0	0	0	153	153	76.5	38.25	19.13
1	0	1	0	0	1	155	155	77.5	38.75	19.38
1	0	1	0	1	0	156	156	78	39	19.5
1	0	1	0	1	1	157	157	78.5	39.25	19.63
1	0	1	1	0	0	159	159	79.5	39.75	19.88
1	0	1	1	0	1	161	161	80.5	40.25	20.13
1	0	1	1	1	0	163	163	81.5	40.75	20.38
1	0	1	1	1	1	164	164	82	41	20.5
1	1	0	0	0	0	168	168	84	42	21
1	1	0	0	0	1	170	170	85	42.5	21.25
1	1	0	0	1	0	172	172	86	43	21.5
1	1	0	0	1	1	175	175	58.33	29.17	14.58
1	1	0	1	0	0	177	177	59	29.5	14.75
1	1	0	1	0	1	180	180	60	30	15
1	1	0	1	1	0	182	182	60.67	30.33	15.17
1	1	0	1	1	1	184	184	61.33	30.67	15.33
1	1	1	0	0	0	186	186	62	31	15.5
1	1	1	0	0	1	188	188	62.67	31.33	15.67
1	1	1	0	1	0	190	190	63.33	31.67	15.83
1	1	1	0	1	1	192	192	64	32	16
1	1	1	1	0	0	194	194	64.67	32.33	16.17
1	1	1	1	0	1	196	196	65.33	32.67	16.33
1	1	1	1	1	0	198	198	66	33	16.5
1	1	1	1	1	1	200	200	66.67	33.33	16.67

6.1 Register 0: Control Register

Bit	@PowerUp	Pin	Description
7	0	-	Reserved
6	1	1	REF2X(Active / Inactive)
5	0	-	Reserved
4	0	-	Reserved
3	0	-	Reserved
2	1	23	24_48MHz(Active / Inactive)
1	1	21,22	48MHz_0, 48MHz_1(Active / Inactive)
0	1	31	SDRAM8(Active / Inactive)

6.2 Register 1 : SDRAM Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	32	SDRAM7 (Active / Inactive)
6	1	33	SDRAM6 (Active / Inactive)
5	1	35	SDRAM5 (Active / Inactive)
4	1	36	SDRAM4 (Active / Inactive)
3	1	37	SDRAM3 (Active / Inactive)
2	1	39	SDRAM2 (Active / Inactive)
1	1	40	SDRAM1 (Active / Inactive)
0	1	41	SDRAM0 (Active / Inactive)

6.3 Register 2: PCI Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	19	PCICLK7 (Active / Inactive)
6	1	18	PCICLK6 (Active / Inactive)
5	1	17	PCICLK5 (Active / Inactive)
4	1	15	PCICLK4 (Active / Inactive)
3	1	14	PCICLK3 (Active / Inactive)
2	1	13	PCICLK2 (Active / Inactive)
1	1	11	PCICLK1 (Active / Inactive)
0	1	10	PCICLK0 (Active / Inactive)

6.4 Register 3: CPU Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	0	-	Reserved
6	1	8	3V66_1(Active / Inactive)
5	1	7	3V66_0(Active / Inactive)
4	0	-	Reserved
3	1	47	IOAPIC(Active / Inactive)
2	1	44	CPUCLK1 (Active / Inactive)
1	1	43	CPUCLK0 (Active / Inactive)
0	0	-	Reserved

6.5 Register 4: Control Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	0	-	SSEL3 (Frequency table selection by software via I^2C)
6	0	-	SSEL2 (Frequency table selection by software via I^2C)
5	0	-	SSEL1 (Frequency table selection by software via I^2C)
4	0	-	SSEL0 (Frequency table selection by software via I^2C)
3	0	-	0 = Selection by hardware 1 = Selection by software I^2C - Bit (1,2, 4:6)
2	0	-	SSEL4 (Frequency table selection by software via I^2C)
1	0	-	SSEL5 (Frequency table selection by software via I^2C)
0	0	-	Reserved

6.6 Register 5: Control Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	0	-	0 = ¡ó0.5% Center type Spread Spectrum Modulation 1 = ¡ó0.75% Center type Spread Spectrum Modulation
6	0	-	Reserved
5	0	-	Reserved
4	0	-	Reserved
3	0	-	Reserved
2	0	-	Reserved
1	0	-	0 = Normal 1 = Spread Spectrum enabled
0	0	-	Reserved

6.7 Register 6: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	1	-	Winbond Chip ID
6	0	-	Winbond Chip ID
5	0	-	Winbond Chip ID
4	1	-	Winbond Chip ID
3	0	-	Winbond Chip ID
2	0	-	Winbond Chip ID
1	1	-	Winbond Chip ID
0	0	-	Winbond Chip ID

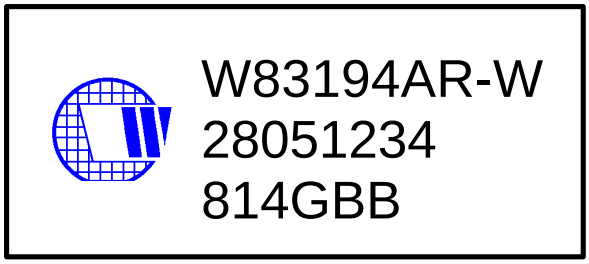
6.8 Register 7: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	0	-	Winbond Chip ID
6	0	-	Winbond Chip ID
5	0	-	Winbond Chip ID
4	0	-	Winbond Chip ID
3	0	-	Winbond Chip ID
2	0	-	Winbond Chip ID
1	0	-	Winbond Chip ID
0	1	-	Winbond Chip ID

7.0 ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83194AR-W	48 PIN SSOP	Commercial, 0°C to +70°C

8.0 HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83194AR-W

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

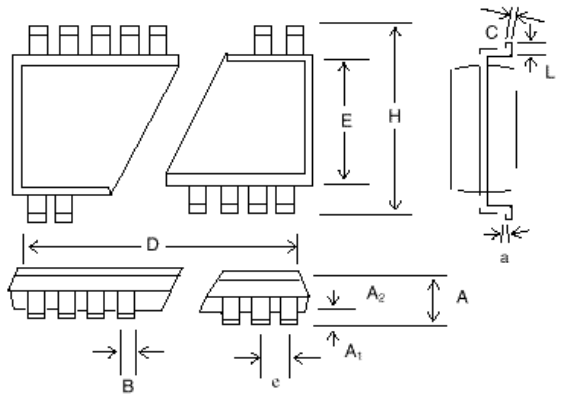
3rd line: Tracking code 814 G B B

814: packages made in '98, week 14

G: assembly house ID; A means ASE, S means SPIL, G means GR

BB: IC revision

9.0 PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0°	5°	8°	0°	5°	8°

Winbond Electronics Corp.

Headquarters
No. 4, Creation Rd. III
Science-Based Industrial Park
Hsinchu, Taiwan
TEL: 886-35-770066
FAX: 886-35-789467
www: http://www.winbond.com.tw/

Taipei Office
11F, No. 115, Sec. 3, Min-Sheng East Rd.
Taipei, Taiwan
TEL: 886-2-7190505
FAX: 886-2-7197502
TLX: 16485 WINTPE

Winbond Electronics (H.K.) Ltd.
Rm. 803, World Trade Square, Tower II
123 Hoi Bun Rd., Kwun Tong
Kowloon, Hong Kong
TEL: 852-27516023-7
FAX: 852-27552064

Winbond Electronics (North America) Corp.
2730 Orchard Parkway
San Jose, CA 95134 U.S.A.
TEL: 1-408-9436666
FAX: 1-408-9436668