W83194BR-323/W83194BG-323
STEPLESS CLOCK FOR INTEL BROOKDALE CHIPSET

Date: 03/22/2006 Revision: 2.1

STEPLESS CLOCK FOR INTEL BROOKDALE CHIPSET

W83194BR-323 Data Sheet Revision History

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
1	n.a.			n.a.	All of the versions before 0.50 are for internal use.
2	n.a.	13/May	1.0	n.a	Change version and version on web site to 1.0
3	P13	02/August	1.1	1.1	Delete Test mode register.
4	All	02/20/2003	2.0	2.0	Update new form
5		03/22/2006	2.1		Add lead free part number --- W83194BG-323
6					
7					
8					
9					
10					

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

STEPLESS CLOCK FOR INTEL BROOKDALE CHIPSET

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STEPLESS CLOCK FOR INTEL BROOKDALE CHIPSET

1. GENERAL DESCRIPTION

The W83194BR-323 is a Clock Synthesizer for Intel Brook dale 845 chipset. W83194BR-323 provides all clocks required for high-speed microprocessor and provides step-less frequency programming and 32 different frequencies of CPU, PCI, and 3V66 clocks setting. All clocks are externally selectable with smooth transitions.

The W83194BR-323 provides I^2C serial bus interface to program the registers to enable or disable each clock outputs and provides -0.5% and +/-0.25% center type spread spectrum or programmable S.S.T. scale to reduce EMI.

The W83194BR-323 also has watchdog timer and reset output pin to support auto-reset when systems hanging caused by improper frequency setting.

The W83194BR-323 accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. High drive PCI CLOCK outputs typically provide greater than 1 V /ns slew rate into 30 pF loads. The fixed frequency outputs as REF and 48 MHz provide better than 0.5V /ns slew rate.

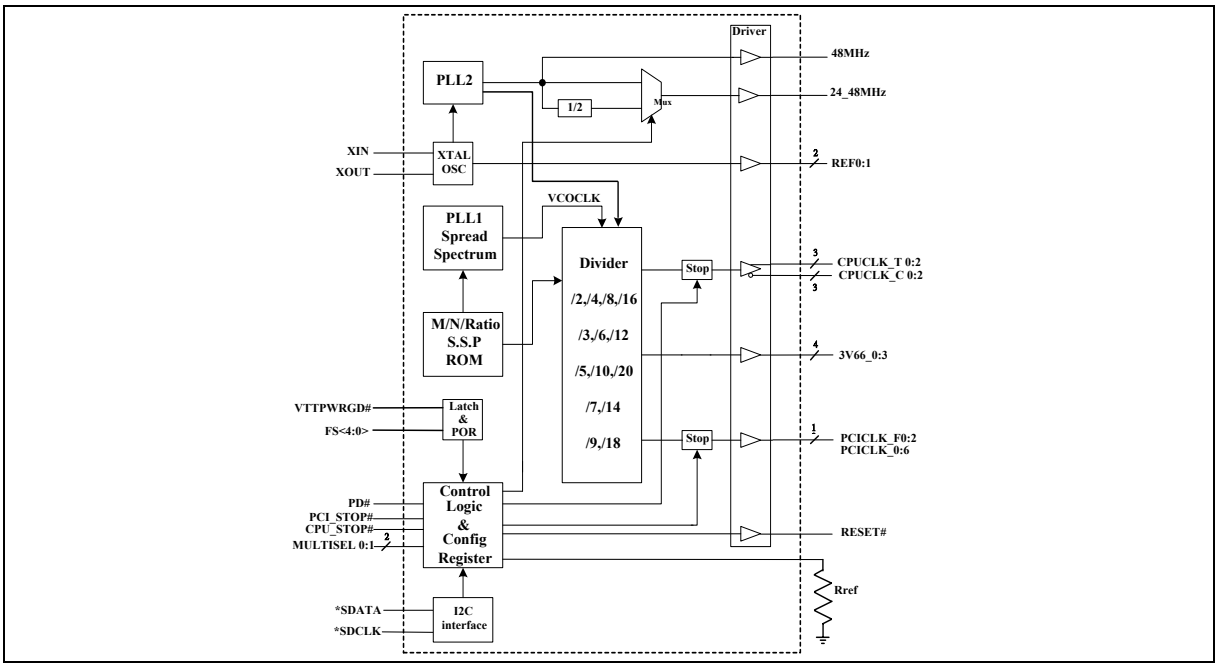
2. PRODUCT FEATURES

3 Differential pairs of CPU clock outputs

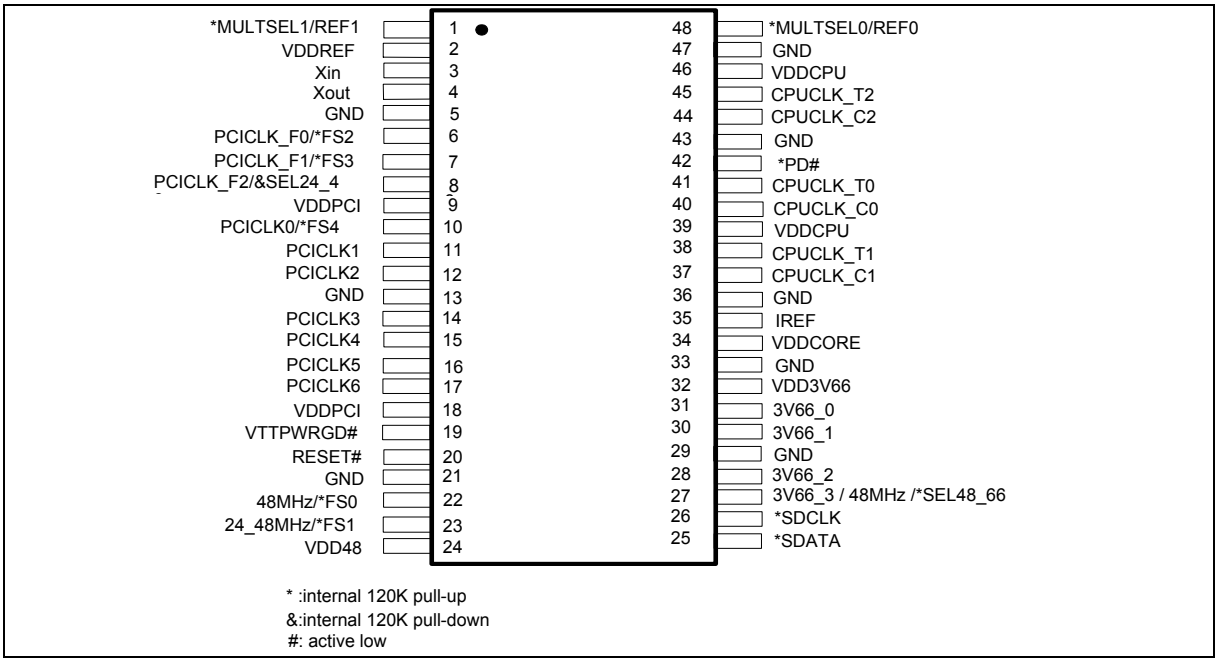
- 4 3V66 clock outputs
- 10 PCI synchronous clocks
- 24_48Mhz clock output for super I/O.
- 48 MHz clock output for USB.
- Skew form CPU to PCI clock 1 to 4 ns, center 2.6 ns
- Smooth frequency switch with selections from 66.8 to 200MHz
- Step-less frequency programming
- I^2C 2-Wire serial interface and support byte read/write and block read/write.
- -0.5% and +/- 0.25% center type spread spectrum
- Programmable S.S.T. scale to reduce EMI
- Programmable registers to enable/stop each output and select modes
- Watch Dog Timer and RESET# output pins
- 48-pin SSOP package

STEPLESS CLOCK FOR INTEL BROOKDALE CHIPSET

3. BLOCK DIAGRAM



4. PIN CONFIGURATION



* :internal 120K pull-up
&:internal 120K pull-down
#: active low

5. PIN DESCRIPTION

BUFFER TYPE SYMBOL	DESCRIPTION
IN	Input
IN_{td120k}	Input pin and internal 120K pull down
OUT	Output
OD	Open Drain
I/O	Bi-directional Pin
I/OD	Bi-directional Pin, Open Drain
#	Active Low
*	Internal 120kΩ pull-up
&	Internal 120kΩ pull-down

5.1 Crystal I/O

PIN	PIN NAME	TYPE	DESCRIPTION
3	XIN	IN	Crystal input with internal loading capacitors (18pF) and feedback resistors.
4	XOUT	OUT	Crystal output at 14.318MHz nominally with internal loading capacitors (18pF).

5.2 CPU, 3V66, and PCI Clock Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
41,38, 40,37 45,44	CPUCLK_T [0:2] CPUCLK_C [0:2]	OUT	Low skew (< 250ps) differential clock outputs for host frequencies of CPU and chipset.
31,30,28	3V66_0:2	OUT	3.3V 66MHz clock outputs.
27	3V66_3 / 48MHz	OUT	3V66_3 or 48MHz clock output.
	*SEL48_66	IN_{tp120k}	Latched input for 48MHz or 66MHz select pin. This is internal 120K pull up default 66MHz. In power on reset period, it is a hardware-latched pin, and it can be R/W by I2C control after power on reset period. Select by register 16 bit 6.
35	IREF	IN	Deciding the reference current for the CPUCLK pairs. The pin was connected to the precision resistor tied to ground to decide the appropriate current. There are several modes to select different current via power on trapping the Pin 1 & 48 (MULTISEL0, 1). The table is show as follows.
20	RESET#	OD	System reset signal when the watchdog is time out. This pin will generate 250ms low phase when the watchdog timer is timeout.
19	VTTPWRGD#	IN	Power good input signal comes from ACPI with low active. This 3.3V input is level sensitive strobe used to determine FS [4:0] and MULTISEL0, MULTISEL1, input are valid and is ready to sampled. This pin is low active.

CPU, 3V66, and PCI Clock Outputs, continued

PIN	PIN NAME	TYPE	DESCRIPTION
42	PD#	IN	Power Down Function. This is power down pin, low active (PD#). Internal 120K pull up
6	PCICLK_F0	OUT	3.3V free running PCI clock output.
	*FS2	IN_{tp120k}	Latched input for FS2 at initial power up for H/W selecting the output frequency, This is internal 120K pull up.
7	PCICLK_F1	OUT	3.3V free running PCI clock output.
	*FS3	IN_{tp120k}	Latched input for FS3 at initial power up for H/W selecting the output frequency, This is internal 120K pull up.
8	PCICLK_F2	OUT	3.3V free running PCI clock outputs.
	&SEL24_48	IN_{td120k}	Latched input for 24MHz or 48MHz select pin. This is internal 120K pull down default 24MHz.
10	PCICLK0	OUT	Low skew (< 250ps) PCI clock outputs.
	*FS4	IN_{tP120k}	Latched input for FS4 at initial power up for H/W selecting the output frequency, This is internal 120K pull up.
11, 12, 14, 15, 16, 17	PCICLK [1:6]	OUT	Low skew (< 250ps) PCI clock outputs.

5.3 I^2C Control Interface

PIN	Pin Name	Type	Description
25	SDATA*	I/OD	Serial data of I^2C 2-wire control interface with internal pull-up resistor.
26	SCLK*	IN	Serial clock of I^2C 2-wire control interface with internal pull-up resistor.

5.4 Fixed Frequency Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
48	REF0	OUT	14.318NHz output.
	MULTSEL0*	IN_{tp120k}	Latched input for MULTSEL0 at initial power up, internal 120K pull up
1	REF1	OUT	14.318NHz output.
	MULTSEL1*	IN_{tp120k}	Latched input for MULTSEL1 at initial power up, internal 120K pull up
22	48MHz	OUT	48MHz clock output for USB.
	*FS0	IN_{tp120k}	Latched input for FS0 at initial power up for H/W selecting the output frequency. This is internal 120K pull up.
23	24_48MHz	OUT	24(default) or 48MHz clock output, In power on reset period, it is a hardware-latched pin, and it can be R/W by I2C control after power on reset period. Select by register 16 bit 7.
	*FS1	IN_{tp120k}	Latched input for FS1 at initial power up for H/W selecting the output frequency. This is internal 120K pull up.

5.5 Power Pins

PIN	PIN NAME	TYPE	DESCRIPTION
2	VDDREF	PWR	3.3V power supply for REF.
9,18	VDDPCI	PWR	3.3V power supply for PCI.
32	VDD3V66	PWR	3.3V power supply for 3V66.
39,46	VDDCPU	PWR	3.3V power supply for CPU.
34	VDDCORE	PWR	3.3V power supply for analog core.
24	VDD48	PWR	Analog power 3.3V for 48MHz.
5, 13, 21, 29, 33, 36, 43, 47	GND	PWR	Ground pin for 3.3 V

Hardware MULTSEL [1:0] selects Function

MULTSEL1	MULTSEL0	BOARD TARGET TRACE/TERM Z	REFERENCE R,IREF = VDD/(3*RR)	OUTPUT CURRENT	VOH @ Z
0	0	50 Ω	Rr =221 1% IREF = 5.00mA	Ioh=4*IREF	1.0V @ 50
0	0	60 Ω	Rr =221 1% IREF = 5.00mA	Ioh=4*IREF	1.2V @ 60
0	1	50 Ω	Rr =221 1% IREF = 5.00mA	Ioh=5*IREF	1.25V @ 50
0	1	60 Ω	Rr =221 1% IREF = 5.00mA	Ioh=5*IREF	1.5V @ 60
1	0	50 Ω	Rr =221 1% IREF = 5.00mA	Ioh=6*IREF	1.5V @ 50
1	0	60 Ω	Rr =221 1% IREF = 5.00mA	Ioh=6*IREF	1.8V @ 60
1	1	50 Ω	Rr =221 1% IREF = 5.00mA	Ioh=7*IREF	1.75V @ 50
1	1	60 Ω	Rr =221 1% IREF = 5.00mA	Ioh=7*IREF	2.1V @ 50
0	0	50 Ω	Rr =475 1% IREF = 2.32mA	Ioh=4*IREF	0.47V @ 50
0	0	60 Ω	Rr =475 1% IREF = 2.32mA	Ioh=4*IREF	0.56V @ 50
0	1	50 Ω	Rr =475 1% IREF = 2.32mA	Ioh=5*IREF	0.58V @ 50
0	1	60 Ω	Rr =475 1% IREF = 2.32mA	Ioh=5*IREF	0.7V @ 60
1	0	50 Ω	Rr =475 1% IREF = 2.32mA	Ioh=6*IREF	0.7V @ 50
1	0	60 Ω	Rr =475 1% IREF = 2.32mA	Ioh=6*IREF	0.84V @ 60
1	1	50 Ω	Rr =475 1% IREF = 2.32mA	Ioh=7*IREF	0.81V @ 50
1	0	60 Ω	Rr =475 1% IREF = 2.32mA	Ioh=6*IREF	0.97V @ 60

6. FREQUENCY SELECTION BY HARDWARE OR SOFTWARE

This frequency table is used at power on latched FS [4:0] value or software programming at SSEL [4:0] (Register 0 bit 6 ~ 2).

FS4	FS3	FS2	FS1	FS0	CPU (MHZ)	3V66(MHZ)	PCI (MHZ)	SPREAD %
0	0	0	0	0	102.0	68.0	34.0	+/-0.25%
0	0	0	0	1	105.0	70.0	35.0	+/-0.25%
0	0	0	1	0	108.0	72.0	36.0	+/-0.25%
0	0	0	1	1	111.0	74.0	37.0	+/-0.25%
0	0	1	0	0	114.0	76.0	38.0	+/-0.25%
0	0	1	0	1	117.0	78.0	39.0	+/-0.25%
0	0	1	1	0	120.0	80.0	40.0	+/-0.25%
0	0	1	1	1	123.0	82.0	41.0	+/-0.25%
0	1	0	0	0	126.0	63.0	31.5	+/-0.25%
0	1	0	0	1	130.0	65.0	32.5	+/-0.25%
0	1	0	1	0	136.0	68.0	34.0	+/-0.25%
0	1	0	1	1	140.0	70.0	35.0	+/-0.25%
0	1	1	0	0	144.0	72.0	36.0	+/-0.25%
0	1	1	0	1	148.0	74.0	37.0	+/-0.25%
0	1	1	1	0	152.0	76.0	38.0	+/-0.25%
0	1	1	1	1	156.0	78.0	39.0	+/-0.25%
1	0	0	0	0	160.0	80.0	40.0	+/-0.25%
1	0	0	0	1	164.0	82.0	41.0	+/-0.25%
1	0	0	1	0	166.6	66.6	33.3	+/-0.25%
1	0	0	1	1	170.0	68.0	34.0	+/-0.25%
1	0	1	0	0	175.0	70.0	35.0	+/-0.25%
1	0	1	0	1	180.0	72.0	36.0	+/-0.25%
1	0	1	1	0	185.0	74.0	37.0	+/-0.25%
1	0	1	1	1	190.0	76.0	38.0	+/-0.25%
1	1	0	0	0	66.8	66.8	33.4	+/-0.25%
1	1	0	0	1	100.2	66.8	33.4	+/-0.25%
1	1	0	1	0	133.6	66.8	33.4	+/-0.25%
1	1	0	1	1	200.4	66.8	33.4	+/-0.25%
1	1	1	0	0	66.6	66.6	33.3	-0.5%
1	1	1	0	1	100.0	66.6	33.3	-0.5%
1	1	1	1	0	200.0	66.6	33.3	-0.5%
1	1	1	1	1	133.3	66.6	33.3	-0.5%

7. I2C CONTROL AND STATUS REGISTERS

7.1 Register 0: Frequency Select Register (default = 0)

BIT	NAME	PWD	DESCRIPTION
7	EN_SPSP	0	Enable Spread Spectrum in the frequency table. 0 = Normal 1 = Spread Spectrum enabled
6	SSEL [4]	0	Frequency selection by software via I^2C.
5	SSEL [3]	0	
4	SSEL [2]	0	
3	SSEL [1]	0	
2	SSEL [0]	0	
1	EN_SSEL	0	Enable software program FS [4:0]. 0 = Select frequency by hardware. 1= Select frequency by software I^2C - Bit 6 ~ 2.
0	EN_SAFE_FREQ	0	Enable reload safe frequency when the watchdog is timeout. 0 = reload the FS [4:0] latched pins when watchdog time out. 1 = reload the safe frequency bit defined at Register 5 bit 4~0.

7.2 Register 1: CPU Clock Register (1 = enable, 0 = Stopped)

BIT	PIN NO	PWD	DESCRIPTION
7	44,45	1	CPUCLK_T2 / C2
6	37,38	1	CPUCLK_T1 / C1
5	40,41	1	CPUCLK_T0 / C0
4	-	X	FS [4] Read back.
3	-	X	FS [3] Read back
2	-	X	FS [2] Read back
1	-	X	FS [1] Read back
0	-	X	FS [0] Read back

7.3 Register 2: PCI Clock Register (1 = enable, 0 = Stopped)

BIT	PIN NO	PWD	DESCRIPTION
7	48	X	MULTISEL0 trapping pin data read back
6	17	1	PCICLK6
5	16	1	PCICLK5
4	15	1	PCICLK4
3	14	1	PCICLK3
2	12	1	PCICLK2
1	11	1	PCICLK1
0	10	1	PCICLK0

7.4 Register 3: PCI, 48MHz Clock Register (1 = enable, 0 = Stopped)

BIT	PIN NO	PWD	DESCRIPTION
7	22	1	48MHZ
6	23	1	24_48MHz
5	48	1	REF0
4	1	1	REF1
3	Reserved	1	Reserved
2	8	1	PCICLK_F2
1	7	1	PCICLK_F1
0	6	1	PCICLK_F0

7.5 Register 4: 3V66 Control Register (1 = enable, 0 = Stopped)

BIT	PIN NO	PWD	DESCRIPTION
7	-	1	Reserved
6	-	1	Reserved
5	-	1	Reserved
4	-	1	Reserved
3	27	1	3V66_3 / 48MHz
2	28	1	3V66_2
1	30	1	3V66_1
0	31	1	3V66_0

7.6 Register 5: Watchdog Control Register

BIT	NAME	PWD	DESCRIPTION
7	MULTISEL1	X	MULTISEL1 trapping pin data read back
6	EN_WD	0	Enable Watchdog Timer if set to 1. Set to 0, disable watchdog timer. Read this bit will return a counting state. If timer continues down count, this bit will return 1. Otherwise, this bit will return 0.
5	WD_TIMEOUT	0	Watchdog Timeout Status. If the watchdog is started and timer down counts to zero, this bit will be set to 1. Clear this bit to logic 0, If set to 1, when the watchdog is restart in the next time. This bit is Read Only.
4	SAF_FREQ [4]	0	Watchdog safe frequency bits. These bits will be reloaded into FS [4:0], if the watchdog is timeout and enable reload safe frequency bits.
3	SAF_FREQ [3]	0	
2	SAF_FREQ [2]	0	
1	SAF_FREQ [1]	0	
0	SAF_FREQ [0]	0	

7.7 Register 6: Watchdog Timer Register

BIT	NAME	PWD	DESCRIPTION
7	WD_TIME [7]	0	Watchdog timeout time. The bit resolution is 250mS. The default time is 8*250mS = 2.0 seconds. If the watchdog timer is start, this register will be down count. Read this register will return a down count value.
6	WD_TIME [6]	0	
5	WD_TIME [5]	0	
4	WD_TIME [4]	0	
3	WD_TIME [3]	1	
2	WD_TIME [2]	0	
1	WD_TIME [1]	0	
0	WD_TIME [0]	0	

7.8 Register 7: M/N Program Register

BIT	NAME	PWD	DESCRIPTION
7	N_DIV [8]	1	Programmable N divisor value. Bit 7 ~0 are defined in the Register 8.
6	TEST1	1	Test bit 1. Winbond test bit, do not change them.
5	TEST0	0	Test bit 0. Winbond test bit, do not change them.
4	M_DIV [4]	0	Programmable M divisor value.
3	M_DIV [3]	1	
2	M_DIV [2]	1	
1	M_DIV [1]	0	
0	M_DIV [0]	1	

7.9 Register 8: M/N Program Register

BIT	NAME	PWD	DESCRIPTION
7	N_DIV [7]	0	Programmable N divisor value bit 7 ~0. The bit 8 is defined in Register 7.
6	N_DIV [6]	1	
5	N_DIV [5]	1	
4	N_DIV [4]	0	
3	N_DIV [3]	0	
2	N_DIV [2]	1	
1	N_DIV [1]	1	
0	N_DIV [0]	1	

7.10 Register 9: Spread Spectrum Programming Register

BIT	NAME	PWD	DESCRIPTION
7	SP_UP [3]	0	Spread Spectrum Up Counter bit 3.
6	SP_UP [2]	0	Spread Spectrum Up Counter bit 2.
5	SP_UP [1]	0	Spread Spectrum Up Counter bit 1.
4	SP_UP [0]	1	Spread Spectrum Up Counter bit 0
3	SP_DOWN [3]	1	Spread Spectrum Down Counter bit 3
2	SP_DOWN [2]	1	Spread Spectrum Down Counter bit 2
1	SP_DOWN [1]	1	Spread Spectrum Down Counter bit 1
0	SP_DOWN [0]	1	Spread Spectrum Down Counter bit 0

7.11 Register 10: Divisor and Step-less Enable and Skew Control Register

BIT	NAME	PWD	DESCRIPTION
7	EN_MN_PROG	0	0: use frequency table 1: use M/N register to program frequency The equation is **VCO freq. = 14.318MHz * (N+4)/ M**. When the watchdog timer is timeout, this will be clear. In this time, the frequency is set to hardware default latched or safe frequency set by EN_SFAE_FREQ (Register 0 bit 0).
6	RATIO_SEL [3]	0	CPU, 3V66, and PCI ratio selection. The ratio is shown as following table.
5	RATIO_SEL [2]	0	
4	RATIO_SEL [1]	1	
3	RATIO_SEL [0]	0	
2	CPU_3V66_SKEW [2]	1	CPU to 3V66 skew.
1	CPU_3V66_SKEW [1]	0	
0	CPU_3V66_SKEW [0]	0	

Table of CPU, 3V66, and PCI clock selection.

I2C Reg10 Definition

REG10	REG10	REG10	REG10			
BIT6	BIT5	BIT4	BIT3	CPU	3V66	PCI
SSEL3	SSEL2	SSEL1	SSEL0	RATIO	RATIO	RATIO
0	0	0	0	2	5	10
0	0	0	1	2	6	12
0	0	1	0	3	6	12
0	0	1	1	4	6	12
0	1	0	0	4	8	16
0	1	0	1	6	6	12

7.12 Register 11: Winbond Chip ID Register (Read Only)

BIT	NAME	PWD	DESCRIPTION
7	CHPI_ID [7]	0	Winbond Chip ID. W83194BR-323 is 0x57.
6	CHPI_ID [6]	1	Winbond Chip ID.
5	CHPI_ID [5]	0	Winbond Chip ID.
4	CHPI_ID [4]	1	Winbond Chip ID.
3	CHPI_ID [3]	0	Winbond Chip ID.
2	CHPI_ID [2]	1	Winbond Chip ID.
1	CHPI_ID [1]	1	Winbond Chip ID.
0	CHPI_ID [0]	1	Winbond Chip ID.

7.13 Register 12: Winbond Chip ID Register (Read Only)

BIT	NAME	PWD	DESCRIPTION
7	SUB_ID [3]	0	The sub-chip ID of W83194BR-323 is defined as 0010b.
6	SUB_ID [2]	0	Winbond Sub-Chip ID.
5	SUB_ID [1]	1	Winbond Sub-Chip ID.
4	SUB_ID [0]	0	Winbond Sub-Chip ID.
3	VER_ID [3]	0	Winbond Version ID. The Version ID of W83194BR-323 is 0010b.
2	VER_ID [2]	0	Winbond Version ID.
1	VER_ID [1]	1	Winbond Version ID.
0	VER_ID [0]	0	Winbond Version ID.

7.14 Register 13: Reserved

BIT	NAME	PWD	DESCRIPTION
7	Reserved	0	Reserved
6	Reserved	0	Reserved
5	Reserved	1	Reserved
4	Reserved	0	Reserved
3	Reserved	0	Reserved
2	Reserved	1	Reserved
1	Reserved	1	Reserved
0	Reserved	1	Reserved

7.15 Register 14: CPU to PCI Skew Control

BIT	NAME	PWD	DESCRIPTION
7	Reserved	1	
6	Reserved	0	
5	Reserved	0	
4	CPU_PCI_SKEW [2]	1	CPU to PCI Skew
3	CPU_PCI_SKEW [1]	0	
2	CPU_PCI_SKEW [0]	0	
1	Reserved	0	
0	Reserved	0	

7.16 Register 15: SEL24_48 and SEL48_66 Control

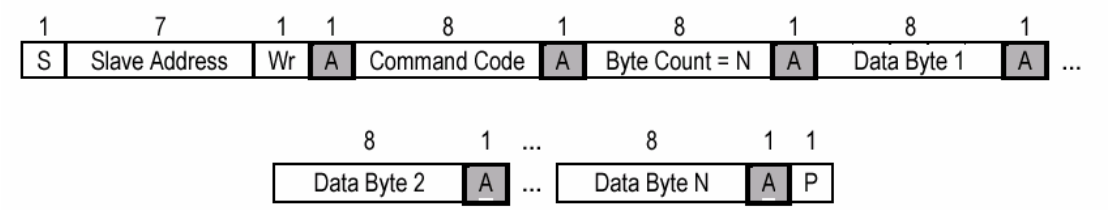
BIT	NAME	PWD	DESCRIPTION
7	SEL24_48	X	In power on reset period, it is a hardware-latched pin, and it can be R/W by I2C control after power on reset period. 0-> 24 MHz, 1->48MHz.
6	SEL_48_66	X	In power on reset period, it is a hardware-latched pin, and it can be R/W by I2C control after power on reset period. 0-> 48 MHz, 1->66MHz.
5	Reserved	0	Reserved for Winbond internal use, do not change them
4	Reserved	0	Reserved for Winbond internal use, do not change them
3	Reserved	0	
2	Reserved	0	
1	Reserved	0	
0	Reserved	1	

8. ACCESS INTERFACE

The W83194BR-323 provides I^2C Serial Bus for microprocessor to read/write internal registers. In the W83194BR-323 is provided Block Read/Block Write and Byte-Data Read/Write protocol. The I^2C address is defined at 0xD2.

Block Read and Block Write Protocol

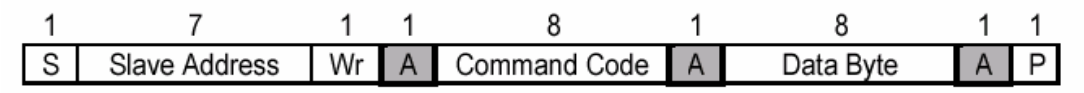
8.1 Block Write protocol



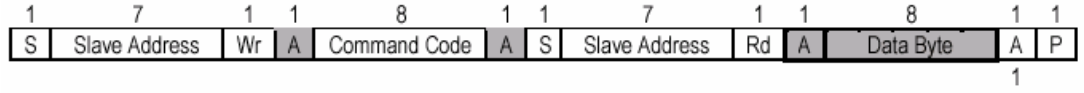
8.2 Block Read protocol

In block mode, the command code must filled 8'h00

8.3 Byte Write protocol



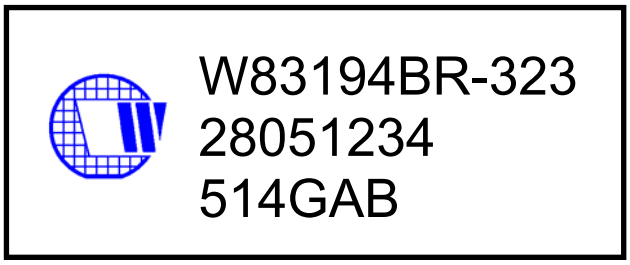
8.4 Byte Read protocol

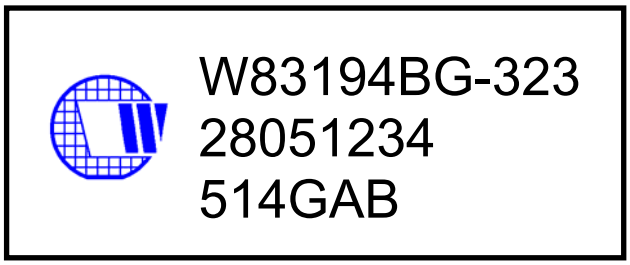


9. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83194BR-323	48 PIN SSOP	Commercial, 0°C to +70°C
W83194BG-323	48 PIN SSOP (Lead free package)	Commercial, 0°C to +70°C

10. HOW TO READ THE TOP MARKING





1st line: Winbond logo and the type number:

Normal part:W83194BR-323, Lead free part:W83194BG-323

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 514 G BB

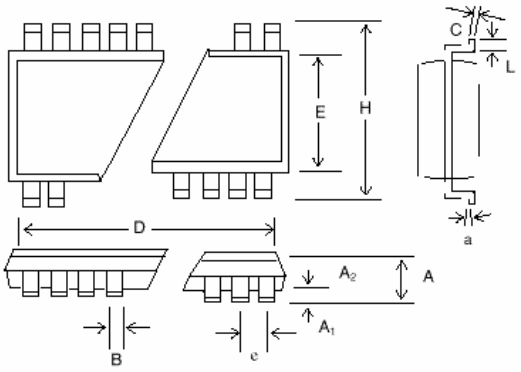
514: packages made in '2005, week 14

G: assembly house ID; O means OSE, G means GR

A: Internal use code

B: IC revision

11. PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0°	5°	8°	0°	5°	8°

Important Notice

Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

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