W83194BR-903 & W83194BG-903
STEPLESS VIA PT/PM MAIN CLOCK GENERATOR

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W83194BR-903 Datasheet Revision History

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
1	n.a.			n.a.	All of the versions before 0.50 are for internal use.
2	n.a.	09/07/03	0.5	n.a.	First published preliminary version.
3	6	10/28/03	0.6	n.a.	Modify frequency table
4	7,9,19	12/18/03	0.7	n.a.	Correction IC version, correction some description and default value
5		05/02/06	1.0	1.0	Update on Web and add lead free part
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9					
10					

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1. GENERAL DESCRIPTION

The W83194BR-903 is a Clock Synthesizer for VIA PT880/PM880 chipset. W83194BR-903 provides all clocks required for high-speed microprocessor and provides step-less frequency programming and 32 different frequencies of CPU, PCI, and AGP clocks setting, support two 25MHz clock outputs, all clocks are externally selectable with smooth transitions.

The W83194BR-903 provides I^2C serial bus interface to program the registers to enable or disable each clock outputs and provides -0.5% and +/-0.25% center type spread spectrum or programmable S.S.T. scale to reduce EMI.

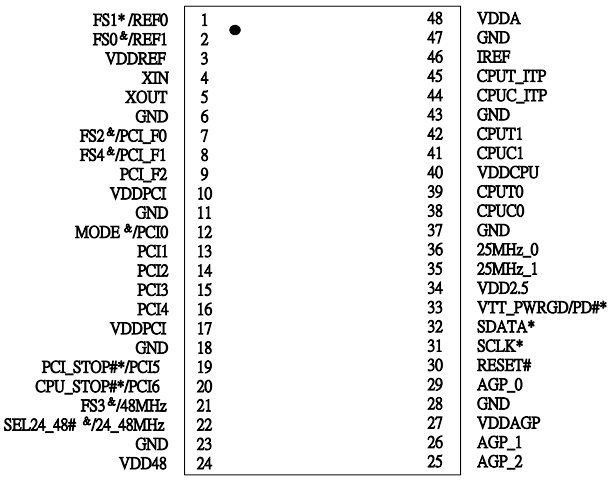
The W83194BR-903 also has watchdog timer and reset output pin to support auto-reset when systems hanging caused by improper frequency setting.

The W83194BR-903 accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply.

2. PRODUCT FEATURES

- 3 0.7V current-mode Differential pairs clock outputs
- 2 2.5V 25MHz clock outputs
- 3 AGP clock outputs
- 10 PCI synchronous clocks
- 1 24_48Mhz clock output for super I/O.
- 1 48 MHz clock output for USB.
- 2 14.318MHz REF clock outputs.
- AGP/PCI clock out supports synchronous and asynchronous mode
- Smooth frequency switch with selections from 100 to 400MHz
- Step-less frequency programming
- I^2C 2-Wire serial interface and support byte read/write and block read/write.
- -0.5% and +/- 0.25% center type spread spectrum
- Programmable S.S.T. scale to reduce EMI
- Programmable registers to enable/stop each output and select modes
- Programmable clock outputs Slew rate control and Skew control
- Watch Dog Timer and RESET# output pins
- 48-pin SSOP package

3. PIN CONFIGURATION

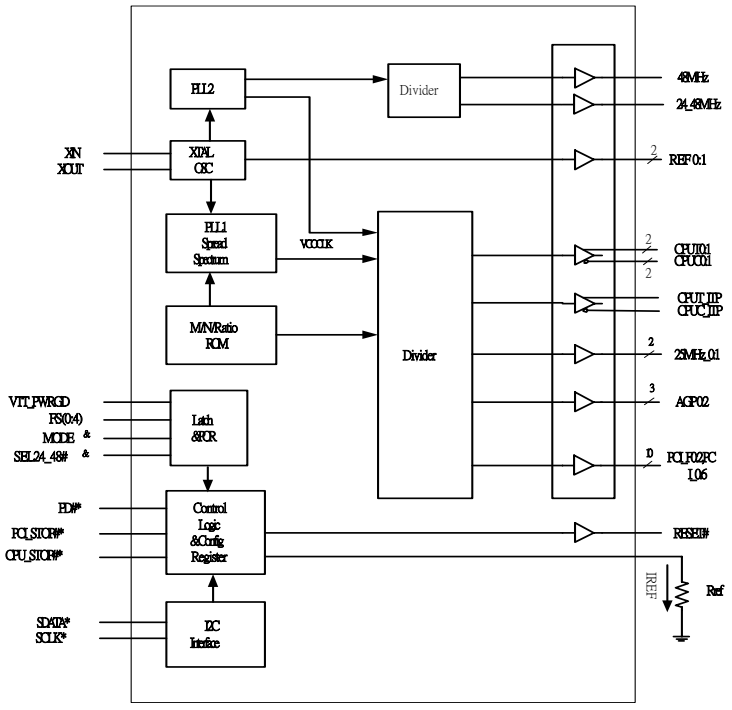


#: Active low

*: Internal pull up resistor 120K to VDD

&: Internal Pull-down resistor 120K to GND

4. BLOCK DIAGRAM



5. PIN DESCRIPTION

BUFFER TYPE SYMBOL	DESCRIPTION
IN	Input
IN_{tp120k}	Latched input at power up, internal 120kΩ pull up.
IN_{td120k}	Latched input at power up, internal 120kΩ pull down.
OUT	Output
OD	Open Drain
I/OD	Bi-directional Pin, Open Drain.
#	Active Low
*	Internal 120kΩ pull-up
&	Internal 120 kΩ pull-down

5.1 Crystal I/O

PIN	PIN NAME	TYPE	DESCRIPTION
4	XIN	IN	Crystal input with internal loading capacitors (18pF) and feedback resistors.
5	XOUT	OUT	Crystal output at 14.318MHz nominally with internal loading capacitors (18pF).

5.2 CPU, AGP, and PCI Clock Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
42,39,41,38	CPUT [0:1] CPUC [0:1]	OUT	Low skew (< 250ps) differential clock outputs for host frequencies of CPU
45,44	CPUT_ITP, CPUC_ITP	OUT	Differential clock outputs for host frequencies of CPU
29,26,25	AGP0: 2	OUT	3.3V AGP clock outputs.
7	PCI_F0	OUT	3.3V PCI free running clock output.
	FS2&	IN_{td120k}	Latched input for FS2 at initial power up for H/W selecting the output frequency. This is internal 120K pull down.
8	PCI_F1	OUT	3.3V PCI free running clock output.
	FS4&	IN_{td120k}	Latched input for FS4 at initial power up for H/W selecting the output frequency, This is internal 120K pull down.
12	PCI0	OUT	3.3V PCI clock output.
	MODE&	IN_{td120k}	Latched input for pin 19,20 at initial power up selecting the 0=PCI5, PCI6 clock output, 1=PCI_STOP and CPU _STOP control pin. This is internal 120KΩ pull down.

CPU, AGP, and PCI Clock Outputs, continued.

PIN	PIN NAME	TYPE	DESCRIPTION
9	PCI_F2	OUT	3.3V PCI free running clock output.
19	PCI5	OUT	3.3V PCI clock output. Select by pin 12 MODE& power up initial =0.
	PCI_STOP#*	IN_{tp120k}	Active low, Stop all PCI clock output besides the free running clocks. Select by pin 12 MODE& power up initial =1.
20	PCI6	OUT	3.3V PCI clock output. Select by pin 12 MODE& power up initial =0.
	CPU_STOP#*	IN_{tp120k}	Active low, Stop all CPU clock outputs. Select by pin 12 MODE& power up initial =1.
13,14,15,16	PCI [1:4]	OUT	Low skew (< 250ps) PCI clock outputs.

5.3 Fixed Frequency Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
1	REF0	OUT	14.318MHz output.
	FS1*	IN_{tp120k}	Latched input for FS1 at initial power up for H/W selecting the output frequency. This is internal 120K pull up.
2	REF1	OUT	14.318MHz output.
	FS0&	IN_{td120k}	Latched input for FS0 at initial power up for H/W selecting the output frequency. This is internal 120K pull down.
21	48MHz	OUT	48MHz clock output for USB.
	FS3&	IN_{td120k}	Latched input for FS3 at initial power up for H/W selecting the output frequency. This is internal 120K pull down.
22	24_48MHz	OUT	24MHz or 48MHz(default) clock output, In power on reset period, it is a hardware-latched pin, and it can be R/W by I2C control after power on reset period. Select by register 5 bit 7.
	SEL24_48#&	IN_{td120k}	Latched input for 24MHz or 48MHz select pin. This is internal 120K pull down default 48MHz. In power on reset period, it is a hardware-latched pin, and it can be R/W by I2C control after power on reset period. Select by register 5 bit 7.
36,35	25MHz_[0:1]	OUT	25MHz 2.5V push pull clock output.

5.4 I^2C Control Interface

PIN	PIN NAME	TYPE	DESCRIPTION
32	SDATA*	I/OD	Serial data of I^2C 2-wire control interface with internal 120K pull-up resistor.
31	SCLK*	IN_{tp120k}	Serial clock of I^2C 2-wire control interface with internal 120K pull-up resistor.

5.5 Power Management Pins

PIN	PIN NAME	TYPE	DESCRIPTION
33	VTT_PWRGD	IN	Power good input signal is power on trapping with HIGH active. This 3.3V input is level sensitive strobe used to determine FS [4:0]. This pin is HIGH active.
	PD#*	IN_{tp120k}	Power Down Function. This is power down pin, low active (PD#). Internal 120K pull up
46	IREF	OUT	Deciding the reference current for the CPUCLK pairs. The pin was connected to the precision resistor tied to ground to decide the appropriate current.
30	RESET#	OD	System reset signal when the watchdog is time out. This pin will generate 250ms low phase when the watchdog timer is timeout.

5.6 IREF selects Function

BOARD TARGET TRACE/TERM Z	REFERENCE R, IREF = ADD/(3*RR)	OUTPUT CURRENT	VOH @ Z
50 Ω	Rr =221 1% IREF = 5.00mA	Ioh=4*IREF	1.0V @ 50
50 Ω	Rr =475 1% IREF = 2.32mA	Ioh=6*IREF	0.7V @ 50

5.7 Power Pins

PIN	PIN NAME	TYPE	DESCRIPTION
3	VDDREF	PWR	3.3V power supply for REF.
10,17	VDDPCI	PWR	3.3V power supply for PCI.
27	VDDAGP	PWR	3.3V power supply for AGP.
40	VDDCPU	PWR	3.3V power supply for CPU.
24	VDD48	PWR	3.3 power supply for 48MHz.
34	VDD2.5	PWR	2.5V power supply for 25MHz.
48	VDDA	PWR	3.3V power for Analog power
6,11,18,23,28, 37,43,47	GND	PWR	Ground pin

6. FREQUENCY SELECTION BY HARDWARE OR SOFTWARE

This frequency table is used at power on latched FS [4:0] value or software programming at SSEL [4:0] (Register 0 bit 7 ~ 3).

FS4	FS3	FS2	FS1	FS0	CPU (MHZ)	3V66 (MHZ)	PCI (MHZ)
0	0	0	0	0	100.00	66.67	33.33
0	0	0	0	1	200.01	66.67	33.33
0	0	0	1	0	133.34	66.67	33.33
0	0	1	0	0	200.01	66.67	33.33
0	0	1	0	1	400.01	66.67	33.33
0	0	1	1	0	266.68	66.67	33.33
0	1	0	0	0	101.1	67.34	33.67
0	1	0	0	1	202.2	67.34	33.67
0	1	0	1	0	134.68	67.34	33.67
1	0	0	0	0	100.00	66.67	33.33
1	0	0	0	1	200.01	66.67	33.33
1	0	0	1	0	133.34	66.67	33.33
1	0	1	0	0	200.01	66.67	33.33
1	0	1	0	1	400.01	66.67	33.33
1	0	1	1	0	266.68	66.67	33.33
1	1	0	0	0	105.04	70.02	35.01
1	1	0	0	1	210.07	70.02	35.01
1	1	0	1	0	140.05	70.02	35.01

7. I²C CONTROL AND STATUS REGISTERS

7.1 Register 0: Frequency Select (Default = 10h)

BIT	NAME	PWD	DESCRIPTION
7	SSEL [4]	0	Frequency selection by software via I²C
6	SSEL [3]	0	
5	SSEL [2]	0	
4	SSEL [1]	1	
3	SSEL [0]	0	
2	EN_SSEL	0	Enable software program FS [4:0]. 0 = Select frequency by hardware. 1= Select frequency by software I²C - Bit 7~ 3.
1	EN_SPSP	0	Enable Spread Spectrum in the frequency table. 0 = Normal 1 = Spread Spectrum Enabled
0	EN_SAFE_FREQ	0	Enable reload safe frequency when the watchdog is timeout. 0 = reload the FS [4:0] latched pins when watchdog time out. 1 = reload the safe frequency bit defined at Register 5 bit 4~0.

7.2 Register 1: CPU Clock (1 = Enable, 0 = Stopped) (Default: E2h)

BIT	PIN NO	PWD	DESCRIPTION
7	45,44	1	CPUT_IPT/CPUC_IPT output control.
6	42,41	1	CPUT1 / C1 output control.
5	39,38	1	CPUT0 / C0 output control.
4	-	X	Power on latched value of FS4 pin. Default: 0 (Read only)
3	-	X	Power on latched value of FS3 pin. Default: 0 (Read only)
2	-	X	Power on latched value of FS2 pin. Default: 0 (Read only)
1	-	X	Power on latched value of FS1 pin. Default: 1 (Read only)
0	-	X	Power on latched value of FS0 pin. Default: 0 (Read only)

7.3 Register 2: PCI Clock (1 = Enable, 0 = Stopped) (Default: FFh)

BIT	PIN NO	PWD	DESCRIPTION
7	9	1	PCI_F2 output control.
6	8	1	PCI_F1 output control.
5	7	1	PCI_F0 output control.
4	Reserve	1	Reserved
3	20	1	PCI6 output control.
2	19	1	PCI5 output control.
1	16	1	PCI4 output control.
0	15	1	PCI3 output control.

7.4 Register 3: PCI, AGP Clock (1 = Enable, 0 = Stopped) (Default: FFh)

BIT	PIN NO	PWD	DESCRIPTION
7	14	1	PCI2 output control.
6	13	1	PCI1 output control.
5	12	1	PCI0 output control.
4	-	1	Don't modify it
3	25	1	AGP_2 output control.
2	26	1	AGP_1 output control.
1	29	1	AGP_0 output control.
0	-	1	Don't modify it

7.5 Register 4: 24_48MHz, 48MHz, REF, 25MHz Control (1 = Enable, 0 = Stopped) (Default: BFh)

BIT	PIN NO	PWD	DESCRIPTION
7	22	1	24_48MHz output control.
6	-	0	Reserved
5	21	1	48MHz output control.
4	-	1	Reserved
3	2	1	REF1 output control.
2	1	1	REF0 output control.
1	35	1	25MHz_1 output control.
0	36	1	25MHz_0 output control.

7.6 Register 5: Watchdog Control (Default: 02h)

BIT	NAME	PWD	DESCRIPTION
7	SEL24_48	X	24 / 48 MHz output selection, 1: 24 MHz.0: 48 MHz. (Default) Default value follow hardware trapping data on SEL24_48# pin.
6	EN_WD	0	Program this bit => 1: Enable Watchdog Timer feature. 0: Disable Watchdog Timer feature. Read-back this bit => During timer count down the bit read back to 1. If count to zero, this bit read back to 0.
5	WD_TIMEOUT	0	Read Back only, Timeout Flag, This bit is Read Only. 1: Watchdog has ever started and counts to zero. 0: Watchdog is restarted and counting.
4	SAF_FREQ [4]	0	These bits will be reloaded in Reg-0 to select frequency table. As the watchdog is timeout and EN_SAFE_FREQ=1.
3	SAF_FREQ [3]	0	
2	SAF_FREQ [2]	0	
1	SAF_FREQ [1]	1	
0	SAF_FREQ [0]	0	

7.7 Register 6: Reserved (Default: 50h) (Read Only)

BIT	NAME	PWD	DESCRIPTION
7	Reserved	0	Reserved
6	Reserved	1	
5	Reserved	0	Reserved
4	Reserved	1	
3	Reserved	0	Reserved
2	Reserved	0	
1	Reserved	0	Reserved
0	Reserved	0	

7.8 Register 7: Winbond Chip ID (Default: 70h) (Read Only)

BIT	NAME	PWD	DESCRIPTION
7	CHPI_ID [7]	0	Winbond Chip ID. W83194BR-903 (SA5870)
6	CHPI_ID [6]	1	Winbond Chip ID.
5	CHPI_ID [5]	1	Winbond Chip ID.
4	CHPI_ID [4]	1	Winbond Chip ID.
3	CHPI_ID [3]	0	Winbond Chip ID.
2	CHPI_ID [2]	0	Winbond Chip ID.
1	CHPI_ID [1]	0	Winbond Chip ID.
0	CHPI_ID [0]	0	Winbond Chip ID.

7.9 Register 8: M/N Program (Default: 90h)

BIT	NAME	PWD	DESCRIPTION
7	N_DIV [8]	1	Programmable N divisor value. Bit 7 ~0 are defined in the Register 9.
6	M_DIV [6]	0	Programmable M divisor value.
5	M_DIV [5]	0	
4	M_DIV [4]	1	
3	M_DIV [3]	0	
2	M_DIV [2]	0	
1	M_DIV [1]	0	
0	M_DIV [0]	0	

7.10 Register 9: M/N Program (Default: 7Ah)

BIT	NAME	PWD	DESCRIPTION
7	N_DIV [7]	0	Programmable N divisor value bit 7 ~0. The bit 8 is defined in Register 8.
6	N_DIV [6]	1	
5	N_DIV [5]	1	
4	N_DIV [4]	1	
3	N_DIV [3]	1	
2	N_DIV [2]	0	
1	N_DIV [1]	1	
0	N_DIV [0]	0	

7.11 Register 10: M/N Program (Default: BBh)

BIT	NAME	PWD	DESCRIPTION
7	N_DIV [9]	1	Programmable N divisor bit 9.
6	N3<6>	0	Programmable N3 divisor bit 6 ~0 for programmable 25M clocks.
5	N3<5>	1	M3=10000 (Fix)
4	N3<4>	1	Frequency range: 21.7M ~ 28.8M
3	N3<3>	1	Resolution: 56K
2	N3<2>	0	
1	N3<1>	1	
0	N3<0>	1	

7.12 Register 11: Spread Spectrum Programming (Default: 0Bh)

BIT	NAME	PWD	DESCRIPTION
7	SP_UP [3]	0	Spread Spectrum Up Counter bit 3 ~ bit 0.
6	SP_UP [2]	0	
5	SP_UP [1]	0	
4	SP_UP [0]	0	
3	SP_DOWN [3]	1	Spread Spectrum Down Counter bit 3 ~ bit 0
2	SP_DOWN [2]	0	2's complement representation.
1	SP_DOWN [1]	1	Ex: 1 -> 1111; 2 -> 1110; 7 -> 1001; 8 -> 1000
0	SP_DOWN [0]	1	

7.13 Register 12: Divisor and Step-less Enable Control (Default: FBh)

BIT	NAME	PWD	DESCRIPTION
7	Reserved	1	Reserved
6	DS9	1	Define the AGP divider ratio
5	DS5	1	Table-2 integrate the all divider configuration
4	Reserved	1	Reserved
3	Reserved	1	
2	DS2	0	Define the CPU divider ratio
1	DS1	1	Refer to Table-2
0	DS0	1	

Table-2 CPU, AGP, PCI divider ratio selection Table

LSB / MSB		AGP		CPU			
		Bit5		Bit1, 0			
		0	1	00	01	10	11
Bit2/ Bit9	0	Div6	Div7	Div2	Div3	Div4	Div6
	1	Div10	Div12	Div8	Div8	Div8	Div8

7.14 Register 13: Divisor and Step-less Enable Control (Default: 0Fh)

BIT	NAME	PWD	DESCRIPTION
7	EN_MN_PROG	0	0: Output frequency depend on frequency table 1: Program all clock frequency by changing M/N value The equation is **VCO =14.318MHz*(N+4)/ M**. Once the watchdog timer timeout, the bit will be clear. Then the frequency will be decided by hardware default FS<4:0> or desired frequency select SAF_FREQ [4:0] depend on EN_SAFE_FREQ (Reg0 - bit 0).
6	Reserved	0	Reserved
5	Reserved	0	Reserved
4	Reserved	0	Reserved
3	IVAL<3>	1	Charge pump current selection
2	IVAL<2>	1	
1	IVAL<1>	1	
0	IVAL<0>	1	

7.15 Register 14: Control (Default: 0Ah)

BIT	NAME	PWD	DESCRIPTION
7	CPUT_DRI	0	CPUT output state in during POWER DOWN or Stop mode assertion. 1: Driven (2*Iref), 0: Tristate (Floating) CPUC always tri-state (floating) in power down Assertion.
6	Reserved	0	Reserved
5	SPCNT [5]	0	Spread Spectrum Programmable time, the resolution is 280ns. Default period is 11.8us
4	SPCNT [4]	0	
3	SPCNT [3]	1	
2	SPCNT [2]	0	
1	SPCNT [1]	1	
0	SPCNT [0]	0	

7.16 Register 15: SST & Skew Control (Default: 2Ch)

BIT	NAME	PWD	DESCRIPTION
7	INV_CPU	0	Invert the CPU phase, 0: Default, 1: Inverse
6	Reserved	0	Reserved
5	SPSP_TYPE	1	Spread spectrum implementation method 1: Pendulum type, 0: Original
4	SPSP1	0	Spread Spectrum type select. 00: Down 1% 01: Down 0.5% 10: Center +/- 0.5% 11: Center +/- 0.25%
3	SPSP0	1	
2	ASKEW [2]	1	CPU to AGP skew control, Skew resolution is 340ps Expand the skew direction is same as CPU_AGP_SKEW [2:0] setting
1	ASKEW [1]	0	
0	ASKEW [0]	0	

7.17 Register 16: Skew Control (Default: 24h)

BIT	NAME	PWD	DESCRIPTION
7	INV_AGP	0	Invert the AGP phase, 0: Default, 1: Inverse
6	INV_PCI	0	Invert the PCI phase, 0: Default, 1: Inverse
5	Reserved	1	Reserved
4	Reserved	0	
3	Reserved	0	
2	PSKEW [2]	1	CPU to PCI skew control, Skew resolution is 340ps Expand the skew direction is same as CPU_PCI_SKEW [2:0] setting
1	PSKEW [1]	0	
0	PSKEW [0]	0	

7.18 Register 17: Slew rate Control (Default: 00h)

BIT	NAME	PWD	DESCRIPTION
7	PCI_F2_S2	0	PCI_F2 slew rate control 11: Strong, 00: Weak, 10/01: Normal
6	PCI_F2_S1	0	
5	PCI_F0_S2	0	PCI_F1 / PCI_F0 slew rate control 11: Strong, 00: Weak, 10/01: Normal
4	PCI_F0_S1	0	
3	AGP_2_S2	0	AGP2 slew rate control 11: Strong, 00: Weak, 10/01: Normal
2	AGP_2_S1	0	
1	AGP_10_S2	0	AGP_1 /AGP_0 slew rate control 11: Strong, 00: Weak, 10/01: Normal
0	AGP_10_S1	0	

7.19 Register 18: Slew rate Control (Default: 00h)

BIT	NAME	PWD	DESCRIPTION
7	PCI_65_S2	0	PCI6, 5 slew rate control
6	PCI_65_S1	0	11: Strong, 00: Weak, 10/01: Normal
5	PCI_42_S2	0	PCI4, 3,2 slew rate control
4	PCI_42_S1	0	11: Strong, 00: Weak, 10/01: Normal
3	PCI_10_S2	0	PCI1, 0 slew rate control
2	PCI_10_S1	0	11: Strong, 00: Weak, 10/01: Normal
1	REF_S2	0	REF0, 1 slew rate control
0	REF_S1	0	11: Strong, 00: Weak, 10/01: Normal

7.20 Register 19: Slew rate Control (Default: D2h)

BIT	NAME	PWD	DESCRIPTION
7	CPU1STOP_EN	1	Stop CPU1 clocks, 1: Enable stop feature, 0: Disable
6	CPU0STOP_EN	1	Stop CPU0 clocks, 1: Enable stop feature, 0: Disable
5	25MHz_S2	0	25MHz_1,0 slew rate control
4	25MHz_S1	1	11: Strong, 00: Weak, 10/01: Normal
3	INV_48MHz	0	Invert the 48MHz phase, 0: In phase with 24_48MHz 1: 180 degrees out of phase
2	48MHz_S2	0	48MHz/24_48MHz slew rate control
1	48MHz_S1	1	11: Strong, 00: Weak, 10/01: Normal
0	MODE	X	Pin 19,20 Mode selection 1: PCI_STOP, CPU_STOP Control pin 0: PCI5, PCI6 (Default) Default value follow hardware trapping data on MODE$^{\&}$/PCI0 pin.

7.21 Register 20: Watch dog timer (Default: 08h)

BIT	NAME	PWD	DESCRIPTION
7	SRCF1	0	SRC frequency select, 00/01: 25MHz(Default), 10: 100mhZ, 11: 200MHz
6	WD_TIME [6]	0	Setting the down count depth. One bit resolution represents 250ms. Default time depth is 8*250ms = 2.0 second. If the watchdog timer is counting, this register will return present down count value
5	WD_TIME [5]	0	
4	WD_TIME [4]	0	
3	WD_TIME [3]	1	
2	WD_TIME [2]	0	
1	WD_TIME [1]	0	
0	WD_TIME [0]	0	

7.22 Register21: Fix Mode Control (Default: 00h)

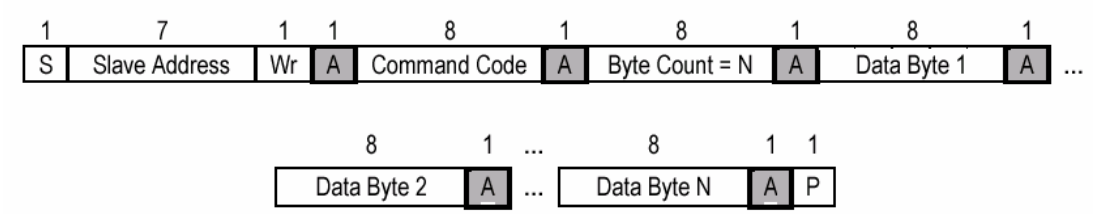
BIT	NAME	PWD	DESCRIPTION
7	Tri-state	0	Tri-state all output if set 1
6	Reserved	0	Don't modify it
5	Reserved	0	Don't modify it
4	FIX_SEL	0	AGP output frequency select mode 0: Output frequency according to frequency selection table 1: Output frequency according to FIX frequency Reg21 bit 0~2
3	SRCF0	0	SRC frequency select
2	ASEL_2	0	Asynchronous AGP/PCI frequency table selection ASEL_<2:0> 001: 66 / 33M 010: 75.43 / 37.7M 011: 88 / 44M 100: 88 / 44M 101: 66 / 33M 110: 75.43 / 33M 111: 88 / 33M 000: Clock from PLL1
1	ASEL_1	0	
0	ASEL_0	0	

8. ACCESS INTERFACE

The W83194BR-903 provides I^{2}C Serial Bus for microprocessor to read/write internal registers. In the W83194BR-903 is provided Block Read/Block Write and Byte-Data Read/Write protocol. The I^{2}C address is defined at 0xD2.

Block Read and Block Write Protocol

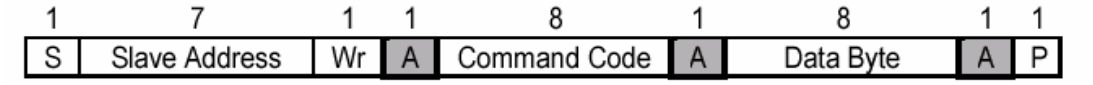
8.1 Block Write protocol



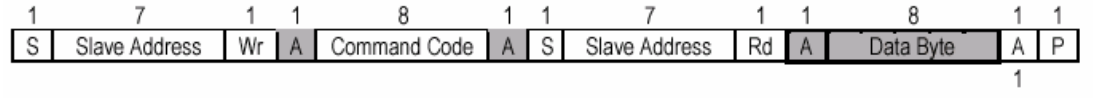
8.2 Block Read protocol

In block mode, the command code must filled 8'h00

8.3 Byte Write protocol



8.4 Byte Read protocol



9. SPECIFICATIONS

9.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Subjection to maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or VDD).

PARAMETER	RATING
Absolute 3.3V Core Supply Voltage	-0.5V to +4.6V
Absolute 3.3V I/O Supple Voltage	- 0.5 V to + 4.6 V
Operating 3.3V Core Supply Voltage	3.135V to 3.465V
Operating 3.3V I/O Supple Voltage	3.135V to 3.465V
Storage Temperature	- 65°C to + 150°C
Ambient Temperature	- 55°C to + 125°C
Operating Temperature	0°C to + 70°C
Input ESD protection (Human body model)	2000V

9.2 General Operating Characteristics

VDDA=VDDAGP=VDDCPU=VDDREF=VDDPCI= 3.3V ± 5 %, TA = 0℃ to +70℃, CI=10pF					
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Input Low Voltage	V_{IL}		0.8	V_{dc}	
Input High Voltage	V_{IH}	2.0		V_{dc}	
Output Low Voltage	V_{OL}		0.4	V_{dc}	All outputs using 3.3V power
Output High Voltage	V_{OH}	2.4		V_{dc}	All outputs using 3.3V power
Operating Supply Current	I_{dd}		350	mA	CPU = 100 to 400 MHz PCI = 33.3 Mhz with load
Input pin capacitance	Cin		5	pF	
Output pin capacitance	Cout		6	pF	
Input pin inductance	Lin		7	nH	

9.3 Skew Group timing clock

VDDA=VDDAGP=VDDCPU=VDDREF=VDDPCI = 3.3V ± 5 %, TA = 0℃ to +70℃, Cl=10pF					
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**	**TEST CONDITIONS**
AGP to PCI Skew	1.5	2.6	3.5	ns	Measured at 1.5V
CPU to CPU Skew			200	ps	Crossing point
AGP to AGP Skew			250	ps	Measured at 1.5V
PCI to PCI Skew			500	ps	Measured at 1.5V
48MHz to 48MHz Skew			1000	ps	Measured at 1.5V
REF to REF Skew			500	ps	Measured at 1.5V

9.4 CPU 0.7V Electrical Characteristics

*VDDA=VDDCPU= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load Rs=33, Rp=49.9 Cl=10pF, Vr=475, IREF=2.32mA, Ioh=6*IREF*				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	175	700	ps	100 to 200 Mhz
Fall Time	175	700	ps	100 to 200Mhz
Absolute crossing point Voltages	250	550	mV	100 to 200Mhz
Cycle to Cycle jitter		150	ps	100 to 200Mhz
Duty Cycle	45	55	%	100 to 200Mhz

9.5 AGP Electrical Characteristics

VDDAGP= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	500	2000	ps	Measure from 0.4V to 2.4V
Fall Time	500	2000	ps	Measure from 2.4V to 0.4V
Cycle to Cycle jitter		250	ps	Measure 1.5V point
Duty Cycle	45	55	%	
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

9.6 PCI Electrical Characteristics

VDDPCI= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	500	2000	ps	Measure from 0.4V to 2.4V
Fall Time	500	2000	ps	Measure from 2.4V to 0.4V
Cycle to Cycle jitter		250	ps	Measure 1.5V point
Duty Cycle	45	55	%	
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

9.7 24M, 48M Electrical Characteristics

VDD48= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	500	2000	ps	Measure from 0.4V to 2.4V
Fall Time	500	2000	ps	Measure from 2.4V to 0.4V
Long term jitter		500	ps	Measure 1.5V point
Duty Cycle	45	55	%	
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

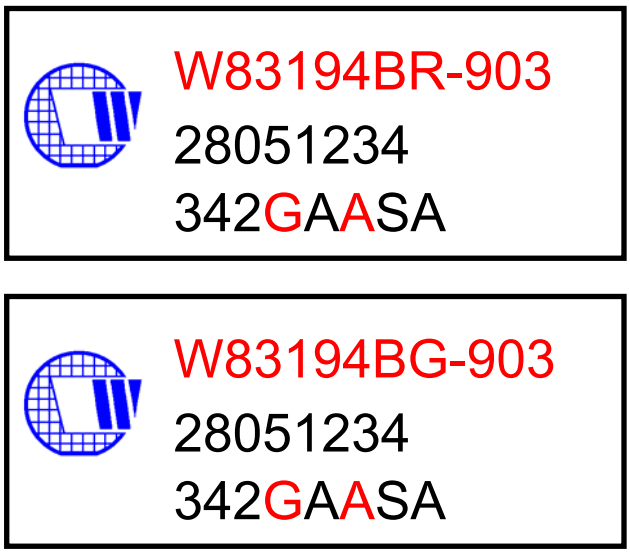
9.8 REF Electrical Characteristics

VDDREF= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	1000	4000	ps	Measure from 0.4V to 2.4V
Fall Time	1000	4000	ps	Measure from 2.4V to 0.4V
Cycle to Cycle jitter		1000	ps	Measure 1.5V point
Duty Cycle	45	55	%	
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

10. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83194BR-903	48 PIN SSOP	Commercial, 0°C to +70°C
W83194BG-903	48 PIN SSOP (Lead free part)	Commercial, 0°C to +70°C

11. HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number:

Normal:W83194BR-903, Lead free part:W83194BG-903

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 342 G A A SA

320: packages made in '2003, week 42

G: assembly house ID; O means OSE, G means GR

A: Internal use code

A: IC revision

SA: Internal use code

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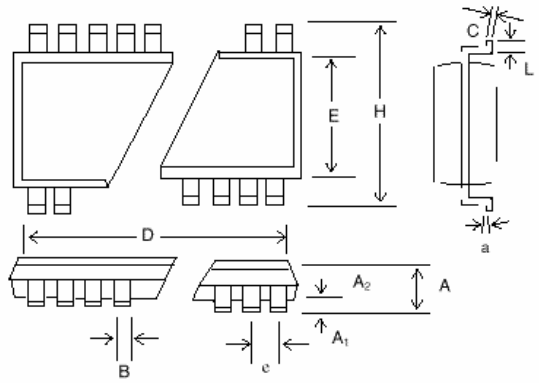
12. PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0°	5°	8°	0°	5°	8°

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