Winbond Electronics Corp.

166MHZ CLOCK FOR SIS CHIPSET

1.0 GENERAL DESCRIPTION

The W83194BR-730 is a Clock Synthesizer which provides all clocks required for high-speed RISC or CISC microprocessor such as AMD K7. W83194BR-730 provides 64 CPU/PCI frequencies which are selectable with smooth transitions by hardware or software. W83194BR-730 also provides 13 SDRAM clocks.

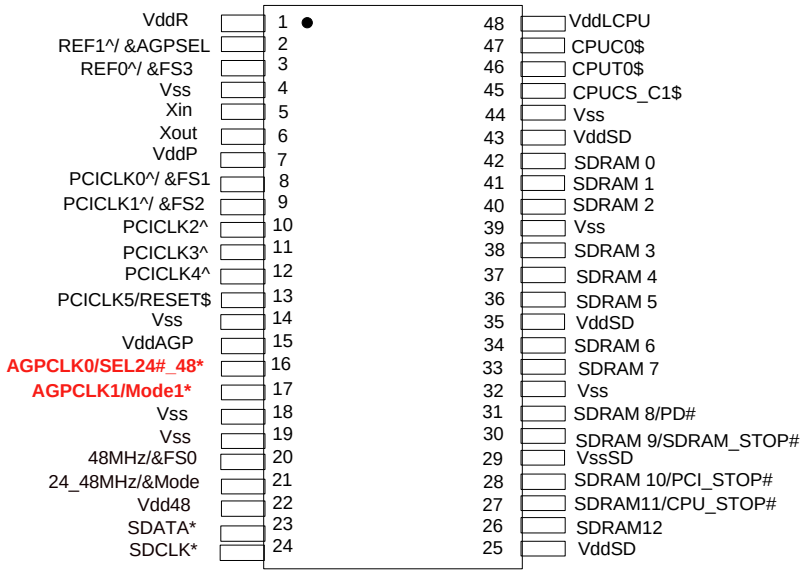
The W83194BR-730 provides step-less frequency programming by controlling the VCO freq. and the programmable PCI clock output divisor ratio. A watch dog timer is quipped and when time out, the RESET# pin will output 4ms pulse signal.

The W83194BR-730 accepts a 14.318 MHz reference crystal as its input. Spread spectrum built in at 0~-0.5% or ±0.25% to reduce EMI. Programmable stopping individual clock outputs and frequency selection through I^2C interface. The device meets the Pentium power-up stabilization, which requires CPU and PCI clocks be stable within 2 ms after power-up. Using dual function pin for the slots(ISA, PCI, CPU, DIMM) is not recommend.

2.0 PRODUCT FEATURES

- Supports AMD CPU with I^2C.
- 3 CPU clocks (one free-running CPU clock)
- 13 SDRAM clocks for 3 DIMMs
- 6 PCI synchronous clocks
- 2 AGP clocks
- 2 REF clocks as 14.318MHz outputs
- < 250ps skew among CPU and SDRAM clocks
- < 250ps skew among PCI clocks
- Skew from CPU(earlier) to PCI clock 1 to 4ns, center 2.6ns.
- Smooth frequency switch with selections from 66 MHz to 200 MHz CPU
- Stepless frequency programming by controlling the VCO freq. and the clock output divisor ratio
- Programmable skew for CPU to SDRAM and CPU to AGP clock outputs
- I^2C 2-Wire serial interface and I^2C read back
- ±0.25% or 0~-0.5% spread spectrum function to reduce EMI
- Programmable registers to enable/stop each output and select modes
- MODE pin for power Management and RESET# out when system hang
- One 48 MHz for USB & one 24_48 MHz for super I/O
- 48-pin SSOP package

3.0 PIN CONFIGURATION



*** : 120K pull-up**
&: 120K pull-down
^ : 2X driving stength
$: Open-drain
#: Active LOW

4.0 PIN DESCRIPTION

IN - Input

OUT - Output

I/O - Bi-directional Pin

- Active Low

* - Internal 250kΩ pull-up

4.1 Crystal I/O

SYMBOL	PIN	I/O	FUNCTION
Xin	5	IN	Crystal input with internal loading capacitors and feedback resistors.
Xout	6	OUT	Crystal output at 14.318MHz nominally.

4.2 CPU, SDRAM, PCI, AGP Clock Outputs

SYMBOL	PIN	I/O	FUNCTION
CPUC0$ CPUT0$	47,46	OD	Open drain output clock for host frequencies CPU. Powered by VddLCPU. Stopped if CPU_STOP# is low.
CPUCS_C1$	45	OD	Open drain clock for chipset. Stopped if CPU_STOP# is low and Register1 bit7=0. The same phase as CPUC0$.
SDRAM [0:7],12	42,41,40,38,37 ,36,34,33, 26	OUT	SDRAM clock outputs. The same phase as CPUC0$
SDRAM 8/PD#	31	OUT	Pin21 &Mode=0, SDRAM clock outputs. Pin21 &Mode=1, PD# input
SDRAM9/ SDRAM_STOP#	30	OUT	Pin21 &Mode=0, SDRAM clock outputs. Pin21 &Mode=1, SDRAM_STOP# input
SDRAM 10/ PCI_STOP#	28	OUT	Pin21 &Mode=0, SDRAM clock outputs. Pin21 &Mode=1, PCI_STOP# input
SDRAM 11/ CPU_STOP#	27	OUT	Pin21 &Mode=0, SDRAM clock outputs. Pin21 &Mode=1, CPU_STOP# input
PCICLK0^/&FS1	8	I/O	Low skew (< 250ps) PCI clock outputs. Latched input for FS1 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
PCICLK1^/&FS2	9	I/O	Low skew (< 250ps) PCI clock outputs. Latched input for FS2 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
PCICLK [2:4]^	10,11,12	I/O	Low skew (< 250ps) PCI clock outputs. Latched Input.
PCICLK5/ RESET$	13	I/O	PCI clock during normal operation. (pin 17 MODE1=1) If pin17 MODE1=0, RESET# (open drain, 4ms low active pulse when Watch Dog time out)
AGPCLK0/ SEL24#_48*	16	I/O	Low skew (< 250ps) AGP clock output. Latched Input. SEL24#_48*=1, Pin 21 is 24MHz; SEL24_48*=0, Pin21 is 48MHz
AGPCLK1/ Mode1*	17	OUT	AGP clock outputs Latched Input. Mode1*=1, Pin 13 is PCICLK; Mode1*=0, Pin13 is RESET#

4.3 I²C Control Interface

SYMBOL	PIN	I/O	FUNCTION
SDATA*	23	I/O	Serial data of I²C 2-wire control interface
SDCLK*	24	IN	Serial clock of I²C 2-wire control interface

4.4 Fixed Frequency Outputs

SYMBOL	PIN	I/O	FUNCTION
REF0 ^/ &AGPSEL	2	I/O	14.318MHz reference clock. This REF output is the atched input for &AGPSEL at initial power up for H/W selecting the output frequency of AGP clocks.
REF1 ^/ &FS3	3	I/O	14.318MHz reference clock. Latched input for FS3 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
24_48MHz / &Mode	21	I/O	24_48MHz output clock, selected by pin16. Latched Input. &Mode=0, Pin 27,28,30,31 are SDRAM clocks; &Mode=0, Pin27,28,29,31 areCPU_STOP#, SDRAM_STOP#, PCI_STOP#,PD#
48MHz / &FS0	20	I/O	48MHz output for USB during normal operation. Latched input for FS0 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.

4.5 Power Pins

SYMBOL	PIN	FUNCTION
VddR	1	Power supply for Ref [0:1] crystal and core logic.
VddAGP	15	Power supply for AGP output, 3.3V.
VddLCPU	48	Power supply for CPUC0,T0,CS_C1, either 2.5V or 3.3V.
VddP	7	Power supply for PCICLK[0:5], 3.3V.
VddSD	43,35,29,25	Power supply for SDRAM[0:12], and CPU PLL core, nominal 3.3V.
Vdd48	19	Power for 24 & 48MHz output buffers and fixed PLL core.
Vss	4,14,18,19,29,32,39,44	Circuit Ground.

5.0 FREQUENCY SELECTION BY HARDWARE

FS3	FS2	FS1	FS0	VCO (MHz)	CPU (MHz)	SDRAM (MHz)	PCI (MHz)	AGPSEL=0 (MHz)	AGPSEL=1 (MHz)
0	0	0	0	400	100	100	33.3	66.6	50
0	0	0	1	400	100	133	33.3	66.6	50
0	0	1	0	300	100	150	30.0	60	50
0	0	1	1	400	100	66.6	33.3	66.6	50
0	**1**	**0**	**0**	**336**	**112**	**112**	**33.6**	67.2	56
0	1	0	1	500	125	100	31.3	62.5	50
0	1	1	0	372	124	124	31	62	46.5
0	1	1	1	400	133	100	33.3	66.6	50
1	0	0	0	400	133	133	33.3	66.6	50
1	0	0	1	300	150	150	30	60	50
1	**0**	**1**	**0**	**333**	**111**	**166**	**33.3**	66.6	55.6
1	**0**	**1**	**1**	**330**	**110**	**165**	**33.0**	66	55
1	1	0	0	332	166	166	33.3	66.6	55.6
1	1	0	1	360	90	90	30	60	45
1	1	1	0	192	48	48	32	64	48
1	**1**	**1**	**1**	**192**	**45**	**60**	**30**	**60**	**45**

6.0 SERIAL CONTROL REGISTERS

The Pin column lists the affected pin number and the @PowerUp column gives the default state at true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the sequence described below (Register 0, Register 1, Register 2, ...) will be valid and acknowledged.

Bytes sequence order for I^2C controller :

Clock Address A(6:0) & R/W	**Ack**	**8 bits dummy Command code**	**Ack**	**8 bits dummy Byte count**	**Ack**	**Byte0,1,2... until Stop**

Set R/W to 1 when Read back", the data sequence is as follows :

Clock Address A(6:0) & R/W	**Ack**	**Byte 0**	**Ack**	**Byte 1**	**Ack**	**Byte2, 3, 4... until Stop**

FREQUENCY BY SOFTWARE

SSEL5	SSEL4	SSEL3	SSEL2	SSEL1	SSEL0	VCO (MHz)	CPU (MHz)	SDRAM (MHz)	PCI (MHz)	AGPSEL=0 (MHz)	AGPSEL=1 (MHz)
0	0	0	0	0	0	400	100	100	33.3	66.6	50
0	0	0	0	0	1	400	100	133	33.3	66.6	50
0	0	0	0	1	0	300	100	150	30.0	60	50
0	0	0	0	1	1	400	100	66.6	33.3	66.6	50
0	**0**	**0**	**1**	**0**	**0**	**336**	**112**	**112**	**33.6**	67.2	56
0	0	0	1	0	1	500	125	100	31.3	62.5	50
0	0	0	1	1	0	372	124	124	31	62	46.5
0	0	0	1	1	1	400	133	100	33.3	66.6	50
0	0	1	0	0	0	400	133	133	33.3	66.6	50
0	0	1	0	0	1	300	150	150	30	60	50
0	**0**	**1**	**0**	**1**	**0**	**333**	**111**	**166**	**33.3**	66.6	55.6
0	**0**	**1**	**0**	**1**	**1**	**330**	**110**	**165**	**33.0**	66	55
0	0	1	1	0	0	332	166	166	33.3	66.6	55.6
0	0	1	1	0	1	360	90	90	30	60	45
0	0	1	1	1	0	192	48	48	32	64	48
0	**0**	**1**	**1**	**1**	**1**	**192**	**45**	**60**	**30**	**60**	**45**
0	1	0	0	0	0	368	92	92	30.67	61.33	46
0	1	0	0	0	1	380	95	95	31.67	63.33	47.5
0	1	0	0	1	0	384	96	96	32	64	48
0	1	0	0	1	1	392	98	98	32.67	65.33	49
0	1	0	1	0	0	368	92	122.67	30.67	61.33	46
0	1	0	1	0	1	380	95	126.67	31.67	63.33	47.5
0	1	0	1	1	0	384	96	128	32	64	48
0	1	0	1	1	1	392	98	130.67	32.67	65.33	49
0	1	1	0	0	0	354	118	88.5	29.5	59	44.25
0	1	1	0	0	1	360	120	90	30	60	45
0	1	1	0	1	0	366	122	91.5	30.5	61	45.75
0	1	1	0	1	1	378	126	94.5	31.5	63	47.25
0	1	1	1	0	0	378	126	126	31.5	63	47.25
0	1	1	1	0	1	384	128	128	32	64	48
0	1	1	1	1	0	390	130	130	32.5	65	48.75
0	1	1	1	1	1	408	136	136	34	68	51

SSEL5	SSEL4	SSEL3	SSEL2	SSEL1	SSEL0	VCO (MHz)	CPU (MHz)	SDRAM (MHz)	PCI (MHz)	AGPSEL=0 (MHz)	AGPSEL=1 (MHz)
1	0	0	0	0	0	408	102	102	34	68	51
1	0	0	0	0	1	412	103	103	34.33	68.67	51.5
1	0	0	0	1	0	416	104	104	34.67	69.33	52
1	0	0	0	1	1	420	105	105	35	70	52.5
1	0	0	1	0	0	408	102	136	34	68	51
1	0	0	1	0	1	412	103	137.33	34.33	68.67	51.5
1	0	0	1	1	0	416	104	138.67	34.67	69.33	52
1	0	0	1	1	1	424	106	141.33	35.33	70.67	53
1	0	1	0	0	0	390	130	97.5	32.5	65	48.75
1	0	1	0	0	1	405	135	101.25	33.75	67.5	50.63
1	0	1	0	1	0	414	138	103.5	34.5	69	51.75
1	0	1	0	1	1	426	142	106.5	35.5	71	53.25
1	0	1	1	0	0	411	137	137	34.25	68.5	51.38
1	0	1	1	0	1	414	138	138	34.5	69	51.75
1	0	1	1	1	0	417	139	139	34.75	69.5	52.13
1	0	1	1	1	1	429	143	143	35.75	71.5	53.63
1	1	0	0	0	0	429	143	107.25	35.75	71.5	53.63
1	1	0	0	0	1	432	144	108	36	54	43.2
1	1	0	0	1	0	435	145	108.75	36.25	54.38	43.5
1	1	0	0	1	1	438	146	109.5	36.5	54.75	43.8
1	1	0	1	0	0	441	147	110.25	29.4	55.13	44.1
1	1	0	1	0	1	444	148	111	29.6	55.5	44.4
1	1	0	1	1	0	456	152	114	30.4	57	45.6
1	1	0	1	1	1	459	153	114.75	30.6	57.38	45.9
1	1	1	0	0	0	468	156	117	31.2	58.5	46.8
1	1	1	0	0	1	474	158	118.5	31.6	59.25	47.4
1	1	1	0	1	0	480	160	120	32	60	48
1	1	1	0	1	1	489	163	122.25	32.6	61.13	48.9
1	1	1	1	0	0	498	166	124.5	33.2	62.25	49.8
1	1	1	1	0	1	525	175	131.25	35	65.63	52.5
1	1	1	1	1	0	534	178	133.5	35.6	66.75	53.4
1	1	1	1	1	1	540	180	135	36	67.5	54

5.1 Register 0: Frequency Select Register

Bit	@PowerUp	Pin	Description
7	0	-	SSEL5 (Frequency table selection by software via I^2C)
6	0	-	SSEL4 (Frequency table selection by software via I^2C)
5	0	-	SSEL3 (Frequency table selection by software via I^2C)
4	0	-	SSEL2 (Frequency table selection by software via I^2C)
3	0	-	SSEL1 (Frequency table selection by software via I^2C)
2	0	-	SSEL0 (Frequency table selection by software via I^2C)
1	0	-	0 = Selection by hardware 1 = Selection by software I^2C - Bit (7:2)
0	0	-	0 = Running 1 = Tristate all outputs

5.2 Register 1 : CPU Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	-	CPUCS_C1$ free running control 1: stopped by CPU_STOP# 0: Free running pin
6	1	27	SDRAM11 (Active / Inactive)
5	0	-	0 = Normal 1 = Spread spectrum enable
4	0	-	0 = ±0.25% Center type Spread Spectrum Modulation 1= 0 ~ (-0.5%) Down type Spread Spectrum Modulation
3	1	26	SDRAM12 (Active / Inactive)
2	1	45	CPUCS_C1$(Active / Inactive)
1	1	46	CPUC0$ (Active / Inactive)
0	1	47	CPUT0$ (Active / Inactive)

5.3 Register 2: PCI, AGP Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	17	AGPCLK1(Active / Inactive)
6	1	16	AGPCLK0(Active / Inactive)
5	1	13	PCICLK5 (Active / Inactive)
4	1	12	PCICLK4 (Active / Inactive)
3	1	11	PCICLK3 (Active / Inactive)
2	1	10	PCICLK2 (Active / Inactive)
1	1	9	PCICLK1 (Active / Inactive)
0	1	8	PCICLK0 (Active / Inactive)

5.4 Register 3: SDRAM Clock Additional Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	33	SDRAM7 (Active / Inactive)
6	1	34	SDRAM6 (Active / Inactive)
5	1	36	SDRAM5 (Active / Inactive)
4	1	37	SDRAM4 (Active / Inactive)
3	1	38	SDRAM3 (Active / Inactive)
2	1	40	SDRAM2 (Active / Inactive)
1	1	41	SDRAM1 (Active / Inactive)
0	1	42	SDRAM0 (Active / Inactive)

5.5 Register 4: SDRAM Clock Additional Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	**X**	**-**	**AGPSEL#**
6	**X**	**-**	**FS3#**
5	**X**	**-**	**FS2#**
4	**X**	**-**	**FS1#**
3	**X**	**-**	**FS0#**
2	1	28	SDRAM10 (Active / Inactive)
1	1	30	SDRAM9 (Active / Inactive)
0	1	31	SDRAM8 (Active / Inactive)

5.6 Register 5: Skew Register

Bit	@PowerUp	Pin	Description
7	**1**	**-**	**CSkew2 (SDRAM to CPU skew program bit)**
6	**0**	**-**	**CSkew1 (SDRAM to CPU skew program bit)**
5	**0**	**-**	**CSkew0 (SDRAM to CPU skew program bit)**
4	1	-	**CAkew2 (AGP to CPU skew program bit)**
3	0	-	**CAkew1 (AGP to CPU skew program bit)**
2	0	-	**CAkew0 (AGP to CPU skew program bit)**
1	1	21	24_48MHz(Active / Inactive)
0	1	20	48MHz(Active / Inactive)

5.7 Register 6: Watchdog Timer Register

Bit	@PowerUp	Pin	Description
7	0	-	Enable Count 1 = start timer 0 = stop timer
6	X	-	Second timeout status (READ ONLY)
5	0	-	Second count 5
4	0	-	Second count 4
3	0	-	Second count 3
2	0	-	Second count 2
1	0	-	Second count 1
0	0	-	Second count 0

5.8 Register 7: M/N Program Register and Divisor

Bit	@PowerUp	Pin	Description
7	0	-	N value bit 8
6	**1**	**-**	**Test 1 (Internal test use)**
5	0	-	Test 0 (Internal test use)
4	0	-	M value bit 4
3	0	-	M value bit 3
2	0	-	M value bit 2
1	0	-	M value bit 1
0	0	-	M value bit 0

5.9 Register 8: M/N Program Register

Bit	@PowerUp	Pin	Description
7	0	-	N value bit 7
6	0	-	N value bit 6
5	0	-	N value bit 5
4	0	-	N value bit 4
3	0	-	N value bit 3
2	0	-	N value bit 2
1	0	-	N value bit 1
0	0	-	N value bit 0

5.10 Register 9: Spread Spectrum Register

Bit	@PowerUp	Pin	Description
7	0	-	Spread spectrum up count 3
6	0	-	Spread spectrum up count 2
5	0	-	Spread spectrum up count 1
4	0	-	Spread spectrum up count 0
3	0	-	Spread spectrum down count 3
2	0	-	Spread spectrum down count 2
1	0	-	Spread spectrum down count 1
0	0	-	Spread spectrum down count 0

5.11 Register 10: Divisor Register

Bit	@PowerUp	Pin	Description
7	0	-	0: use frequency table 1: use M/N register to program frequency The equation is **VCO freq. = 14.318MHz * (N+4)/ M**
6	X	-	Ratio SEL3 (See ratio selection table)
5	X	-	Ratio SEL2 (See ratio selection table)
4	X	-	Ratio SEL1 (See ratio selection table)
3	X	-	Ratio SEL0 (See ratio selection table)
2	X	-	AGP Ratio SEL2 (See ratio selection table1)
1	X	-	AGP Ratio SEL1 (See ratio selection table1)
0	X	-	AGP Ratio SEL0 (See ratio selection table1)

5.12 Register 11: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	**0**	**-**	**Winbond Chip ID**
6	**0**	**-**	**Winbond Chip ID**
5	**0**	**-**	**Winbond Chip ID**
4	**0**	**-**	**Winbond Chip ID**
3	**0**	**-**	**Winbond Chip ID**
2	**1**	**-**	**Winbond Chip ID**
1	**0**	**-**	**Winbond Chip ID**
0	**1**	**-**	**Winbond Chip ID**

5.13 Register 12: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	0	-	Winbond Chip ID
6	0	-	Winbond Chip ID
5	1	-	Winbond Chip ID
4	1	-	Winbond Chip ID
3	0	-	Version ID
2	0	-	Version ID
1	0	-	Version ID
0	1	-	Version ID

Ratio Selection Table

Reg10 bit6	Reg10 bit5	Reg10 bit4	Reg10 bit3	VCO/ CPU	VCO/ SDRAM	VCO/ PCI
SSEL3	SSEL2	SSEL1	SSEL0	ratio	ratio	ratio
0	0	0	0	2	2	10
0	0	0	1	2	3	10
0	0	1	0	3	2	10
0	0	1	1	3	3	10
0	1	0	0	3	3	12
0	1	0	1	3	3	16
0	1	1	0	3	4	12
0	1	1	1	3	4	16
1	0	0	0	4	3	10
1	0	0	1	4	3	12
1	0	1	0	4	3	16
1	0	1	1	4	4	12
1	1	0	0	4	6	12
1	1	0	1	6	3	12
1	1	1	0	6	4	12
1	1	1	1	6	6	12

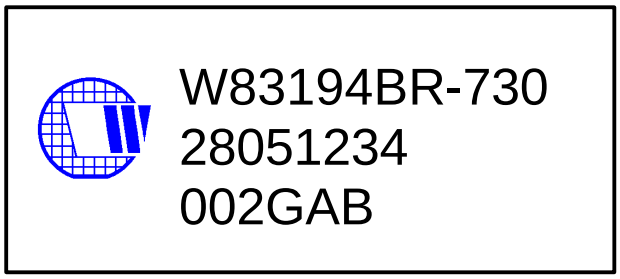
Ratio Selection Table 1

Reg10 bit2	Reg10 bit1	Reg10 bit0	VCO/AGP
AGP2	AGP1	AGP0	ratio
0	0	0	3
0	0	1	5
0	1	0	6
0	1	1	8
1	0	0	4
1	0	1	-
1	1	0	-
1	1	1	10

ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83194BR-730	48 PIN SSOP	Commercial, 0°C to +70°C

HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83194BR-730

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 814 G B B

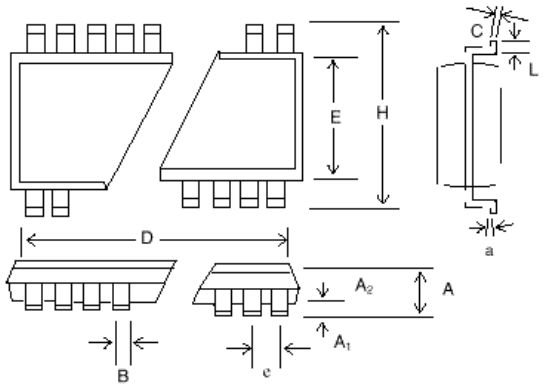
002: packages made in '00, week 02

G: assembly house ID; O means OSE, G means GR

A: Internal use code

B: IC revision

PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0°	5°	8°	0°	5°	8°

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