Winbond Electronics Corp.

133MHZ 3-DIMM K7 CLOCK

1.0 GENERAL DESCRIPTION

The W83194R-KX is a clock generator which provides all clocks required for AMD K7 system. W83194R-KX provides one differential pair CPU clock open drain outputs up to 143MHz which are externally selectable with smooth transitions. W83194R-KX also provides 6 PCI clocks and 13 SDRAM clocks controlled by the none-delay buffer_in pin.

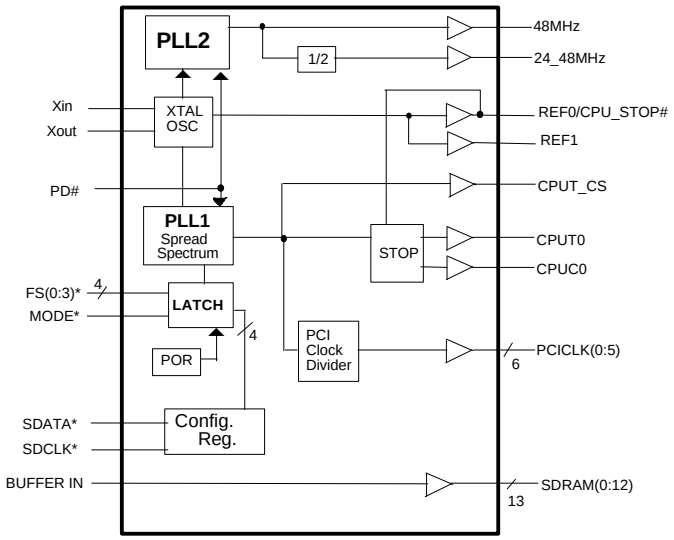
The W83194R-KX accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. Spread spectrum built in at ±0.5% or ±0.25% to reduce EMI. Programmable stopping individual clock outputs and frequency selection through I^2C interface. The device meets the Pentium power-up stabilization, which requires CPU and PCI clocks be stable within 2 ms after power-up.

High drive six PCI and thirteen SDRAM CLOCK outputs typically provide greater than 1 V /ns slew rate into 30 pF loads. Two CPU CLOCK outputs typically provide better than 1 V /ns slew rate into 20 pF loads, when maintaining 50± 5% duty cycle. The fixed frequency outputs, such as REF, 24MHz, and 48 MHz provide better than 0.5V /ns slew rate.

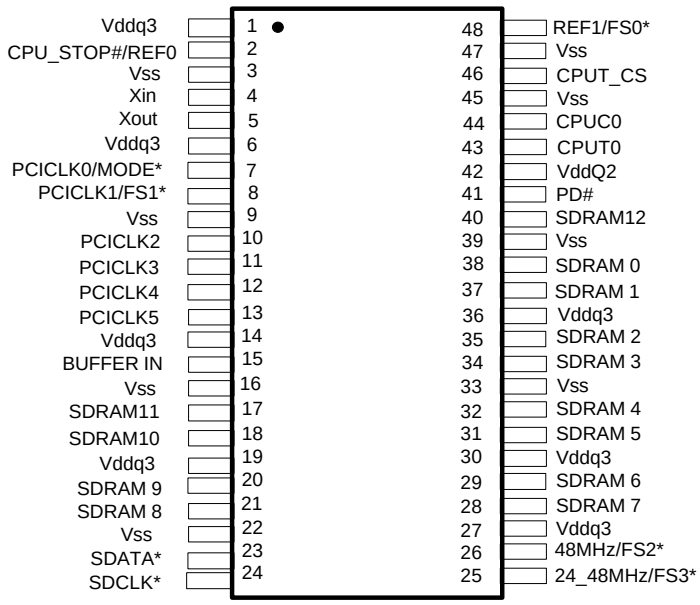
2.0 PRODUCT FEATURES

- Supports AMD K7 CPU with I^2C.
- One pair of differential CPU clocks
- One chipset clock
- 13 SDRAM clocks for 3 DIMMs
- 6 PCI synchronous clocks
- Optional single or mixed supply:
  (Vddq3=Vddq2 =3.3V) or (Vddq3 = 3.3V, Vddq2 = 2.5V)
- < 250ps skew among CPU clocks
- < 250ps skew among PCI clocks
- < 5ns propagation delay SDRAM from buffer input
- Skew from CPU(earlier) to PCI clock 1.5 to 4ns, center 2.6ns.
- Smooth frequency switch with selections from 66.8 MHz to 143 MHz CPU
- I^2C 2-Wire serial interface and I^2C read back
- ± 0.25% or ± 0.5% spread spectrum function to reduce EMI
- Programmable registers to enable/stop each output and select modes
  (mode as Tri-state or Normal)
- One 48 MHz for USB & one 24 MHz for super I/O
- 48-pin SSOP package

3.0 BLOCK DIAGRAM



4.0 PIN CONFIGURATION



5.0 PIN DESCRIPTION

IN - Input

OUT - Output

I/O - Bi-directional Pin

- Active Low

* - Internal 250kΩ pull-up

5.1 Crystal I/O

SYMBOL	PIN	I/O	FUNCTION
Xin	4	IN	Crystal input with internal loading capacitors and feedback resistors.
Xout	5	OUT	Crystal output at 14.318MHz nominally.

5.2 CPU, SDRAM, PCI, IOAPIC Clock Outputs

SYMBOL	PIN	I/O	FUNCTION
CPUT_CS CPU_C0 CPU_T0	46 44 43	OD	CPU_C0 and CPU_T0 are the differential open drain CPU clocks for K7. CPUT_CS is the open drain pin for the chipset. It has the same phase relationship as CPU_T0.

SDRAM [0:12]	17,18,20,21,28,29,31,32,34, 35,37,38,40	OUT	SDRAM clock outputs. Fanout buffer outputs from BUFFER IN pin.(Controlled by chipset) They are disabled when PD# is set LOW.
PCICLK0/ *MODE	7	I/O	Free running PCI clock during normal operation. Latched Input. Mode=1, Pin 2 is REF0; Mode=0, Pin2 is CPU_STOP#
PCICLK1/*FS1	8	I/O	Low skew (< 250ps) PCI clock outputs. Latched input for FS1 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
PCICLK [2:5]	10,11,12,13	OUT	Low skew (< 250ps) PCI clock outputs. Synchronous to CPU clocks with 1-48ns skew(CPU early).
BUFFER IN	15	IN	Inputs to fanout for SDRAM outputs.
PD#	41	IN	The all clocks will be stopped when this pin set to LOW .

5.3 I²C Control Interface

SYMBOL	PIN	I/O	FUNCTION
*SDATA	23	I/O	Serial data of I²C 2-wire control interface with internal pull-up resistor.
*SDCLK	24	IN	Serial clock of I²C 2-wire control interface with internal pull-up resistor.

5.4 Fixed Frequency Outputs

SYMBOL	PIN	I/O	FUNCTION
REF0 / CPU_STOP#	2	I/O	14.318MHz reference clock. This REF output is the stronger buffer for ISA bus loads. Halt CPU clocks at logic 0 level, when input low (In mobile mode. MODE=0)
REF1 / *FS0	48	I/O	14.318MHz reference clock. Latched input for FS0 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
24_48MHz / *FS3	25	I/O	24MHz output clock. Latched input for FS3 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
48MHz / *FS2	26	I/O	48MHz output for USB during normal operation. Latched input for FS2 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.

5.5 Power Pins

SYMBOL	PIN	FUNCTION
Vddq2	42	Power supply for CPU clocks, 2.5V or 3.3V.
Vddq3	1,6,14,19,27,30,36	Power supply for PCI, 24_48MHz, SDRAM[0:12], and CPU PLL core, nominal 3.3V.
Vss	3,9,16,22,33,39,45, 47	Circuit Ground.

6.0 FREQUENCY SELECTION

6.1 H/W Setting Frequency Table

FS3	FS2	FS1	FS0	CPU(MHz)	PCI(MHz)
1	1	1	1	**95**	**31.7**
1	1	1	0	**103**	**34.3**
1	1	0	1	**105**	**35**
1	1	0	0	**108**	**36**
1	0	1	1	**90**	**30**
1	0	1	0	110	36.7
1	0	0	1	115	38.3
1	0	0	0	120	30
0	1	1	1	133.3	33.3
0	1	1	0	83	33.3
0	1	0	1	100.2	33.3
0	1	0	0	66.8	33.4
0	0	1	1	124	31
0	0	1	0	129	32.3
0	0	0	1	138	34.5
0	0	0	0	143	35.8

7.0 MODE PIN -POWER MANAGEMENT INPUT CONTROL

MODE, Pin7 (Latched Input)	PIN 2
0	CPU_STOP# (Input)
1	REF0 (Output)

8.0 FUNTION DESCRIPTION

8.1 POWER MANAGEMENT FUNCTIONS

All clocks can be individually enabled or disabled via the 2-wire control interface. On power up, external circuitry should allow 3 ms for the VCO to stabilize prior to enabling clock outputs to assure correct pulse widths. When MODE=0, pins 2 is inputs (CPU_STOP#), when MODE=1, these functions are not available. The W83194R-KXmay be disabled in the low state according to the PD# pin41 in order to reduce power consumption. All clocks are stopped in the Power Down state when PD# is set to LOW, but maintain a valid high period on transitions from running to stop.

8.2 2-WIRE I^{2}C CONTROL INTERFACE

The clock generator is a slave I^{2}C component which can be read back the data stored in the latches for verification. All proceeding bytes must be sent to change one of the control bytes. The 2-wire control interface allows each clock output individually enabled or disabled. On power up, the W83194R-KX initializes with default register settings. Use of the 2-wire control interface is then optional.

The SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high during normal data transfer. There are only two exceptions. One is a high-to-low transition on SDATA while SDCLK is high used to indicate the beginning of a data transfer cycle. The other is a low-to-high transition on SDATA while SDCLK is high used to indicate the end of a data transfer cycle. Data is always sent as complete 8-bit bytes followed by an acknowledge generated.

Byte writing starts with a “Start” condition followed by 7-bit slave address and a write command bit [1101 0010], command code checking [0000 0000], and byte count checking. After successful reception of each byte, an “acknowledge“ (low) on the SDATA wire will be generated by the clock chip. Controller can start to write to internal I^{2}C registers after the string of data. The sequence order is as follows:

Bytes sequence order for I^{2}C controller :

Clock Address A(6:0) & R/W	**Ack**	**8 bits dummy Command code**	**Ack**	**8 bits dummy Byte count**	**Ack**	**Byte0,1,2... until Stop**

Set R/W to 1 when “Read back”, the data sequence is as follows, address is [1101 0011] :

Clock Address A(6:0) & R/W	**Ack**	**Byte 0**	**Ack**	**Byte 1**	**Ack**	**Byte2, 3, 4... until Stop**

8.3 SERIAL CONTROL REGISTERS

The Pin column lists the affected pin number and the @PowerUp column gives the default state at true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the sequence described below (Register 0, Register 1, Register 2, ...) will be valid and acknowledged.

Frequency table by software via I2C

SSEL3	SSEL2	SSEL1	SSEL0	CPU(MHz)	PCI(MHz)
1	1	1	1	**95**	**31.7**
1	1	1	0	**103**	**34.3**
1	1	0	1	**105**	**35**
1	1	0	0	**108**	**36**
1	0	1	1	**90**	**30**
1	0	1	0	110	36.7
1	0	0	1	115	38.3
1	0	0	0	120	30
0	1	1	1	133.3	33.3
0	1	1	0	83	33.3
0	1	0	1	100.2	33.3
0	1	0	0	66.8	33.4
0	0	1	1	124	31
0	0	1	0	129	32.3
0	0	0	1	138	34.5
0	0	0	0	143	35.8

8.3.1 Register 0: Frequency Select Register (default = 0)

Bit	@PowerUp	Pin	Description
7	0	-	Reserved
6	0	-	SSEL2 (for frequency table selection by software via I^2C)
5	0	-	SSEL1 (for frequency table selection by software via I^2C)
4	0	-	SSEL0 (for frequency table selection by software via I^2C)
3	0	-	0 = Selection by hardware 1 = Selection by software I^2C - Bit 6:4, Bit2
2	0	-	SSEL3 (for frequency table selection by software via I^2C)
1	0	-	Reserved
0	0	-	Reserved

8.3.2 Register 1 : CPU Clock Register (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	0	-	Reserved
6	0	-	Reserved
5	0	-	Reserved
4	0	-	Reserved
3	1	40	SDRAM12 (Active / Inactive)
2	0	-	Reserved
1	1	43 44	CPUT0 CPUC0 (Active / Inactive)
	1	46	CPUT_CS (Active / Inactive)

8.3.3 Register 2: PCI Clock Register (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	1	-	Reserved
6	1	7	PCICLK0 (Active / Inactive)
5	1	-	Reserved
4	1	13	PCICLK5 (Active / Inactive)
3	1	12	PCICLK4 (Active / Inactive)
2	1	11	PCICLK3 (Active / Inactive)
1	1	10	PCICLK2(Active / Inactive)
0	1	8	PCICLK1 (Active / Inactive)

8.3.4 Register 3: SDRAM, 24MHz, 48MHz Clock Register (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	0	-	Reserved
6	0	-	SEL24_48 (Select 24MHz or 48MHz for pin25)
5	1	26	48MHz (Active / Inactive)
4	1	25	24_48MHz (Active / Inactive)
3	0	-	Reserved
2	1	21,20,18, 17	SDRAM(8:11) (Active / Inactive)
1	1	32,31,29, 28	SDRAM(4:7) (Active / Inactive)
0	1	38,37,35, 34	SDRAM(0:3) (Active / Inactive)

8.3.5 Register 4: Reserved Register (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	X	-	Latched FS3#
6	X	-	Latched FS2#
5	X	-	Latched FS1#
4	X	-	Latched FS0#
3	0	-	Reserved
2	0	-	Reserved
1	0	-	0 = ±0.75% Spread Spectrum Modulation 1 = ±0.5% Spread Spectrum Modulation
0	0	-	0 = Normal 1 = Spread Spectrum enabled

8.3.6 Register 5: Peripheral Control (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	0	-	Reserved
6	0	-	Reserved
5	0	-	Reserved
4	0	-	Reserved
3	0	-	Reserved
2	0	-	Reserved
1	1	46	REF1 (Active / Inactive)
0	1	2	REF0 (Active / Inactive)

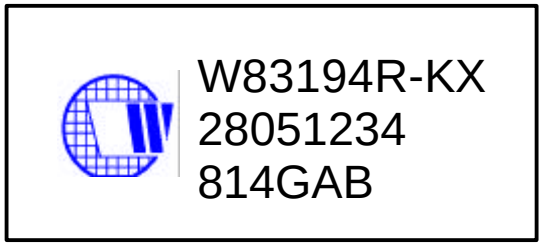
8.2.7 Register 6: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	0	-	Winbond Chip ID
6	1	-	Winbond Chip ID
5	0	-	Winbond Chip ID
4	1	-	Winbond Chip ID
3	0	-	Winbond Chip ID
2	1	-	Winbond Chip ID
1	1	-	Winbond Chip ID
0	1	-	Winbond Chip ID

13.0 ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83194R-KX	48 PIN SSOP	Commercial, 0°C to +70°C

14.0 HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83194R-KX

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 814 G A B

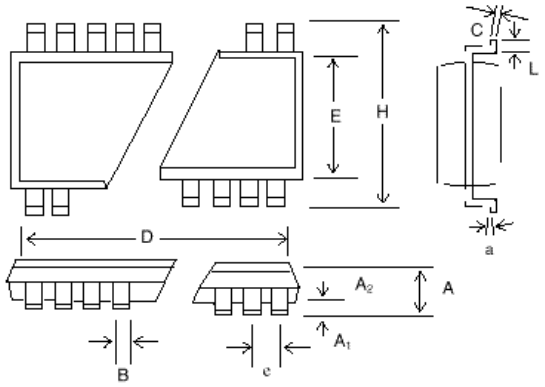
814: packages made in '98, week 14

G: assembly house ID; A means ASE, S means SPIL, G means GR

A: Internal use ID

B: IC revision

15.0 PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0°	5°	8°	0°	5°	8°

Winbond Electronics Corp.

Headquarters
No. 4, Creation Rd. III
Science-Based Industrial Park
Hsinchu, Taiwan
TEL: 886-35-770066
FAX: 886-35-789467
www: http://www.winbond.com.tw/

Taipei Office
11F, No. 115, Sec. 3, Min-Sheng East Rd.
Taipei, Taiwan
TEL: 886-2-7190505
FAX: 886-2-7197502
TLX: 16485 WINTPE

Winbond Electronics (H.K.) Ltd.
Rm. 803, World Trade Square, Tower II
123 Hoi Bun Rd., Kwun Tong
Kowloon, Hong Kong
TEL: 852-27516023-7
FAX: 852-27552064

Winbond Electronics (North America) Corp.
2730 Orchard Parkway
San Jose, CA 95134 U.S.A.
TEL: 1-408-9436666
FAX: 1-408-9436668