Winbond
ACPI-STR Controller
W83301DR-O

Date: 2002/07 Revision: 1.0

W83301DR-O
Data Sheet Revision History

	Pages	Dates	Version	Version on Web	Main Contents
1	N.A.	07/2002	1.0	1.0	1st Release

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

1. General Description

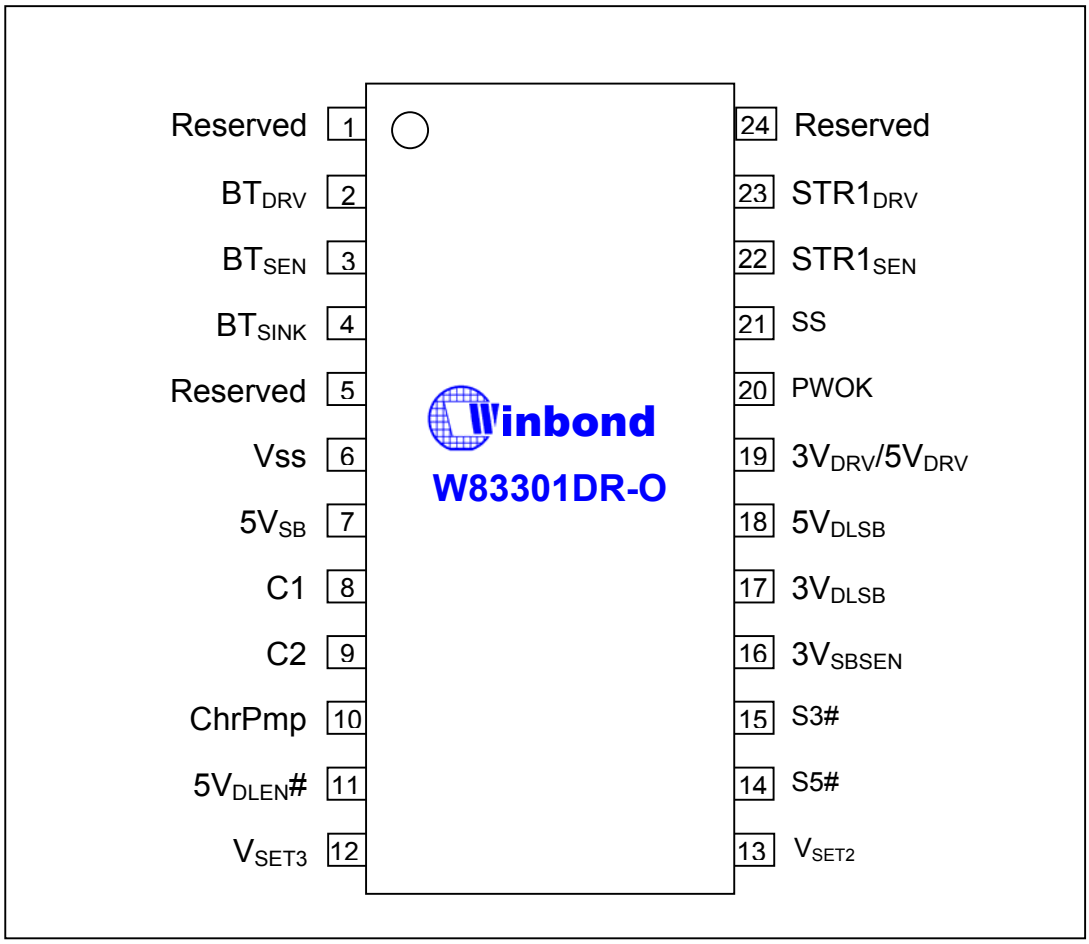
The W83301DR-O is an ACPI-compliant controller for microprocessor and other computer applications. The part provides functions - two switch controllers to generate a $5V_{DL}$ and a 3.3 V_{DL} voltage from ATX power supply; a linear controller – STR1 ($2.5V_{DUAL}$), and a bus termination controller – STR2 (1.25 V_{DUAL}) for high-speed bus such as RDRAM/DDRAM current sinking and sourcing. Besides, the W83301DR-O also can provide extra voltage up to 0.4V in each regulator output for over-clocking application and more performance by two hardware pins - V_{SET2}, and V_{SET3}. In order to reduce the customer's cost, and simplify the circuit design, the W83301DR-O integrates a charge-pump engine into the chip to provide higher driving voltage to drive single N-channel MOSFETs. The W83301DR-O also offers PWOK and over current detection to protect each output and soft-start protects all linear controllers from rush current attack. The W83301DR-O is available in a 24-pin TSSOP package.

2. Features

- Provides various voltages for DDR-STR applications
  - Provide a switch controller to generate $5V_{DUAL}$ voltage
  - Provide a switch controller to generate $3.3V_{DUAL}$ voltage
  - Linear controller STR1–$2.5V_{DUAL}$ for DDR application
  - Bus termination controller STR2 –$1.25V_{DUAL}$ for high speed bus termination to sink and drive redundant current
- Provide a switch $5V_{DLEN}$ pin to enable/disable $5V_{DL}$ output in S5 state for USB application
- Supports DDR ACPI-STR Functions
- Drives all N-Channel MOSFETs
- Power-Up Softstart for all controllers
- Up to 0.4V/0.2V incremental voltage on STR1/STR2 for over-clocking application.
- Under-Voltage Fault Monitor
- Soft-Start function
- 24-Pin TSSOP Package

Publication Release Date: Jul., 2002
Revision 1.0

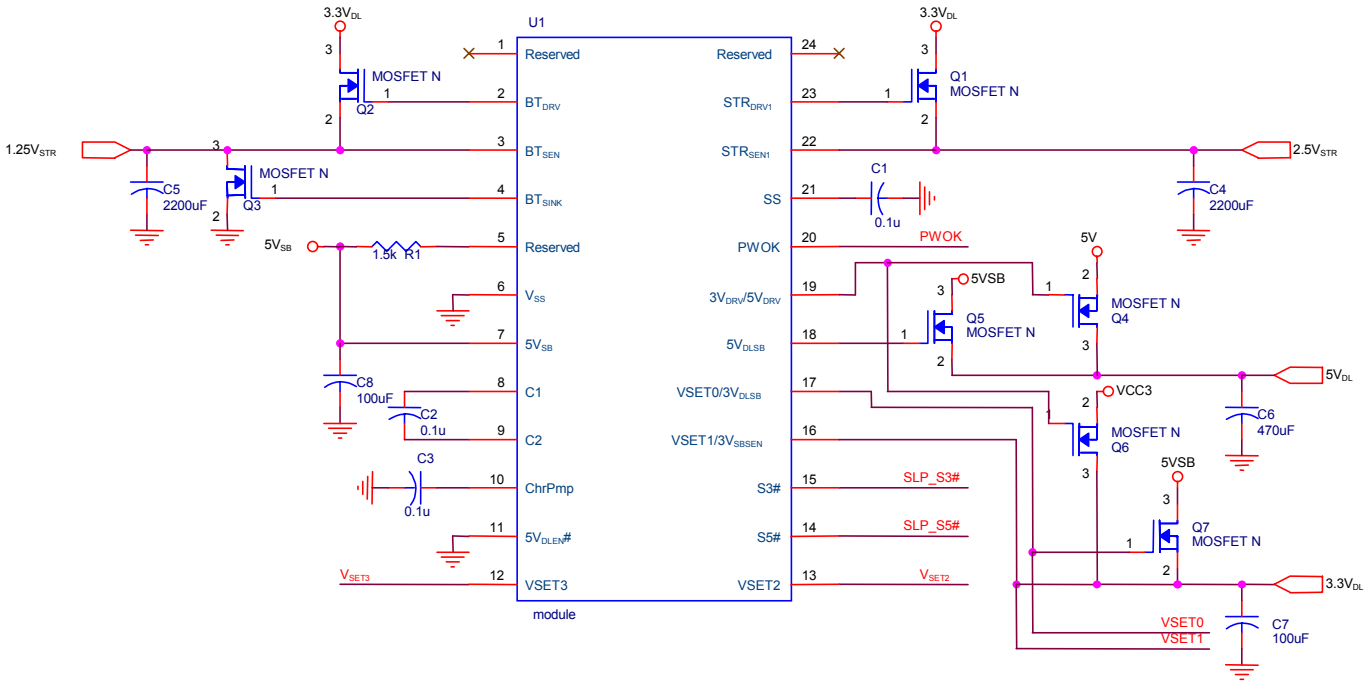
3. W83301DR-O Pin Configuration



4. Pin Description

SYMBOL	PIN	FUNCTION
Reserved	1	**Pin Reserved**
BT_{DRV}	2	**BT Current Source.** Connect this pin to the gate of a suitable N-channel MOSFET for driving bus termination regulator output.
BT_{SEN}	3	**BT Sense.** Connect this pin to the bus termination regulator output.
BT_{SINK}	4	**BT Current Sink.** This pin is used to drive a N-channel MOSFET to sink the redundant current in the high-speed bus.
Reserved	5	**Function Reserved.** Pull up this pin to +5VSB through a 1.5 Kohm resistor.
Vss	6	**Power Ground.** Connect this pin to ground.
$5V_{SB}$	7	**Power $5V_{SB}$.** Input $5V_{SB}$ supply.
C1	8	**Charge Pump Cap.** Attach flying capacitor between this pin and C2 to generate internally used high voltage from 5V power supply.
C2	9	**Charge Pump Cap.** Attach flying capacitor between this pin and C1 to generate internally used high voltage from 5V power supply.
ChrPmp	10	**Charge Pump output.** This pin produces voltage doubled 5V supply by charge pumping. Bypass with a 0.1uF capacitor.
$5V_{DLEN}$#	11	**5VDL Enable.** Control $5V_{DL}$ voltage output. Pull-up internally.
V_{SET3}	12	**Voltage Selection.** Combine with VSET2 to select output voltages of STR regulators.
V_{SET2}	13	**Voltage Selection.** Combine with VSET3 to select output voltages of STR regulators.
S5#	14	**S5 Signal.** Control signal governing the soft off state S5. Pull-up internally.
S3#	15	**S3 Signal.** Control signal governing the soft off state S3. Pull-up internally.
$3V_{SBSEN}$	16	**$3V_{DL}$ Sense.** Connect this pin to the STR1 output.
$3V_{DLSB}$	17	**$3V_{DL}$ Drive.** Connect this pin to the gate of a suitable N-channel MOSFET for driving STR1 output.
$5V_{DLSB}$	18	**5VSB Output Control.** Connect this pin to the gate of a N-MOSFET to output 5VSB power to $5V_{DL}$.
$3V_{DRV}/5V_{DRV}$	19	**3.3V/5V Output Control.** Connect this pin to the gate of a N-MOSFET to output 3.3V/5V power to $3.3V_{DL}/5V_{DL}$.
PWOK	20	**Power OK.** Open collector input/output. Used to indicate the ready of 5Vin supply. If any STR supply occurs over current and induce under-voltage, PWOK will be pull down.
SS	21	**Soft-Start.** Attach a capacitor (0.033u) to this pin to determine the softstart rate. A ramp generated by charging this capacitor with internal soft-start current (18uA) is used to clamp the voltage rising slew rate of STR regulators and $5V_{DL}$. Soft starting avoids too much rush current during voltage setup.
$STR1_{SEN}$	22	**STR1 Sense.** Connect this pin to the STR1 output.
$STR1_{DRV}$	23	**STR1 Drive.** Connect this pin to the gate of a suitable N-channel MOSFET for driving STR1 output.
Reserved	24	Pin Reserved

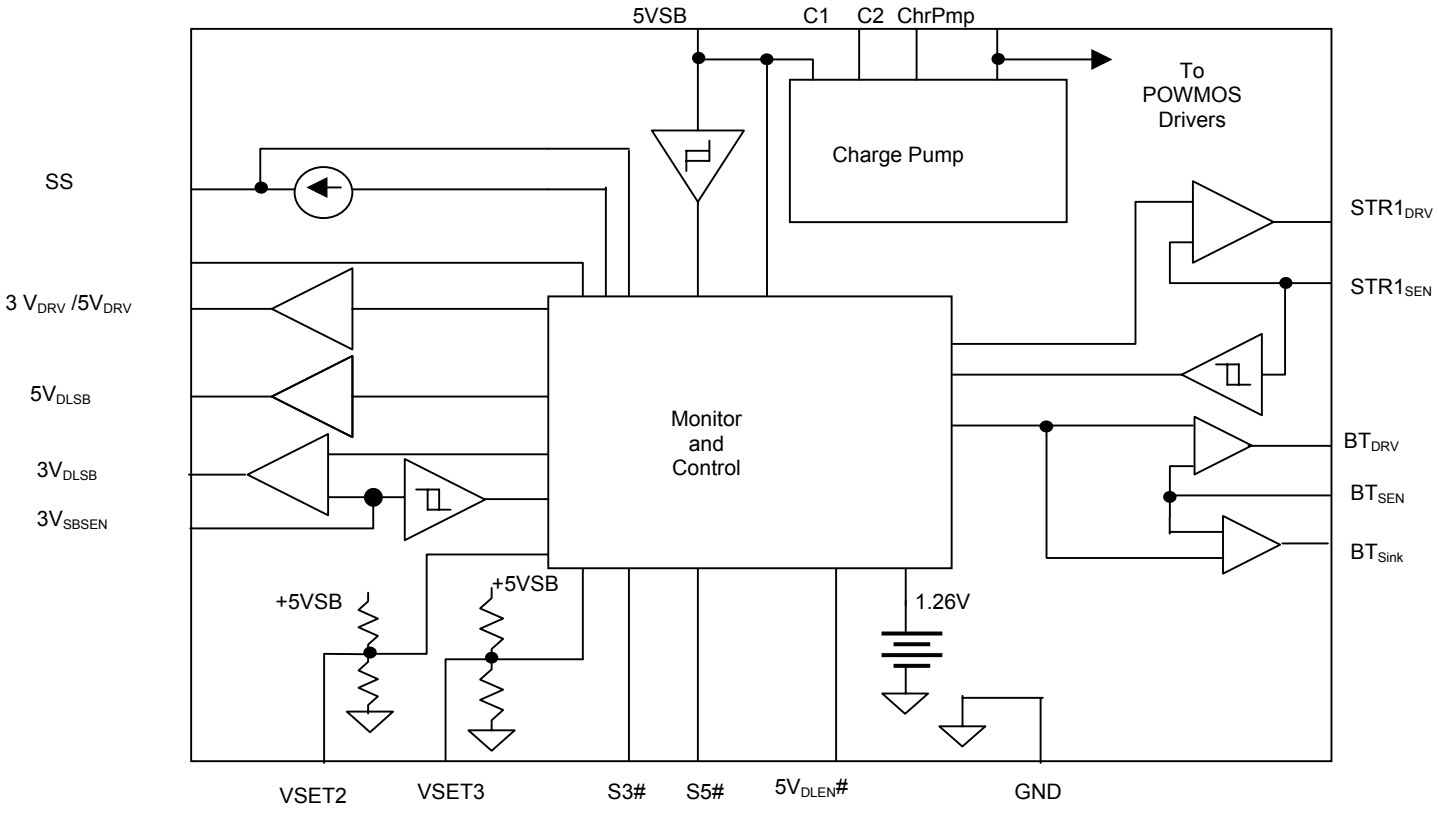
5. W83301DR-O Dual-Layout with W83301R/W83301DR



Mode	VSET0	VSET1	STR1	Bus Termination Controller
DDR 20-pin	0V	0V	2.5VSTR	1.25VSTR
	0V	NC	2.6VSTR	1.30VSTR
	0V	5V	2.7VSTR	1.35VSTR

Mode	VSET2	VSET3	STR1	Bus Termination Controller
DDR 24-pin	0V	0V	2.5VSTR	1.25VSTR
	5V	0V	2.63VSTR	1.325VSTR
	0V	5V	2.77VSTR	1.385VSTR
	5V	5V	2.9VSTR	1.45VSTR

6. Internal Block Diagram



7. Functional Description

7.1 ACPI State Control

In order to meet the ACPI specification, the W83301DR-O implements an internal state machine to generate ACPI-compliant power state transition.

There are five states in the state machine, the five states are G3 (Mechanical-Off State), S0 (Full-Power State), S3 (Sleeping State-Suspend to RAM), $S5_{On}$ (Soft-Off State), $S5_{Off}$ and all of the state changes to the other according to the value of S3#, S5# and $5V_{DLEN}$#. On the other hand, cause of the W83301DR-O allows the user to disable/enable the $5V_{DUAL}$ output in S5 state via the $5V_{DLEN}$# pin, there are two states - $S5_{On}$ and $S5_{Off}$, corresponding to S5 state. Besides, a soft ramp-up mechanism is needed to protect the $5V_{DL}$ output from the rush current attack during the $S5_{Off}$ to $S5_{On}$ state transition. Same as the $5V_{DL}$ output, the W83301DR-O also implements soft ramp-up mechanism in each STR outputs during the $S5_{On}$ state transfers to the S0 state.

As the internal state machine, when the power turns on, the voltage of 5VSB of the ATX power supply ramps up to 4.5V, the chip will enters the $S5_{Off}$ state from the G3 state, and will enters the $S5_{On}$ state if the signal of $5V_{DLEN}$#=0 and S5#=0; When the signals S3#=1 and S5#=1, the system will enters the S0 state from $S5_{off}$.

In the $S5_{On}$ state, the chip will returns back to the $S5_{Off}$ state if the $5V_{DLEN}$#=1 is set.

When the system in the S0 state, the system will enters the S3 (S3#=0, S5#=1) or S5 (S5#=0) state when the system is idle for a long time or user presses the power button.

When the system enters the S3 state, the system will waked up and enter the S0 state by (S3#=1, S5#=1,PWOK=1), or gets into S5 state by (S5#=0).

Table 1. W83301DR-O Outputs Table

State	$5V_{DL}$	$3V_{DL}$	STR1	STR2	LUV Activity *
G3	Off	Off	Off	Off	No
S5 ($5V_{DL}$ Off)	Off	On (Driven by $3V_{DLSB}$)	Off	Off	No
S5 ($5V_{DL}$ On)	On (Driven by $5V_{DLSB}$)	On (Driven by $3V_{DLSB}$)	Off	Off	No
S0	On (Driven by $5V_{DRV}$)	On (Driven by $3V_{DRV}$)	On	On	Yes
S3	On (Driven by $5V_{DLSB}$)	On (Driven by $3V_{DLSB}$)	On	On	Yes

* Only the STR1 has linear under voltage function.

7.3 Charge Pump

In order to simply the design circuit and provide a cost-effective solution for customer, the W83301DR-O integrates with a switched-capacitor voltage doublers charge pump to provide a higher driving voltage (Up to 10 volt) and can drive single N-channel MOSFETs in each output.

7.4 Power OK

The W83301DR-O use a bi-direction Power OK signal to ensure the system can work normally. When the system jump from the state S3 to the state S0, the W83301DR-O will monitor the input signal from PWOK pin to ensure that external system power is OK and then will switches each outputs into the S0 state; In the other hand, the W83301DR-O will pulls down the Power OK signal to inform the system a over current and induce under-voltage occurred.

7.5 Soft-Start

During the 'S5off' to the 'S5on' and the 'S5on' to the 'S0' state transitions, the 5Vdual/3Vdual and STR voltages need to ramp up from 0V to the setting values respectively. The charging current flowing to output capacitors must be limited to avoid supply drop-off.

In W83301DR-O, an internal 18 uA current source (Iss) charges an external capacitor (Css) to generate a linear ramp-up voltage on SS pin (Vss). The Vss slews from 0V to about 9V during the above-mentioned state transitions, and the Vss slew rate is used to clamp the ramp-up rate of 5Vdual and STR output voltages. This output clamping allows power-ups free of supply drop-off events.

Since the outputs are ramped up in a constant slew-rate, the current dedicated to charge any output capacitor can be calculated with the following formula:

I_{COUT} = Iss x (Cout / Css)

Some technique are included in W83301DR-O to further reduce the total charging current: the bus-terminator is input clamped, and its output voltage slew-rate, so as its charging current, will be limited to half of that of STR1.

Note that, too slow ramp-up rate is not recommended. If so, the state transition mentioned above will be prolonged to much. Before Vss ramps up to its upper limit (about 9V), the state transition will not be completed and will not go into next state.

8. Electrical Characteristics

8.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Subjection to maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or Vdd).

Symbol	Parameter	Rating
Vss, V_{cc}	Voltage on any pin with respect to GND	- 0.5 V to + 7.0 V
ChrPmp		- 0.5 V to + 12.0 V
Hi-V Pins	Pin# 2,3,4,5,9,10,17,18,19,21,22,23	GND-0.3 V to $V_{Chr-Pmp}$ + 0.3V
Lo-V Pins	Pin# 8,11,12,13,14,15,16,20	GND-0.3 V to Vcc + 0.3V
T_{STG}	Storage Temperature	- 65°C to + 150°C
T_B	Ambient Temperature	- 55°C to + 125°C
T_A	Operating Temperature	0°C to + 70°C

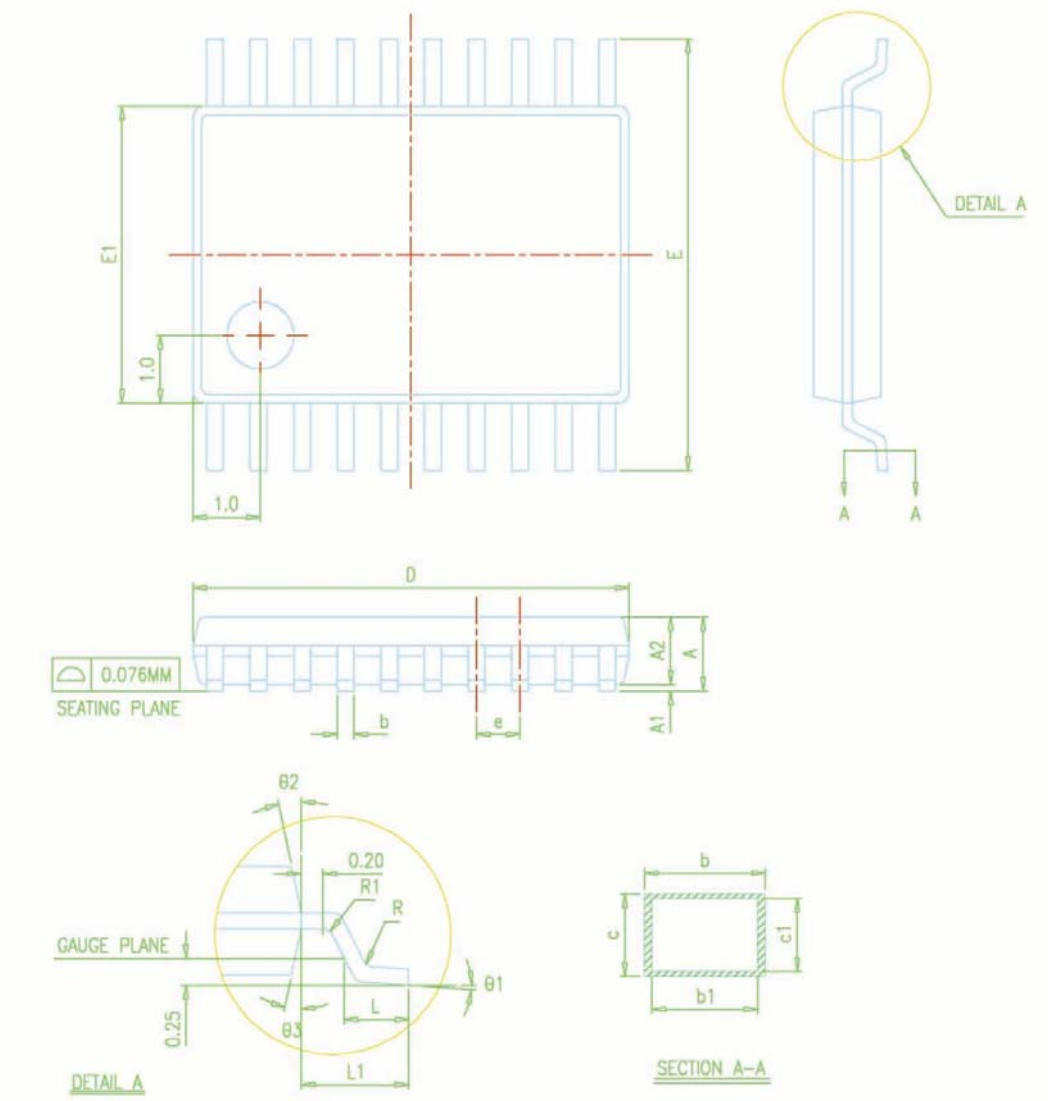
8.2 AC CHARACTERISTICS

Vcc=5V ± 5 %, T_A = 0°C to +70°C						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
Vcc SUPPLY CURRENT						
Norminal Supply Current	**I_{5VSB}**		6		mA	
POWER-ON RESET						
Rising V_{5VSB} Threshold				4.3	V	V_{Chr_Pmp} > 8.5V
5VSB Hysteresis			1		V	
Rising V_{Chr_Pmp} Threshold				8.5	V	V_{5VSB} > 4.3V
V_{Chr_Pmp} Hysteresis			1		V	
SOFT-START						
Soft-Start Current	**Iss**		18		uA	
V_{SS} upper limit			9		V	

8.2 AC CHARACTERISTICS (Continued)

Vcc=5V ± 5 %, T_A = 0℃ to +70℃						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
STR1 LINEAR REGULATOR						
Nominal Output Voltage			2.5		V	Vset2=0V; Vset3=0V
Nominal Output Voltage			2.63		V	Vset2=5V; Vset3=0V
Nominal Output Voltage			2.77		V	Vset2=0V; Vset3=5V
Nominal Output Voltage			2.90		V	Vset2=5V; Vset3=5V
Regulation		3		3	%	
STR_{SEN1} Under-Voltage Falling Threshold			80		%	
MAX STR_{DRV1} Output Voltage		6			V	I ($STR1_{DRV}$) < 0.1mA
BUS TERMINATION REGULATOR						
Nominal Output Voltage / $V_{STRSEN1}$			50		%	The output is always the 50% of STR1
Regulation		-2		3	%	
5VDUAL SWITCH CONTROLLER						
$5V_{DRV}$ Output High Voltage		9				Cload=3000p
$5V_{DRV}$ Sourcing Current			7		mA	Cload=3000p
$5V_{DRV}$ Sinking Current			400		uA	Cload=3000p
$5V_{DLSB}$ Output High Voltage		9				Cload=3000p
$5V_{DLSB}$ Sourcing Current			7		mA	Cload=3000p
$5V_{DLSB}$ Sinking Current			230		uA	Cload=3000p
$3V_{CC}$ SWITCH CONTROLLER						
$3V_{DRV}$ Output High Voltage		9				Cload=3000p
$3V_{DRV}$ Sourcing Current			7		mA	Cload=3000p
$3V_{DRV}$ Sinking Current			400		uA	Cload=3000p
$3.3V_{SB}$ LINEAR REGULATOR						
Nominal Output Voltage			3.3		V	
Regulation		3		3	%	
STR_{SEN1} Under-Voltage Falling Threshold			80		%	
MAX $3.3V_{DLSB}$ Output Voltage		6			V	I ($3.3V_{DLSB}$) < 0.1mA
S3#,S5#,5VDLEN#, PWOK,CHARGE PUMP						
Input Logic High	2.2				V	
Input Logic Low				0.8	V	
PWOK Output Inpedence		150			ohm	LUV active
Charge Pump Frequency			200		KHz	

9. Package Dimension 24-TSSOP 173mil



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.20			0.043
A1	0.05		0.15	0.002		0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
L	0.50	0.60	0.75	0.020	0.024	0.030
E	6.40 BSC.			0.252 BSC.		
E1	4.30	4.40	4.50	0.169	0.173	0.177
R	0.09			0.004		
R1	0.09			0.004		
b	0.19		0.30	0.007		0.012
b1	0.19	0.22	0.25	0.007	0.009	0.010
c	0.09		0.20	0.004		0.008
c1	0.09		0.16	0.004		0.006
L1	1.0 REF.			0.039 REF.		
e	0.65 BSC.			0.026 BSC.		
θ1	0		8	0		8
θ2	12 REF.			12 REF.		
θ3	12 REF.			12 REF.		

	D (MM)			JEDEC
N	MIN.	NOM	MAX.	
14	4.90	5.00	5.10	MO-153 (AB-1)
16	4.90	5.00	5.10	MO-153 (AB)
20	6.40	6.50	6.60	MO-153 (AC)
24	7.70	7.80	7.90	MO-153 (AD)
28	9.60	9.70	9.80	MO-153 (AE)

10. Ordering Information

Part Number	Package Type	Production Flow
W83301DR-O	24-PIN TSSOP	Commercial, 0°C to +70°C

11. How to Read the Top Marking

1st line: Winbond logo
2nd line: W83301DR-O – the part number
3rd line: Tracking code Tracking code 106 O B 1 1039050-21NA
106: packages made in Year 01', week 6
O: assembly house ID; O means OSE, G means GR, …
B: the IC version
1: wafers manufactured in Winbond FAB I
1039050-21NA: wafer production series number

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