W83527HG

Nuvoton LPC I/O

Date: December 25, 2009 Version: 1.5

TABLE OF CONTENTS –

List of Figures

List of Tables

1. GENERAL DESCRIPTION

The W83527HG is a member of Nuvoton's Super I/O product line. This family features the LPC (Low Pin Count) interface. This interface is more economical than its ISA counterpart, in that it has approximately forty pins fewer, yet still provides as great performance. In addition, the improvement allows even more efficient operation of software, BIOS and device drivers.

In addition to providing an LPC interface for I/O, the W83527HG monitors several critical parameters in PC hardware, including fan speeds, and temperatures. In terms of temperature monitoring, the W83527HG adopts the Current Mode (dual current source) approach. The W83527HG also supports the Smart Fan control system, including "SMART FAN™ I and SMART FAN™ III, which makes the system more stable and user-friendly.

The W83527HG provides flexible I/O control functions through a set of 18 general purpose I/O (GPIO) ports. These GPIO ports may serve as simple I/O ports or may be individually configured to provide alternative functions.

The W83527HG fully complies with the Microsoft© PC98, PC99 and PC2001 System Design Guides and meets the requirements of ACPI.

The configuration registers inside the W83527HG support mode selection, function enable and disable, and power-down selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature in Windows 95/98/2000/XP™, making the allocation of the system resources more efficient than ever.

One special characteristic of the Super I/O product line is the separation of the power supply in normal operation from that in standby operation. Please pay attention to the layout of these two power supplies to avoid short circuits. Otherwise, the feature will not function.

2. FEATURES

General

- Meet LPC Spec. 1.01
- SERIRQ (Serialized IRQ)
- Integrated hardware monitor functions
- Compliant with Microsoft PC98/PC99/PC2001 System Design Guide
- ACPI (Advanced Configuration and Power Interface)
- Programmable configuration settings
- Single 24- or 48-MHz clock input
- Support selective pins of 5 V tolerance
- Support Watch Dog Timer function

Keyboard Controller

- 8042-based keyboard controller
- Asynchronous Access to two data registers and one status register
- Software-compatible with 8042
- Support PS/2 mouse
- Support Port 92
- Support both interrupt and polling modes
- Fast Gate A20 and Hardware Keyboard Reset
- 6, 8, 12, or 16 MHz operating frequency

Hardware Monitor Functions

- Smart Fan control system, supporting the functions of SMART FANTM I -- "Thermal Cruise™" and "Speed Cruise™" modes, and SMART FAN™ III
- Programmable threshold temperature to speed fan fully while current temperature exceeds this threshold in the Thermal Cruise™ mode
- Two thermal inputs from the different combinations of remote thermistors, and the thermal diode output
- Support Current Mode (dual current source) temperature sensing method
- Three fan-speed monitoring inputs
- Three fan-speed controls
- Dual mode for fan control (PWM and DC)
- Programmable hysteresis and setting points for all monitored items
- Over-temperature indicator output
- Issue SMI#, OVT# to activate system protection

- Nuvoton Hardware Doctor™ support

General Purpose I/O Ports

- 18 programmable general purpose I/O ports
- GP31 and GP35 can distinguish whether the input pins undergo any transitions by reading the registers. Both GPIOs can assert PSOUT# to wake up the system if each of them undergoes any transition.

OnNow Functions

- Keyboard Wake-Up by programmable keys
- Mouse Wake-Up by programmable buttons
- OnNow Wake-Up from all of the ACPI sleeping states (S1-S5)

PECI Interface

- Support PECI 1.0 and 1.1a Specifications
- Support 4 CPU addresses and 2 domains per CPU address

Package

- 48-pin LQFP
- Pb-free/RoHS

3. BLOCK DIAGRAM

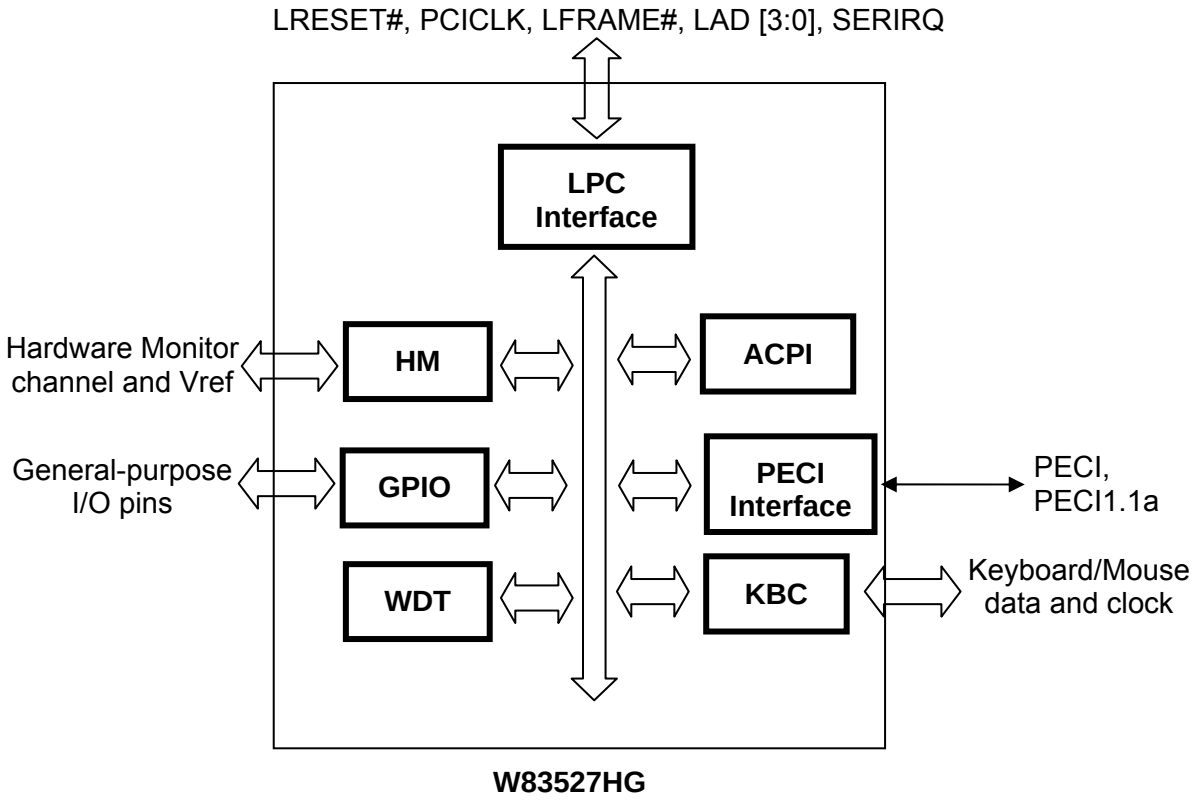


Figure 3-1 W83527HG Block Diagram

4. PIN LAYOUT

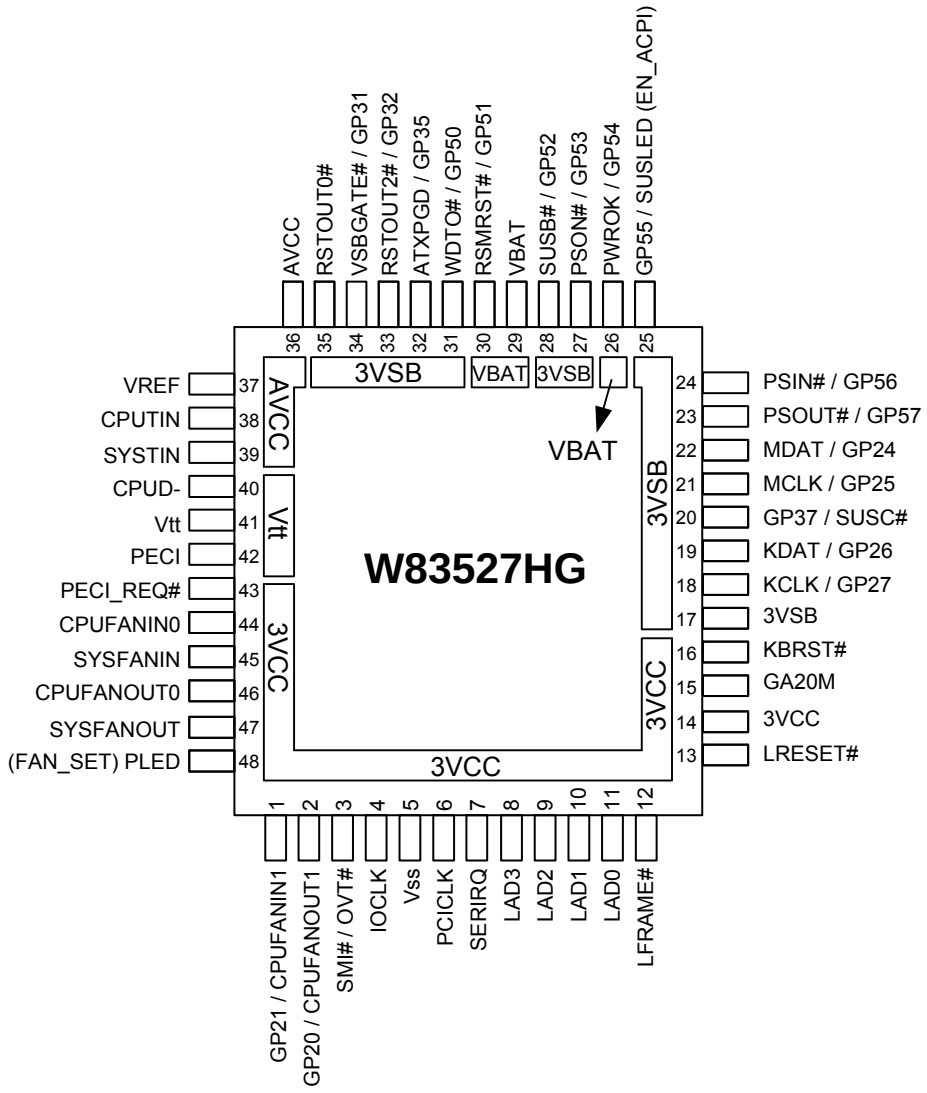


Figure 4-1 Pin Layout for W83527HG

5. PIN DESCRIPTION

Note: Please refer to 17.2 DC CHARACTERISTICS for details.

AOUT - Analog output pin
AIN - Analog input pin
IN_{cd} - CMOS-level input pin with internal pull-down resistor
IN_{cs} - CMOS-level, Schmitt-trigger input pin
IN_{csu} - CMOS-level, Schmitt-trigger input pin with internal pull-up resistor
IN_{t} - TTL-level input pin
IN_{td} - TTL-level input pin with internal pull-down resistor
IN_{ts} - TTL-level, Schmitt-trigger input pin
IN_{tp3} - 3.3V, TTL-level input pin
IN_{tsp3} - 3.3V TTL level Schmitt-trigger input pin
IN_{tu} - TTL-level input pin with internal pull-up resistor
I/O_{8} - bi-directional pin with 8-mA source-sink capability
I/O_{8t} - TTL-level, bi-directional pin with 8-mA source-sink capability
I/O_{12} - bi-directional pin with 12-mA source-sink capability
I/O_{12t} - TTL-level, bi-directional pin with 12-mA source-sink capability
I/O_{12ts} - Schmitt-trigger, bi-directional pin with 12-mA source-sink capability
I/O_{12tp3} - 3.3V, TTL-level, bi-directional pin with 12-mA source-sink capability
I/OD_{8t} - TTL-level, bi-directional pin. Open-drain output with 8-mA sink capability
I/OD_{12} - Bi-directional pin. Open-drain output with 12-mA sink capability
I/OD_{12t} - TTL-level bi-directional pin. Open-drain output with 12-mA sink capability
I/OD_{12cs} - CMOS-level, bi-directional, Schmitt-trigger pin. Open-drain output with 12-mA sink capability
I/OD_{12ts} - TTL-level, bi-directional, Schmitt-trigger pin. Open-drain output with 12-mA sink capability
I/OD_{12tp3} - 3.3V, TTL-level, bi-directional pin. Open-drain output with 12-mA sink capability
I/OD_{16t} - TTL-level, bi-directional pin. Open-drain output with 16-mA sink capability
I/OD_{16ts} - Schmitt-trigger, bi-directional pin. Open-drain output with 16-mA sink capability
I/OD_{16cs} - CMOS-level, Schmitt-trigger, bi-directional pin. Open-drain output with 16-mA sink capability
I/OD_{24t} - TTL-level, bi-directional pin. Open-drain output with 24-mA sink capability
O_{12p3} - 3.3V output pin with 12-mA source-sink capability
O_{12tp3} - 3.3V, TTL-level output pin with 12-mA source-sink capability
O_{8} - TTL-level output pin with 8-mA source-sink capability
O_{12} - TTL-level output pin with 12-mA source-sink capability
O_{24} - TTL-level output pin with 24-mA source-sink capability
OD_{8} - Open-drain output pin with 8-mA sink capability
OD_{12} - Open-drain output pin with 12-mA sink capability
OD_{24} - Open-drain output pin with 24-mA sink capability
I_{V3} - Bi-direction pin with source capability of 6 mA and sink capability of 1 mA
I/O_{V3} - Bi-direction pin with source capability of 6 mA and sink capability of 1 mA

5.1 LPC Interface

SYMBOL	PIN	I/O	DESCRIPTION
IOCLK	4	IN_{tp3}	System clock input, either 24MHz or 48MHz. The actual frequency must be specified in the register. The default value is 48MHz.
PCICLK	6	IN_{tsp3}	PCI-clock 33-MHz input.
SERIRQ	7	I/OD_{12tp3}	Serialized IRQ input / output.
LAD[3:0]	8-11	I/O_{12tp3}	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
LFRAME#	12	IN_{tsp3}	Indicates the start of a new cycle or the termination of a broken cycle.
LRESET#	13	IN_{tsp3}	Reset signal. It can be connected to the PCIRST# signal on the host.

5.2 KBC Interface

SYMBOL	PIN	I/O	DESCRIPTION
GA20M	15	O_{12}	Gate A20 output. This pin is high after system reset.
KBRST#	16	O_{12}	Keyboard reset. This pin is high after system reset.
KCLK	18	I/OD_{16ts}	Keyboard Clock. (Default)
GP27		I/OD_{16t}	General-purpose I/O port 2 bit 7.
KDAT	19	I/OD_{16ts}	Keyboard Data. (Default)
GP26		I/OD_{16t}	General-purpose I/O port 2 bit 6.
MCLK	21	I/OD_{16ts}	PS2 Mouse Clock. (Default)
GP25		I/OD_{16t}	General-purpose I/O port 2 bit 5.
MDAT	22	I/OD_{16ts}	PS2 Mouse Data. (Default)
GP24		I/OD_{16t}	General-purpose I/O port 2 bit 4.

5.3 Hardware Monitor Interface

SYMBOL	PIN	I/O	DESCRIPTION
VREF	37	AOUT	Reference Voltage (2.048 V).
CPUTIN	38	AIN	The input of temperature sensor 2. It is used for CPU temperature sensing.
SYSTIN	39	AIN	The input of temperature sensor 1. It is used for system temperature sensing.
OVT#	3	OD_{12}	The output of over temperature Shutdown. This pin indicates the temperature is over the temperature limit. (Default after LRESET#)
SMI#		OD_{12}	System Management Interrupt channel output.

SYMBOL	PIN	I/O	DESCRIPTION
CPUFANIN0	44	I/O_{12ts}	0 to +3 V amplitude fan tachometer input.
SYSFANIN	45		
CPUFANIN1	1	I/O_{12ts}	0 to +3 V amplitude fan tachometer input. (Default)
GP21		I/OD_{12t}	General-purpose I/O port 2 bit 1.
CPUFANOUT0	46	AOUT/ OD_{12}/ O_{12}	DC/PWM fan output control. CPUFANOUT0 is default PWM mode; CPUFANOUT1 and SYSFANOUT are default DC mode.
SYSFANOUT	47		
CPUFANOUT1	2	AOUT/ O_{12}/ OD_{12}	DC/PWM fan output control. (Default) CPUFANOUT0 is default PWM mode; CPUFANOUT1 and SYSFANOUT are default DC mode.
GP20		I/OD_{12t}	General-purpose I/O port 2 bit 0.
FAN_SET	48	IN_{td}	Determines the initial FAN speed. Power on configuration for 2 fan speeds, 50% or 100%. During power-on reset, this pin is pulled down internally and the fan speed is 50%. Only CPUFANOUT0 is supported.
PLED		O_{12}	Power LED output. Drive high 3.3 V after strapping.

5.4 PECI Interface

SYMBOL	PIN	I/O	DESCRIPTION
PECI_REQ#	43	OD_{12}	INTEL® CPU PECI interface.
PECI	42	I/O_{V3}	INTEL® CPU PECI interface. Connect to CPU.
Vtt	41	Power	INTEL® CPU Vtt Power. This pin is connected to GND if the PECI function is not in use.

5.5 Advanced Configuration and Power Interface

SYMBOL	PIN	I/O	DESCRIPTION
GP55	25	I/O_{12t}	General-purpose I/O port 5 bit 5. (Default)
EN_ACPI		IN_{cd}	During VSB power reset (RSMRST), this pin is pulled down internally and is defined as EN_ACPI (enabling particular ACPI functions), which provides the value for CR2Ch bit 4 (EN_ACPI). The PCB layout should reserve space for a 1-kΩ resistor to pull down this pin to ensure successful disabling of particular ACPI functions, and a 1-kΩ resistor is recommended to pull the pin up if wish to enable particular ACPI functions.
SUSLED		O_{12}	Suspended LED output.
PSIN#	24	IN_{tu}	Panel Switch Input. This pin is active-low with an internal pulled-up resistor.

SYMBOL	PIN	I/O	DESCRIPTION
GP56		I/OD_{12t}	General-purpose I/O port 5 bit 6.
PSOUT#	23	OD_{12}	Panel Switch Output. This signal is used to wake-up the system from S3/S5 state. (Default)
GP57		I/OD_{12t}	General-purpose I/O port 5 bit 7.
RSMRST#	30	OD_{12}	Resume reset signal output. (Default)
GP51		I/OD_{12t}	General-purpose I/O port 5 bit 1.
SUSB#	28	IN_t	System S3 state input. (Default)
GP52		I/OD_{12t}	General-purpose I/O port 5 bit 2.
PSON#	27	OD_{12}	Power supply on-off output.
GP53		I/OD_{12t}	General-purpose I/O port 5 bit 3.
PWROK	26	OD_{12}	This pin generates the PWROK signal while 3VCC comes in. (Default)
GP54		I/OD_{12t}	General-purpose I/O port 5 bit 4.
RSTOUT0#	35	OD_{12}	PCI Reset Buffer 0.
RSTOUT2#	33	O_{12}	PCI Reset Buffer 2. (Default)
GP32		I/OD_{12t}	General-purpose I/O port 3 bit 2.

5.6 General Purpose I/O Port

5.6.1 GPIO Power Source

SYMBOL	POWER SOURCE
GPIO port 2 (Bit0-1)	3VCC
GPIO port 2 (Bit4-7)	3VSB
GPIO port 3	3VSB
GPIO port 5	3VSB

5.6.2 GPIO-2 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GP20	2	I/OD_{12t}	General-purpose I/O port 2 bit 0.
CPUFANOUT1		AOUT/ $OD_{12/}$ O_{12}	DC/PWM fan output control. (Default) CPUFANOUT0 is default PWM mode; CPUFANOUT1 and SYSFANOUT are default DC mode.
GP21	1	I/OD_{12t}	General-purpose I/O port 2 bit 1.
CPUFANIN1		I/O_{12ts}	0 to +3 V amplitude fan tachometer input. (Default)
GP24	22	I/OD_{16t}	General-purpose I/O port 2 bit 4.
MDAT		I/OD_{16ts}	PS2 Mouse Data. (Default)
GP25	21	I/OD_{16t}	General-purpose I/O port 2 bit 5.
MCLK		I/OD_{16ts}	PS2 Mouse Clock. (Default)

SYMBOL	PIN	I/O	DESCRIPTION
GP26	19	I/OD_{16t}	General-purpose I/O port 2 bit 6.
KDAT		I/OD_{16ts}	Keyboard Data. (Default)
GP27	18	I/OD_{16t}	General-purpose I/O port 2 bit 7.
KCLK		I/OD_{16ts}	Keyboard Clock. (Default)

5.6.3 GPIO-3 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GP31	34	I/OD_{12t}	General-purpose I/O port 3 bit 1.
VSBGATE#		O_{12}	Switch 3VSB power to memory when in S3 state. The default is disabled while the particular ACPI functions are enabled. The control bit is at Logical Device A, CR [E4h] bit 4.
GP32	33	I/OD_{12t}	General-purpose I/O port 3 bit 2.
RSTOUT2#		O_{12}	PCI Reset Buffer 2. (Default)
GP35	32	I/OD_{12t}	General-purpose I/O port 3 bit 5.
ATXPGD		IN_t	ATX power good input signal. It is connected to the PWROK signal from the power supply for PWROK generation. The default is enabled. (Default)
GP37	20	I/OD_{12t}	General-purpose I/O port 3 bit 7.
SUSC#		IN_t	SLP_S5# input.

5.6.4 GPIO-5 Interface

SYMBOL	PIN	I/O	DESCRIPTION
GP50	31	I/O_{12t}	General-purpose I/O port 5 bit 0. (Default after strapping)
WDTO#		O_{12}	Watchdog Timer output signal.
GP51	30	I/OD_{12t}	General-purpose I/O port 5 bit 1.
RSMRST#		OD_{12}	Resume reset signal output.
GP52	28	I/OD_{12t}	General-purpose I/O port 5 bit 2.
SUSB#		IN_t	System S3 state input.
GP53	27	I/OD_{12t}	General-purpose I/O port 5 bit 3.
PSON#		OD_{12}	Power supply on-off output.
GP54	26	I/OD_{12t}	General-purpose I/O port 5 bit 4.
PWROK		OD_{12}	This pin generates the PWROK signal while 3VCC comes in.
GP55	25	I/O_{12t}	General-purpose I/O port 5 bit 5. (Default)

SYMBOL	PIN	I/O	DESCRIPTION
EN_ACPI		IN_{cd}	During VSB power reset (RSMRST), this pin is pulled down internally and is defined as EN_ACPI (enabling particular ACPI functions), which provides the value for CR2C bit 4 (EN_ACPI). The PCB layout should reserve space for a 1-kΩ resistor to pull down this pin to ensure successful disabling of particular ACPI functions, and a 1-kΩ resistor is recommended to pull the pin up if wish to enable particular ACPI functions. (This pin function is for UBE version only)
SUSLED		O_{12}	Suspended LED output.
GP56	24	I/OD_{12t}	General-purpose I/O port 5 bit 6.
PSIN#		IN_{tu}	Panel Switch Input. This pin is active-low with an internal pulled-up resistor.
GP57	23	I/OD_{12t}	General-purpose I/O port 5 bit 7.
PSOUT#		OD_{12}	Panel Switch Output. This signal is used to wake-up the system from S3/S5 state.

5.7 Particular ACPI Function pins

SYMBOL	PIN	I/O	DESCRIPTION
SUSC#	20	IN_t	SLP_S5# input.
GP37		I/OD_{12t}	General-purpose I/O port 3 bit 7
EN_ACPI	25	IN_{cd}	During VSB power reset (RSMRST), this pin is pulled down internally and is defined as EN_ACPI (enabling particular ACPI functions), which provides the value for CR2Ch bit 4 (EN_ACPI). The PCB layout should reserve space for a 1-kΩ resistor to pull down this pin to ensure successful disabling of particular ACPI functions, and a 1-kΩ resistor is recommended to pull the pin up if wish to enable particular ACPI functions.
GP55		I/O_{12t}	General-purpose I/O port 5 bit 5.
SUSLED		O_{12}	Suspended LED output.
VSBGATE#	34	O_{12}	Switch 3VSB power to memory when in S3 state. The default is disabled while the particular ACPI functions are enabled. The control bit is at Logical Device A, CR[E4h] bit 4.
GP31		I/OD_{12t}	General-purpose I/O port 3 bit 1.
ATXPGD	32	IN_t	ATX power good input signal. It is connected to the PWROK signal from the power supply for PWROK generation. The default is enabled. (Default)
GP35		I/OD_{12}	General-purpose I/O port 3 bit 5.

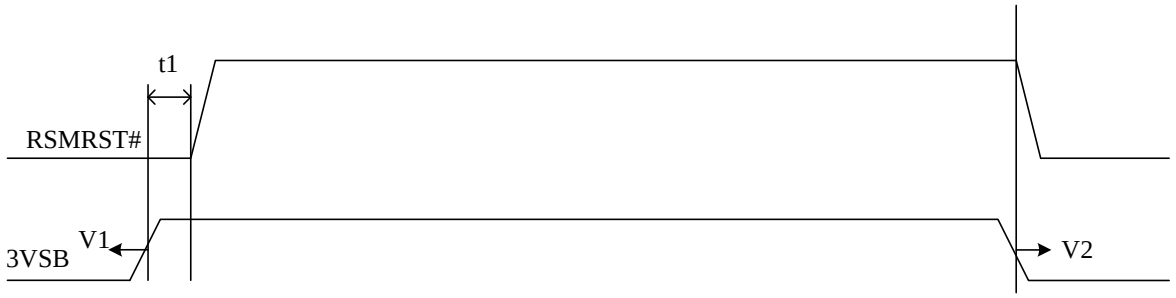
5.8 POWER PINS

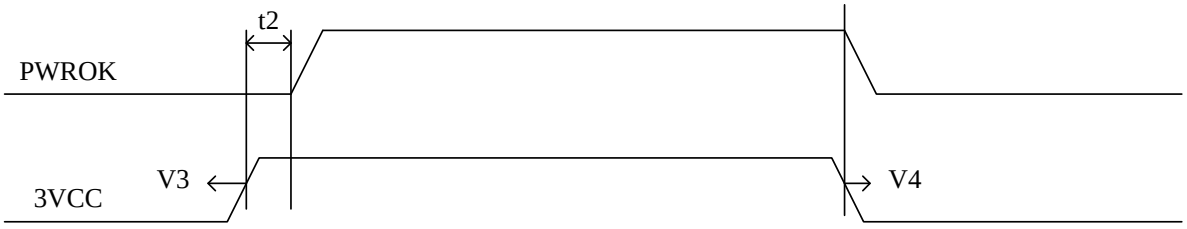
SYMBOL	PIN	DESCRIPTION
3VSB	17	+3.3 V stand-by power supply for the digital circuits.
VBAT	29	+3 V on-board battery for the digital circuits.
3VCC	14	+3.3 V power supply for driving 3 V on host interface.
AVCC	36	Analog +3.3 V power input. Internally supply power to all analog circuits.
CPUD-(AGND)	40	Analog ground. The ground reference for all analog input. Internally connected to all analog circuits.
VSS	5	Ground.
Vtt	41	INTEL® CPU Vtt power.

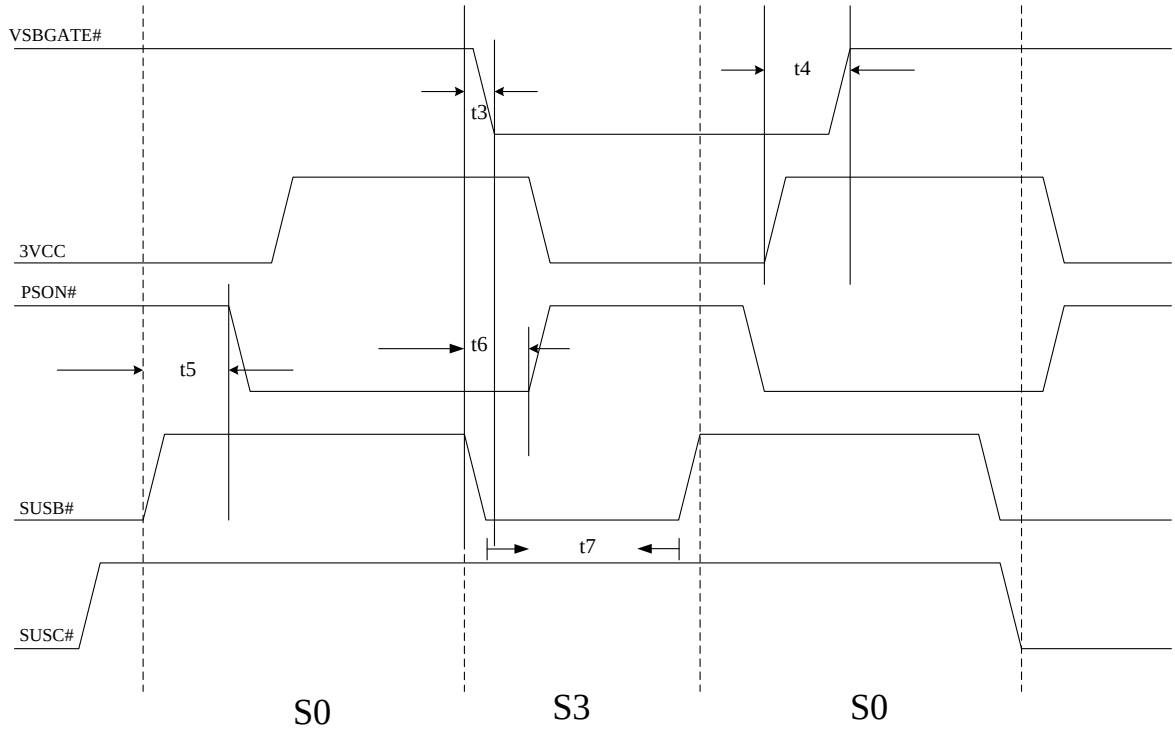
6. ACPI GLUE LOGIC

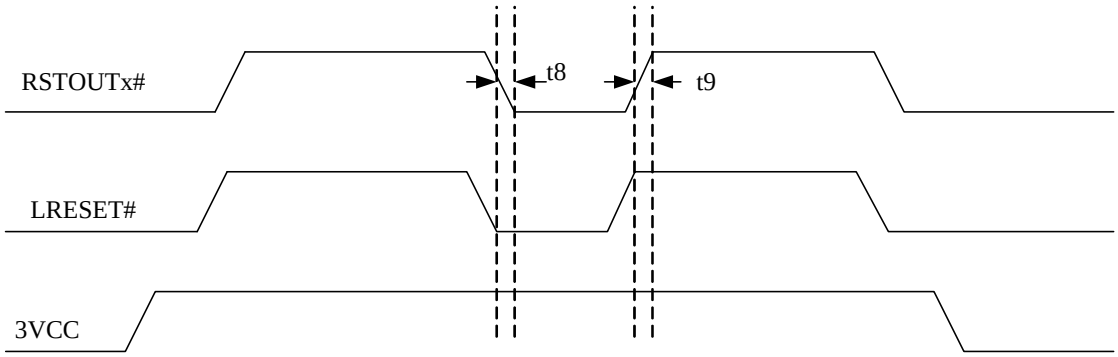
Table 6-1 Pin Description

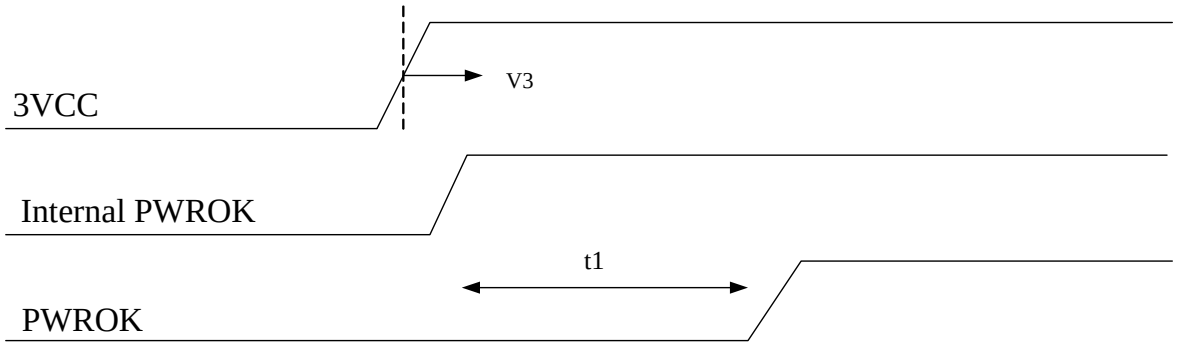
SYMBOL	PIN	DESCRIPTION
SUSC#	20	SLP_S5# input.
VSBGATE#	34	Switch 3VSB power to memory when in S3 state.
PWROK	26	This pin generates the PWRGD signals while 3VCC is present.
ATXPGD	32	ATX power good input signal. It is connected to the PWROK signal from the power supply for PWROK/PWRGD generation. The default is enabled.

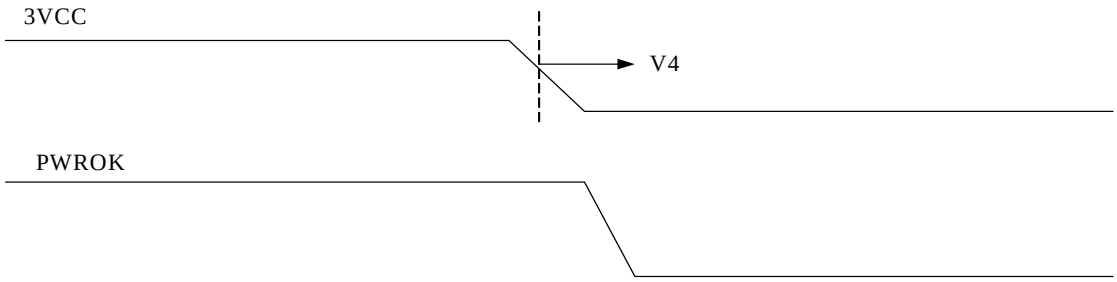





VSBGATE#
t3
t4
3VCC
PSON#
t5
t6
SUSB#
t7
SUSC#
S0
S3
S0


RSTOUTx#
t8
t9
LRESET#
3VCC


3VCC
V3
Internal PWROK
t1
PWROK



TIMING	PARAMETER	MIN	MAX	UNIT
t1	Valid 3VSB to RSMRST# inactive	100	200	mS
t2	Valid 3VCC to PWROK/PWRGD active	300	500	mS
t3	SUSB# active to VSBGATE# active	0	80	nS
t4	PSON# active to VSBGATE# inactive	90	142	mS
t5	SUSB# inactive to PSON# active	0	80	nS
t6	SUSB# active to PSON# inactive	15	45	mS
t7	SUSB# minimal Low Time	40	-	mS
t8	LRESET# active to RSTOUTx# active	0	80	nS
t9	LRESET# inactive to RSTOUTx# inactive	0	80	nS

DC	PARAMETER	MIN	MAX	UNIT
V1	3VSB Valid Voltage	-	3.0	Volt
V2	3VSB Ineffective Voltage	2.4	-	Volt
V3	3VCC Valid Voltage	-	3.0	Volt
V4	3VCC Ineffective Voltage	2.4	-	Volt

Note： 1. The values above are the worst-case results of R&D simulation.

7. CONFIGURATION REGISTER ACCESS PROTOCOL

The W83527HG uses Super I/O protocol to access configuration registers to set up different types of configurations. The W83527HG has totally six Logical Devices: Keyboard Controller (Logical Device 5), WDTO# & PLED (Logical Device 8), GPIO2, 3, 5 (Logical Device 9), ACPI (Logical Device A), Hardware Monitor (Logical Device B), and PECI (Logical Device C). Each Logical Device has its own configuration registers (above CR30). The host can access those registers by writing an appropriate Logical Device Number into the Logical Device select register at CR7.

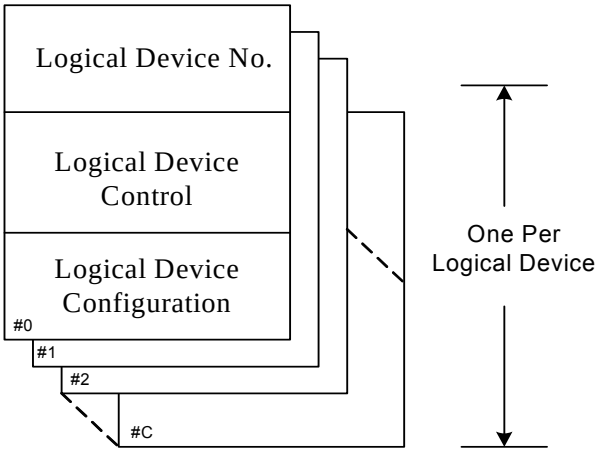


Figure 7-1 Structure of the Configuration Register

Table 7-1 Devices of I/O Base Address

LOGICAL DEVICE NUMBER	FUNCTION	I/O BASE ADDRESS
0	Reserved	
1	Reserved	
2	Reserved	
3	Reserved	
4	Reserved	
5	Keyboard Controller	100h ~ FFFh
6	Reserved	
7	Reserved	
8	PLED	Reserved
9	GPIO 2, 3, 5	Reserved
A	ACPI	Reserved
B	Hardware Monitor	100h ~ FFEh
C	PECI	Reserved

7.1 Configuration Sequence

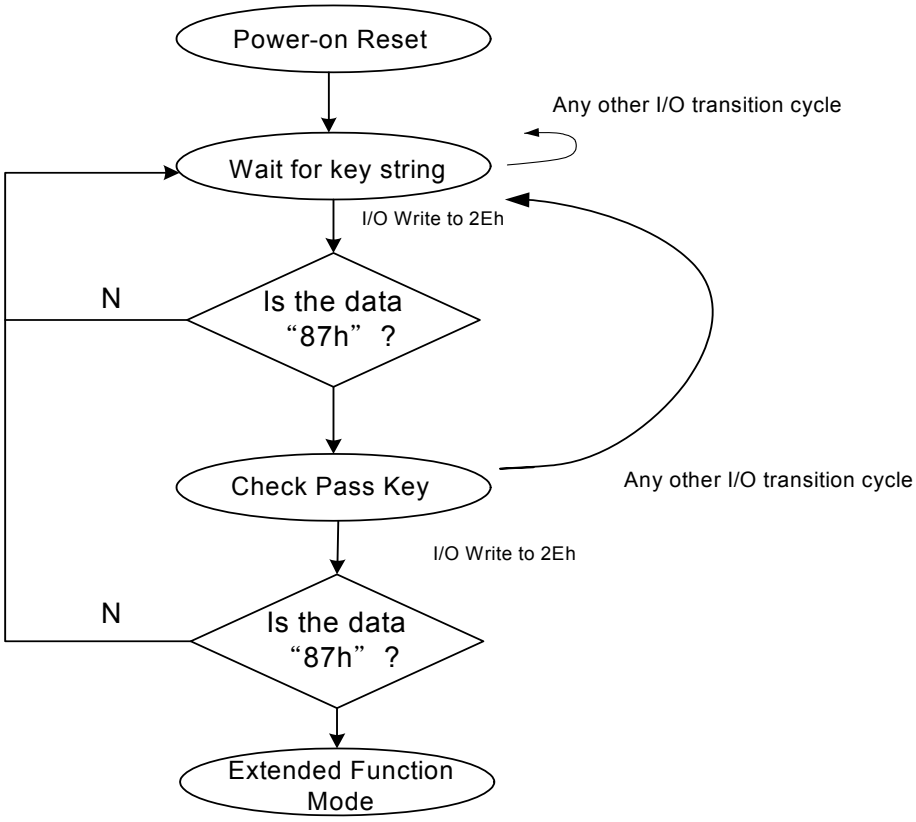


Figure 7-2 Configuration Register

To program the W83527HG configuration registers, the following configuration procedures must be followed in sequence:

(1). Enter the Extended Function Mode.

(2). Configure the configuration registers.

(3). Exit the Extended Function Mode.

7.1.1 Enter the Extended Function Mode

To place the chip into the Extended Function Mode, two successive writes of 0x87 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

7.1.2 Configure the Configuration Registers

The chip selects the Logical Device and activates the desired Logical Devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). The EFIR is located at the same address as the EFER, and the EFDR is located at address (EFIR+1).

First, write the Logical Device Number (i.e. 0x07) to the EFIR and then write the number of the desired Logical Device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required.

Secondly, write the address of the desired configuration register within the Logical Device to the EFIR and then write (or read) the desired configuration register through the EFDR.

7.1.3 Exit the Extended Function Mode

To exit the Extended Function Mode, writing 0xAA to the EFER is required. Once the chip exits the Extended Function Mode, it is in the normal running mode and is ready to enter the configuration mode.

7.1.4 Software Programming Example

The following example is written in Intel 8086 assembly language. It assumes that the EFER is located at 2Eh, so the EFIR is located at 2Eh and the EFDR is located at 2Fh. If the HEFRAS (CR26 bit 6) is set, 2Eh can be directly replaced by 4Eh and 2Fh replaced by 4Fh.

```
;----------------------------------------------------
; Enter the Extended Function Mode
;----------------------------------------------------
MOV    DX, 2EH
MOV    AL, 87H
OUT    DX, AL
OUT    DX, AL
;--------------------------------------------------------------------------
; Configure Logical Device 1, Configuration Register CRF0
;--------------------------------------------------------------------------
MOV    DX, 2EH
MOV    AL, 07H
OUT    DX, AL          ; point to Logical Device Number Reg.
MOV    DX, 2FH
MOV    AL, 01H
OUT    DX, AL          ; select Logical Device 1
;
MOV    DX, 2EH
MOV    AL, F0H
OUT    DX, AL          ; select CRF0
MOV    DX, 2FH
```

```
MOV     AL, 3CH
OUT     DX, AL              ; update CRF0 with value 3CH
;-------------------------------------------------------------------------
; Exit the Extended Function Mode
;-------------------------------------------------------------------------
MOV     DX, 2EH
MOV     AL, AAH
OUT     DX, AL
```

Table 7-2 Chip (Global) Control Registers

INDEX	R/W	DEFAULT VALUE	DESCRIPTION
02h	Write Only		Software Reset
07h	R/W	00h	Logical Device
20h	Read Only	B0h	Chip ID, MSB
21h	Read Only	7xh	Chip ID, LSB
22h	R/W	FFh	Device Power Down
23h	R/W	00h	Immediate Power Down
24h	R/W	0100_0ss0b	Global Option
25h	R/W	00h	Interface Tri-state Enable
26h	R/W	0s000000b	Global Option
27h	Reserved		
28h	R/W	50h	Global Option
29h	R/W	00h	Multi-function Pin Selection
2Ah	R/W	00h	Reserved
2Bh	Reserved		
2Ch	R/W	E2h	Multi-function Pin Selection
2Dh	R/W	21h	Multi-function Pin Selection
2Eh	R/W	00h	Reserved
2Fh	R/W	00h	Reserved

S: Strapping; x: chip version.

8. HARDWARE MONITOR

8.1 General Description

The W83527HG monitors several critical parameters in PC hardware, including fan speeds and temperatures, all of which are very important for a high-end computer system to work stably and properly.

The W83527HG can simultaneously monitor all of the following inputs:

- Four intrinsic voltage inputs: VBAT, 3VSB, 3VCC and AVCC power
- Three fan tachometer inputs
- Two remote temperatures, by thermistor or from the CPU thermal-diode output (voltage or Current Mode)

These inputs are converted to digital values using a built-in, eight-bit analog-to-digital converter (ADC).

In response to these inputs, the W83527HG can generate the following outputs:

- Three PWM (pulse width modulation) or DC fan outputs for the fan speed control
- SMI#
- OVT# signals for system protection events

The W83527HG provides hardware access to all monitored parameters through the LPC or I^2C interface and software access through application software, such as Nuvoton's Hardware Doctor™, or BIOS. In addition, the W83527HG can generate pop-up warnings or beep tones when a parameter goes outside of a user-specified range.

The rest of this section introduces the various features of the W83527HG hardware-monitor capability. These features are divided into the following sections:

- Access Interfaces
- Analog Inputs
- Fan Speed Measurement and Control
- Smart Fan Control
- SMI# interrupt mode
- OVT# interrupt mode
- Registers and Value RAM

8.2 Access Interface

The W83527HG provides LPC interface for the microprocessor to read or write the internal registers of the hardware monitor.

8.2.1 LPC Interface

This interface uses the LPC bus to access the index and data ports. These two ports are located at the 16-bit port specified in CR60 and CR61, plus 5h and 6h, respectively. If the 16-bit port value is 290h, so the default index and data port addresses are 295h and 296h, respectively. The structure of the internal registers is shown in the following figure.

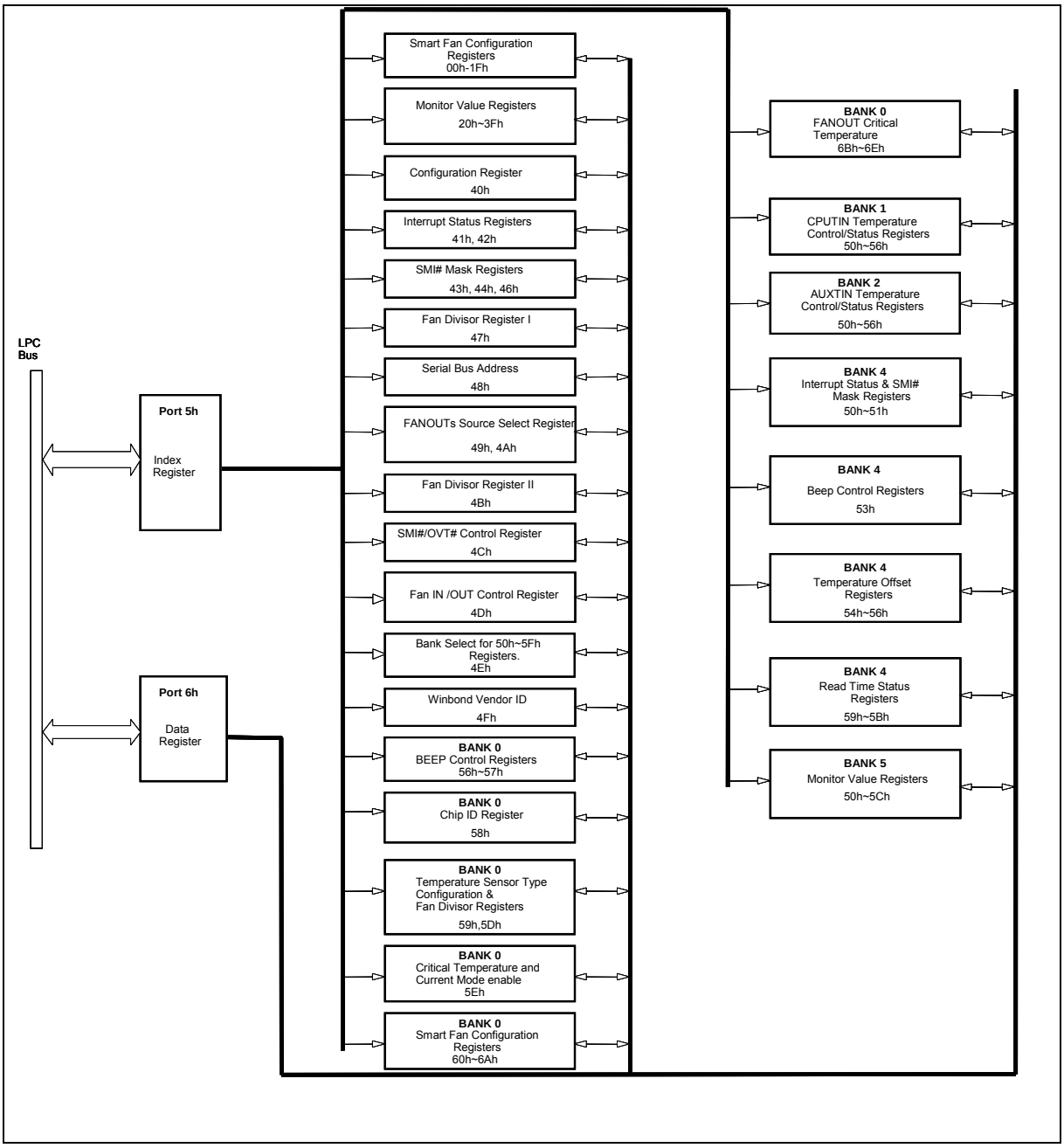


Figure 8-1 LPC Bus' Reads from / Write to Internal Registers

8.3 Analog Inputs

The maximum input voltage on analog pins is 2.048 V because the 8-bit ADC has an 8-mV LSB. Usually, the voltage ports of battery (pin 29), 3VSB (pin 17), 3VCC (pin 14), and AVCC (pin 36) can be directly connected to their respective analog pins, as illustrated in the figure below.

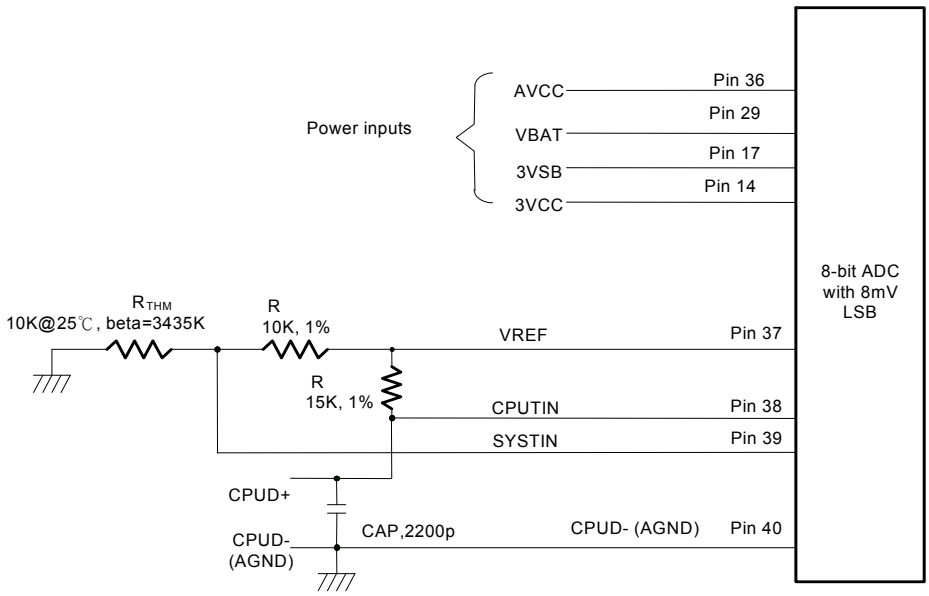


Figure 8-2 Analog Inputs and Application Circuit of the W83527HG

8.3.1 Power Pin Voltage Detection

The W83527HG uses the same approach. Pins 14 and 36 provide two functions. One, these pins are connected to VCC at +3.3 V to supply internal (digital / analog) power to the W83527HG. Two, these pins monitor VCC. The W83527HG has two internal, 34-KΩ serial resistors that reduce the ADC-input voltage to 1.65 V.

$$V_{in} = VCC \times \frac{34K\Omega}{34K\Omega + 34K\Omega} \cong 1.65V$$, where VCC is set to 3.3V

Pin 17 is implemented likewise to monitor its +3.3 V stand-by power supply.

8.3.2 Temperature Sensing

The data format for sensor SYSTIN is 8-bit, two's-complement, and the data format for sensor CPUTIN is 9-bit, two's-complement. This is illustrated in the table below.

Table 8-1 Temperature Data Format

TEMPERATURE	8-BIT DIGITAL OUTPUT		9-BIT DIGITAL OUTPUT	
	8-BIT BINARY	8-BIT HEX	9-BIT BINARY	9-BIT HEX
+125°C	0111,1101	7Dh	0,1111,1010	0FAh

TEMPERATURE	8-BIT DIGITAL OUTPUT		9-BIT DIGITAL OUTPUT	
	8-BIT BINARY	8-BIT HEX	9-BIT BINARY	9-BIT HEX
+25°C	0001,1001	19h	0,0011,0010	032h
+1°C	0000,0001	01h	0,0000,0010	002h
+0.5°C	-	-	0,0000,0001	001h
+0°C	0000,0000	00h	0,0000,0000	000h
-0.5°C	-	-	1,1111,1111	1FFh
-1°C	1111,1111	FFh	1,1111,1110	1FFh
-25°C	1110,0111	E7h	1,1100,1110	1CEh
-55°C	1100,1001	C9h	1,1001,0010	192h

Eight-bit temperature data is read from Index [27h]. For nine-bit temperature data, the 8 MSB are read from Bank1 / Bank2 Index [50h], and the LSB is read from Bank1 / Bank2 Index[51h], bit 7.
There is one source of temperature data: thermal diodes.

8.3.2.1. Monitor Temperature from Thermal Diode (Current Mode)

The W83527HG can also sense the diode temperature through Current Mode and the circuit is shown in the following figure.

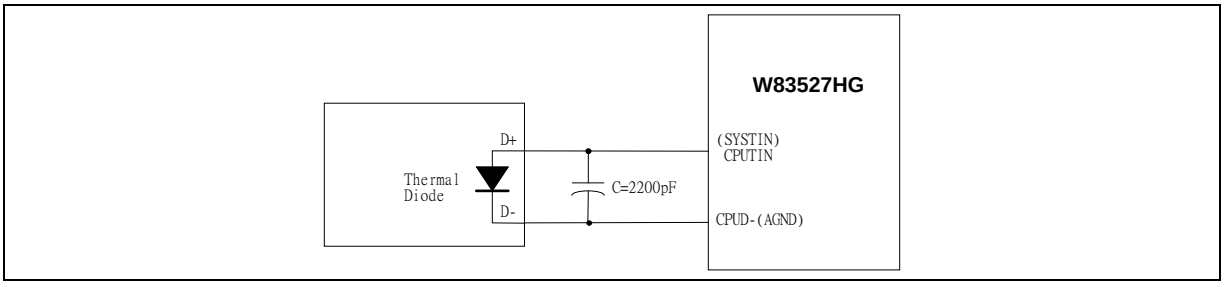


Figure 8-3 Monitoring Temperature from Thermal Diode (Current Mode)

The pin of processor D- is connected to CPUD- (pin 39) and the pin D+ is connected to temperature sensor pin in the W83527HG. A bypass capacitor C=2200pF should be added to filter the high frequency noise.

8.4 PECI

PECI (Platform Environment Control Interface) is a new digital interface to read the CPU temperature of Intel® CPUs. With a bandwidth ranging from 2 Kbps to 2 Mbps, PECI uses a single wire for self-clocking and data transfer. By interfacing to the Digital Thermal Sensor (DTS) in the Intel® CPU, PECI reports a negative temperature (in counts) relative to the processor's temperature at which the thermal control circuit (TCC) is activated. At the TCC Activation temperature, the Intel CPU will operate at reduced performance to prevent the device from thermal damage.

PECI is one of the temperature sensing methods that the W83527HG supports. The W83527HG contains a PECI master and reads the CPU PECI temperature. The CPU is a PECI client.

The PECI temperature values returning from the CPU are in "counts" which are approximately linear in relation to changes in temperature in degrees centigrade. However, this linearity is approximate and cannot be guaranteed over the entire range of PECI temperatures. For further information, refer to the PECI specification. All references to "temperature" in this section are in "counts" instead of "°C".

Figure 8-4 shows a typical fan speed (PWM duty cycle) and PECI temperature relationship.

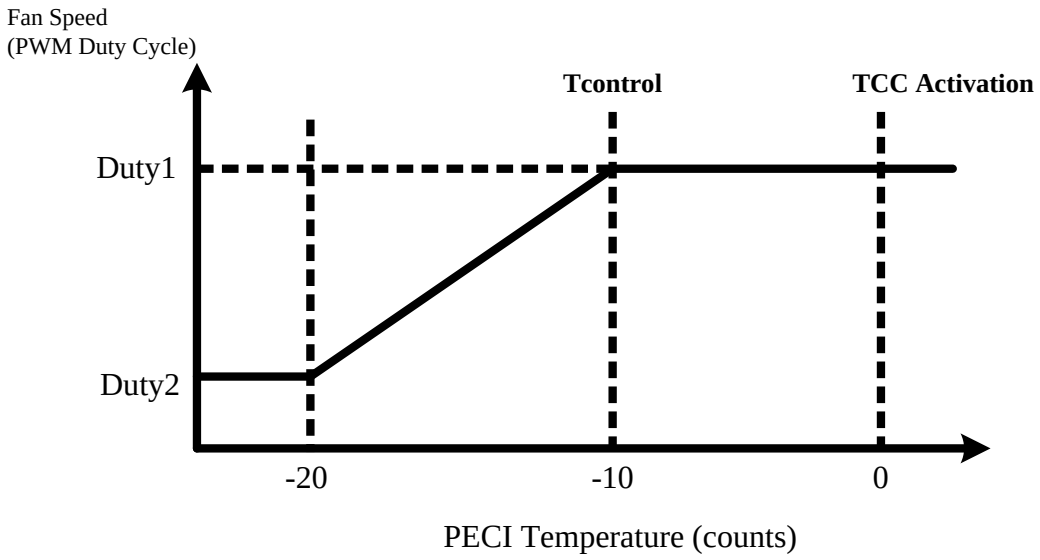


Figure 8-4

In this illustration, when PECI temperature is -20, the PWM duty cycle for fan control is at Duty2. When CPU is getting hotter and the PECI temperature is -10, the PWM duty cycle is at Duty1.

At TControl PECI temperature, the recommendation from Intel is to operate the CPU fan at full speed. Therefore Duty1 is 100% if this recommendation is followed. The value of TControl can be obtained by reading the related Machine Specific Register (MSR) in the Intel CPU. The TControl MSR address is usually in the BIOS Writer's guide for the CPU family in question. Refer to the relevant CPU documentation from Intel for more information. In this example, TControl is -10.

When the PECI temperature is below -20, the duty cycle is fixed at Duty2 to maintain a minimum (and constant) RPM for the CPU fan.

W83527HG's fan control circuit can only accept positive real-time temperature inputs and limits setting (in Smart Fan ™ mode). The device provides offset registers to 'shift' the negative PECI readings to positive values otherwise the fan control circuit will not function properly. The offset registers are the TBase registers located at Logical Device C, CR[E1h]~CR[E4h]. These registers should be programmed with (positive) values so that the resultant value (Tbase + PECI) is always positive. The unit of the TBase register contents is "count" to match that of PECI values. The resultant value (TBase + PECI) should not be interpreted as the "temperature" (whether in count or °C) of the PECI client (CPU).

Figure 8-5 shows the temperature/fan speed relationship after Tbase offsets are applied (based on Figure 8-4). This view is from the perspective of the W83527HG fan control circuit.

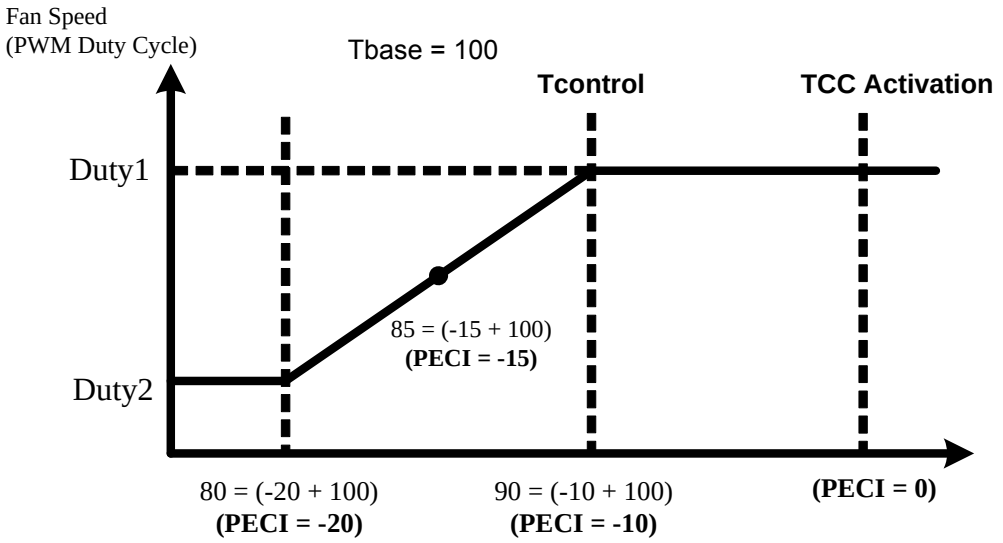


Figure 8-5

Assuming TBase is set to 100 and the PECI temperature is -15 , the real-time temperature value to the fan control circuit will be 85 (-15 + 100). The value of 55 (hex) will appear in the relevant real-time temperature register.

While using Smart Fan control function of W83527HG, BIOS/software must include Tbase in determining the thresholds (limits). In this example, assuming TControl is -10 and Tbase is set to 100 (1), the threshold temperature value corresponding to the "100% fan duty cycle" event is 90 (-10+100). The value of 5A (hex) should be written to the relevant threshold register.

(1) *TControl is typically -10 to -20 for PECI-enabled CPUs. Base on that, a value of 85 ~100 for Tbase could be set for proper operation of the fan control circuit. This recommendation is applicable for most designs. In general, the concept presented in this section could be used to determine the optimum value of TControl to match the specific application.*

8.5 Fan Speed Measurement and Control

This section is divided into two parts, one to measure the speed and one to control the speed.

8.5.1 Fan Speed Measurement

The W83527HG can measure fan speed for fans equipped with tachometer outputs. The tachometer signals should be set to TTL-level, and the maximum input voltage cannot exceed +3.3 V. If the tachometer signal exceeds +3.3 V, an external trimming circuit should be added to reduce the voltage accordingly.

The fan speed counter is read from Bank0 Index 28h, 29h, 2Ah, and 3Fh and Bank5 Index 53h. The fan speed can then be evaluated by the following equation:

$$RPM = \frac{1.35 \times 10^6}{Count \times Divisor}$$

The default divisor is 2 and is specified at Bank0 Index 47h, bits 7 ~ 4; Index 4Bh, bits 7 ~ 6; Index 4Ch, bit 7; Index 59h, bit 7 and bits 3 ~ 2; and Index 5Dh, bits 5 ~ 7. There are three bits for each divisor, and the corresponding divisor is listed in the table below.

Table 8-2 Fan Divisor Definition

BIT 2	BIT 1	BIT 0	FAN DIVISOR	BIT 2	BIT 1	BIT 0	FAN DIVISOR
0	0	0	***1***	1	0	0	***16***
0	0	1	***2***	1	0	1	***32***
0	1	0	***4***	1	1	0	***64***
0	1	1	***8***	1	1	1	***128***

The following table provides some examples of the relationship between divisor, RPM, and count.

Table 8-3 Divisor, RPM, and Count Relation

DIVISOR	NOMINAL RPM	TIME PER REVOLUTION	COUNTS	70% RPM	TIME FOR 70%
1	8800	6.82 ms	*153*	6160	9.84 ms
2 (default)	4400	13.64 ms	*153*	3080	19.48 ms
4	2200	27.27 ms	*153*	1540	38.96 ms
8	1100	54.54 ms	*153*	770	77.92 ms
16	550	109.08 ms	*153*	385	155.84 ms
32	275	218.16 ms	*153*	192	311.68 ms
64	137	436.32 ms	*153*	96	623.36 ms
128	68	872.64 ms	*153*	48	1246.72 ms

8.5.2 Fan Speed Control

The W83527HG has three output pins for fan control, each of which offers PWM duty cycle and DC voltage to control the fan speed. The output type (PWM or DC) of each pin is configured by Bank0 Index 04h, bits 1 ~ 0; Index 12h, bit 0; and Index 62h, bit 6.

For PWM, the duty cycle is programmed by eight-bit registers at Bank0 Index 01h, Index 03h, Index 11h and Index 61h. The duty cycle can be calculated using the following equation:

$$\text{Dutycycle}(\%) = \frac{\text{Programmed 8 - bit Register Value}}{255} \times 100\%$$

The default duty cycle is FFh, or 100%. The PWM clock frequency is programmed at Bank0 Index 00h, Index 02h, Index 10h and Index 60h.

For DC, the W83527HG has a six bit digital-to-analog converter (DAC) that produces 0 to 3.3 Volts DC. The analog output is programmed at Bank0 Index 01h, Index 03h, Index 11h and Index 61h. The analog output can be calculated using the following equation:

$$\text{OUTPUT Voltage (V)} = AVCC \times \frac{\text{Programmed 6 - bit Register Value}}{64}$$

The default value is 111111YY, or nearly 3.3 V, and Y is a reserved bit.

8.5.3 SMART FAN™ Control

The W83527HG supports two SMART FAN™ I features—Thermal Cruise™ mode and Fan Speed Cruise™ mode, SMART FAN™ III features, and SMART FAN™ III+ features. Each of these is discussed in the following sections.

Each fan output and corresponding temperature sensor is illustrated in the figure below.

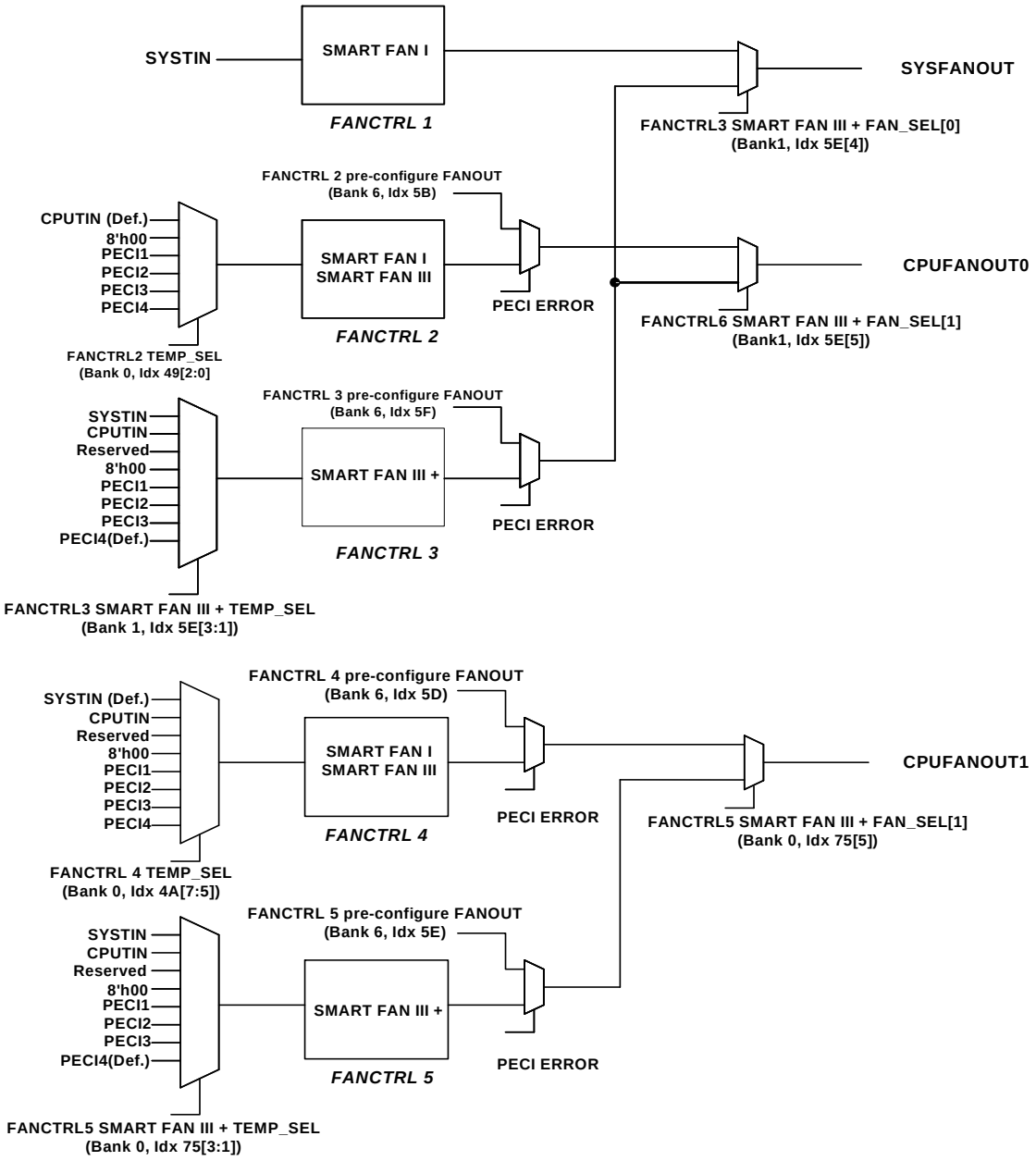


Figure 8-6 FANOUT and Corresponding Temperature Sensors in SMART FAN™ I, III, and III+.

8.5.3.1. Thermal Cruise™ Mode

Three pairs of temperature sensors and fan outputs in Thermal Cruise™ mode:

- SYSTIN and SYSFANOUT
- CPUFANOUT0 and the temperature sensor selected by Bank0 Index 49h, bits 2 ~ 0
- CPUFANOUT1 and the temperature sensor selected by Bank0 Index 4Ah, bits 7 ~ 5

Thermal Cruise™ mode controls the fan speed to keep the temperature in a specified range. First, this range is defined in BIOS by a temperature and the interval (e.g., 55 °C ± 3 °C). As long as the current temperature remains below the low end of this range (i.e., 52 °C), the fan is off. Once the temperature exceeds the low end, the fan turns on at a speed defined in BIOS (e.g., 20% output). Thermal Cruise™ mode then controls the fan output according to the current temperature. Three conditions may occur:

(1) If the temperature still exceeds the high end, fan output increases slowly. If the fan is operating at full speed but the temperature still exceeds the high end, a warning message is issued to protect the system.

(2) If the temperature falls below the high end (i.e., 58 °C) but remains above the low end (e.g., 52 °C), fan output remains the same.

(3) If the temperature falls below the low end (e.g., 52 °C), fan output decreases slowly to zero or to a specified "stop value". This stop value is enabled by Bank0 Index 12h, bits 3 ~ 5, and the value itself is specified in Bank0 Index 08h, Index 09h, Index 15h, and Index 64h. The fan remains at the stop value for the period of time defined in Bank0 Index 0Ch, Index 0Dh, Index 17h, and Index 66h.

In general, Thermal Cruise™ mode means

- if the current temperature is higher than the high end, increase the fan speed;
- if the current temperature is lower than the low end, decrease the fan speed;
- otherwise, keep the fan speed the same.

The following figures illustrate two examples of Thermal Cruise™ mode.

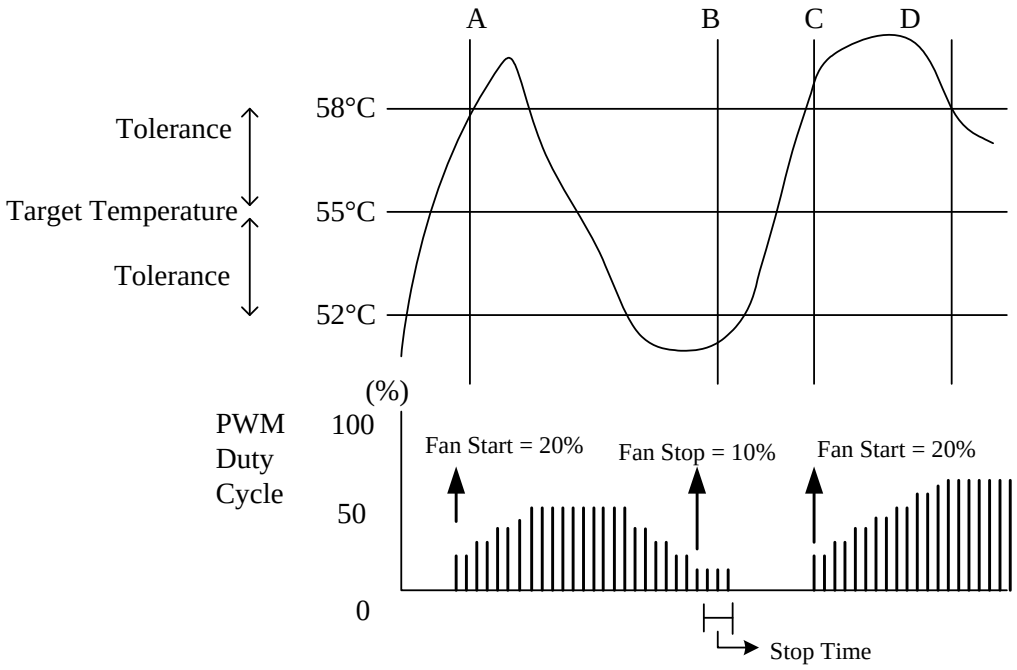


Figure 8-7 Mechanism of Thermal Cruise™ Mode (PWM Duty Cycle)

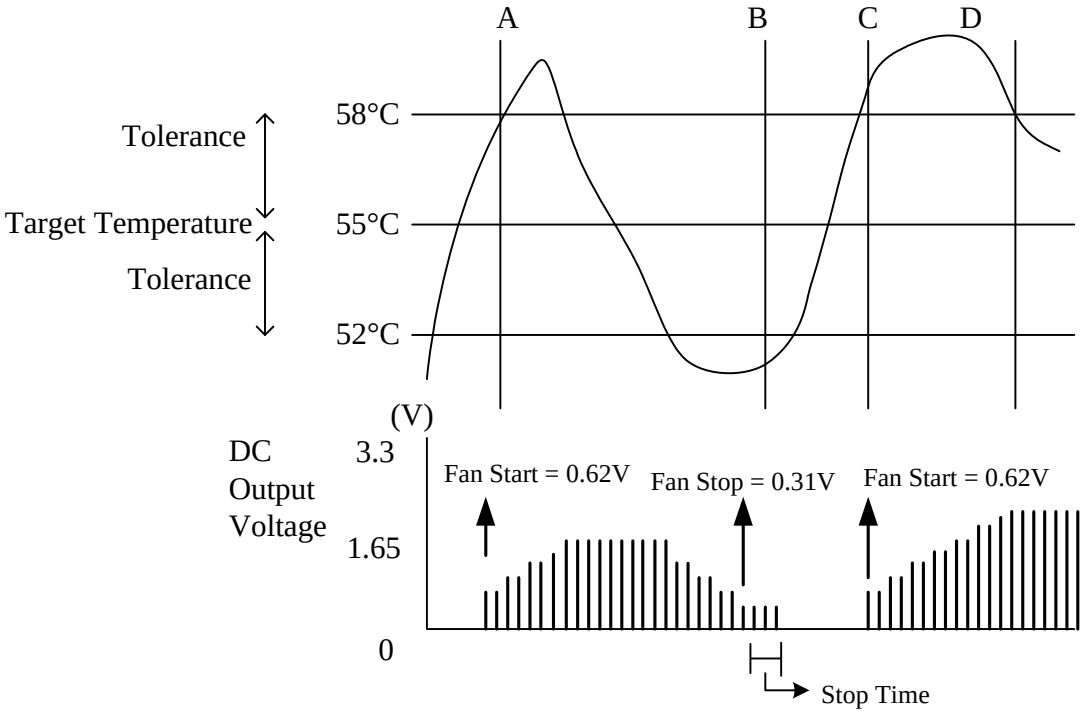


Figure 8-8 Mechanism of Thermal Cruise™ Mode (DC Output Voltage)

8.5.3.2. Fan Speed Cruise™ Mode

Three pairs of fan input sensors and fan outputs in Fan Speed Cruise™ mode.

- SYSFANIN and SYSFANOUT
- CPUFANOUT0 and the temperature sensor selected by Bank0 Index 49h, bits 2 ~ 0
- CPUFANOUT1 and the temperature sensor selected by Bank0 Index 4Ah, bits 7 ~ 5

Fan Speed Cruise™ mode keeps the fan speed in a specified range. First, this range is defined in BIOS by a fan speed count (the amount of time between clock input signals, not the number of clock input signals in a period of time) and an interval (e.g., 160 ± 10). As long as the fan speed count is in the specified range, fan output remains the same. If the fan speed count is higher than the high end (e.g., 170), fan output increases to make the count lower. If the fan speed count is lower than the low end (e.g., 150), fan output decreases to make the count higher. One example is illustrated in this figure.

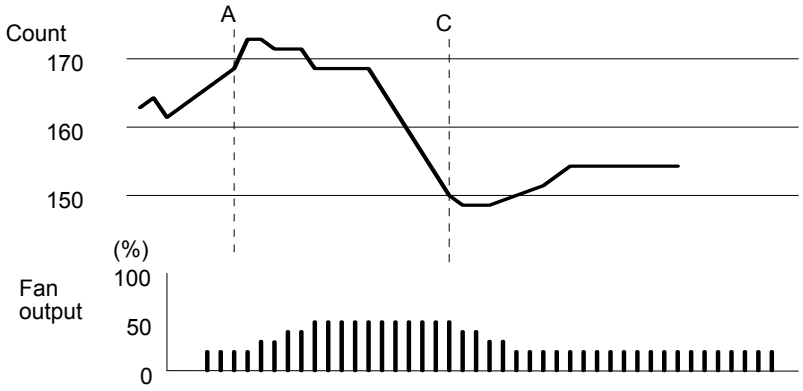


Figure 8-9 Mechanism of Fan Speed Cruise™ Mode

The following tables show current temperatures, fan output values and the relative control registers at Thermal Cruise™ and Fan Speed Cruise™ mode.

Table 8-4 Display Registers - at SMART FAN™ I Mode

DESCRIPTION	REGISTER ADDRESS	REGISTER NAME	ATTRIBUTE	BIT DATA
Current CPU Temperature	Bank1 Index 50h ,51h	CPUTIN Temperature Sensor	Read only	8 MSB, 1°C bit 7, 0.5 °C
Current SYS Temperature	Bank 0 Index 27h	SYSTIN Temperature Sensor	Read only	8 MSB, 1°C
Current CPUFANOUT0 Output Value	Bank0 Index 03h	CPUFANOUT0 Output Value Select	80h / FFh by strapping	bits 7~0 CPUFANOUT0 Value
Current SYSFANOUT Output Value	Bank0 Index 01h	SYSFANOUT Output Value Select	FFh	bits 7~0 SYSFANOUT Value
Current CPUFANOUT1 Output Value	Bank0 Index 61h	CPUFANOUT1 Output Value Select	80h / FFh by strapping	bits 7~0 CPUFANOUT1 Value

Table 8-5 Relative Registers - at Thermal Cruise™ Mode

THERMAL-CRUISE™ MODE	TARGET TEMPERATURE	TOLERANCE	START-UP VALUE	STOP VALUE	KEEP MIN. FAN OUTPUT VALUE	STOP TIME	STEP-DOWN TIME	STEP-UP TIME
SYSFANOUT	Bank0, 05h	Bank0, 07h Bit0-3	Bank0, 0Ah	Bank0, 08h	Bank0, 12h, Bit5	Bank0, 0Ch	Bank0, 0Eh	Bank0, 0Fh
CPUFANOUT0	Bank0, 06h	Bank0, 07h, Bit4-7	Bank0, 0Bh	Bank0, 09h	Bank0, 12h, Bit4	Bank0, 0Dh		

THERMAL-CRUISE™ MODE	TARGET TEMPERATURE	TOLERANCE	START-UP VALUE	STOP VALUE	KEEP MIN. FAN OUTPUT VALUE	STOP TIME	STEP-DOWN TIME	STEP-UP TIME
CPUFANOUT1	Bank0, 63h	Bank0, 62h, Bit0-3	Bank0, 65h	Bank0, 64h	Bank0, 12h, Bit6	Bank0, 66h		

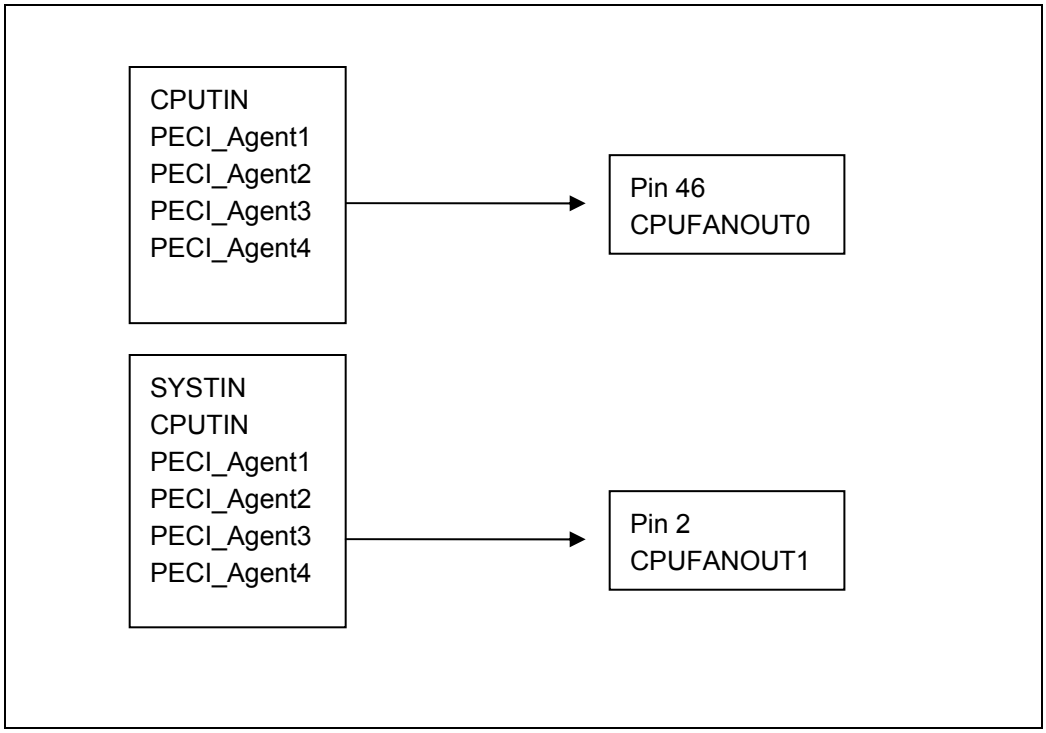
Table 8-6 Relative Registers-at Fan Speed Cruise™ Mode

SPEED CRUISE™ MODE	TARGET-SPEED COUNT	TOLERANCE	KEEP MIN. FAN OUTPUT VALUE	STEP-DOWN TIME	STEP-UP TIME
SYSFANOUT	Bank0, Index 05h	Bank0, Index 07h, bits 0-3	Bank0, Index 12h, Bit5	Bank0, Index 0Eh	Bank0, Index 0Fh
CPUFANOUT0	Bank0, Index 06h	Bank0, Index 07h, bits 4-7	Bank0, Index 12h, Bit4		
CPUFANOUT1	Bank0, Index 63h	Bank0, Index 62h, bits 0-3	Bank0, Index 12h, Bit6		

8.5.3.3. SMART FAN™ III

SMART FAN™ III controls the fan speed so that the temperature meets the target temperature set in BIOS or application software. There are only two pairs of fan outputs and temperature sensors in SMART FAN™ III mode.

- CPUFANOUT0 and the temperature sensor selected by Bank0 Index 49h, bits 2 ~ 0
- CPUFANOUT1 and the temperature sensor selected by Bank0 Index 4Ah, bits 7 ~ 5



The algorithm is as follows:

(1) The target temperature, temperature tolerance, maximum and minimum fan outputs and step are set.

(2) The following figure shows the initial conditions. If the current temperature is within (Target Temperature ± Temperature Tolerance), the fan speed remains constant.

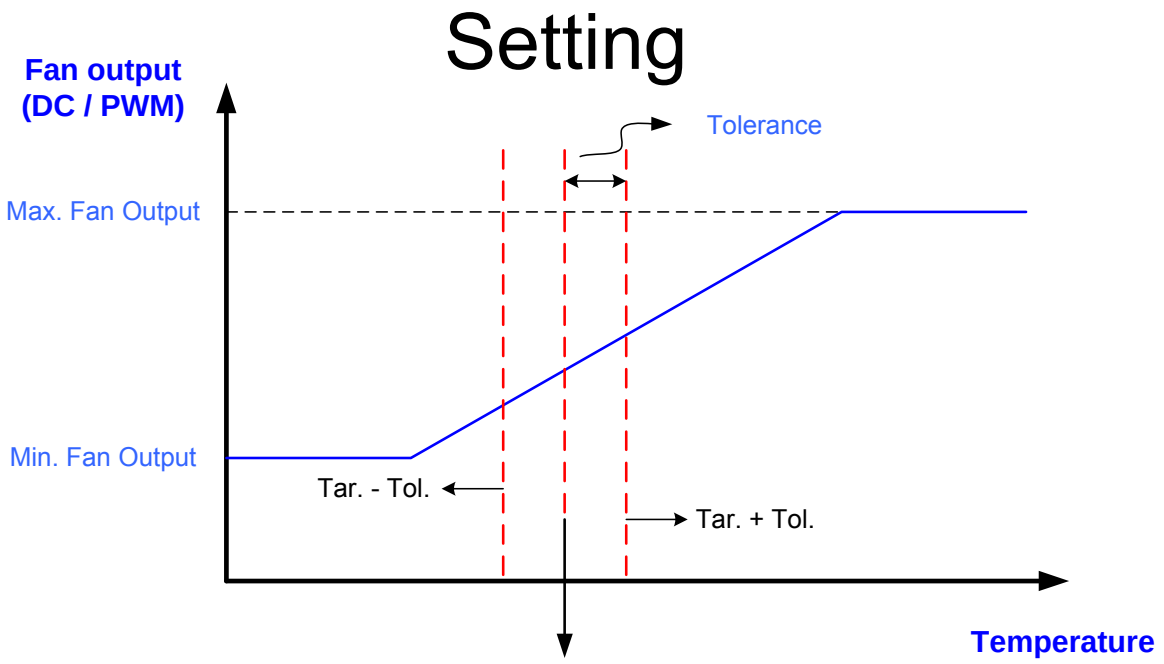


Figure 8-10 Setting of SMART FAN™ III

(3) If the current temperature is higher than (Target Temperature + Temperature Tolerance), fan speed rises one step. The step is the value in the CPUFANOUT Output Value Select Register, Bank0 Index 03h or Index 61h. In addition, the target temperature shifts to (Target Temperature + Temperature Tolerance), creating a new target temperature, named Target Temperature 1 in this figure.

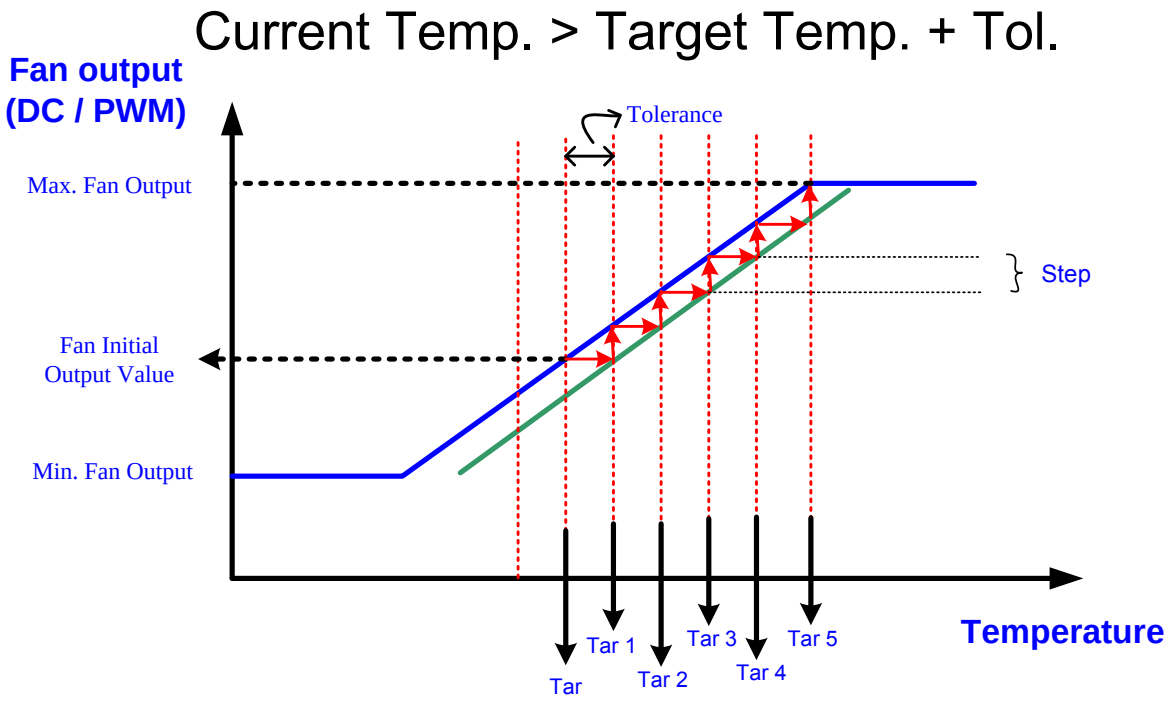


Figure 8-11 SMART FAN™ III Mechanism (Current Temp. > Target Temp. + Tol.)

If the current temperature rises higher than (Target Temperature 1 + Temperature Tolerance), the fan speed rises one step again, and the target temperature shifts to (Target Temperature 1 + Temperature Tolerance), or Target Temperature 2. This process repeats whenever the current temperature is higher than (Target Temperature X ± Temperature Tolerance) or until the fan speed reaches its maximum speed.

(4) If the current temperature falls below (Target Temperature — Temperature Tolerance), the fan speed falls one step. The step is the value in the CPUFANOUT Output Value Select Register, Bank0 Index 03h or Index 61h. In addition, the target temperature shifts to (Target Temperature — Temperature Tolerance), creating a new target temperature named Target Temperature 1.This is illustrated in the figure below.

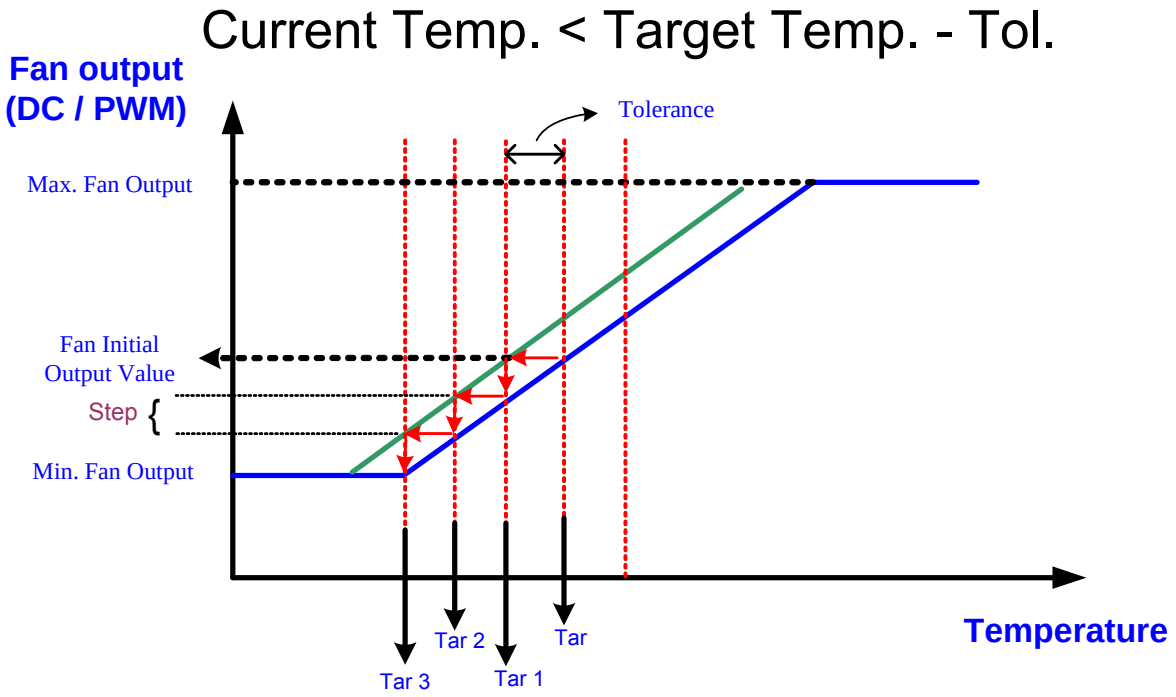


Figure 8-12 SMART FANTM III Mechanism (Current Temp. < Target Temp. - Tol.)

If the current temperature falls lower than (Target Temperature 1 — Temperature Tolerance), the fan speed is reduced one step again, and the target temperature shifts to (Target Temperature 1 — Temperature Tolerance), or Target Temperature 2. This process repeats whenever the current temperature is lower than (Target Temperature X — Temperature Tolerance) or until the fan speed reaches its minimum speed.

(5) If the current temperature is always lower than (Target Temperature X — Temperature Tolerance), the fan speed decreases slowly to zero or to a specified stop value. The stop value is enabled by register Bank0 Index 12h, bit 4 and bit 6, and the stop value is specified in Bank0 Index 09h and Index 64h. The fan remains at the stop value for the period of time defined in Bank0 Index 0Dh and Index 66h.

The following tables show current temperatures, fan output values and the relative control registers at SMART FAN™ III mode.

Table 8-7 Display Register - in SMART FAN™ III Mode

DESCRIPTION	REGISTER ADDRESS	REGISTER NAME	ATTRIBUTE	BIT DATA
Current CPU Temperature	Bank1 Index 50h ,51h	CPUTIN Temperature Sensor	Read only	8 MSB, 1°C bit 7, 0.5 °C
Current SYS Temperature	Bank 0 Index 27h	SYSTIN Temperature Sensor	Read only	8 MSB, 1°C
Current CPUFANOUT0 Output Value	Bank0 Index 03h	CPUFANOUT0 Output Value Select	80h / FFh by strapping	bits 7~0 CPUFANOUT0 Value
Current CPUFANOUT1 Output Value	Bank0 Index 61h	CPUFANOUT1 Output Value Select	80h / FFh by strapping	bits 7~0 CPUFANOUT1 Value

Table 8-8 Relative Register - in SMART FAN™ III Control Mode

SMART FAN™ III MODE	TARGET TEMPERATURE	TOLERANCE	STOP VALUE (MIN. FAN OUTPUT)	MAX. FAN OUTPUT	STOP TIME
CPUFANOUT0	Bank0, Index 06h	Bank0, Index 07h, bits 4-7	Bank0, Index 09h	Bank0, Index 67h	Bank0, Index 0Dh
CPUFANOUT1	Bank0, Index 63h	Bank0, Index 62h, bits 0-3	Bank0, Index 64h	Bank0, Index 69h	Bank0, Index 66h
SMART FAN™ III MODE	**OUTPUT STEP**	**STEP DOWN TIME**	**STEP UP TIME**	**KEEP MIN. FAN OUTPUT VALUE**	**INITIAL VALUE**
CPUFANOUT0	Bank0, Index 68h	Bank0, Index 0Eh	Bank0, Index 0Fh	Bank0, Index 12h, bit 4	Bank0, Index 03h
CPUFANOUT1	Bank0, Index 6Ah			Bank0, Index 12h, bit 6	Bank0, Index 03h

8.5.3.4. SMART FAN™ III+

SMART FAN™ III+ offers 2 slopes to control the fan speed. There are three fan outputs and temperature sensors in SMART FAN™ III+ mode.

- The temperature sensor is selected by Bank0 Index 75h, bits 3~1 & Bank1 Index 5Eh, bits 3~1.
- The fan output (SYSFANOUT, CPUFANOUT0 & CPUFANOUT1) is selected by Bank0 Index 75, bits 5~4 & Bank1 Index 5Eh, bit 5~4.

The 2 slopes can be obtained by setting PWM1~PWM3 and Temperature1~Temperature3 through the registers. When the temperature changes, FAN Output will calculate the DC/PWM output based on the current slope. For example, in the following figure, T1~T3 are the temperature set and DC/PWM1 ~ DC/PWM3 are the fan output set. Assume Tx and Ty are the current temperature and DC/PWMx and DC/PWMy are the fan outputs, then

The slope:

$$X = \frac{(DC/PWM2)-(DC/PWM1)}{(T2-T1)}$$

$$Y = \frac{(DC/PWM3)-(DC/PWM2)}{(T3-T2)}$$

Fan Output:

$$DC/PWMx = (DC/PWM1)+(Tx-T1)\cdot X$$

$$DC/PWMy = (DC/PWM2)+(Ty-T2)\cdot Y$$

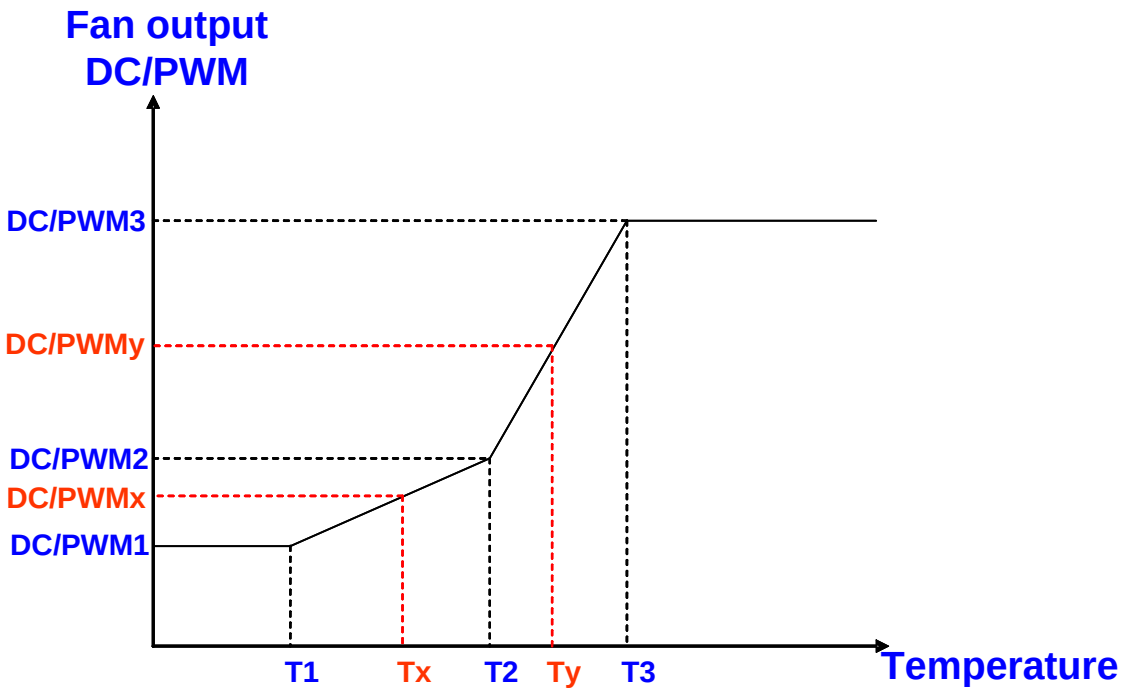


Figure 8-19 SMART FAN™ III+ Mechanism

Table 8-9 Display Registers - in SMART FAN™ III+ Mode

DESCRIPTION	REGISTER ADDRESS	REGISTER NAME	ATTRIBUTE
FANCTRL3 SMART FAN™ III + Temperature 1	Bank1 Index 58h	FANCTRL3 SMART FAN™ III + Temperature 1	Read / Write
FANCTRL3 SMART FAN™ III + Temperature 2	Bank1 Index 59h	FANCTRL3 SMART FAN™ III + Temperature 2	Read / Write
FANCTRL3 SMART FAN™ III + Temperature 3	Bank1 Index 5Ah	FANCTRL3 SMART FAN™ III + Temperature 3	Read / Write
FANCTRL3 SMART FAN™ III + DC/PWM 1	Bank1 Index 5Bh	FANCTRL3 SMART FAN™ III + DC/PWM 1	Read / Write
FANCTRL3 SMART FAN™ III + DC/PWM 2	Bank1 Index 5Ch	FANCTRL3 SMART FAN™ III + DC/PWM 2	Read / Write
FANCTRL3 SMART FAN™ III + DC/PWM 3	Bank1 Index 5Dh	FANCTRL3 SMART FAN™ III + DC/PWM 3	Read / Write
FANCTRL3 SMART FAN™ III + input source & output FAN select	Bank1 Index 5Eh, bit5-1	FANCTRL3 SMART FAN™ III + input source & output FAN select	Read / Write

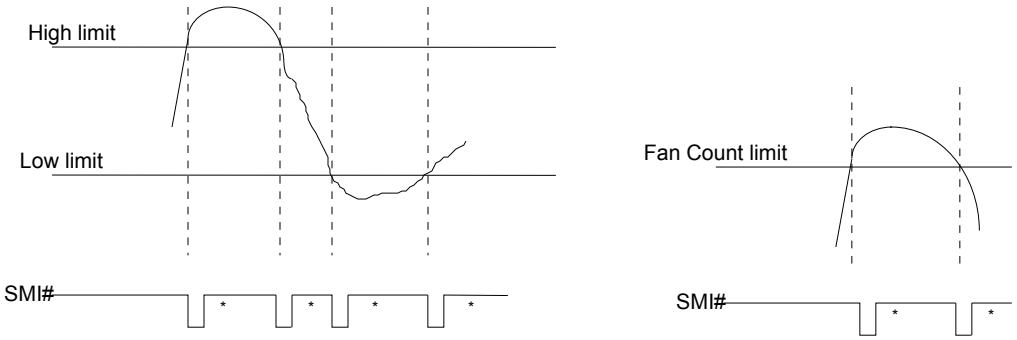
8.6 Interrupt Detection

8.6.1 SMI# Interrupt Mode

The SMI#/OVT# pin (pin 3) is a multi-function pin. It can be in SMI# mode or in OVT# mode by setting Configuration Register CR [29h], bit 6 to one or zero, respectively. In SMI# mode, it can monitor voltages, fan counts, or temperatures.

8.6.1.1. Voltage SMI# Mode

The SMI# pin can create an interrupt if a voltage exceeds a specified high limit or falls below a specified low limit. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This mode is illustrated in the following figure.



*Interrupt Reset when Interrupt Status Registers are read

Figure 8-13 SMI Mode of Voltage and Fan Inputs

8.6.1.2. Fan SMI# Mode

The SMI# pin can create an interrupt if a fan count crosses a specified fan limit (rises above it or falls below it). This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This mode is illustrated in the figure above.

8.6.1.3. Temperature SMI# Mode

The SMI# pin can create interrupts that depend on the temperatures measured by SYSTIN and CPUTIN. These interrupts are divided into two parts, one for SYSTIN and the other for CPUTIN.

8.6.1.3.1 Temperature Sensor 1(SYSTIN) SMI# Interrupt

The SMI# pin has four interrupt modes with SYSTIN.

(1) Shut-down Interrupt Mode

This mode is enabled by setting T_{HYST} (Temperature Hysteresis) lower than T_{OL} and setting Bank0 Index 40h, bit 4 to 1.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_{OL} or Shut-down mode high limit temperature, and when the current temperature falls below T_{HYST} or Shut-down mode low limit temperature. Once the temperature rises above T_{OL}, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_{OL}, until the temperature falls below T_{HYST}. This interrupt must be reset by reading

all the interrupt status registers, or subsequent events do not generate interrupts, except the first time current temperature rises above Shut-down mode high limit temperature. This is illustrated in the following figure.

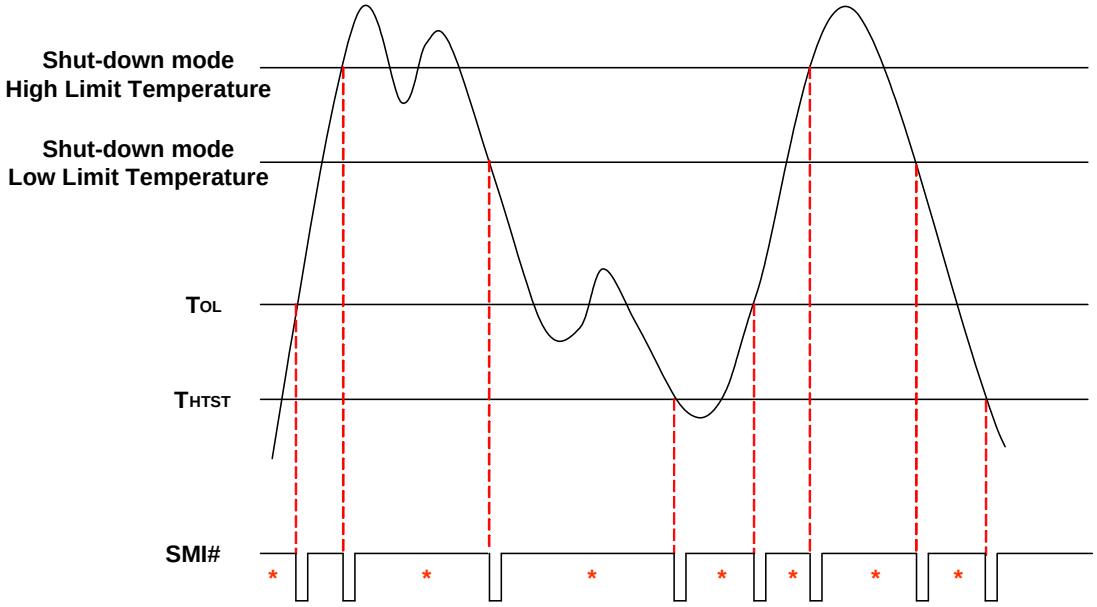
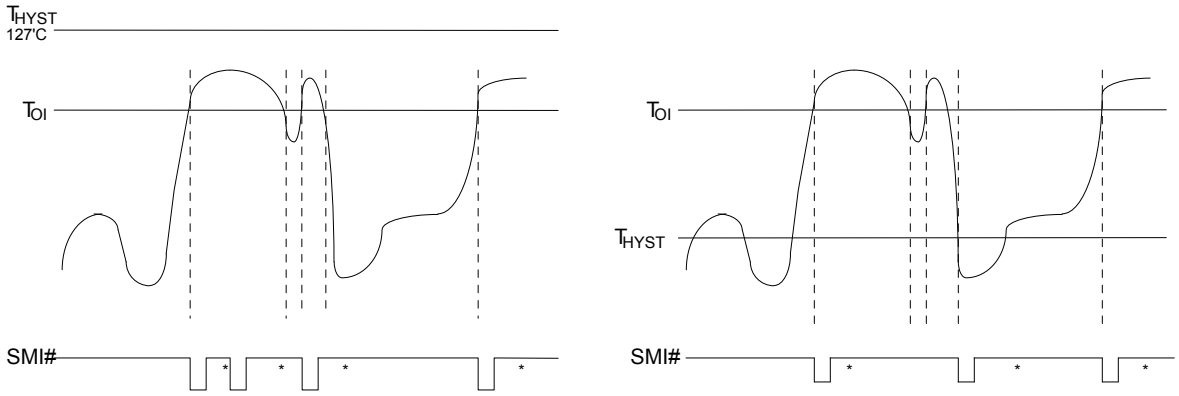


Figure 8-14 Shut-down Interrupt Mode

(2) Comparator Interrupt Mode

This mode is enabled by setting T_{HYST} (Temperature Hysteresis) to 127°C.

In this mode, the SMI# pin can create an interrupt as long as the current temperature exceeds T_O (Over Temperature). This interrupt can be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. If the interrupt is reset, the SMI# pin continues to create interrupts until the temperature goes below T_O. This is illustrated in the figure below.



*Interrupt Reset when Interrupt Status Registers are read

Comparator Interrupt Mode **Two-Time Interrupt Mode**

Figure 8-15 SMI Mode of SYSTIN1

(3) Two-Time Interrupt Mode

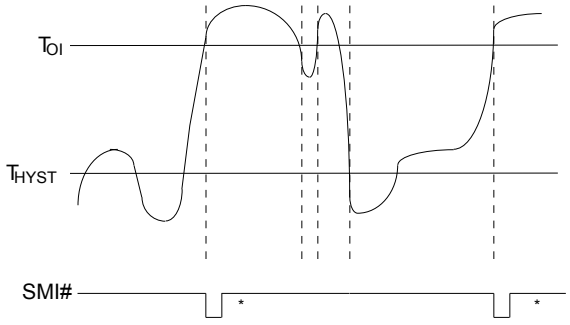
This mode is enabled by setting T_{HYST} (Temperature Hysteresis) lower than T_O and setting Bank0 Index 4Ch, bit 5 to zero.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O or when the current temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure above.

(4) One-Time Interrupt Mode

This mode is enabled by setting T_{HYST} (Temperature Hysteresis) lower than T_O and setting Bank0 Index 4Ch, bit 5 to one.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the following figure.



*Interrupt Reset when Interrupt Status Registers are read

One-Time Interrupt Mode

Figure 8-16 SMI Mode of SYSTIN II

8.6.1.3.1 Temperature Sensor 2(CPUTIN) SMI# Interrupt

The SMI# pin has three interrupt modes with CPUTIN.

(1) Shut-down Interrupt Mode

This mode is enabled by setting Bank0 Index 4Ch, bit 6 to zero and Bank0 Index 40h, bit 6-5 to one.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_{OL} or Shut-down mode high limit temperature, and when the current temperature falls below T_{HYST} or

Shut-down mode low limit temperature. Once the temperature rises above T_{OL}, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_{OL}, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts, except the first time current temperature rises above Shut-down mode high limit temperature. This is illustrated in the following figure.

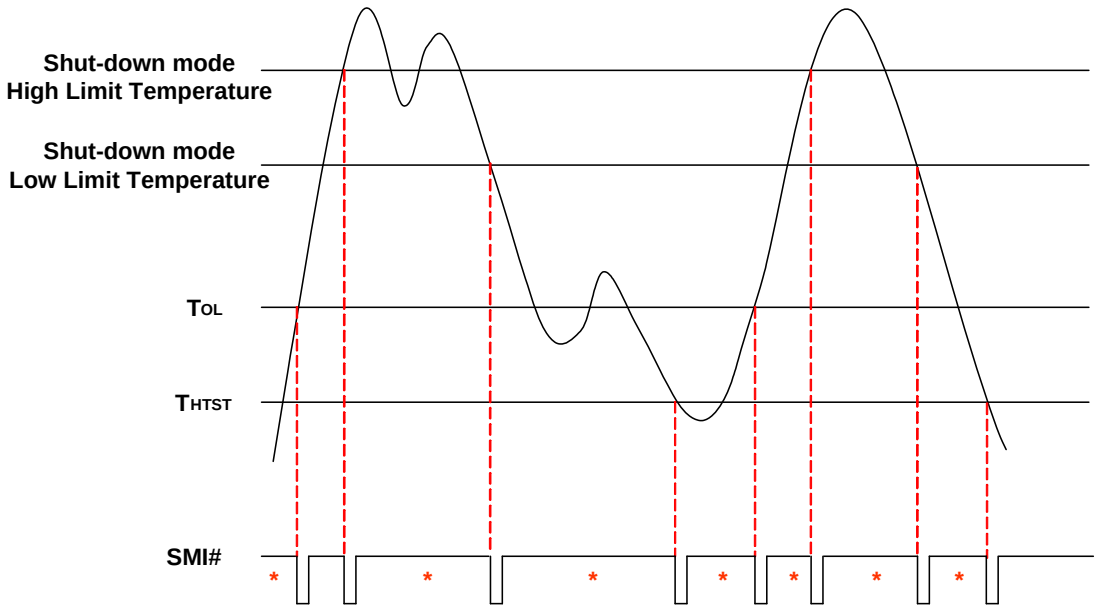
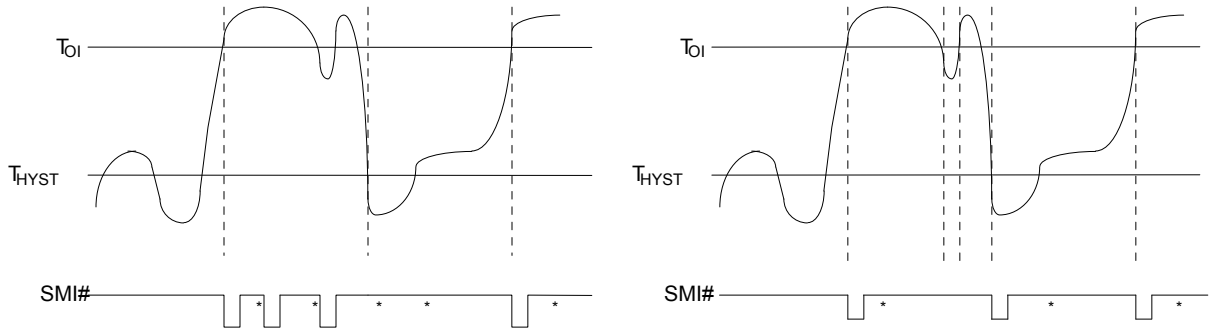


Figure 8-17 Shut-down Interrupt Mode

(2) Comparator Interrupt Mode

This mode is enabled by setting Bank0 Index 4Ch, bit 6, to one.

In this mode, the SMI# pin can create an interrupt when the current temperature exceeds T_O (Over Temperature) and continues to create interrupts until the temperature falls below T_{HYST}. This interrupt can be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure below.



Comparator Interrupt Mode **Two-Time Interrupt Mode**

Figure 8-18 SMI Mode of CPUTIN

(3) Two-Times Interrupt Mode

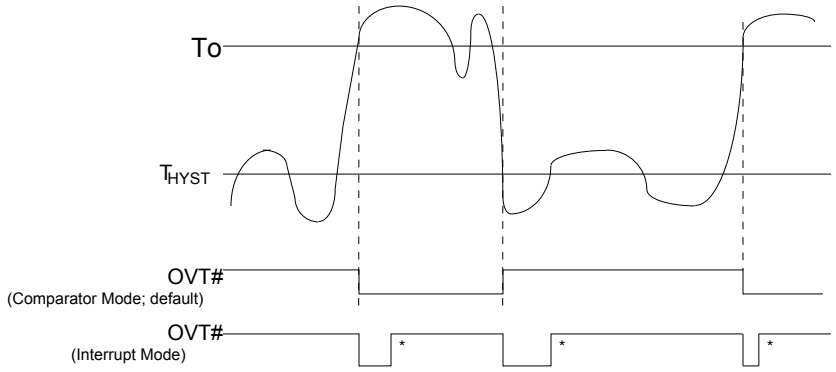
This mode is enabled by setting Bank0 Index 4Ch, bit 6, to zero.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O or when the current temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure above.

8.6.2 OVT# Interrupt Mode

The SMI#/OVT# pin is a multi-function pin. It can be in SMI# mode or in OVT# mode by setting Configuration Register CR [29h], bit 6 to one or zero, respectively. In OVT# mode, it can monitor temperatures, and it is enabled or disabled for SYSTIN and CPUTIN by Bank0 Index 18h, bit 6; Bank0 Index 4Ch, bit 3.

The OVT# pin has two interrupt modes, comparator and interrupt. The modes are illustrated in this figure.



*Interrupt Reset when Temperature sensor registers are read

Figure 8-19 OVT# Modes of Temperature Inputs

If Bank0 Index 18h, bit 4, Bank1 Index 52h, bit 1, and Bank2 Index 52h, bit1 are set to zero, the OVT# pin is in comparator mode. In comparator mode, the OVT# pin can create an interrupt once the current temperature exceeds T_O and continues to create interrupts until the temperature falls below T_{HYST}. The OVT# pin is asserted once the temperature has exceeded T_O and has not yet fallen below T_{HYST}.

If Bank0 Index 18h, bit 4, Bank1 Index 52h, bit1, and Bank2 Index 52h, bit 1 are set to one, the OVT# pin is in interrupt mode. In interrupt mode, the OVT# pin can create an interrupt once the current temperature rises above T_O or when the temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers. The OVT# pin is asserted when an interrupt is generated and remains asserted until the interrupt is reset.

9. HARDWARE MONITOR REGISTER SET

The base address of the Address Port and Data Port is specified in registers CR [60h] and CR [61h] of Device B, the hardware monitor device. CR [60h] is the high byte, and CR [61h] is the low byte. The Address Port and Data Port are located at the base address, plus 5h and 6h, respectively. For example, if CR [60h] is 02h and CR [61h] is 90h, the Address Port is at 0x295h, and the Data Port is at 0x296h.

9.1 Address Port (Port x5h)

Attribute: Bit 6:0 Read/write , Bit 7: Reserved

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	A6	A5	A4	A3	A2	A1	A0
DEFAULT	0	00h (Address Pointer)						

BIT	DESCRIPTION
7	**Reserved.**
6-0	**Read/Write.**

9.2 Data Port (Port x6h)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Data							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Data to be read from or to be written to Value RAM and Register.

9.3 SYSFANOUT PWM Output Frequency Configuration Register - Index 00h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL1	PWM_SCALE1						
DEFAULT	0	0	0	0	0	1	0	0

The register is meaningful only when SYSFANOUT is programmed for PWM output (i.e., Bank0 Index 04h, bit 0 is 0).

BIT	DESCRIPTION
7	**SYSFANOUT PWM Input Clock Source Select.** This bit selects the clock source for PWM output frequency. 0: The clock source is 24 MHz. 1: The clock source is 180 KHz.
6-0	**SYSFANOUT PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. $\text{PWM output frequency} = \frac{\text{Input Clock}}{\text{Pre\_Scale Divider}} * \frac{1}{256}$ The maximum value of the divider is 127 (7Fh), and it should not be set to 0.

9.4 SYSFANOUT Output Value Select Register - Index 01h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT VALUE							
DEFAULT	1	1	1	1	1	1	1	1

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output (Bank 0, Index 04h, bit 0 is 0)	DESCRIPTION	The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
	DEFAULT	1	1	1	1	1	1	1	1
DC Voltage Output (Bank 0, Index 04h, bit 0 is 1)	DESCRIPTION	SYSFANOUT voltage control. The output voltage is calculated according to this equation: **OUTPUT Voltage =** $AVCC * \frac{FANOUT}{64}$						Reserved	
	DEFAULT	1	1	1	1	1	1		

9.5 CPUFANOUT0 PWM Output Frequency Configuration Register - Index 02h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL2	PWM_SCALE2						
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7	**CPUFANOUT0 PWM Input Clock Source Select.** This bit selects the clock source for PWM output. 0: The clock source is 24 MHz. 1: The clock source is 180 KHz.
6-0	**CPUFANOUT0 PWM Pre-Scale divider.** The clock source for PWM output is divided by the seven-bit value to calculate the actual PWM output frequency. **PWM output frequency =** $\frac{\text{Input Clock}}{\text{Pre\_Scale Divider}} * \frac{1}{256}$ The maximum value of the divider is 127 (7Fh), and it should not be set to 0.

The register is meaningful only when CPUFANOUT0 is programmed for PWM output.

9.6 CPUFANOUT0 Output Value Select Register - Index 03h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT0 VALUE							
DEFAULT	Strap by FAN_SET (Pin 48)							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output (Bank 0, Index 04h, bit 1 is 0)	DESCRIPTION	**CPUFANOUT0 PWM Duty Cycle.** The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
	DEFAULT	Strap by FAN_SET (Pin 48)							
DC Voltage Output (Bank 0, Index 04h, bit 1 is 1)	DESCRIPTION	**CPUFANOUT0 Voltage Control.** The output voltage is calculated according to this equation: **OUTPUT Voltage =** $AVCC * \frac{FANOUT}{64}$						Reserved	
	DEFAULT	Strap by FAN_SET (Pin 48)							

9.7 FAN Configuration Register I - Index 04h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		CPUFANOUT0_MODE		SYSFANOUT_MODE		CPUFANOUT0_SEL	SYSFANOUT_SEL
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-6	**Reserved.**
5-4	**CPUFANOUT0 Mode Control.** **Bits** **5 4** 0 0: CPUFANOUT0 is in Manual Mode. (Default) 0 1: CPUFANOUT0 is in Thermal Cruise™ Mode. 1 0: CPUFANOUT0 is in Fan Speed Cruise™ Mode. 1 1: CPUFANOUT0 is in SMART FAN™ III Mode.
3-2	**SYSFANOUT Mode Control.** **Bits** **3 2** 0 0: SYSFANOUT is in Manual Mode. (Default) 0 1: SYSFANOUT is in Thermal Cruise™ Mode. 1 0: SYSFANOUT is in Fan Speed Cruise™ Mode. 1 1: Reserved.
1	**CPUFANOUT0 Output Mode Selection.** 0: CPUFANOUT0 pin produces a PWM output duty cycle. (Default) 1: CPUFANOUT0 pin produces DC output.
0	**SYSFANOUT Output Mode Selection.** 0: SYSFANOUT pin produces a PWM duty cycle output. 1: SYSFANOUT pin produces DC output. (Default)

9.8 SYSTIN Target Temperature Register/ SYSFANIN Target Speed Register - Index 05h (Bank 0)

Attribute: Read/Write
Size: 8 bits

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	Reserved	SYSTIN Target Temperature						
	DEFAULT	0	0	0	0	0	0	0	0
Fan Speed Cruise™	DESCRIPTION	SYSFANIN Target Speed							
	DEFAULT	0	0	0	0	0	0	0	0

9.9 CPUTIN Target Temperature Register/ CPUFANIN0 Target Speed Register - Index 06h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUTIN Target Temperature / CPUFANIN0 Target Speed							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™ or SMART FAN™ III	DESCRIPTION	Reserved	CPUTIN Target Temperature						
	DEFAULT	0	0	0	0	0	0	0	0
Fan Speed Cruise™	DESCRIPTION	CPUFANIN0 Target Speed							
	DEFAULT	0	0	0	0	0	0	0	0

9.10 Tolerance of Target Temperature or Target Speed Register - Index 07h (Bank 0)

Attribute: Read/Write
Size: 8 bits

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™ or SMART FAN™ III	DESCRIPTION	Tolerance of CPUTIN Target Temperature				Tolerance of SYSTIN Target Temperature			
	DEFAULT	0	0	0	0	0	0	0	0
Fan Speed Cruise™	DESCRIPTION	Tolerance of CPUFANIN0 Target Speed				Tolerance of SYSFANIN Target Speed			
	DEFAULT	0	0	0	0	0	0	0	0

9.11 SYSFANOUT Stop Value Register - Index 08h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT STOP VALUE							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise™ mode, the SYSFANOUT value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.12 CPUFANOUT0 Stop Value Register - Index 09h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT0 STOP VALUE							
DEFAULT	0	0	0	0	0	0	0	1

InThermal Cruise™ mode or SMART FAN™ III mode, the CPUFANOUT0 value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.13 SYSFANOUT Start-up Value Register - Index 0Ah (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT START-UP VALUE							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise™ mode, SYSFANOUT value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan.

9.14 CPUFANOUT0 Start-up Value Register - Index 0Bh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT0 START-UP VALUE							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise™ mode, CPUFANOUT0 value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan.

9.15 SYSFANOUT Stop Time Register - Index 0Ch (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT STOP TIME							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise™ mode, if the stop value is enabled, this register determines the amount of time it takes the SYSFANOUT value to fall from the stop value to zero.
(1)For PWM output:
The units are intervals of 0.1 seconds. The default time is 6 seconds.
(2)For DC output:
The units are intervals of 0.4 seconds. The default time is 24 seconds.

9.16 CPUFANOUT0 Stop Time Register - Index 0Dh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT0 STOP TIME							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise™ mode or SMART FAN™ III mode, this register determines the amount of time it takes the CPUFANOUT0 value to fall from the stop value to zero.
(1)For PWM output:
The units are intervals of 0.1 seconds. The default time is 6 seconds.
(2)For DC output:
The units are intervals of 0.4 seconds. The default time is 24 seconds.

9.17 Fan Output Step Down Time Register - Index 0Eh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANOUT VALUE STEP DOWN TIME							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time it takes FANOUT to decrease its value by one step.
(1)For PWM output:
The units are intervals of 0.1 seconds. The default time is 1 seconds.
(2)For DC output:
The units are intervals of 0.4 seconds. The default time is 4 seconds.

9.18 Fan Output Step Up Time Register - Index 0Fh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANOUT VALUE STEP UP TIME							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time it takes FANOUT to increase its value by one step.

(1)For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

(2)For DC output:

The units are intervals of 0.4 second. The default time is 4 seconds.

9.19 FAN Configuration Register II - Index 12h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	CPUFANOUT1 _MIN_VALUE	SYSFANOUT _MIN_VALUE	CPUFANOUT0 _MIN_VALUE	RESERVED			
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**RESERVED.**
6	**CPUFANOUT1_MINT_VALUE.** 0: CPUFANOUT1 value decreases to zero when the temperature goes below the target range. 1: CPUFANOUT1 value decreases to the value specified in Index 64h when the temperature goes below the target range.
5	**SYSFANOUT_MIN_VALUE.** 0: SYSFANOUT value decreases to zero when the temperature goes below the target range. 1: SYSFANOUT value decreases to the value specified in Index 08h when the temperature goes below the target range.
4	**CPUFANOUT0_MIN_VALUE.** 0: CPUFANOUT0 value decreases to zero when the temperature goes below the target range. 1: CPUFANOUT0 value decreases to the value specified in Index 09h when the temperature goes below the target range.
3-0	**RESERVED**

9.20 OVT# Configuration Register - Index 18h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	DIS_OVT1	RESERVED	OVT1_MODE	RESERVED			
DEFAULT	0	1	0	0	0	0	1	1

BIT	DESCRIPTION
7	**RESERVED.**
6	**DIS_OVT1.** 0: Enable SYSTIN OVT# output. (Default) 1: Disable temperature sensor SYSTIN over-temperature (OVT#) output.
5	**RESERVED.**
4	**OVT1_MODE.** 0: Compare Mode. (Default) 1: Interrupt Mode.
3-0	**RESERVED.**

9.21 Reserved Registers - Index 19h ~ 1Fh (Bank 0)

9.22 Value RAM — Index 20h ~ 3Fh (Bank 0)

ADDRESS A6-A0	DESCRIPTION
20h	Reserved
21h	Reserved
22h	AVCC reading
23h	3VCC reading
24h	Reserved
25h	Reserved
26h	Reserved
27h	SYSTIN temperature sensor reading
28h	SYSFANIN reading Note: This location stores the number of counts of the internal clock per revolution.
29h	CPUFANIN0 reading Note: This location stores the number of counts of the internal clock per revolution.
2Ah	Reserved

ADDRESS A6-A0	DESCRIPTION
2Bh	Reserved
2Ch	Reserved
2Dh	Reserved
2Eh	Reserved
2Fh	AVCC High Limit
30h	AVCC Low Limit
31h	3VCC High Limit
32h	3VCC Low Limit
33h	Reserved
34h	Reserved
35h	Reserved
36h	Reserved
37h	Reserved
38h	Reserved
39h	SYSTIN temperature sensor High Limit
3Ah	SYSTIN temperature sensor Hysteresis Limit
3Bh	SYSFANIN Fan Count Limit **Note:** It is the number of counts of the internal clock for the Limit of the fan speed.
3Ch	CPUFANIN0 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Limit of the fan speed.
3Dh	Reserved
3Eh	CPUFANIN1 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Limit of the fan speed.
3Fh	CPUFANIN1 reading Note: This location stores the number of counts of the internal clock per revolution.

9.23 Configuration Register - Index 40h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	INITIALIZATION	Reserved	EN_WS1	EN_WS	INT_CLEAR	RESERVED	SMI#ENABLE	START
DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION
7	**Initialization.** A one restores the power-on default values to some registers. This bit clears itself since the power-on default of this bit is zero.
6	**Reserved.**
5	**EN_WS1.** 1: SMI# output type of temperature CPUTIN is Shut-down Interrupt Mode. 0: SMI# output type is in Shut_down Interrupt Mode. (Default)
4	**EN_WS.** 1: SMI# output type of temperature SYSTIN is Shut-down Interrupt Mode. 0: SMI# output type is in Shut-down Interrupt Mode. (Default)
3	**INT_Clear.** A one disables the SMI# output without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit.
2	**Reserved.**
1	**SMI#Enable.** A one enables the SMI# Interrupt output.
0	**Start.** A one enables startup of monitoring operations. A zero puts the part in standby mode. **Note:** Unlike the "INT_Clear" bit, the outputs of interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred.

9.24 Interrupt Status Register 1 - Index 41h (Bank 0)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN0	SYSFANIN	CPUTIN	SYSTIN	3VCC	AVCC	Reserved	Reserved
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**CPUFANIN0.** A one indicates the fan count limit of CPUFANIN0 has been exceeded.
6	**SYSFANIN.** A one indicates the fan count limit of SYSFANIN has been exceeded.
5	**CPUTIN.** A one indicates the high limit of CPUTIN temperature has been exceeded.
4	**SYSTIN.** A one indicates the high limit of SYSTIN temperature has been exceeded.
3	**3VCC.** A one indicates the high or low limit of 3VCC has been exceeded.
2	**AVCC.** A one indicates the high or low limit of AVCC has been exceeded.
1~0	**Reserved**

9.25 Interrupt Status Register 2 - Index 42h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TAR2	TAR1	Reserved					
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**TAR2.** A one indicates that the CPUTIN temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise™ mode.
6	**TAR1.** A one indicates that the SYSTIN temperature has been over the target temperature for three minutes at full fan speed in Thermal CruiseTM mode.
5~0	**Reserved**

9.26 SMI# Mask Register 1 - Index 43h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN0	SYSFANIN	CPUTIN	SYSTIN	3VCC	AVCC	Reserved	
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION	
7	**CPUFANIN0**	A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 1 – Index 41h (Bank0))
6	**SYSFANIN**	
5	**CPUTIN**	
4	**SYSTIN**	
3	**3VCC**	
2	**AVCC**	
1~0	**Reserved**	

9.27 SMI# Mask Register 2 - Index 44h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TAR2	TAR1	Reserved					
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION	
7	**TAR2**	A one disables the corresponding interrupt status bit for the interrupt. (See Interrupt Status Register 2 – Index 42h (Bank0))
6	**TAR1**	
5~0	**Reserved**	

9.28 Interrupt Status Register 4 - Index 45h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved.						Shut_CPU	Shut_SYS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-2	**Reserved.**
1	**Shut_CPU.** A one indicates the SMI# Shut-down mode high limit of CPUTIN temperature has been exceeded.
0	**Shut_SYS.** A one indicates the SMI# Shut-down mode high limit of SYSTIN temperature has been exceeded.

9.29 SMI# Mask Register 3 - Index 46h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			Shut_CPU	Shut_SYS	RESERVED	CPUFANIN1	RESERVED
DEFAULT	0	0	1	1	1	1	1	1

BIT	DESCRIPTION	
7~5	**Reserved**	
4	**Shut_CPU**	A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 4 – Index 45h (Bank 0)).
3	**Shut_SYS**	
2	**Reserved**	
1	**CPUFANIN1.** A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4)).	
0	**Reserved.**	

9.30 Fan Divisor Register I - Index 47h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN0 DIV_B1	CPUFANIN0 DIV_B0	SYSFANIN DIV_B1	SYSFANIN DIV_B0	FANOPV4	FANINC4	Reserved	
DEFAULT	0	1	0	1	0	1	0	1

BIT	DESCRIPTION	
7	**CPUFANIN0 DIV_B1.**	CPUFANIN0 Divisor, bits 1-0. (See VBAT Monitor Control Register – Index 5Dh (Bank 0))
6	**CPUFANIN0 DIV_B0.**	
5	**SYSFANIN DIV_B1.**	SYSFANIN Divisor, bits 1-0. (See VBAT Monitor Control Register – Index 5Dh (Bank0))
4	**SYSFANIN DIV_B0.**	
3	**FANOPV4. CPUFANIN1 output value**, only if bit 2 is set to zero. Otherwise, this bit has no meaning. 1: Pin 1 (CPUFANIN1) generates a logic-high signal. 0: Pin 1 generates a logic-low signal. (Default)	
2	**FANINC4. CPUFANIN1 Input Control.** 1: Pin 1 (CPUFANIN1) acts as a FAN tachometer input. (Default) 0: Pin 1 acts as a FAN control signal, and the output value is set by register bit 3.	
1~0	**Reserved**	

9.31 Serial Bus Address Register - Index 48h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	SERIAL BUS ADDR.						
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7	**RESERVED.** (Read only)
6-0	**SERIAL BUS ADDR.** Serial Bus address <7:1>.

9.32 CPUFANOUT0 monitor Temperature source select register - Index 49h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED					CPUFANOUT0 TEMP_SEL[2]	CPUFANOUT0 TEMP_SEL[1]	CPUFANOUT TEMP_SEL[0]
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7-3	**RESERVED**	
2	**CPUFANOUT0 TEMP_SEL[2].**	**CPUFANOUT0 Temperature Source Select**. **Bits 2 1 0** 0 0 0: Select CPUTIN as CPUFANOUT0 monitor source. (Default) 0 0 1: Reserved. 0 1 0: Select PECI Agent 1 as CPUFANOUT0 monitor source. 0 1 1: Select PECI Agent 2 as CPUFANOUT0 monitor source. 1 0 0: Select PECI Agent 3 as CPUFANOUT0 monitor source. 1 0 1: Select PECI Agent 4 as CPUFANOUT0 monitor source.
1	**CPUFANOUT0 TEMP_SEL[1].**	
0	**CPUFANOUT0 TEMP_SEL[0].**	

9.33 CPUFANOUT1 Monitor Temperature Source Select Register - Index 4Ah (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT1 TEMP_SEL[2]	CPUFANOUT1 TEMP_SEL[1]	CPUFANOUT1 TEMP[0]	RESERVED				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7	**CPUFANOUT1 TEMP_SEL[2].**	**CPUFANOUT1 Temperature Source Select Bits** **7 6 5** 0 0 0: Select SYSTIN as CPUFANOUT1 monitor source. (Default) 0 0 1: Select CPUTIN as CPUFANOUT1 monitor source. 0 1 0: Reserved. 0 1 1: Reserved. 1 0 0: Select PECI Agent 1 as CPUFANOUT1 monitor source. 1 0 1: Select PECI Agent 2 as CPUFANOUT1 monitor source. 1 1 0: Select PECI Agent 3 as CPUFANOUT1 monitor source. 1 1 1: Select PECI Agent 4 as CPUFANOUT1 monitor source.
6	**CPUFANOUT1 TEMP_SEL[1].**	
5	**CPUFANOUT1 TEMP_SEL[0].**	
4-0	**RESERVED.**	

9.34 Fan Divisor Register II - Index 4Bh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		ADCOVSEL		RESERVED			
DEFAULT	0	1	0	0	0	1	0	0

BIT	DESCRIPTION
7-6	**RESERVED.**
5-4	**ADCOVSEL. A/D Converter Clock Input select.** **Bits** **5 4** 0 0: ADC clock select 22.5 KHz. (Default) 0 1: ADC clock select 5.6 KHz. (22.5K/4) 1 0: ADC clock select 1.4 KHz. (22.5/16) 1 1: ADC clock select 0.35 KHz. (22.5/64)
3-2	**RESERVED.** These two bits should be set to 01h, the default value.
1-0	**RESERVED.**

9.35 SMI#/OVT# Control Register - Index 4Ch (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN1 DIV_B2	T2T3_INT MODE	EN_T1 _ONE	RESERVED	DIS_ OVT2	OVTPOL	RESERVED	
DEFAULT	0	0	0	1	0	0	0	0

BIT	DESCRIPTION
7	**CPUFANIN1 DIV_B2. CPUFANIN1 Divisor bit 2.**
6	**T2T3_INT MODE.** 1: SMI# output type of Temperature CPUTIN is in Comparator Interrupt mode. 0: SMI# output type is in Two-Times Interrupt mode. (Default)
5	**EN_T1_ONE.** 1: SMI# output type of temperature SYSTIN is One-Time Interrupt mode. 0: SMI# output type is Two-Times Interrupt mode. (Default)
4	**RESERVED.**
3	**DIS_OVT2.** 1: Disable temperature sensor CPUTIN over-temperature (OVT) output. 0: Enable CPUTIN OVT output through pin OVT#. (Default)
2	**OVTPOL. Over-temperature polarity.** 1: OVT# active high. 0: OVT# active low. (Default)
1-0	**RESERVED.**

9.36 FAN IN/OUT Control Register - Index 4Dh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				FANOPV2	FANINC2	FANOPV1	FANINC1
DEFAULT	1	0	0	1	0	1	0	1

BIT	DESCRIPTION
7-4	**RESERVED.**
3	**FANOPV2. CPUFANIN0 output value**, only if bit 2 is set to zero. 1: Pin 44 (CPUFANIN0) generates a logic-high signal. 0: Pin 44 generates a logic-low signal. (Default)
2	**FANINC2. CPUFANIN0 Input Control.** 1: Pin 44 (CPUFANIN0) acts as a FAN tachometer input. (Default) 0: Pin 44 acts as a FAN control signal, and the output value is set by bit 3.
1	**FANOPV1. SYSFANIN output value**, only if bit 0 is set to zero.

BIT	DESCRIPTION
	1: Pin 45 (SYSFANIN) generates a logic-high signal. 0: Pin 45 generates a logic-low signal. (Default)
0	**FANINC1. SYSFANIN Input Control.** 1: Pin 45 (SYSFANIN) acts as a FAN tachometer input. (Default) 0: Pin 45 acts as a FAN control signal, and the output value is set by bit 1.

9.37 Register 50h ~ 5Fh Bank Select Register - Index 4Eh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	HBACS	RESERVED		EN_CPUFANIN1_BP	RESERVED	BANKSEL2	BANKSEL1	BANKSEL0
DEFAULT	1	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7	**HBACS. High Byte Access.** 1: Access Index 4Fh high-byte register. (Default) 0: Access Index 4Fh low-byte register.	
6-5	**RESERVED.**	
4	**EN_CPUFANIN1_BP. BEEP output control for CPUFANIN1** if the monitored value exceeds the threshold value. 1: Enable BEEP output. 0: Disable BEEP output. (Default)	
3	**RESERVED.** This bit should be set to 0.	
2	**BANKSEL2.**	Bank Select for Index Ports 0x50h ~ 0x5Fh. The three-bit binary value corresponds to the bank number. For example, “010” selects Bank 2.
1	**BANKSEL1.**	
0	**BANKSEL0.**	

9.38 Nuvoton Vendor ID Register - Index 4Fh (Bank 0)

Attribute: Read Only
Size: 16 bits

BIT	15	14	13	12	11	10	9	8
NAME	VIDH							
DEFAULT	0	1	0	1	1	1	0	0

BIT	7	6	5	4	3	2	1	0
NAME	VIDL							
DEFAULT	1	0	1	0	0	0	1	1

BIT	DESCRIPTION
15-8	Vendor ID High-Byte, if Index 4Eh, bit 7 is 1. Default 5Ch.
7-0	Vendor ID Low-Byte, if Index 4Eh, bit 7 is 0. Default A3h.

9.39 Reserved Register - Index 50h ~ 55h (Bank 0)

9.40 Chip ID - Index 58h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CHIPID							
DEFAULT	1	1	0	0	0	0	0	1

BIT	DESCRIPTION
7-0	CHIPID. Nuvoton Chip ID number. Default C1h.

9.41 Fan Divisor Selection Register - Index 59h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED						CPUFANIN1 DIV_B1	CPUFANIN1 DIV_B0
DEFAULT	0	1	1	1	0	0	0	0

BIT	DESCRIPTION	
7~2	Reserved	
1	**CPUFANIN1 DIV_B1**	CPUFANIN1 Divisor, bits 1-0. (See VBAT Monitor Control Register – Index 5Dh (Bank 0))
0	**CPUFANIN1 DIV_B0**	

9.42 Reserved Register - Index 5Ah ~ 5Ch (Bank 0)

9.43 VBAT Monitor Control Register - Index 5Dh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	CPUFANIN0 DIV_B2	SYSFANIN DIV_B2	RESERVED		DIODES2	DIODES1	EN_VBAT _MNT
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7	**RESERVED**
6	**CPUFANIN0 DIV_B2. CPUFANIN0 Divisor, bit 2.**
5	**SYSFANIN DIV_B2. SYSFANIN Divisor, bit 2.**
4~3	**RESERVED**
2	**DIODES2. Sensor Type Selection for CPUTIN.** 1: Diode sensor. 0: Thermistor sensor.
1	**DIODES1. Sensor Type Selection for SYSTIN.** 1: Diode Sensor. 0: Thermistor sensor.
0	**EN_VBAT_MNT.** 1: Enable battery voltage monitor. When this bit changes from zero to one, it takes one monitor cycle time to update the VBAT reading value register. 0: disable battery voltage monitor.

Fan divisor table:

BIT 2	BIT 1	BIT 0	FAN DIVISOR	BIT 2	BIT 1	BIT 0	FAN DIVISOR
0	0	0	**1**	1	0	0	**16**
0	0	1	**2**	1	0	1	**32**
0	1	0	**4**	1	1	0	**64**
0	1	1	**8**	1	1	1	**128**

9.44 Critical Temperature and Current Mode Enable Register - Index 5Eh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	EN_ CPUFANOUT1 CRITICAL TEMP	RESERVED	EN_ CPUFANOUT CRITICAL TEMP	EN_ SYSFANOUT CRITICAL TEMP	RESERVED	EN_ CPUTIN CURRENT MODE	EN_ SYSTIN CURRENT MODE	RESERVED
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7	**EN_CPUFANOUT1 CRITICAL TEMP.**

BIT	DESCRIPTION
	1: Enable CPUFANOUT1 critical temperature protection. 0: Disable CPUFANOUT1 critical temperature protection. (Default)
6	**RESERVED**
5	**EN_CPUFANOUT CRITICAL TEMP.** 1: Enable CPUFANOUT0 critical temperature protection. 0: Disable CPUFANOUT0 critical temperature protection. (Default)
4	**EN_SYSFANOUT CRITICAL TEMP.** 1: Enable SYSFANOUT critical temperature protection. 0: Disable SYSFANOUT critical temperature protection. (Default)
3	**RESERVED**
2	**EN_CPUTIN CURRENT MODE.** (To enable the current mode, please also set Bank0, Index 5Dh, Bit 2 to '1') 1: Temperature sensing of CPUTIN by Current Mode. (Default) 0: Temperature sensing of CPUTIN depends on the setting of Index 5Dh.
1	**EN_SYSTIN CURRENT MODE.** (To enable the current mode, please also set Bank0, Index 5Dh, Bit 1 to '1') 1: Temperature sensing of SYSTIN by Current Mode. 0: Temperature sensing of SYSTIN depends on the setting of Index 5Dh. (Default)
0	**RESERVED**

9.45 Reserved Register - Index 5Fh (Bank 0)

9.46 CPUFANOUT1 PWM Output Frequency Configuration Register - Index 60h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL4	PWM_SCALE4						
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7	**PWM_CLK_SEL4. CPUFANOUT1 PWM Input Clock Source Select.** This bit selects the clock source for PWM output. 0: The clock source is 24 MHz. 1: The clock source is 180 KHz.
6-0	**PWM_SCALE4. CPUFANOUT1 PWM Pre-Scale Divider.** The clock source of PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. PWM output frequency = $\frac{\text{Input Clock}}{\text{Pre\_Scale Divider}} * \frac{1}{256}$ The maximum value of the divider is 127 (7Fh), and it should not be set to 0.

The register is only meaningful when CPUFANOUT1 is programmed for PWM output.

9.47 CPUFANOUT1 Output Value Select Register - Index 61h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT1 Value							
DEFAULT	0	1	1	1	1	1	1	1

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output (Bank 0, Index 62h, bit 6 is 0)	DESCRIPTION	CPUFANOUT1 PWM Duty Cycle. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and creates a duty cycle of 0%.							
DC Output (Bank 0, Index 62h, bit 6 is 1)	DESCRIPTION	CPUFANOUT1 Voltage Control. The output voltage is calculated according to this equation: **OUTPUT Voltage =** $AVCC * \frac{FANOUT}{64}$						Reserved	

9.48 FAN Configuration Register III - Index 62h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	CPUFANOUT1 _SEL	CPUFANOUT1_MODE		TARGET TEMPERATURE TOLERANCE / CPUFANIN1 TARGET SPEED TOLERANCE			
DEFAULT	0	1	0	0	0	0	0	0

BIT	DESCRIPTION	
7	**RESERVED.**	
6	**CPUFANOUT1_SEL. CPUFANOUT1 Output Mode Selection.** 0: CPUFANOUT1 pin produces a PWM output duty cycle. 1: CPUFANOUT1 pin produces DC output. (Default)	
5-4	**CPUFANOUT1_MODE. CPUFANOUT1 Mode Control.** **Bits** **5 4** 0 0: CPUFANOUT1 is in Manual Mode. (Default) 0 1: CPUFANOUT1 is in Thermal Cruise™ Mode. 1 0: CPUFANOUT1 is in Fan Speed Cruise™ Mode. 1 1: CPUFANOUT1 is in SMART FAN™ III Mode.	
3-0	In Thermal Cruise™ mode or SMART FAN™ III Mode: **Tolerance of select temperature source Target Temperature.**	In Fan Speed Cruise™ mode: **Tolerance of CPUFANIN1 Target Speed.**

9.49 Target Temperature Register/CPUFANIN1 Target Speed Register - Index 63h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Target Temperature / Target Speed							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™ or SMART FAN™ III mode	DESCRIPTION	Reserved	Target Temperature of select temperature source.						
	DEFAULT	0	0	0	0	0	0	0	0
Fan Speed Cruise™	DESCRIPTION	CPUFANIN1 Target Speed							
	DEFAULT	0	0	0	0	0	0	0	0

9.50 CPUFANOUT1 Stop Value Register - Index 64h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT1 STOP VALUE							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise™ mode, the CPUFANOUT1 value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.51 CPUFANOUT1 Start-up Value Register - Index 65h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT1 START-UP VALUE							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise™ mode, CPUFANOUT1 value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan.

9.52 CPUFANOUT1 Stop Time Register - Index 66h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT1 STOP TIME							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise™ mode or SMART FAN™ III mode, if the stop value is enabled, this register determines the amount of time it takes the CPUFANOUT1 value to fall from the stop value to zero.
(1)For PWM output:
The units are intervals of 0.1 second. The default time is 6 seconds.
(2)For DC output:
The units are intervals of 0.4 second. The default time is 24 seconds.

9.53 CPUFANOUT0 Maximum Output Value Register - Index 67h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT0 MAX. VALUE							
DEFAULT	1	1	1	1	1	1	1	1

In SMART FAN™ III mode, the CPUFANOUT0 value increases to this value. This value cannot be zero, and it cannot be lower than the CPUFANOUT0 Stop value.

9.54 CPUFANOUT0 Output Step Value Register - Index 68h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT0 STEP							
DEFAULT	0	0	0	0	0	0	0	1

In SMART FAN™ III mode, the CPUFANOUT0 value decreases or increases by this eight-bit value, when needed.

9.55 CPUFANOUT1 Maximum Output Value Register - Index 69h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT1 MAX. VALUE							
DEFAULT	1	1	1	1	1	1	1	1

In SMART FAN™ III mode, the CPUFANOUT1 value increases to this value. This value cannot be zero, and it cannot be lower than the CPUFANOUT1 Stop value.

9.56 CPUFANOUT1 Output Step Value Register - Index 6Ah (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT1 STEP							
DEFAULT	0	0	0	0	0	0	0	1

In SMART FAN™ III mode, the CPUFANOUT1 value decreases or increases by this eight-bit value, when needed.

9.57 SYSFANOUT Critical Temperature register - Index 6Bh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT THRESHOLD TEMPERATURE							
DEFAULT	1	1	1	1	1	1	1	1

In Thermal Cruise™ mode, when the function of SYSFANOUT temperature sensing is enabled, and the monitored temperature exceeds the threshold temperature, the SYSFANOUT will work at full speed.

9.58 CPUFANOUT0 Critical Temperature Register - Index 6Ch (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT0 CRITICAL TEMPERATURE							
DEFAULT	1	1	1	1	1	1	1	1

In Thermal Cruise™ mode, when the function of CPUFANOUT0 temperature sensing is enabled, and the monitored temperature exceeds the threshold temperature, the CPUFANOUT0 will work at full speed.

9.59 CPUFANOUT1 Critical Temperature Register - Index 6Eh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT1 CRITICAL TEMPERATURE							
DEFAULT	1	1	1	1	1	1	1	1

In Thermal Cruise™ mode, when the function of CPUFANOUT1 temperature sensing is enabled, and the monitored temperature exceeds the threshold temperature, the CPUFANOUT1 will work at full speed.

9.60 FANCTRL5 SMART FAN™ III+ Temperature 1 Register (T1) – Index 6Fh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMART FAN IV III+ Temperature 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SMART FAN™ III+ Temperature 1 Register (T1).**

9.61 FANCTRL5 SMART FAN™ III+ Temperature 2 Register (T2) – Index 70h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMART FAN ™ III+ Temperature 2							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SMART FAN™ III+ Temperature 2 Register (T2).**

9.62 FANCTRL5 SMART FAN™ III+ Temperature 3 Register (T3) – Index 71h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMART FAN ™ III+ Temperature 3							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SMART FAN™ III+-1 Temperature 3 Register (T3).**

9.63 FANCTRL5 SMART FAN™ III+ DC/PWM 1 Register - Index 72h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMART FAN ™ III+ DC/PWM 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SMART FAN™ III+ DC/PWM 1 Register.**

9.64 FANCTRL5 SMART FAN™ III+ DC/PWM 2 Register - Index 73h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMART FAN ™ III+ DC/PWM 2							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SMART FAN™ III+ DC/PWM 2 Register.**

9.65 FANCTRL5 SMART FAN™ III+ DC/PWM 3 Register - Index 74h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMART FAN™ III+ DC/PWM 3							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SMART FAN™ III+ DC/PWM 3 Register.**

9.66 FANCTRL5 SMART FAN™ III+ input source & output FAN select Register - Index 75h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		FANCTRL5 SMART FAN™ III+ FAN_SEL		FANCTRL5 SMART FAN™ III+ TEMP_SEL			Reserved
DEFAULT	0	0	0	0	1	1	1	0

BIT	DESCRIPTION
7-6	**Reserved.**
5-4	**FANCTRL5 SMART FAN™ III+ FAN_SEL.** **Bits** **5 4** 0 0: SMART FAN™ I or III → CPUFANOUT1 0 1: SMART FAN™ I or III → CPUFANOUT1 1 0: SMART FAN™ III+ → CPUFANOUT1 1 1: SMART FAN™ III+ → CPUFANOUT1
3-1	**FANCTRL5 SMART FAN™ III+ TEMP_SEL .** **Bits** **3 2 1** 0 0 0: SYS Temperature 0 0 1: CPU Temperature 0 1 0: Reserved 0 1 1: PECI1 1 0 0: PECI2 1 0 1: PECI3

BIT	DESCRIPTION
	1 1 0: PECI4 1 1 1: 8'h00 (Default)
0	**Reserved.**

9.67 SYSTIN SMI# Shut-down mode High Limit Temperature Register - Index 76h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSTIN SMI# Shut-down mode High Limit Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SYSTIN SMI# Shut-down mode High Limit Temperature.**

9.68 SYSTIN SMI# Shut-down mode Low Limit Temperature Register - Index 77h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSTIN SMI# Shut-down mode Low Limit Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SYSTIN SMI# Shut-down mode Low Limit Temperature.**

9.69 CPUTIN SMI# Shut-down mode High Limit Temperature Register - Index 78h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUTIN SMI# Shut-down mode High Limit Temperature							

DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUTIN SMI# Shut-down mode High Limit Temperature.**

9.70 CPUTIN SMI# Shut-down mode Low Limit Temperature Register - Index 79h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUTIN SMI# Shut-down mode Low Limit Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUTIN SMI# Shut-down mode Low Limit Temperature.**

9.71 Temperature selection Register - Index 7Ch (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved			MNTEMP2_SEL	MNTEMP1_SEL	Tread_SEL		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**Reserved.**
4	**MNTEMP2_SEL.** 0: CPUTIN Temperature (Default) 1: PECI1
3	**MNTEMP1_SEL.** 0: SYSTIN Temperature (Default) 1: PECI1
2-0	**Tread_SEL. (see Temperature Register – Index 7Dh (Bank 0))** **Bits** **2 1 0** 0 0 0: SYSTIN Temperature (Default) 0 0 1: CPUTIN Temperature 0 1 0: Reserved 0 1 1: 8'h00

BIT	DESCRIPTION
	1 0 0: PECI1 1 0 1: PECI2 1 1 0: PECI3 1 1 1: PECI4

9.72 Temperature Register - Index 7Dh (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Temperature Register							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**Temperature Register. (see Temperature selection Register – Index 7C (Bank 0))**

9.73 CPUTIN Temperature Sensor Temperature (High Byte) Register - Index 50h (Bank 1)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<8:1>							
DEFAULT								

BIT	DESCRIPTION
7-0	**TEMP<8:1>. Temperature <8:1> of the CPUTIN sensor.** The nine-bit value is in units of 0.5°C.

9.74 CPUTIN Temperature Sensor Temperature (Low Byte) Register - Index 51h (Bank 1)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<0>	RESERVED						

DEFAULT								

BIT	DESCRIPTION
7	**TEMP<0>. Temperature <0> of the CPUTIN sensor.** The nine-bit value is in units of 0.5°C.
6-0	**RESERVED.**

9.75 CPUTIN Temperature Sensor Configuration Register - Index 52h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FAULT		RESERVED	OVTMOD	STOP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**RESERVED.** These bits should be set to zero.
4-3	**FAULT.** Number of faults to detect before setting OVT# output. This avoids false strapping due to noise.
2	**RESERVED.** This bit should be set to zero.
1	**OVTMOD. OVT# Mode Select.** 0: Compare mode. (Default) 1: Interrupt mode.
0	**STOP.** 0: Monitor CPUTIN. 1: Stop monitoring CPUTIN.

9.76 CPUTIN Temperature Sensor Hysteresis (High Byte) Register - Index 53h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	**THYST<8:1>. Hysteresis temperature bits 8-1.** The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.77 CPUTIN Temperature Sensor Hysteresis (Low Byte) Register - Index 54h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST<0>	RESERVED						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**THYST<0>. Hysteresis temperature bit 0.** The nine-bit value is in units of 0.5°C.
6-0	**RESERVED.**

9.78 CPUTIN Temperature Sensor Over-temperature (High Byte) Register - Index 55h (Bank1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	**TOVF<8:1>. Over-temperature bits 8-1.** The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.79 CPUTIN Temperature Sensor Over-temperature (Low Byte) Register - Index 56h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<0>	RESERVED						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**TOVF<0>. Over-temperature bit 0.** The nine-bit value is in units of 0.5°C.
6-0	**RESERVED.**

9.80 FANCTRL3 SMART FAN™ III+ Temperature 1 Register (T1) – Index 58h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMART FAN ™ III+ Temperature 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SMART FAN™ III+ Temperature 1 Register (T1).**

9.81 FANCTRL3 SMART FAN™ III+ Temperature 2 Register (T2) – Index 59h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMART FAN ™ III+ Temperature 2							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SMART FAN™ III+ Temperature 2 Register (T2).**

9.82 FANCTRL3 SMART FAN™ III+ Temperature 3 Register (T3) – Index 5Ah (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMART FAN ™ III+ Temperature 3							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SMART FAN™ III+ Temperature 3 Register (T3).**

9.83 FANCTRL3 SMART FAN™ III+ DC/PWM 1 Register - Index 5Bh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMART FAN IV III+ DC/PWM 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SMART FAN™ III+ DC/PWM 1 Register.**

9.84 FANCTRL3 SMART FAN™ III+ DC/PWM 2 Register - Index 5Ch (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMART FAN ™ III+ DC/PWM 2							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SMART FAN™ III+ DC/PWM 2 Register.**

9.85 FANCTRL3 SMART FAN™ III+ DC/PWM 3 Register - Index 5Dh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMART FAN ™ III+ DC/PWM 3							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SMART FAN™ III+ DC/PWM 3 Register.**

9.86 FANCTRL3 SMART FAN™ III+ input source & output FAN select Register - Index 5Eh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		SMART FAN™ III+ FAN_SEL		SMART FAN™ III+ TEMP_SEL			Reserved
DEFAULT	0	0	0	0	1	1	1	0

BIT	DESCRIPTION
7-6	**Reserved.**
5-4	**SMART FAN™ III+ FAN_SEL.** **Bits** **5 4** 0 0: SMART FAN™ I → SYSFANOUT SMART FAN™ I or III → CPUFANOUT0 0 1: SMART FAN™ III+ → SYSFANOUT SMART FAN™ I or III → CPUFANOUT0 1 0: SMART FAN™ I → SYSFANOUT SMART FAN™ III+ → CPUFANOUT0 1 1: SMART FAN™ III+ → SYSFANOUT SMART FAN™ III+ → CPUFANOUT0
3-1	**SMART FAN™ III+ TEMP_SEL.** **Bits** **3 2 1** 0 0 0: SYS Temperature 0 0 1: CPU Temperature 0 1 0: AUX Temperature 0 1 1: Reserved 1 0 0: PECI1 1 0 1: PECI2 1 1 0: PECI3 1 1 1: PECI4 (Default)
0	**Reserved.**

9.87 Interrupt Status Register 3 - Index 50h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			CPUFANIN1	RESERVED	RESERVED	VBAT	3VSB
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**RESERVED**
4	**CPUFANIN1.** A one indicates the fan count limit of CPUFANIN1 has been exceeded.
3	**RESERVED.**
2	**RESERVED**
1	**VBAT.** A one indicates the high or low limit of VBAT has been exceeded.
0	**3VSB.** A one indicates the high or low limit of 3VSB has been exceeded.

9.88 SMI# Mask Register 4 - Index 51h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			TAR3	RESERVED		VBAT	3VSB
DEFAULT	0	0	0	1	0	0	1	1

BIT	DESCRIPTION	
7-5	**RESERVED.**	
4	**TAR3.** A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4)).	
3-2	**RESERVED.**	
1	**VBAT.**	A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4)).
0	**3VSB.**	

9.89 Reserved Register - Index 52h (Bank 4)

9.90 SYSTIN Temperature Sensor Offset Register - Index 54h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**OFFSET<7:0> SYSTIN Temperature Offset Value.** The value in this register is added to the monitored value so that the read value will be the sum of the monitored value and this offset value.

9.91 CPUTIN Temperature Sensor Offset Register - Index 55h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**OFFSET<7:0>. CPUTIN Temperature Offset Value.** The value in this register will be added to the monitored value so that the read value is the sum of the monitored value and this offset value.

9.92 Reserved Register - Index 57h-58h (Bank 4)

9.93 Real Time Hardware Status Register I - Index 59h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN0 _STS	SYSFANIN _STS	CPUTIN _STS	SYSTIN _STS	3VCC _STS	AVCC _STS	RESERVED	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**CPUFANIN0_STS. CPUFANIN0 Status.** 1: The fan speed count is over the threshold value. 0: The fan speed count is in the allowed range.
6	**SYSFANIN_STS. SYSFANIN Status.** 1: The fan speed count is over the threshold value. 0: The fan speed count is in the allowed range.
5	**CPUTIN_STS. CPUTIN Temperature Sensor Status.** 1: The temperature exceeds the over-temperature value. 0: The temperature is under the hysteresis value.
4	**SYSTIN_STS. SYSTIN Temperature Sensor Status.** 1: The temperature exceeds the over-temperature value. 0: The temperature is under the hysteresis value.
3	**3VCC_STS. 3VCC Voltage Status.** 1: The 3VCC voltage is over or under the allowed range. 0: The 3VCC voltage is in the allowed range.
2	**AVCC_STS. AVCC Voltage Status.** 1: The AVCC voltage is over or under the allowed range. 0: The 3VCC voltage is in the allowed range.
1~0	**RESERVED**

9.94 Real Time Hardware Status Register II - Index 5Ah (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	TAR2 _STS	TAR1 _STS	RESERVED			CPUFANIN1 _STS	TAR4 _STS	RESERVED
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**TAR2_STS. Smart Fan of CPUFANIN0 Warning Status.** 1: The selected temperature has been over the target temperature for three minutes at full fan speed in the Thermal Cruise™ mode. 0: The selected temperature has not reached the warning range.
6	**TAR1_STS. Smart Fan of SYSFANIN Warning Status.** 1: The SYSTIN temperature has been over the target temperature for three minutes at full fan speed in the Thermal Cruise™ mode. 0: The SYSTIN temperature has not reached the warning range.
5~3	**RESERVED**
2	**CPUFANIN1_STS. CPUFANIN1 Status.** 1: The fan speed count is over the threshold value. 0: The fan speed count is in the allowed range.
1	**TAR4_STS. Smart Fan of CPUFANIN1 Warning Status.** 1: The selected temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise™ mode. 0: The selected temperature has not reached the warning range.
0	**RESERVED**

9.95 Real Time Hardware Status Register III - Index 5Bh (Bank 4)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED						VBAT _STS	VSB _STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-2	**RESERVED**
1	**VBAT_STS. VBAT Voltage Status.** 1: The VBAT voltage is over or under the allowed range. 0: The VBAT voltage is in the allowed range.
0	**VSB_STS. 3VSB Voltage Status.** 1: The 3VSB voltage is over or under the allowed range. 0: The 3VSB voltage is in the allowed range.

9.96 Reserved Register - Index 5Ch ~ 5Fh (Bank 4)

9.97 Value RAM 2 — Index 50h-59h (Bank 5)

ADDRESS A6-A0	DESCRIPTION
50h	3VSB reading
51h	VBAT reading. The reading is meaningless unless EN_VBAT_MN (Bank0 Index 5Dh, bit0) is set.
52h	Reserved
53h	Reserved
54h	3VSB High Limit
55h	3VSB Low Limit
56h	VBAT High Limit
57h	VBAT Low Limit
58h	Reserved
59h	Reserved
5Ah	Reserved
5Bh	Reserved
5Ch	Reserved

9.98 SYSFANIN SPEED HIGH-BYTE VALUE (RPM) - Index 50h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANIN SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SYSFANIN SPEED HIGH-BYTE VALUE.**

9.99 SYSFANIN SPEED LOW-BYTE VALUE (RPM) - Index 51h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANIN SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SYSFANIN SPEED LOW-BYTE VALUE.**

9.100 CPUFANIN0 SPEED HIGH-BYTE VALUE (RPM) - Index 52h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN0 SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUFANIN0 SPEED HIGH-BYTE VALUE.**

9.101 CPUFANIN0 SPEED LOW-BYTE VALUE (RPM) - Index 53h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN0 SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUFANIN0 SPEED LOW-BYTE VALUE.**

9.102 CPUFANIN1 SPEED HIGH-BYTE VALUE (RPM) - Index 56h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN1 SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUFANIN1 SPEED HIGH-BYTE VALUE.**

9.103 CPUFANIN1 SPEED LOW-BYTE VALUE (RPM) - Index 57h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN1 SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUFANIN1 SPEED LOW-BYTE VALUE.**

9.104 FANOUT Configure register of PECI Error - Index 5Ah (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved.					PECI Error Condition		
DEFAULT	0	0	0	0	1	1	0	1

BIT	DESCRIPTION
7-3	**Reserved.**
2~0	**PECI Error Condition** **Bits** **2 1 0** 0 0 0: FANOUT keeps at its current value. 1 1 1: FANOUT will be set to the pre-configured value.

9.105 FANCTRL2 pre-configured register for PECI error - Index 5Bh (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved.					PECI Error Condition		
DEFAULT	0	0	0	0	1	1	0	1

BIT	DESCRIPTION
7-3	**Reserved.**
2~0	**PECI Error Condition** **Bits** **2 1 0**

BIT	DESCRIPTION
	0 0 0: FANOUT keeps at its current value. 1 1 1: FANOUT will be set to the pre-configured value.

9.106 FANCTRL4 pre-configured register for PECI error - Index 5Dh (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved.					PECI Error Condition		
DEFAULT	0	0	0	0	1	1	0	1

BIT	DESCRIPTION
7-3	**Reserved.**
2~0	**PECI Error Condition** **Bits** **2 1 0** 0 0 0: FANOUT keeps at its current value. 1 1 1: FANOUT will be set to the pre-configured value.

9.107 FANCTRL5 pre-configured register for PECI error - Index 5Eh (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved.					PECI Error Condition		
DEFAULT	0	0	0	0	1	1	0	1

BIT	DESCRIPTION
7-3	**Reserved.**
2~0	**PECI Error Condition** **Bits** **2 1 0** 0 0 0: FANOUT keeps at its current value. 1 1 1: FANOUT will be set to the pre-configured value.

9.108 FANCTRL3 pre-configured register for PECI error - Index 5Fh (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved.					PECI Error Condition		
DEFAULT	0	0	0	0	1	1	0	1

BIT	DESCRIPTION
7-3	**Reserved.**
2~0	**PECI Error Condition** **Bits** **2 1 0** 0 0 0: FANOUT keeps at its current value. 1 1 1: FANOUT will be set to the pre-configured value.

10. KEYBOARD CONTROLLER

The W83527HG KBC (8042 with licensed KB BIOS) circuit is designed to provide the functions needed to interface a CPU with a keyboard and/or a PS/2 mouse and can be used with IBM®-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. Then, the controller asserts an interrupt to the system when data are placed in its output buffer. The keyboard and PS/2 mouse are required to acknowledge all data transmissions. No transmission should be sent to the keyboard or PS/2 mouse until an acknowledgement is received for the previous data byte.

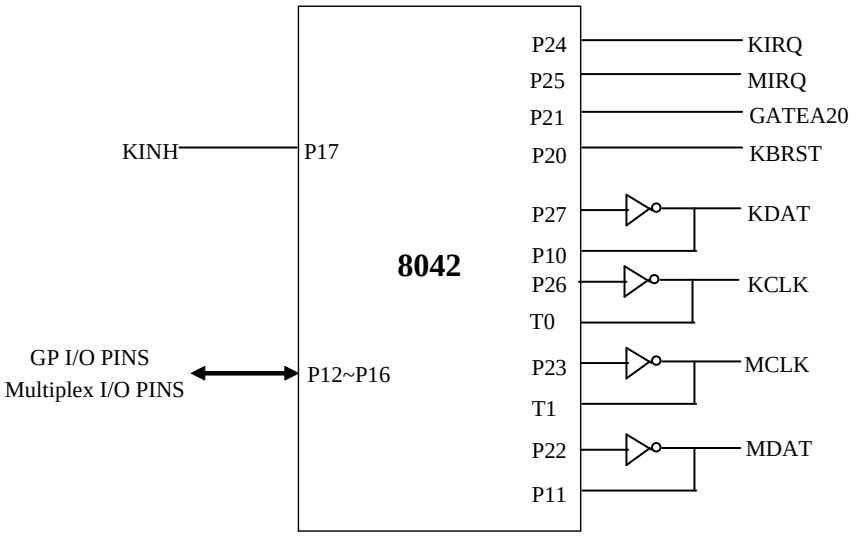


Figure 10-1 Keyboard and Mouse Interface

10.1 Output Buffer

The output buffer is an 8-bit, read-only register at I/O address 60h (Default, PnP programmable I/O address LD5-CR60 and LD5-CR61). The keyboard controller uses the output buffer to send the scan code (from the keyboard) and required command bytes to the system. The output buffer can only be read when the output buffer full bit in the register (in the status register) is logical 1.

10.2 Input Buffer

The input buffer is an 8-bit, write-only register at I/O address 60h or 64h (Default, PnP programmable I/O address LD5-CR60, LD5-CR61, LD5-CR62, and LD5-CR63). Writing to address 60h sets a flag to indicate a data write; writing to address 64h sets a flag to indicate a command write. Data written to I/O address 60h is sent to the keyboard (unless the keyboard controller is expecting a data byte) through the controller's input buffer only if the input buffer full bit (in the status register) is logical 0.

10.3 Status Register

The status register is an 8-bit, read-only register at I/O address 64h (Default, PnP programmable I/O address LD5-CR62 and LD5-CR63) that holds information about the status of the keyboard controller and interface. It may be read at any time.

BIT	BIT FUNCTION	DESCRIPTION
0	Output Buffer Full	0: Output buffer empty 1: Output buffer full
1	Input Buffer Full	0: Input buffer empty 1: Input buffer full
2	System Flag	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller. It defaults to 0 after a power-on reset.
3	Command/Data	0: Data byte 1: Command byte
4	Inhibit Switch	0: Keyboard is inhibited 1: Keyboard is not inhibited
5	Auxiliary Device Output Buffer	0: Auxiliary device output buffer empty 1: Auxiliary device output buffer full
6	General Purpose Time-out	0: No time-out error 1: Time-out error
7	Parity Error	0: Odd parity 1: Even parity (error)

10.4 Commands

COMMAND	FUNCTION
20h	Read Command Byte of Keyboard Controller
60h	Write Command Byte of Keyboard Controller
A4h	Test Password Returns 0Fah if Password is loaded Returns 0F1h if Password is not loaded

BIT	BIT DEFINITION
7	Reserved
6	IBM Keyboard Translate Mode
5	Disable Auxiliary Device
4	Disable Keyboard
3	Reserve
2	System Flag
1	Enable Auxiliary Interrupt
0	Enable Keyboard Interrupt

<table>
<tr><th>COMMAND</th><th>FUNCTION</th></tr>
<tr><td>A5h</td><td>Load Password
Load Password until a logical 0 is received from the system</td></tr>
<tr><td>A6h</td><td>Enable Password
Enable the checking of keystrokes for a match with the password</td></tr>
<tr><td>A7h</td><td>Disable Auxiliary Device Interface</td></tr>
<tr><td>A8h</td><td>Enable Auxiliary Device Interface</td></tr>
<tr><td>A9h</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>Auxiliary Device "Clock" line is stuck low</td></tr>
<tr><td>02</td><td>Auxiliary Device "Clock" line is stuck high</td></tr>
<tr><td>03</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
<tr><td>04</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
</table></td></tr>
<tr><td>AAh</td><td>Self-test
Returns 055h if self-test succeeds</td></tr>
<tr><td>ABh</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>Keyboard "Clock" line is stuck low</td></tr>
<tr><td>02</td><td>Keyboard "Clock" line is stuck high</td></tr>
<tr><td>03</td><td>Keyboard "Data" line is stuck low</td></tr>
<tr><td>04</td><td>Keyboard "Data" line is stuck high</td></tr>
</table></td></tr>
<tr><td>ADh</td><td>Disable Keyboard Interface</td></tr>
<tr><td>AEh</td><td>Enable Keyboard Interface</td></tr>
<tr><td>C0h</td><td>Read Input Port (P1) and send data to the system</td></tr>
<tr><td>C1h</td><td>Continuously puts the lower four bits of Port1 into the STATUS register</td></tr>
<tr><td>C2h</td><td>Continuously puts the upper four bits of Port1 into the STATUS register</td></tr>
<tr><td>D0h</td><td>Send Port 2 value to the system</td></tr>
<tr><td>D1h</td><td>Only set / reset GateA20 line based on system data bit 1</td></tr>
<tr><td>D2h</td><td>Send data back to the system as if it came from the Keyboard</td></tr>
<tr><td>D3h</td><td>Send data back to the system as if it came from Auxiliary Device</td></tr>
<tr><td>D4h</td><td>Output next received byte of data from system to Auxiliary Device</td></tr>
<tr><td>E0h</td><td>Reports the status of the test inputs</td></tr>
<tr><td>FXh</td><td>Pulse only RC (the reset line) low for 6μs if the Command byte is even</td></tr>
</table>

10.5 Hardware GATEA20/Keyboard Reset Control Logic

The KBC includes hardware control logic to speed-up GATEA20 and KBRESET. This control logic is controlled by LD5-CRF0 as follows:

10.5.1 KB Control Register

BIT	7	6	5	4	3	2	1	0
NAME	KCLKS1	KCLKS0	Reserved			P92EN	HGA20	HKBRST#
DEFAULT	1	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7	**KCLKS1**	These two bits select the KBC clock rate. **Bits** **7 6** 0 0: KBC clock input is 6 MHz. 0 1: KBC clock input is 8 MHz. 1 0: KBC clock input is 12 MHz. 1 1: KBC clock input is 16 MHz.
6	**KCLKS0**	
5-3	**RESERVED.**	
2	**P92EN. Port 92 Enable.** 1: Enable Port 92 to control GATEA20 and KBRESET. 0: Disable Port 92 functions.	
1	**HGA20. Hardware GATEA20.** 1: Selects hardware GATEA20 control logic to control GATE A20 signal. 0: Disable hardware GATEA20 control logic function.	
0	**HKBRST#. Hardware Keyboard Reset.** 1: Select hardware KB RESET control logic to control KBRESET signal. 0: Disable hardware KB RESET control logic function.	

When the KBC receives data that follows a "D1" command, the hardware control logic sets or clears GATEA20 according to received data bit 1. Similarly, the hardware control logic sets or clears KBRESET depending on received data bit 0. When the KBC receives an "FE" command, the KBRESET is pulse low for 6μs (Min.) with a 14μs (Min.) delay.

GATEA20 and KBRESET are controlled by either software or hardware logic, and they are mutually exclusive. Then, GATEA20 and KBRESET are merged with Port92 when the P92EN bit is set.

10.5.2 Port 92 Control Register

BIT	7	6	5	4	3	2	1	0
NAME	Res. (0)		Res. (1)	Res. (0)		Res. (1)	SGA20	PLKBRST#
DEFAULT	0	0	1	0	0	1	0	0

SGA20 (Special GATE A20 Control)

1: Drives GATE A20 signal to high.

0: Drives GATE A20 signal to low.

PLKBRST# (Pull-Low KBRESET)

A logical 1 on this bit causes KBRESET to drive low for 6 μS(Min.) with a 14 μS(Min.) delay. Before issuing another keyboard-reset command, the bit must be cleared.

BIT	DESCRIPTION
7-6	**Res. (0)**
5	**Res. (1)**
4-3	**Res. (0)**
2	**Res. (1)**
1	**SGA20. Special GATE A20 Control.** 1: Drives GATE A20 signal to high. 0: Drives GATE A20 signal to low.
0	**PLKBRST#. Pull-Low KBRESET.** A logical 1 on this bit causes KBRESET to drive low for 6 μS(Min.) with a 14 μS(Min.) delay. Before issuing another keyboard-reset command, the bit must e cleared.

11. POWER MANAGEMENT EVENT

11.1 Power Control Logic

This chapter describes how the W83527HG implements its ACPI function via these power control pins: PSIN# (Pin 24), PSOUT# (Pin 23), SUSB# (i.e. SLP_S3#; Pin 28) and PSON# (Pin 27). The following figure illustrates the relationships.

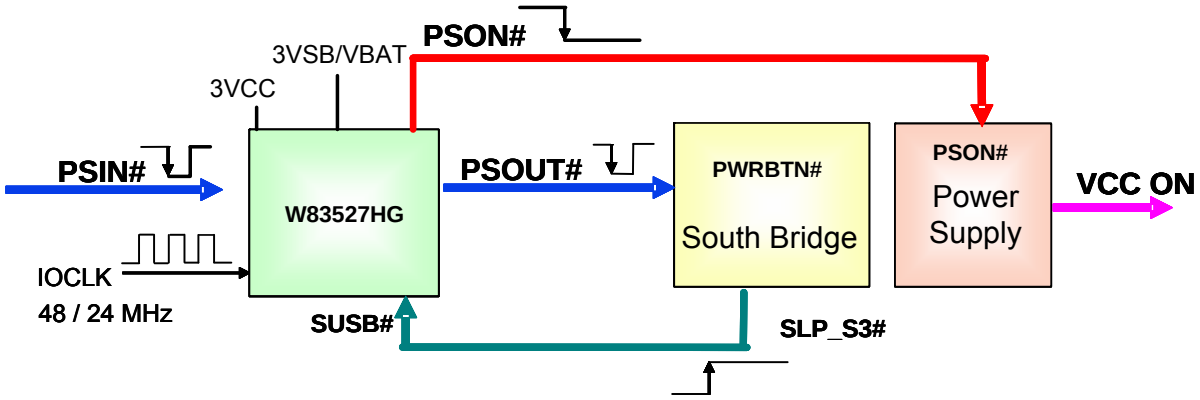


Figure 11-1

11.1.1 PSON# Logic

11.1.1.1. Normal Operation

The PSOUT# signal will be asserted low if the PSIN# signal is asserted low. The PSOUT# signal is held low for as long as the PSIN# is held low. The South Bridge controls the SUSB# signal through the PSOUT# signal. The PSON# is directly connected to the power supply to turn on or off the power.

Figure 15.2 shows the power on and off sequences.

The ACPI state changes from S5 to S0, then to S5

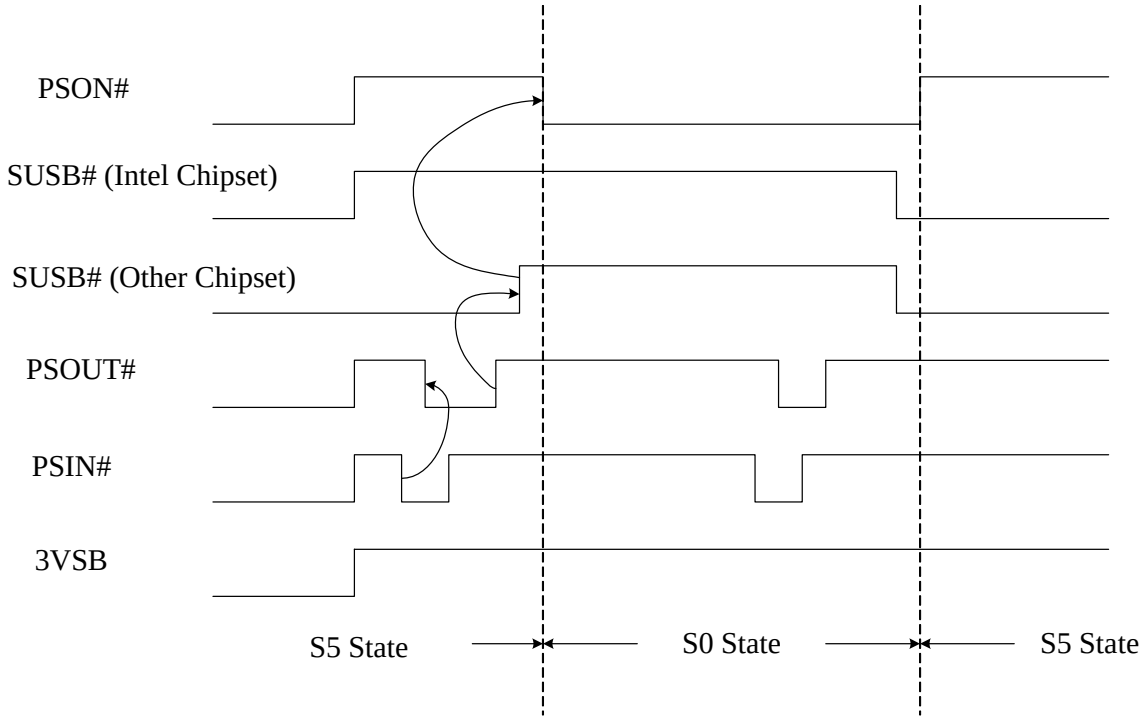


Figure 11-2

11.1.2 AC Power Failure Resume

By definition, AC power failure means that the standby power is removed. The power failure resume control logic of the W83527HG is used to recover the system to a pre-defined state after AC power failure. Two control bits at Logical Device A, CR[E4h], bits[6:5] indicate the pre-defined state. The definition of these two bits is listed in the following table:

LOGICAL DEVICE A, CR[E4H], BITS[6:5]	DEFINITION
00	System always turns off when it returns from AC power failure
01	System always turns on when it returns from AC power failure
10	System turns off / on when it returns from power failure depending on the state before the power failure. (Please see Note 1)
11	User defines the state before the power failure. (The previous state is set at CRE6 [4]. Please see Note 2)

Note1. The W83527HG detects the state before power failure (on or off) through the SUSB# signal and the 3VCC power. The relation is illustrated in the following two figures.

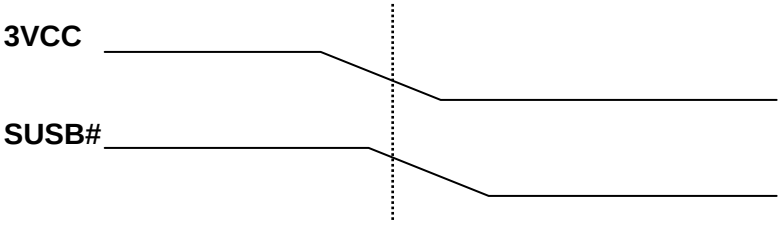


Figure 11-3 The previous state is “on” - 3VCC falls to 2.6V and SUSB# keeps at 2.0V

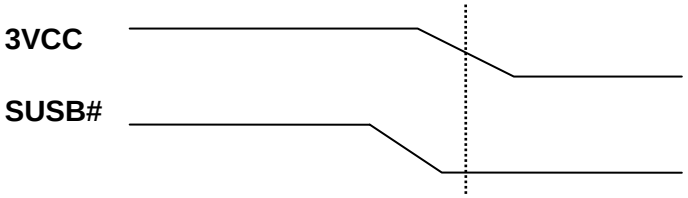


Figure 11-4 The previous state is “off” - 3VCC falls to 2.6V and SUSB# keeps at 0.8V

Note 2.

Logical Device A, CR[E6h] bit [4]	Definition
0	User defines the state to be “on”
1	User defines the state to be “off”

To ensure that VCC does not fall faster than VSB in various ATX Power Supplies, the W83527HG adds the option of “user define mode” for the pre-defined state before AC power failure. BIOS can set the pre-defined state to be “On” or “Off”. According to this setting, the system is returned to the pre-defined state after the AC power recovery.

11.2 Wake Up the System by Keyboard and Mouse

The W83527HG generates a low pulse through the PSOUT# pin to wake up the system when it detects a key code pressed or mouse button clicked. The following sections describe how the W83527HG works.

11.2.1 Waken up by Keyboard events

The keyboard Wake-Up function is enabled by setting Logical Device A, CR[E0h], bit 6 to “1”.

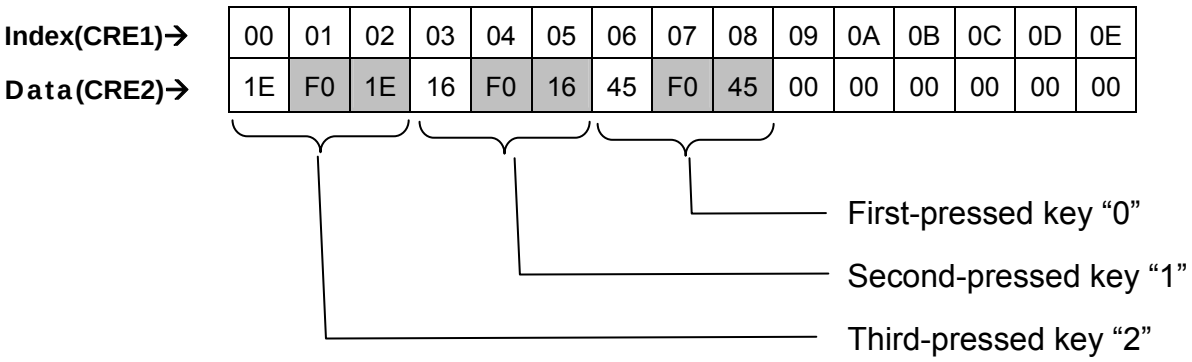
There are two keyboard events can be used for the wake-up

1) Any key – Set bit 0 at Logical Device A, CR[E0h] to “1” (Default).
2) Specific keys (Password) - Set bit 0 at Logical Device A, CR[E0h] to “0”.

Three sets of specific key combinations are stored at Logical Device A. CR[E1h] is an index register to indicate which byte of key code storage (0x00h ~ 0x0Eh, 0x30h ~ 0x3Eh, 0x40h ~ 0x4Eh) is going to be read or written through CR[E2h]. According to IBM 101/102 keyboard specification, a complete key

code contains a 1-byte make code and a 2-byte break code. For example, the make code of “0” is 0x45h, and the corresponding break code is 0xF0h, 0x45h.

The approach to implement Keyboard Password Wake-Up Function is to fill key codes into the password storage. Assume that we want to set “012” as the password. The storage should be filled as below. Please note that index 0x09h ~ 0x0Eh must be filled as 0x00h since the password has only three numbers.



11.2.2 Waken up by Mouse events

The mouse Wake-Up function is enabled by setting Logical Device A, CR[E0h], bit 5 to “1”.

The following specific mouse events can be used for the wake-up:

- Any button clicked or any movement
- One click of the left or the right button
- One click of the left button
- One click of the right button
- Two clicks of the left button
- Two clicks of the right button.

Three control bits (ENMDAT_UP, MSRKEY, MSXKEY) define the combinations of the mouse wake-up events. Please see the following table for the details.

Table 11-1

ENMDAT_UP (LOGICAL DEVICE A, CR[E6H], BIT 7)	MSRKEY (LOGICAL DEVICE A, CR[E0H], BIT 4)	MSXKEY (LOGICAL DEVICE A, CR[E0H], BIT 1)	WAKE-UP EVENT
1	x	1	Any button clicked or any movement.
1	x	0	One click of the left or right button.
0	0	1	One click of the left button.
0	1	1	One click of the right button.
0	0	0	Two clicks of the left button.
0	1	0	Two clicks of the right button.

11.3 Resume Reset Logic

The RSMRST# (Pin 30) signal is a reset output and is used as the 3VSB power-on reset signal for the South Bridge.

When the W83527HG detects the 3VSB voltage rises to “V1”, it then starts a delay – “t1” before the rising edge of RSMRST# asserting. If the 3VSB voltage falls below “V2”, the RSMRST# de-asserts immediately.

Timing and voltage parameters are shown in Figure 11-5

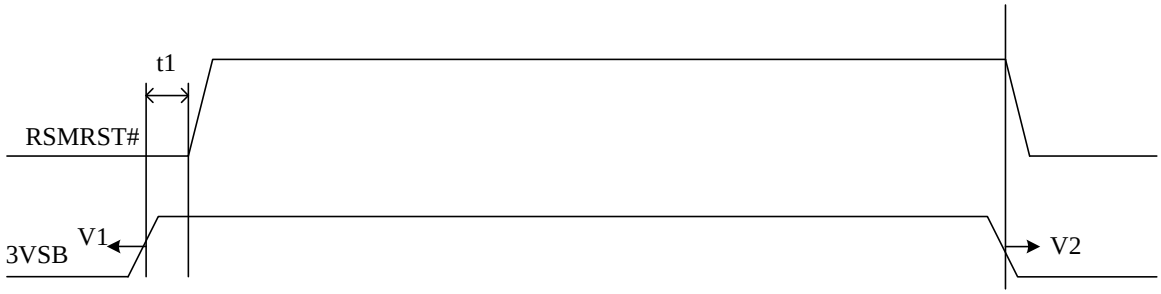


Figure 11-5

11.4 PWROK Generation

The PWROK (Pin 26) signal is an output and is used as the 3VCC power-on reset signal.

When the W83527HG detects the 3VCC voltage rises to “V3”, it then starts a delay – “t2” before the rising edge of PWROK asserting. If the 3VCC voltage falls below “V4”, the PWROK de-asserts immediately.

Timing and voltage parameters are shown in Figure 11-6.

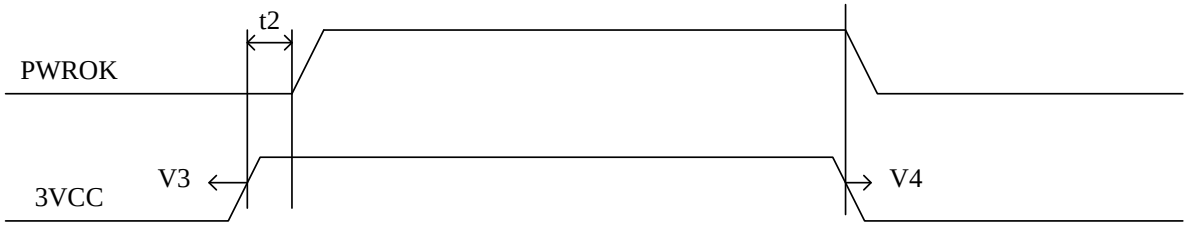


Figure 11-6

Originally, the t2 timing is between 300 mS to 500 mS, but it can be changed to 200 mS to 300 mS by programming Logical Device A, CR[E6h], bit 3 to “1”. Furthermore, the W83527HG provides four different extra delay time of PWROK for various demands. The four extra delay time are designed at Logical Device A, CR[E6h], bits 2~1. The following table shows the definitions of Logical Device A, CR[E6h] bits 3 ~1.

LOGICAL DEVICE A, CR[E6H] BIT	DEFINITION
3	PWROK_DEL (first stage) **(VSB)** Set the delay time when rising from PWROK_LP to PWROK_ST. 0: 300 ~ 500 mS. 1: 200 ~ 300 mS.
2~1	PWROK_DEL **(VSB)** Set the delay time when rising from PWROK_ST to PWROK. 00: No delay time. 01: Delay 32 mS 10: 96 mS 11: Delay 250 mS

For example, if Logical Device A, CR[E6h] bit 3 is set to "0" and bits 2~1 are set to "10", the range of t2 timing is from 396(300 + 96) mS to 596(500 + 96) mS.

11.4.1 The Relation between PWROK and ATXPGD

PWROK signals as well as ATXPGD input signals are interrelated.

Additionally, the ATXPGD signal, too, is used to control the generation of PWROK. In Figure 11-7, the 3VCC voltage rises to "V3", and then starts a delay – "t2" for PWROK generation. However, ATXPGD is still inactive after t2; therefore the delay time before the rising edge of PWROK is t2 plus Td. The length of Td is based on when the ATXPGD signal is active. Once 3VCC falls below "V4" or the ATXPGD signal is inactive, PWROK de-assert immediately.

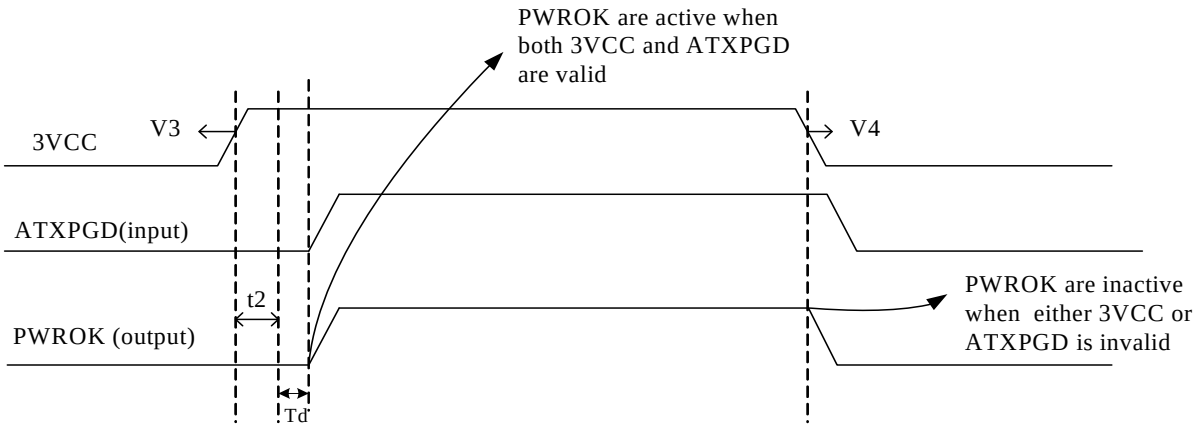


Figure 11-7

In Figure 11-8, the 3VCC voltage rises to "V3", and the ATXPGD is active during t2, so PWROK asserts after t2. The timing of t2 starts when 3VCC voltage rises to "V3". No matter the ATXPGD signal activation is during or after t2, PWROK asserts or de-asserts according to the 3VCC voltage and the ATXPGD signal.

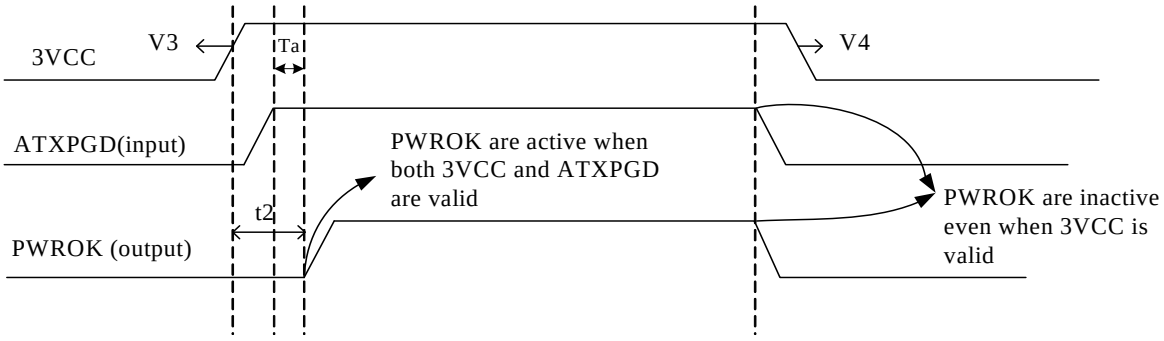


Figure 11-8

Timing and voltage parameters are shown in the following table.

12. SERIALIZED IRQ

The W83527HG supports a serialized IRQ scheme. This allows a signal line to be used to report the parallel interrupt requests. Since more than one device may need to share the signal serial SERIRQ signal, an open drain signal scheme is employed. The clock source is the PCI clock. The serialized interrupt is transferred on the SERIRQ signal, one cycle consisting of three frames types: the Start Frame, the IRQ/Data Frame, and the Stop Frame.

12.1 Start Frame

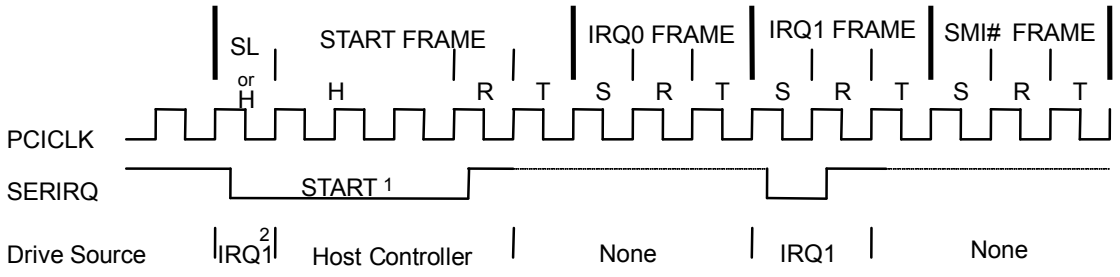
There are two modes of operation for the SERIRQ Start Frame: Quiet mode and Continuous mode.

In the Quiet mode, the W83527HG drives the SERIRQ signal active low for one clock, and then tri-states it. This brings all the state machines of the W83527HG from idle to active states. The host controller (the South Bridge) then takes over driving SERIRQ signal low in the next clock and continues driving the SERIRQ low for programmable 3 to 7 clock periods. This makes the total number of clocks low 4 to 8 clock periods. After these clocks, the host controller drives the SERIRQ high for one clock and then tri-states it.

In the Continuous mode, the START Frame can only be initiated by the host controller to update the information of the IRQ/Data Frame. The host controller drives the SERIRQ signal low for 4 to 8 clock periods. Upon a reset, the SERIRQ signal is defaulted to the Continuous mode for the host controller to initiate the first Start Frame.

Please see the diagram below for more details.

Start Frame Timing with source sampled a low pulse on IRQ1.



H=Host Control SL=Slave Control R=Recovery T=Turn-around S=Sample

Note:

1. The Start Frame pulse can be 4-8 clocks wide.
2. The first clock of Start Frame is driven low by the W83527HG because IRQ1 of the W83527HG needs an interrupt request. Then the host takes over and continues to pull the SERIRQ low.

12.2 IRQ/Data Frame

Once the Start Frame has been initiated, the W83527HG must start counting frames based on the rising edge of the start pulse. Each IRQ/Data Frame has three clocks: the Sample phase, the Recovery phase, and the Turn-around phase.

During the Sample phase, the W83527HG drives SERIRQ low if the corresponding IRQ is active. If the corresponding IRQ is inactive, then SERIRQ must be left tri-stated. During the Recovery phase, the W83527HG device drives the SERIRQ high. During the Turn-around phase, the W83527HG device leaves the SERIRQ tri-stated. The W83527HG starts to drive the SERIRQ line from the beginning of "IRQ0 FRAME" based on the rising edge of PCICLK.

The IRQ/Data Frame has a specific numeral order, as shown in Table 12-1 SERIRQ Sampling Periods.

Table 12-1 SERIRQ Sampling Periods

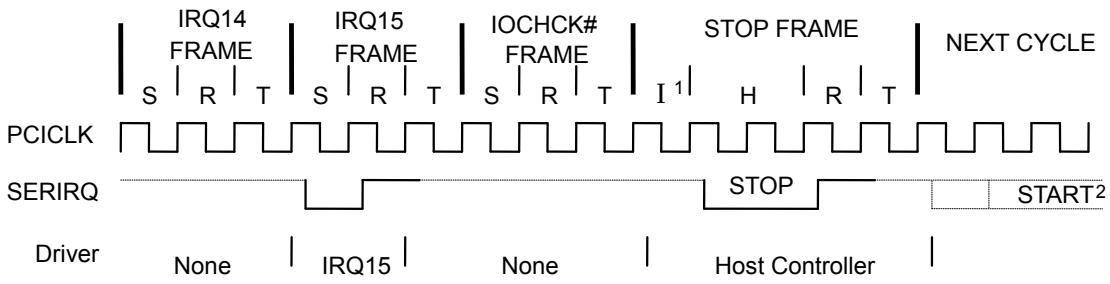
SERIRQ SAMPLING PERIODS			
IRQ/DATA FRAME	**SIGNAL SAMPLED**	**# OF CLOCKS PAST START**	**EMPLOYED BY**
1	IRQ0	2	Reserved
2	IRQ1	5	Keyboard
3	SMI#	8	H/W Monitor & SMI
4	IRQ3	11	Reserved
5	IRQ4	14	Reserved
6	IRQ5	17	-
7	IRQ6	20	Reserved
8	IRQ7	23	Reserved
9	IRQ8	26	-
10	IRQ9	29	-
11	IRQ10	32	-
12	IRQ11	35	-
13	IRQ12	38	Mouse
14	IRQ13	41	Reserved
15	IRQ14	44	-
16	IRQ15	47	-
17	IOCHCK#	50	-
18	INTA#	53	-
19	INTB#	56	-
20	INTC#	59	-
21	INTD#	62	-
32:22	Unassigned	95	-

12.3 Stop Frame

After all IRQ/Data Frames have completed, the host controller will terminates SERIRQ with a Stop frame. Only the host controller can initiate the Stop Frame by driving SERIRQ low for 2 or 3 clocks. If the Stop Frame is low for 2 clocks, the Sample mode of next SERIRQ cycle's Sample mode is the Quiet mode. If the Stop Frame is low for 3 clocks, the Sample mode of next SERIRQ cycle is the Continuous mode.

Please see the diagram below for more details.

Stop Frame Timing with Host Using 17 SERIRQ sampling period.



H=Host Control R=Recovery T=Turn-around S=Sample I= Idle.

Note:

1. There may be none, one or more Idle states during the Stop Frame.
2. The Start Frame pulse of next SERIRQ cycle may or may not start immediately after the turn-around clock of the Stop Frame.

13. WATCHDOG TIMER

The WDTO# pin is a multi-function pin with GP50 functions and is configured to the WDTO# function, if Configuration Register CR [2Dh], bit 0 is set to zero.

The Watchdog Timer of the W83527HG consists of an 8-bit programmable time-out counter and a control and status register. The time-out counter ranges from 1 to 255 minutes in the minute mode, or 1 to 255 seconds in the second mode. The units of Watchdog Timer counter are selected at Logical Device 8, CR [F5h], bit [3]. The time-out value is set at Logical Device 8, CR [F6h]. Writing zero disables the Watchdog Timer function. Writing any non-zero value to this register causes the counter to load this value into the Watchdog Timer counter and start counting down.

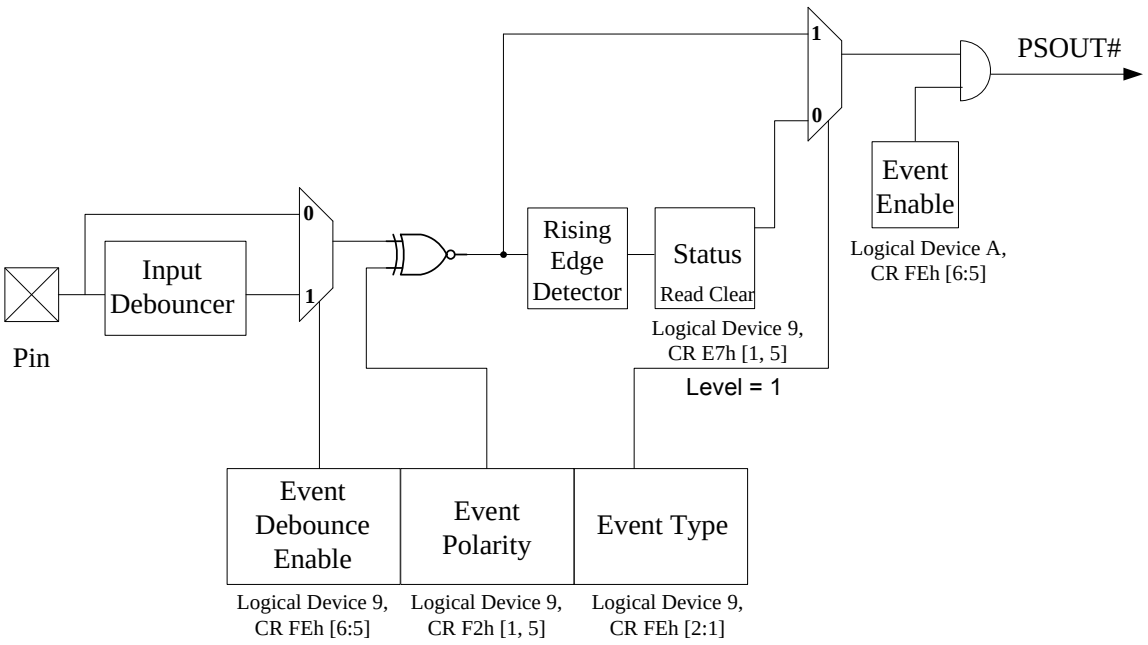
When a time-out event occurs, the W83527HG outputs a low signal through the WDTO# pin (pin 31). In other words, when the value is counted down to zero, the timer stops, and the W83527HG sets the WDTO# status bit in Logical Device 8, CR [F7h], bit [4], outputting a low signal to the WDTO# pin(pin 31). Writing a zero will clear the status bit and the WDTO# pin returns to high. Writing a zero will clear the status bit. This bit will also be cleared if LRESET# or PWROK# signal is asserted.

Please note that the output type of WDTO# (pin 31) is push-pull.

14. GENERAL PURPOSE I/O

The W83527HG provides 18 input/output ports that can be individually configured to perform a simple basic I/O function or alternative, pre-defined function. GPIO ports 2, 3, and 5 are in Logical Device 9. Users can configure each individual port to be an input or output port by programming respective bit in selection register (0 = output, 1 = input). Invert port value by setting inversion register (0 = non - inverse, 1 = inverse). Port value is read / written through data register.

In addition, only GP31 and GP35 are designed to be able to assert PSOUT# signal to wake up the system if any of them has any transitions. There are about 16mS debounced circuit inside these 2 GPIOs and it can be disabled by programming respective bit (LD9, CR [FEh] bit 5~6). Users can set what kind of event type, level or edge, and polarity, rising or falling, to perform the wake-up function. The following table gives a more detailed register map on GP31 and GP35.



	EVENTROUTE (PSOUT#) 0: DISABLE 1: ENABLE	EVENT DEBOUNCED 0 : ENABLE 1 : DISABLE	EVENT TYPE 0 : EDGE 1: LEVEL	EVENT POLARITY 0 : RISING 1 : FALLING	EVENT STATUS
GP31	LDA, CR[FEh] bit5	LD9, CR[FEh] bit5	LD9, CR[FEh] bit1	LD9, CR[F2h] bit1	LD9, CR[E7h] bit1
GP35	LDA, CR[FEh] bit6	LD9, CR[FEh] bit6	LD9, CR[FEh] bit2	LD9, CR[F2h] bit5	LD9, CR[E7h] bit5

15. PCI RESET BUFFERS

The W83527HG has two copies of LRESET# output buffers. LRESET# is LPC Interface Reset, to which PCI Reset is connected. The two copies of LRESET# in the W83527HG are designated RSTOUT0# and RSTOUT2#. All of them are powered by a 3VSB power.

RSTOUT0# is an open-drain output buffer of LRESET#. This signal needs an external pulled-up resistor of 3.3V or 5V.

RSTOUT2# is push-pull output buffers of LRESET#. Each of them outputs 3.3V, voltage and the state is low when the 3VSB power is the only power source.

16. CONFIGURATION REGISTER

16.1 Chip (Global) Control Register

CR 02h. (Software Reset; Write Only)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	Write "1" Only	Software RESET.

CR 07h. (Logical Device; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Logical Device Number.

CR 20h. (Chip ID, High Byte; Read Only)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only	Chip ID number = B0h (high byte).

CR 21h. (Chip ID, Low Byte; Read Only)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only	Chip ID number = 7Xh (low byte). X is the IC version

CR 22h. (Device Power Down; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W	HM Power Down. 0: Powered down. 1: Not powered down.
5-0	Reserved	

CR 23h. (IPD; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	IPD (Immediate Power Down). When set to 1, the whole chip is put into power-down mode immediately.

CR 24h. (Global Option; Default 0100_0ss0b) s: value by strapping

BIT	READ / WRITE	DESCRIPTION
7	R / W	Select output type of CPUFANOUT1 =0 CPUFANOUT1 is Push-pull. (Default) =1 CPUFANOUT1 is Open-drain.

BIT	READ / WRITE	DESCRIPTION
6	R / W	CLKSEL => Input clock rate selection = 0 The clock input on pin 18 is 24 MHz. = 1 The clock input on pin 18 is 48 MHz. (Default)
5	Reserved	
4	R / W	Select output type of SYSFANOUT =0 SYSFANOUT is Open-drain. (Default) =1 SYSFANOUT is Push-pull.
3	R / W	Select output type of CPUFANOUT0 =0 CPUFANOUT0 is Open-drain. (Default) =1 CPUFANOUT0 is Push-pull.
2-0	Reserved	

CR 25h. (Interface Tri-state Enable; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7-0	Reserved.	

CR 26h. (Global Option; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	HEFRAS => = 0 Write 87h to location 2E twice. = 1 Write 87h to location 4E twice.
5	R / W	LOCKREG => = 0 Enable R/W configuration registers. = 1 Disable R/W configuration registers.
4-0	Reserved.	

CR 27h. (Reserved)

CR 28h. (Global Option; Default 50h)

BIT	READ / WRITE	DESCRIPTION
7-0	Reserved	

CR 29h. (Multi-function Pin Selection; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	Pin 3 function select = 0 OVT# = 1 SMI#

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>5-3</td><td colspan="2">Reserved.</td></tr>
<tr><td>2-1</td><td>R / W</td><td>Pin 1 ~ 2 function select
<table>
<tr><th>Bit-2</th><th>Bit-1</th><th>Pin 119 ~ 120 function</th></tr>
<tr><td>0</td><td>0</td><td>Pin 1 ~ 2 → CPUFANIN1, CPUFANOUT1 (Default)</td></tr>
<tr><td>0</td><td>1</td><td>Pin 1 ~ 2 → GP21, GP20</td></tr>
</table></td></tr>
<tr><td>0</td><td colspan="2">Reserved.</td></tr>
</table>

CR 2Ah. (Configuration; Default 00h) **(VSB Power)**

BIT	READ / WRITE	DESCRIPTION
7-1	**Reserved**	
0	R / W	KB, MS pin function select = 0 KB, MS function. = 1 GPIO function.(GP24, GP25, GP26 and GP27)

CR 2Bh. (Reserved)

CR 2Ch. (Multi-function Pin Selection; Default E2h) **(VSB Power)**

BIT	READ / WRITE	DESCRIPTION
7-6	**Reserved**	
5	R / W	Pin 33 Select = 0 GP32 = 1 RSTOUT2# (Default) ***Note: This bit is ignored when CR2Ah, bit 1 is High.***
4	Read Only	EN_ACPI status bit = 0 Particular ACPI functions are disabled. = 1 Particular ACPI functions are enabled. The bit is strapped by Pin 25 (GP55). While particular ACPI functions are enabled (EN_ACPI = 1), GPIO3 pins are disabled and the particular ACPI functions are activated (SUSC#, ATXPGD and VSBGATE#)
3	**Reserved**	
2	R / W	EN_PWRDN. **(VBAT)** = 0 Thermal shutdown function is disabled. = 1 Enable thermal shutdown function.
1~0	**Reserved**	

CR 2Dh. (Multi-function Pin Selection; default 21h) **(VSB Power)**

BIT	READ / WRITE	DESCRIPTION
7	R / W	Pin 23 Select (reset by RSMRST#) = 0 PSOUT# = 1 GPIO57
6	R / W	Pin 24 Select (reset by RSMRST#) = 0 PSIN# = 1 GPIO56
5	R / W	Pin 25 Select (reset by RSMRST#) = 0 SUSLED = 1 GPIO55
4	R / W	Pin 26 Select (reset by RSMRST#) = 0 PWROK = 1 GPIO54
3	R / W	Pin 27 Select (reset by RSMRST#) = 0 PSON# = 1 GPIO53
2	R / W	Pin 28 Select (reset by RSMRST#) = 0 SUSB# = 1 GPIO52
1	R / W	Pin 30 Select (reset by RSMRST#) = 0 RSMRST# = 1 GPIO51
0	R / W	Pin 31 Select (reset by RSMRST#) = 0 WDTO# = 1 GPIO50

CR 2Eh. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Test Mode Bits: Reserved for Nuvoton.

CR 2Fh. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Test Mode Bits: Reserved for Nuvoton.

16.2 Logical Device 5 (Keyboard Controller)

CR 30h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h. (Default 00h,60h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select the first KBC I/O base address <100h: FFFh> on 1-byte boundary.

CR 62h, 63h. (Default 00h,64h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select the second KBC I/O base address <100h: FFFh> on 1 byte boundary.

CR 70h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for KINT. (Keyboard interrupt)

CR 72h. (Default 0Ch)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for MINT. (PS/2 Mouse interrupt)

CR F0h. (Default83h)

BIT	READ / WRITE	DESCRIPTION
7~6	R / W	KBC clock rate selection 00: 6MHz 01: 8MHz 10: 12MHz 11: 16MHz
5~3	Reserved.	
2	R / W	0: Port 92 disable. 1: Port 92 enable.
1	R / W	0: Gate A20 software control. 1: Gate A20 hardware speed up.
0	R / W	0: KBRST# software control. 1: KBRST# hardware speed up.

16.3 Logical Device 8 (WDTO# & PLED)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: WDTO# and PLED are inactive. 1: Activate WDTO# and PLED.

CR F5h. (WDTO#, PLED and KBC P20 Control Mode Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~5	R / W	Select Power LED mode. 000: Power LED pin is driven high. 001: Power LED pin outputs 0.5Hz pulse with 50% duty cycle. 010: Power LED pin is driven low. 011: Power LED pin outputs 2Hz pulse with 50% duty cycle. 100: Power LED pin outputs 1Hz pulse with 50% duty cycle. 101: Power LED pin outputs 4Hz pulse with 50% duty cycle. 110: Power LED pin outputs 0.25Hz pulse with 50% duty cycle. 111: Power LED pin outputs 0.25Hz pulse with 50% duty cycle.
4	R / W	WDTO# count mode is 1000 times faster. 0: Disable. 1: Enable. (If bit-3 is in Seconds Mode, the count mode is 1/1000 sec.) (If bit-3 is in Minutes Mode, the count mode is 1/1000 min.)
3	R / W	Select WDTO# count mode. 0: Second Mode. 1: Minute Mode.
2	R / W	Enable the rising edge of a KBC reset to issue a time-out event. 0: Disable. 1: Enable.
1	R / W	Disable / Enable the WDTO# output low pulse to the KBRST# pin (PIN16) 0: Disable. 1: Enable.
0	Reserved.	

CR F6h. (WDTO# Counter Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Watch Dog Timer Time-out value. Writing a non-zero value to this register causes the counter to load the value into the Watch Dog Counter and start counting down. If CR F7h, bits 7 and 6 are set, any Mouse Interrupt or Keyboard Interrupt event causes the previously-loaded, non-zero value to be reloaded to the Watch Dog Counter and the count down resumes. Reading this register returns the current value in the Watch Dog Counter, not the Watch Dog Timer Time-out value. 00h: Time-out Disable 01h: Time-out occurs after 1 second/minute 02h: Time-out occurs after 2 second/minutes 03h: Time-out occurs after 3 second/minutes ……..... FFh: Time-out occurs after 255 second/minutes

CR F7h. (WDTO# Control & Status Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	Mouse interrupt reset enables watch-dog timer reload 0: Watchdog timer is not affected by mouse interrupt. 1: Watchdog timer is reset by mouse interrupt.
6	R / W	Keyboard interrupt reset enables watch-dog timer reload 0: Watchdog timer is not affected by keyboard interrupt. 1: Watchdog timer is reset by keyboard interrupt.
5	Write “1” Only	Trigger WDTO# event. This bit is self-clearing.
4	R / W Write “0” Clear	WDTO# status bit 0: Watchdog timer is running. 1: Watchdog timer issues time-out event.
3~0	R / W	These bits select the IRQ resource for the WDTO#. (02h for SMI# event.)

16.4 Logical Device 9 (GPIO2, GPIO3, GPIO5)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3	R / W	0: GPIO5 is inactive. 1: GPIO5 is active
2	Reserved	
1	R / W	0: GPIO3 is inactive. 1: GPIO3 is active.
0	R / W	0: GPIO2 is inactive. 1: GPIO2 is active.

CR E0h. (GPIO5 I/O Register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~1	R / W	GPIO50 ~ GPIO57 I/O register 0: The respective GPIO50 ~ GPIO57 pin is programmed as an output port 1: The respective GPIO50 ~ GPIO 57 pin is programmed as an input port.
0	Reserved	

CR E1h. (GPIO5 Data Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	R / W	GPIO50 ~ GPIO57 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For input ports, the respective bits can only be read by the pins. Write accesses are ignored.
0	Reserved	

CR E2h. (GPIO5 Inversion Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	R / W	GPIO50 ~ GPIO57 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)
0	Reserved	

CR E3h. (GPIO2 Register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~4	R / W	GPIO27 ~ GPIO24 I/O register 0: The respective GPIO27 ~ GPIO24 pin is programmed as an output port 1: The respective GPIO27 ~ GPIO24 pin is programmed as an input port
3~2	Reserved	

BIT	READ / WRITE	DESCRIPTION
1~0	R / W	GPIO21 ~ GPIO20 I/O register 0: The respective GPIO21 ~ GPIO20 pin is programmed as an output port 1: The respective GPIO21 ~ GPIO20 pin is programmed as an input port

CR E4h. (GPIO2 Data Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~4	R / W	GPIO27 ~ GPIO24 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For input ports, the respective bits can only be read by the pins. Write accesses are ignored.
3~2	Reserved	
1~0	R / W	GPIO21 ~ GPIO20 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For input ports, the respective bits can only be read by the pins. Write accesses are ignored.

CR E5h. (GPIO2 Inversion Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~4	R / W	GPIO27 ~ GPIO24 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)
3~2	Reserved	
1~0	R / W	GPIO21 ~ GP20 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

CR E6h. (GPIO2 Status Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~4	Read Only Read-Clear	GPIO27 ~ GPIO24 Event Status Bit 7-4 corresponds to GP27-GP24, respectively. 0 : No active edge(rising/falling) has been detected 1 : An active edge(rising/falling) has been detected Read the status bit clears it to 0.
3~2	Reserved	

BIT	READ / WRITE	DESCRIPTION
1~0	Read Only Read-Clear	GPIO21 ~ GPIO20 Event Status Bit 1-0 corresponds to GP21-GP20, respectively. 0 : No active edge(rising/falling) has been detected 1 : An active edge(rising/falling) has been detected Read the status bit clears it to 0.

CR E7h. (GPIO3 Status Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	Read Only Read-Clear	GPIO37 Event Status 0 : No active edge(rising/falling) has been detected 1 : An active edge(rising/falling) has been detected Read the status bit clears it to 0.
6	Reserved	
5	Read Only Read-Clear	GPIO35 Event Status 0 : No active edge(rising/falling) has been detected 1 : An active edge(rising/falling) has been detected Read the status bit clears it to 0.
4-3	Reserved	
2-1	Read Only Read-Clear	GPIO32 ~ GPIO31 Event Status Bit 2-1 corresponds to GP32-GP31, respectively. 0 : No active edge(rising/falling) has been detected 1 : An active edge(rising/falling) has been detected Read the status bit clears it to 0.
0	Reserved	

CR E9h. (GPIO5 Status Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Read Only Read-Clear	GPIO57 ~ GPIO51 Event Status Bit 7-1 corresponds to GP57-GP51, respectively. 0 : No active edge(rising/falling) has been detected 1 : An active edge(rising/falling) has been detected Reading the status bit clears it to 0.
0	Reserved	

CR F0h. (GPIO3 I/O Register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7	R / W	GPIO37 I/O register 0: The respective GPIO37 pin is programmed as an output port 1: The respective GPIO37 pin is programmed as an input port.
6	Reserved	

BIT	READ / WRITE	DESCRIPTION
5	R / W	GPIO35 I/O register 0: The respective GPIO35 pin is programmed as an output port 1: The respective GPIO35 pin is programmed as an input port.
4-3	Reserved	
2-1	R / W	GPIO32 ~ GPIO31 I/O register 0: The respective GPIO32 ~ GPIO31 pin is programmed as an output port 1: The respective GPIO32 ~ GPIO31 pin is programmed as an input port.
0	Reserved	

CR F1h. (GPIO3 Data Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	GPIO37 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For input ports, the respective bits can only be read by the pins. Write accesses are ignored.
6	Reserved	
5	R / W	GPIO35 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For input ports, the respective bits can only be read by the pins. Write accesses are ignored.
4-3	Reserved	
2-1	R / W	GPIO32 ~ GPIO31 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For input ports, the respective bits can only be read by the pins. Write accesses are ignored.
0	Reserved	

CR F2h. (GPIO3 Inversion Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	GPIO37 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)
6	Reserved	
5	R / W	GPIO35 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

BIT	READ / WRITE	DESCRIPTION
4-3	Reserved	
2-1	R / W	GPIO32 ~ GPIO31 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)
0	Reserved	

CR F3h. (Suspend LED Mode Register; Default 00h) (VBAT power)

BIT	READ / WRITE	DESCRIPTION
7~5	R / W	Select Suspend LED mode. 000: Suspend LED pin is driven high. 001: Suspend LED pin outputs 0.5Hz pulse with 50% duty cycle. 010: Suspend LED is driven low. 011: Suspend LED pin outputs 2Hz pulse with 50% duty cycle. 100: Suspend LED pin outputs 1Hz pulse with 50% duty cycle. 101: Suspend LED pin outputs 4Hz pulse with 50% duty cycle. 110: Suspend LED pin outputs 0.25Hz pulse with 50% duty cycle. 111: Suspend LED pin outputs 0.25Hz pulse with 50% duty cycle.
4~0	Reserved.	

CR F8h. (GPIO2 Multi-function Select Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO27 1: GPIO27 → SUSPLED
6	R / W	0: GPIO26 1: GPIO26 → SUSPLED
5	R / W	0: GPIO25 1: GPIO25 → SUSPLED
4	R / W	0: GPIO24 1: GPIO24 → SUSPLED
3-2	Reserved	
1	R / W	0: GPIO21 1: GPIO21 → PLED
0	R / W	0: GPIO20 1: GPIO20 → PLED

CR F9h. (GPIO3 Multi-function Select Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO37 1: GPIO37 → SUSLED
6	Reserved	
5	R / W	0: GPIO35 1: GPIO35 → SUSLED
4-3	Reserved	
2	R / W	0: GPIO32 1: GPIO32 → SUSPLED
1	R / W	0: GPIO31 1: GPIO31 → SUSLED
0	Reserved	

CR FAh. (GPIO5 Multi-function Select Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO57 1: GPIO57 → SUSLED
6	R / W	0: GPIO56 1: GPIO56 → SUSLED
5	R / W	0: GPIO55 1: GPIO55 → SUSLED
4	R / W	0: GPIO54 1: GPIO54 → SUSLED
3	R / W	0: GPIO53 1: GPIO53 → SUSLED
2	R / W	0: GPIO52 1: GPIO52 → SUSPLED
1	R / W	0: GPIO51 1: GPIO51 → SUSLED
0	R / W	0: GPIO50 1: GPIO50 → SUSLED

CR FEh. (GPIO3 Input Detected Type Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	Reserved.
6	R / W	0: Enable GP35 input de-bouncer 1: Disable GP35 input de-bouncer
5	R / W	0: Enable GP31 input de-bouncer 1: Disable GP31 input de-bouncer

BIT	READ / WRITE	DESCRIPTION
4-3	Reserved.	
2	R / W	0: GP35 trigger type : edge 1: GP35 trigger type : level
1	R / W	0: GP31 trigger type : edge 1: GP31 trigger type : level
0	Reserved.	

16.5 Logical Device A (ACPI)

(CR30, CR70 are VCC powered; CRE0~F7 are VRTC powered)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	Reserved.	

CR 70h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	Reserved.	

CR E0h. (Default 01h) (VBAT power)

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>DIS_PSIN => Disable the panel switch input to turn on the system power supply.
0: PSIN is wire-AND and connected to PSOUT#.
1: PSIN is blocked and cannot affect PSOUT#.</td></tr>
<tr><td>6</td><td>R / W</td><td>Enable KBC wake-up
0: Disable keyboard wake-up function via PSOUT#.
1: Enable keyboard wake-up function via PSOUT#.</td></tr>
<tr><td>5</td><td>R / W</td><td>Enable Mouse wake-up
0: Disable mouse wake-up function via PSOUT#.
1: Enable mouse wake-up function via PSOUT#.</td></tr>
<tr><td>4</td><td>R / W</td><td>MSRKEY =>
Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please see the following table for the details.
<table>
<tr><th>ENMDAT_UP</th><th>MSRKEY</th><th>MSXKEY</th><th>Wake-up event</th></tr>
<tr><td>1</td><td>x</td><td>1</td><td>Any button clicked or any movement.</td></tr>
<tr><td>1</td><td>x</td><td>0</td><td>One click of left or right button.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>One click of the left button.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>One click of the right button.</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Two clicks of the left button.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Two clicks of the right button.</td></tr>
</table></td></tr>
<tr><td>3</td><td colspan="2">Reserved.</td></tr>
<tr><td>2</td><td>R / W</td><td>Keyboard / Mouse swap enable
0: Normal mode.
1: Keyboard / Mouse ports are swapped.</td></tr>
</table>

BIT	READ / WRITE	DESCRIPTION
1	R / W	MSXKEY => Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please check out the table in CRE0[4] for the detailed.
0	R / W	KBXKEY => 0: Only the pre-determined key combination in sequence can wake up the system. 1: Any character received from the keyboard can wake up the system.

CR E1h. (KBC Wake-Up Index Register; Default 00h) (VSB power)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Keyboard wake-up index register. This is the index register of CRE2, which is the access window for the keyboard's pre-determined key key-combination characters. The first set of wake-up keys is in of 0x00 - 0x0E, the second set 0x30 – 0x3E, and the third set 0x40 – 0x4E. Incoming key combinations can be read through 0x10 – 0x1E.

CR E2h. (KBC Wake-Up Data Register; Default FFh) (VSB power)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Keyboard wake-up data register. This is the data register for the keyboard's pre-determined key-combination characters, which is indexed by CRE1.

CR E3h. (Event Status Register; Default 08h)

BIT	READ / WRITE	DESCRIPTION
7~6	Reserved.	
5	Read Only Read-Clear	This status flag indicates VSB power off/on.
4	Read Only Read-Clear	If E4[7] is 1 => 0: When power-loss occurs and the VSB power is on, turn on system power. 1: When power-loss occurs and the VSB power is on, turn off system power. If E4[7] is 0 => This bit is always 0.
3	Read Only Read-Clear	Thermal shutdown status. 0: No thermal shutdown event issued. 1: Thermal shutdown event issued.
2	Read Only Read-Clear	PSIN_STS 0: No PSIN event issued. 1: PSIN event issued.

BIT	READ / WRITE	DESCRIPTION
1	Read Only Read-Clear	MSWAKEUP_STS => The bit is latched by the mouse wake-up event. 0: No mouse wake-up event issued. 1: Mouse wake-up event issued.
0	Read Only Read-Clear	KBWAKEUP_STS => The bit is latched by the keyboard wake-up event. 0: No keyboard wake-up event issued. 1: Keyboard wake-up event issued.

CR E4h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6~5	R / W	Power-loss control bits => (**VBAT**) 00: System always turns off when it returns from power-loss state. 01: System always turns on when it returns from power-loss state. 10: System turns off / on when it returns from power-loss state depending on the state before the power loss. 11: User defines the state before power loss.(i.e. the last state set of CRE6[4])
4	R / W	VSBGATE# Enable bit => 0: Disable. 1: Enable.
3	R / W	Keyboard wake-up options. **(LRESET#)** 0: Password or sequence hot keys programmed in the registers. 1: Any key.
2	R / W	Enable the hunting mode for all wake-up events set in CRE0. This bit is cleared when any wake-up events is captured. **(LRESET#)** 0: Disable. 1: Enable.
1~0	Reserved.	

CR E5h. (GPIOs Reset Source Register; Default 00))

BIT	READ / WRITE	DESCRIPTION
7~ 2	Reserved.	
1	R / W	PWROK source selection 0: PSON# 1: SUSB#
0	R / W	ATXPGD signal to control PWROK generation 0: Enable. 1: Disable.

CR E6h. (Default 1Ch)

BIT	READ / WRITE	DESCRIPTION
7	R / W	ENMDAT => **(VSB)** Three keys (ENMDAT_UP, CRE6 [7]; MSRKEY, CRE0 [4]; MSXKEY, CRE0 [1]) define the combinations of the mouse wake-up events. Please see the table in CRE0, bit 4 for the details.
6-5	Reserved	
4	R / W	Power-loss Last State Flag. **(VBAT)** 0: ON 1: OFF.
3~1	R / W	PWROK_DEL **(VSB)** Set the delay time when rising from 3VCC to PWROK. **Bits** **3 2 1** 0 0 0: 300 ~ 600mS 0 0 1: 330 ~ 670mS 0 1 0: 390 ~ 730mS 0 1 1: 520 ~ 860mS 1 0 0: 200 ~ 300mS 1 0 1: 230 ~ 370mS 1 1 0: 290 ~ 430mS 1 1 1: 420 ~ 560mS
0	R / W-Clear	PWROK_TRIG => Write 1 to re-trigger the PWROK signal from low to high.

CR E7h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	ENKD3 => **(VSB)** Enable the third set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 40h to 4eh. 0: Disable the third set of the key combinations. 1: Enable the third set of the key combinations.
6	R / W	ENKD2 => **(VSB)** Enable the second set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 30h to 3eh. 0: Disable the second set of the key combinations. 1: Enable the second set of the key combinations.

BIT	READ / WRITE	DESCRIPTION
5	R / W	ENWIN98KEY => **(VSB)** Enable Win98 keyboard dedicated key to wake-up system via PSOUT# when keyboard wake-up function is enabled. 0: Disable Win98 keyboard wake-up. 1: Enable Win98 keyboard wake-up.
4	R / W	EN_ONPSOUT **(VBAT)** Disable/Enable to issue a 0.5s delay PSOUT# level when system returns from power loss state and is supposed to be on as described in CRE4[6:5], logic device A. (for SiS & VIA chipsets) 0: Disable. 1: Enable.
3-1	Reserved.	
0	R / W	Hardware Monitor RESET source select **(VBAT)** 0: PWROK. 1: LRESET#.

CR E8h. (Reserved)

CR E9h. (Reserved)

CR F2h. (Default 7Ch) (VSB Power)

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W	Enable RSTOUT3# function. 0: Disable RSTOUT3#. 1: Enable RSTOUT3#.
4	R / W	Enable RSTOUT2# function. 0: Disable RSTOUT2#. 1: Enable RSTOUT2#.
3	Reserved	
2	R / W	Enable RSTOUT0# function. 0: Disable RSTOUT0#. 1: Enable RSTOUT0#.
1-0	Reserved	

CR F3h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7-0	Reserved	

CR F4h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7-0	Reserved	

CR F6h. (Default 00h) (VSB Power)

BIT	READ / WRITE	DESCRIPTION
7-0	Reserved	

CR F7h. (Default 00h) (VSB Power)

BIT	READ / WRITE	DESCRIPTION
7-0	Reserved	

CR FEh. (GPIO3 Event Route Selection Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	Reserved
6	R / W	0: Disable GP35 event route to PSOUT#. 1: Enable GP35 event route to PSOUT#.
5	R / W	0: Disable GP31 event route to PSOUT#. 1: Enable GP31 event route to PSOUT#.
4-0	Reserved.	

16.6 Logical Device B (Hardware Monitor)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Logical device is active.

CR 60h, 61h. (Default 00h, 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select the HM base address <100h: FFEh> along a two-byte boundary.

CR 70h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select the IRQ resource for HM.

CR F0h. (Default 81h)

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W	0: Disable AUXFANIN1 input de-bouncer. 1: Enable AUXFANIN1 input de-bouncer (1MHz).
4	R / W	0: Disable CPUFANIN1 input de-bouncer. 1: Enable CPUFANIN1 input de-bouncer (1MHz).
3	R / W	0: Disable AUXFANIN0 input de-bouncer. 1: Enable AUXFANIN0 input de-bouncer (1MHz).
2	R / W	0: Disable CPUFANIN0 input de-bouncer. 1: Enable CPUFANIN0 input de-bouncer (1MHz).
1	R / W	0: Disable SYSFANIN input de-bouncer. 1: Enable SYSFANIN input de-bouncer (1MHz).
0	Reserved	

CR F1h. (Reserved; Default 00h)

CR F2h. (FAN Strapping Status Register; Default 00h) (VCC Power)

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	

BIT	READ / WRITE	DESCRIPTION
0	Read Only	FAN_SET strapping status. This bit is strapped by pin 48(PLED). 0: Initial speed is 100%. 1: Initial speed is 50%.

16.7 Logical Device C (PECI)

CR E0h. (Agent Configuration Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	Agt4EN (Agent 4 Enable Bit) 0: Agent 4 is disabled. 1: Agent 4 is enabled.
6	R / W	Agt3EN (Agent 3 Enable Bit) 0: Agent 3 is disabled. 1: Agent 3 is enabled.
5	R / W	Agt2EN (Agent 2 Enable Bit) 0: Agent 2 is disabled. 1: Agent 2 is enabled.
4	R / W	Agt1EN (Agent 1 Enable Bit) 0: Agent 1 is disabled. 1: Agent 1 is enabled.
3	R / W	RTD4 0: Agent 4 always returns the relative temperature from domain 0. 1: Agent 4 always returns the relative temperature from domain 1.
2	R / W	RTD3 (Agent 3 Return Domain 1 Enable Bit. Functions only when Agt3D1 is set to 1) 0: Agent 3 always returns the relative temperature from domain 0. 1: Agent 3 always returns the relative temperature from domain 1.
1	R / W	RTD2 (Agent 2 Return Domain 1 Enable Bit. Functions only when Agt2D1 is set to 1) 0: Agent 2 always returns the relative temperature from domain 0. 1: Agent 2 always returns the relative temperature from domain 1.
0	R / W	RTD1 (Agent 1 Return Domain 1 Enable Bit. Functions only when Agt1D1 is set to 1) 0: Agent 1 always returns the relative temperature from domain 0. 1: Agent 1 always returns the relative temperature from domain 1.

CR E1h. (Agent 1 TBase Register; Default 48h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6~0	R / W	Agent 1 TBase (Range: 0~127). (Note 1)

CR E2h. (Agent 2 TBase Register; Default 48h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved	

BIT	READ / WRITE	DESCRIPTION
6~0	R / W	Agent 2 TBase (Range: 0~127). (note 1)

CR E3h. (Agent 3 TBase Register; Default 48h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6~0	R / W	Agent 3 TBase (Range: 0~127). (Note 1)

CR E4h. (Agent 4 TBase Register; Default 48h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6~0	R / W	Agent 4 TBase (Range: 0~127). (Note 1)

Note 1: TBase is a temperature refernce based on the experiment of processor actual temperature. For more details, please refer to 8.4 PECI.

CR E5h. (PECI Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	Agt4D1 (Agent 4 Domain 1 Enable Bit) 0: Agent 4 does not have domain 1. 1: Agent 4 has domain 1.
6	R / W	Agt3D1 (Agent 3 Domain 1 Enable Bit) 0: Agent 3 does not have domain 1. 1: Agent 3 has domain 1.
5	R / W	Agt2D1 (Agent 2 Domain 1 Enable Bit) 0: Agent 2 does not have domain 1. 1: Agent 2has domain 1.
4	R / W	Agt1D1 (Agent 1 Domain 1 Enable Bit) 0: Agent 1 does not have domain 1. 1: Agent 1 has domain 1.
3	R / W	PECI_1.1a_en 0: Normal PECI transmission. (Default) 1: PECI _1.1a transmission with PECI_REQUEST#.
2	Reserved	
1	R / W	Return High Temperature 0: The temperature of each agent is returned from domain 0 or domain 1, which is controlled by CRE0 bit 0~3. 1: Return the highest temperature in domain 0 and domain 1 of individual Agent.
0	Reserved	

CR E8h. (PECI Warning Flag Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	**Agent 4 Alert Bit** (When CR E8[3] is 0) 0: Agent 4 has valid FCS. 1: Agent 4 has invalid FCS in the previous 3 transactions.
		Agent 4 Absent Bit (When CR E8[3] is 1) 0: Agent 4 is detected. 1: Agent 4 cannot be detected.
6	R / W	**Agent 3 Alert Bit** (When CR E8[3] is 0) 0: Agent 3 has valid FCS. 1: Agent 3 has invalid FCS in the previous 3 transactions.
		Agent 3 Absent Bit (When CR E8[3] is 1) 0: Agent 3 is detected. 1: Agent 3 cannot be detected.
5	R / W	**Agent 2 Alert Bit** (When CR E8[3] is 0) 0: Agent 2 has valid FCS. 1: Agent 2 has invalid FCS in the previous 3 transactions.
		Agent 2 Absent Bit (When CR E8[3] is 1) 0: Agent 2 is detected. 1: Agent 2 cannot be detected.
4	R / W	**Agent 1 Alert Bit** (When CR E8[3] is 0) 0: Agent 1 has valid FCS. 1: Agent 1 has invalid FCS in the previous 3 transactions.
		Agent 1 Absent Bit (When CR E8[3] is 1) 0: Agent 1 is detected. 1: Agent 1 cannot be detected.
3~2	R / W	**Bank Select.** These two bits are used in Bank index selection. The relative data delivered over PECI interface and PECI Agent Absent Bit can be read from the registers below by setting Bank selection. The relative data delivered over PECI interface can be read in CR EE and CR EF, and the PECI warning flag can be read in CR E8 bit 7~4.
1~0	R / W	**PECI Speed Select.** **Bits** **1 0** 0 0: The PECI speed is 1.5 MHz 0 1: The PECI speed is 750 KHz 1 0: The PECI speed is 375 KHz 1 1: The PECI speed is 187 KHz

CR E9h. (Reserved)

CR EAh. (PECI_1.1a Status Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	Read_Only	**Reserved**
		Agent 4 Alert toggle bit (When CR E8[2] is 1) 0: PECI Alert bit never occurred. 1: PECI Alert bit occurred once. (Read clear)
6	Read_Only	**Reserved**
		Agent 3 Alert toggle bit (When CR E8[2] is 1) 0: PECI Alert bit never occurred. 1: PECI Alert bit occurred once. (Read clear)
5	Read_Only	**Reserved**
		Agent 2 Alert toggle bit (When CR E8[2] is 1) 0: PECI Alert bit never occurred. 1: PECI Alert bit occurred once. (Read clear)
4	Read_Only	**Reserved**
		Agent 2 Alert toggle bit (When CR E8[2] is 1) 0: PECI Alert bit never occurred. 1: PECI Alert bit occurred once. (Read clear)
3~0	Read_Only	**Reserved**. (When CR E8[2] is 0)

CR ECh. (PECI_1.1a Status Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~3	R / W	Reserved.

BIT	READ / WRITE	DESCRIPTION
2~0	R / W	PECI Transmission cycle time: **Bits** **2 1 0** 0 0 0 : Finish one PECI message transmission every 0.0625sec(16Hz) 0 0 1 : Finish one PECI message transmission every 0.125sec(8Hz) 0 1 0 : Finish one PECI message transmission every 0.25sec(4Hz) 0 1 1 : Finish one PECI message transmission every 0.5sec(2Hz) 1 0 0 : Finish one PECI message transmission every 1sec(1Hz) 1 0 1 : Finish one PECI message transmission every 2sec(1/2Hz) 1 1 0 : Finish one PECI message transmission every 4sec(1/4Hz)

CR FEh. (PECI Agent Relative High Byte Temperature Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only	This register shows the retrieved High Byte raw data from PECI interface. When Bank Select (CR E8 bit 3~2) **Bits** **3 2** = 0 0 Agt1RelTemp (High Byte) = 0 1 Agt2RelTemp (High Byte) = 1 0 Agt3RelTemp (High Byte) = 1 1 Agt4RelTemp (High Byte)

CR FFh. (PECI Agent Relative Low ByteTemperature Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only	This register shows the retrieved High Byte raw data from PECI interface. When Bank Select (CR E8 bit 3~2) **Bits** **3 2** = 0 0 Agt1RelTemp (Low Byte) = 0 1 Agt2RelTemp (Low Byte) = 1 0 Agt3RelTemp (Low Byte) = 1 1 Agt4RelTemp (Low Byte)

17. SPECIFICATIONS

17.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNIT
3VCC	Power Supply Voltage (3.3V)	-0.3 to 3.6	V
VI	Input Voltage	-0.3 to 3VCC+0.3	V
	Input Voltage (5V tolerance)	-0.3 to 5.5	V
TA	Operating Temperature	0 to +70	°C
TSTG	Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

17.2 DC CHARACTERISTICS

(T_a = 0°C to 70°C, V_{DD} = 3.3V ± 5%, V_{SS} = 0V)

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
RTC Battery Quiescent Current	I_{BAT}			2.4	μA	V_{BAT} = 2.5 V CASEOPEN Pull-Up to V_{BAT}
ACPI Stand-by Power Supply Quiescent Current	I_{SB}			2.0	mA	V_{SB} = 3.3 V, All ACPI pins are not connected.
VCC Quiescent Current	I_{VCC}			25	mA	V_{SB} = 3.3V V_{CC} (AVCC) = 3.3V LRESET = High IOCLK = 48MHz CASEOPEN Pull-Up to V_{BAT}
Vtt Quiescent Current	I_{VTT}			1	mA	V_{SB} = 3.3V V_{CC} (AVCC) = 3.3V V_{TT} = 1.2V LRESET = High IOCLK = 48MHz CASEOPEN Pull-Up to V_{BAT}
I/O_{8t} – TTL–level, bi-directional pin with 8mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 8 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{12t} – TTL-level, bi-directional pin with 12mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{24t} – TTL-level, bi-directional pin with 24mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{12tp3} – 3.3V TTL-level, bi-directional pin with 12mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{12ts} – TTL–level, Schmitt-trigger, bi-directional pin with 12mA source-sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{CC}=3.3V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{24ts} – TTL–level, Schmitt-trigger, bi-directional pin with 24mA source-sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{CC}= 3.3V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{24tsp3} – 3.3V TTL-level, Schmitt-trigger, bi-directional pin with 24mA source-sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Hystersis	V_{TH}	0.5	1.2		V	V_{CC}=3.3V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/OD_{12t} – TTL–level, bi-directional pin and open-drain output with 12mA sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/OD_{16t} – TTL–level, bi-directional pin and open-drain output with 16mA sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/OD_{24t} – TTL–level, bi-directional pin and open-drain output with 24mA sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
I/O_{12tp3} – 3.3V TTL–level, bi-directional pin and open-drain output with 12mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
$I/OD16_{ts}$ – TTL–level, Schmitt-trigger, bi-directional pin and open-drain output with 16mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{CC}=3.3V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{24ts} – TTL level, Schmitt-trigger, bi-directional pin and open-drain output with 24mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{CC}=3.3V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD12$_{cs}$ – CMOS–level, Schmitt-trigger, bi-directional pin and open-drain output with 12mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
I/OD16$_{cs}$ – CMOS–level, Schmitt-trigger, bi-directional pin and open-drain output with 16mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
I/OD12$_{csd}$ – CMOS–level, Schmitt-trigger, bi-directional pin with internal pulled-down resistor and open-drain output with 12mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
I/OD12$_{csu}$ – CMOS–level, Schmitt-trigger, bi-directional pin with internal pulled-up resistor and open-drain output with 12mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
O4 - Output pin with 4mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -4 mA
O8 – Output pin with 8mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -8 mA
O12 – Output pin with 12mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
O16 – Output pin with 16mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -16 mA
O24 – Output pin with 24mA source-sink capability						

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
O_{12p3} – 3.3V output pin with 12mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
O_{24p3} – 3.3V output pin with 24mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
OD_{12} – Open-drain output pin with 12mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
OD_{24} – Open-drain output pin with 24mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
OD_{12p3} – 3.3V open-drain output pin with 12mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
IN_t – TTL-level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tp3} – 3.3V TTL-level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V

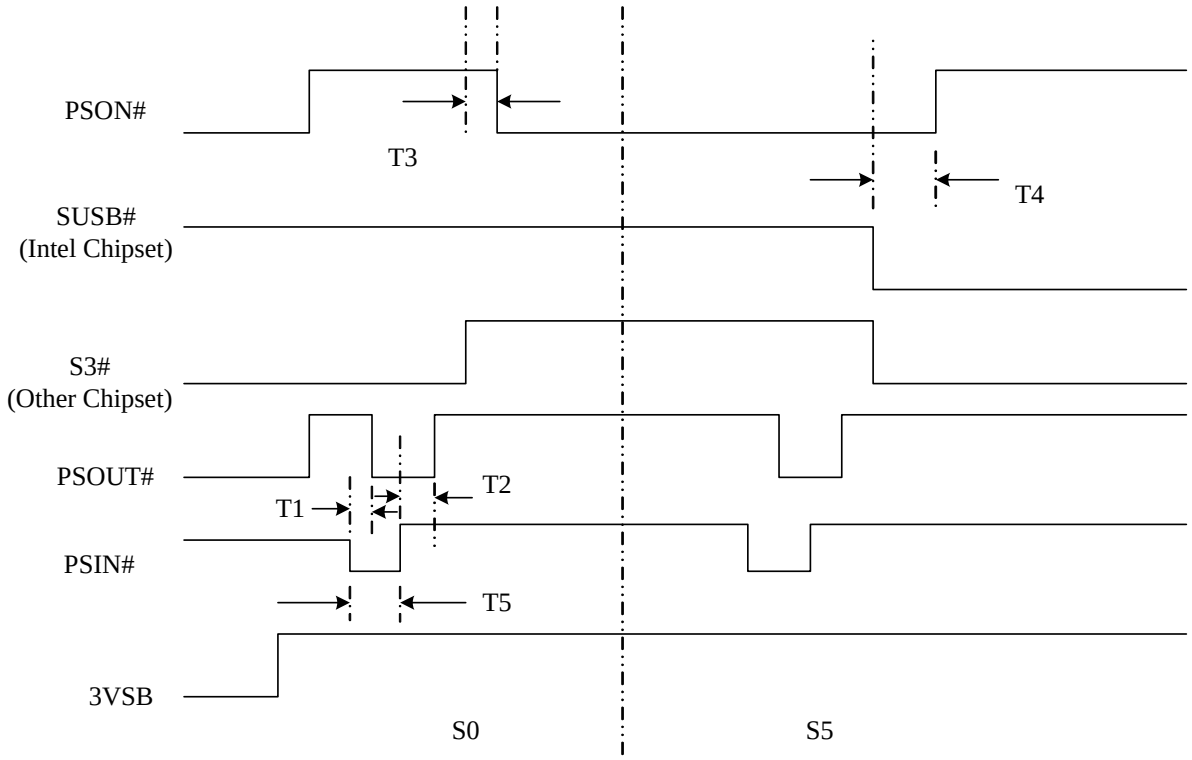
PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{td} – TTL-level input pin with internal pulled-down resistor						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tu} – TTL-level input pin with internal pulled-up resistor						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{ts} – TTL–level, Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tsp3} – 3.3 V TTL-level, Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_C – CMOS-level input pin						
Input Low Voltage	VIL			0.3 V_{CC}	V	
Input High Voltage	VIH	0.7 V_{CC}			V	
Input High Leakage	ILIH			+10	μA	VIN = V_{CC} = 3.3V
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
IN_{cd} – CMOS-level input pin with internal pulled-down resistor						
Input Low Voltage	V_{IL}			0.3 V_{CC}	V	
Input High Voltage	V_{IH}	0.7 V_{CC}			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = V_{CC} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
Input Low Voltage	V_{IL}			0.3 V_{CC}	V	
IN_{cu} – CMOS-level input pin with internal pulled-up resistor						
Input High Voltage	V_{IH}	0.7 V_{CC}			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = V_{CC} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{cs} – CMOS–level, Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	1.3	1.5	1.7	V	V_{CC} = 3.3V
Hystersis	V_{TH}	1.5	2		V	V_{CC} = 3.3V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{csu} – CMOS–level, Schmitt-trigger input pin with internal pulled-up resistor						

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
AOUT – Analog output						
		N.A.				
IN_{V1S} – VID input pin for INTEL® VRM10.0, and VRM11 design						
Input Low Voltage	V_{IL}			0.4	V	
Input High Voltage	V_{IH}	0.6			V	
IN_{V2S} – VID input pin for AMD™VRM design						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	1.4			V	
I/O_{V3} – Bi-direction pin with source capability of 6 mA and sink capability of 1 mA for INTEL® PECI						
Input Low Voltage	V_{IL}	0.275Vtt		0.5Vtt	V	
Input High Voltage	V_{IH}	0.55Vtt		0.725Vtt	V	
Output Low Voltage	V_{OL}			0.25Vtt	V	
Output High Voltage	V_{OH}	0.75Vtt			V	
Hysterisis	V_{Hys}	0.1Vtt			V	

17.3 AC CHARACTERISTICS

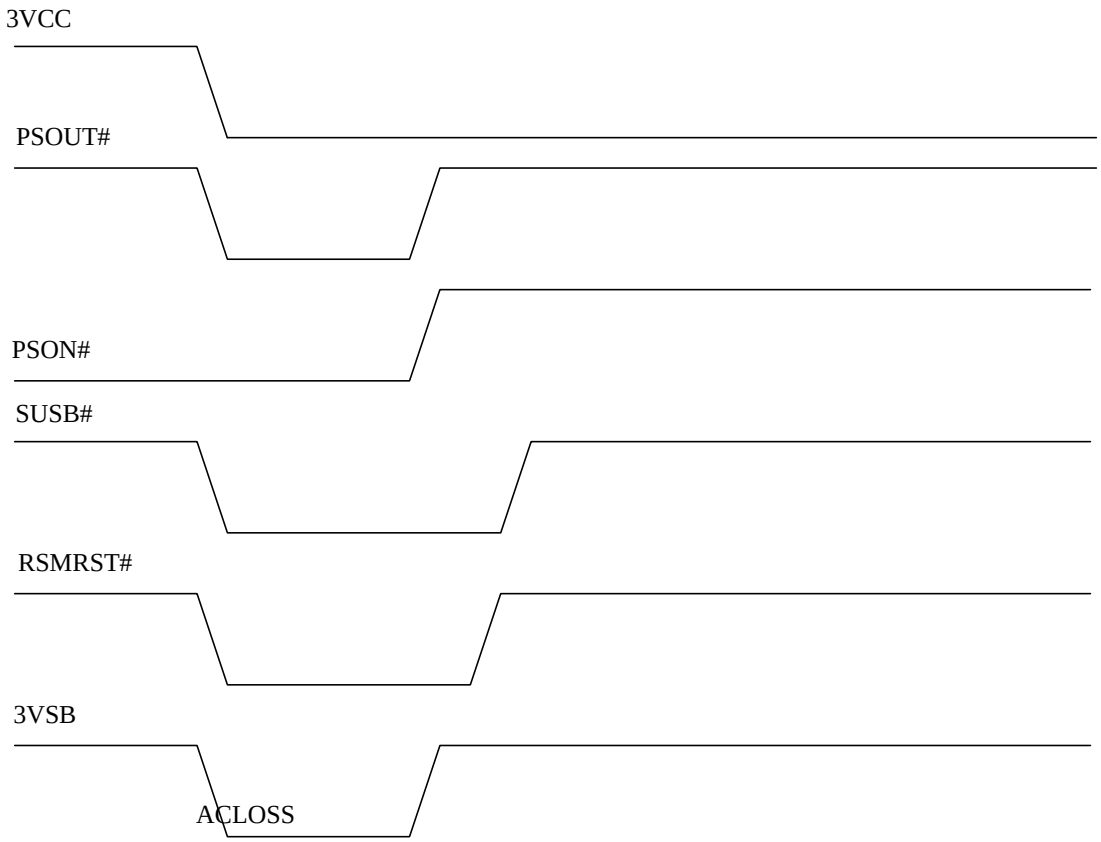
17.3.1 Power On / Off Timing



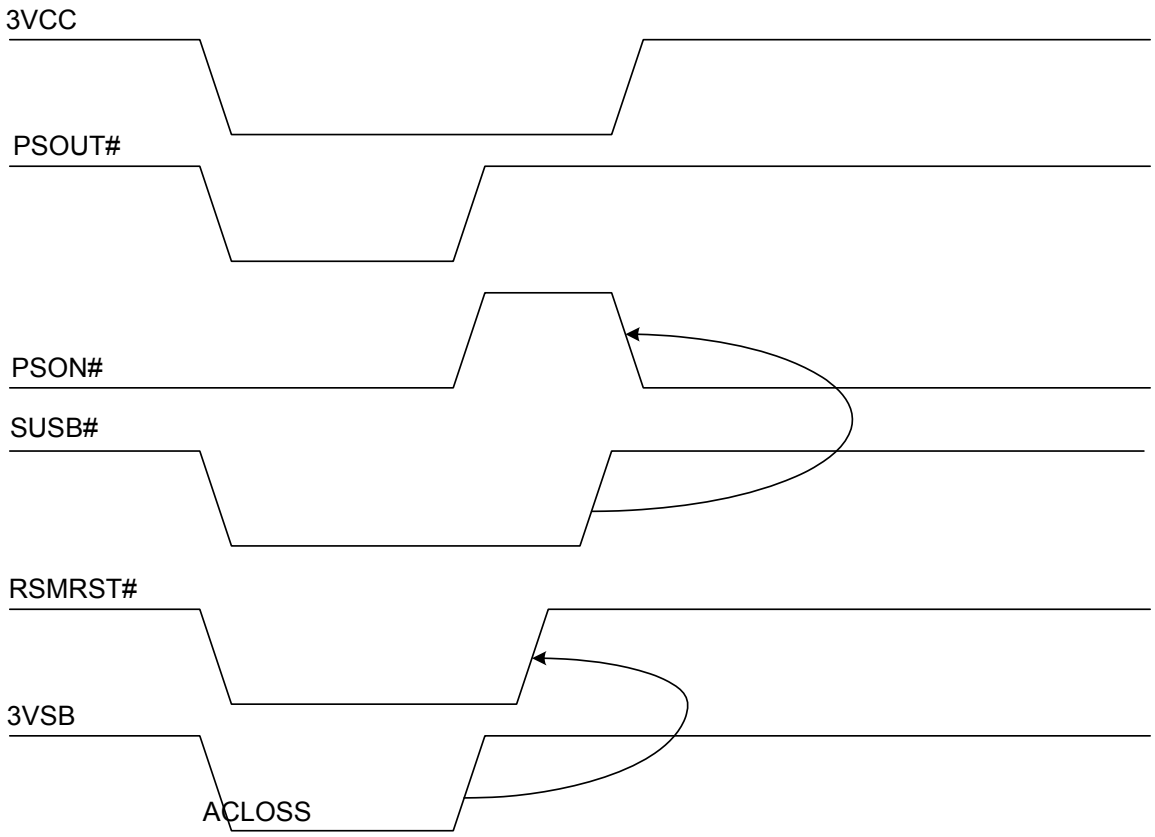
	T1	T2	T3	T4	T5
IDEAL TIMING (SEC)	64m	16m	32m	15-45m	Over 64m at least

17.3.2 AC Power Failure Resume Timing

1. Logical Device A, CR[E4h] bits[6:5]= “00” means “OFF” state
(“OFF” means the system is always turned off after the AC power loss recovered)



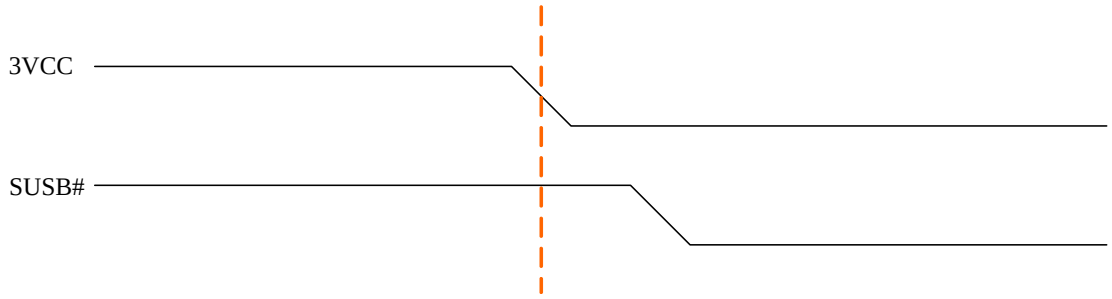
2. Logical Device A, CR[E4h] bits[6:5] = “01” means “ON” state
(“ON” means the system is always turned on after the AC power loss recovered)



**** What's the definition of former state at AC power failure?**

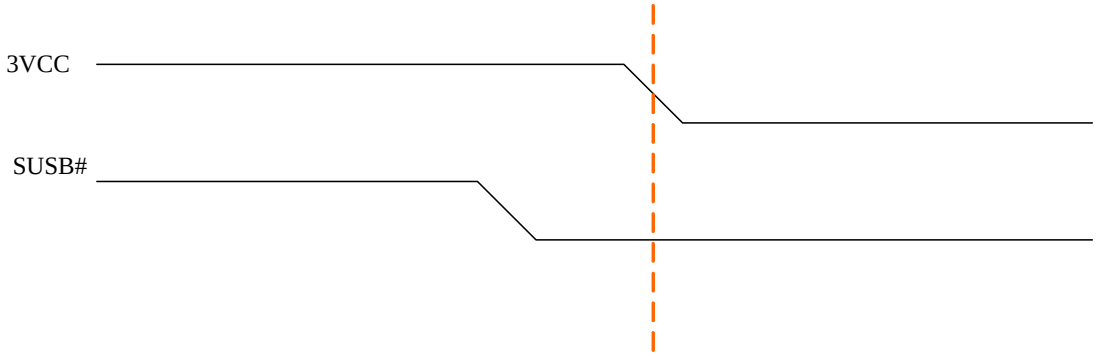
1) The previous state is "ON"

3VCC falls to 2.6V and SUSB# keeps at VIH 2.0V



2) The previous state is "OFF"

3VCC falls to 2.6V and SUSB# keeps at VIL 0.8V



To ensure that VCC does not fall faster than VSB in various ATX Power Supplies, the W83527HG adds the option of "user define mode" for the pre-defined state before AC power failure. BIOS can set the pre-defined state for the system to be "On" or "Off". According to this setting, the system chooses the state after the AC power recovery.

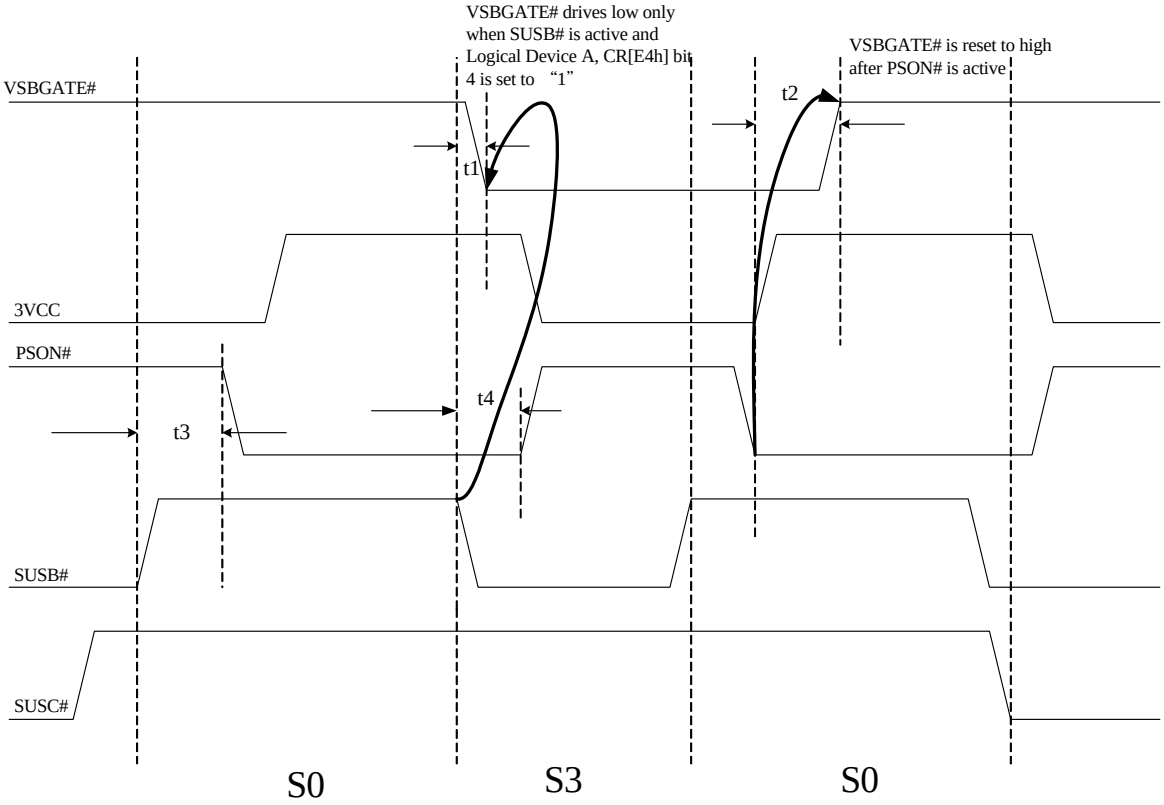
Logical Device A, CR E4h

BIT	READ / WRITE	DESCRIPTION
6~5	R / W	Power-loss control bits => (**VBAT**) 00: System always turns off when it returns from power-loss state. 01: System always turns on when it returns from power-loss state. 10: System turns off / on when it returns from power-loss state depending on the state before the power loss. 11: User defines the state before the power loss. (The previous state is set at CRE6[4])

Logical Device A, CR E6h

BIT	READ / WRITE	DESCRIPTION
4	R / W	Power loss Last State Flag. **(VBAT)** 0: ON 1: OFF

17.3.3 VSBGATE# Timing

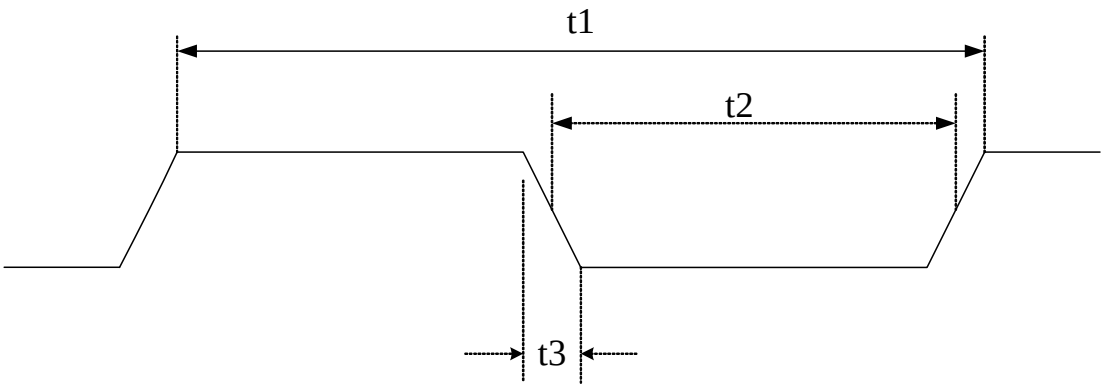


SYMBOL	PARAMETER	MIN	MAX	UNIT
t1	SUSB# active to VSBGATE# active	0	80	nS
t2	PSON# active to VSBGATE# inactive	90	142	mS
t3	SUSB# inactive to PSON# active	0	80	nS
t4	SUSB# active to PSON# inactive	15	45	mS

Note. The values above the worst-case results of R&D simulation

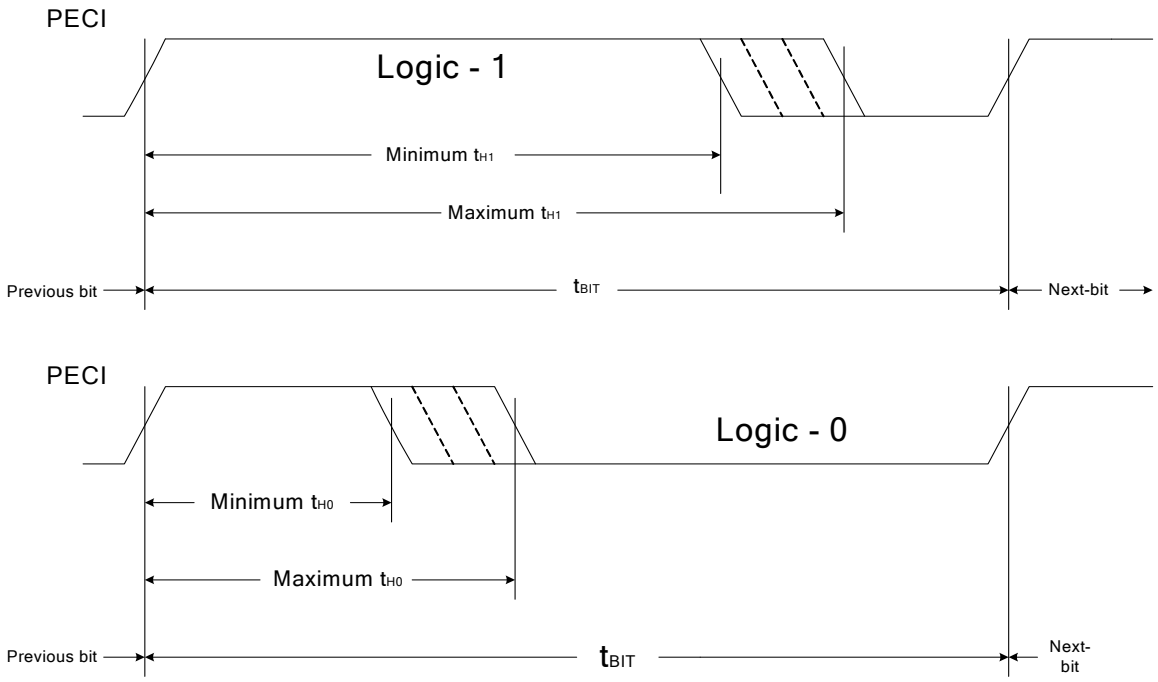
17.3.4 Clock Input Timing

PARAMETER	48MHZ / 24MHZ		UNIT
	MIN	MAX	
Cycle to cycle jitter		300/500	ps
Duty cycle	45	55	%



PARAMETER	DESCRIPTION	48MHZ / 24MHZ			UNIT
		MIN	TYP	MAX	
t1	Clock cycle time		20.8 / 41.7		ns
t2	Clock high time/low time	9 / 19	10 / 21		ns
t3	Clock rising time/falling time (0.4V~2.4V)			3	ns

17.3.5 PECI Timing

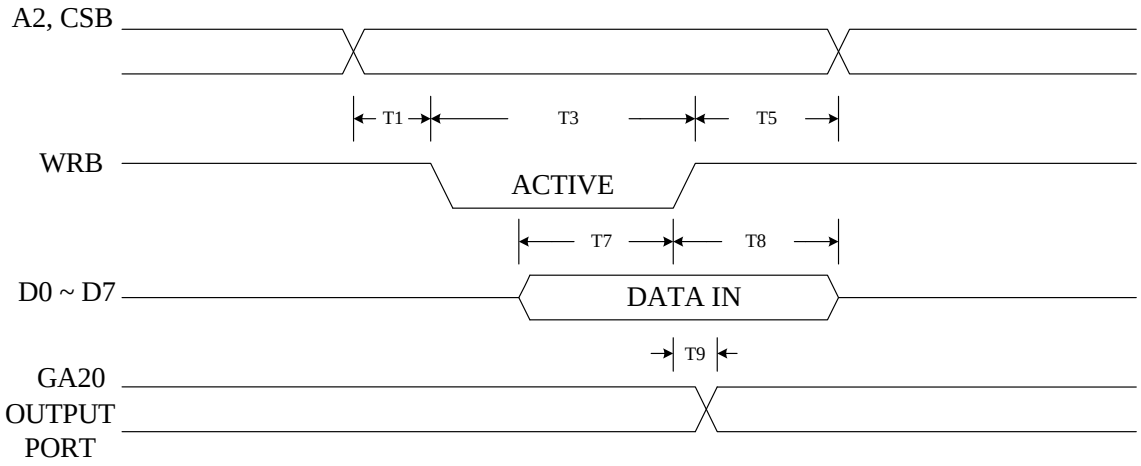


SYMBOL		MIN	TYP	MAX	UNITS
t_{BIT}	Client	0.495		500	μs
	Originator	0.495		250	
t_{H1}		0.6	3/4	0.8	× t_{BIT}
t_{H0}		0.2	1/4	0.4	× t_{BIT}

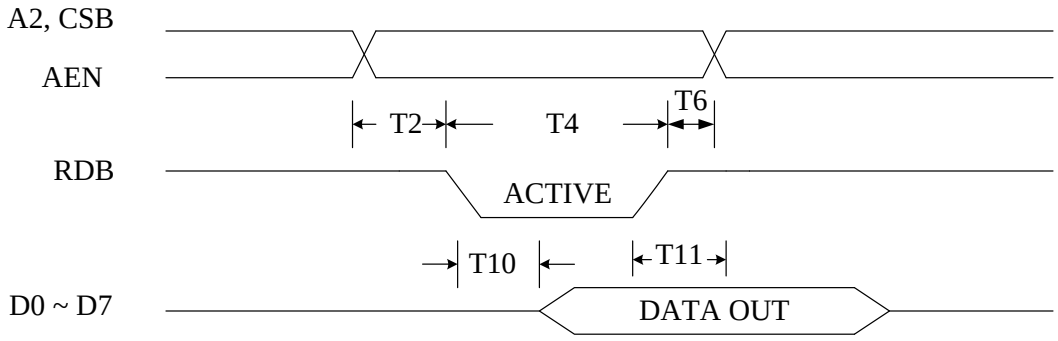
17.3.6 KBC Timing Parameters

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T1	Address Setup Time from WRB	0		nS
T2	Address Setup Time from RDB	0		nS
T3	WRB Strobe Width	20		nS
T4	RDB Strobe Width	20		nS
T5	Address Hold Time from WRB	0		nS
T6	Address Hold Time from RDB	0		nS
T7	Data Setup Time	50		nS
T8	Data Hold Time	0		nS
T9	Gate Delay Time from WRB	10	30	nS
T10	RDB to Drive Data Delay		40	nS
T11	RDB to Floating Data Delay	0	20	nS
T12	Data Valid After Clock Falling (SEND)		4	μS
T13	K/B Clock Period	20		μS
T14	K/B Clock Pulse Width	10		μS
T15	Data Valid Before Clock Falling (RECEIVE)	4		μS
T16	K/B ACK After Finish Receiving	20		μS
T19	Transmit Timeout		2	mS
T20	Data Valid Hold Time	0		μS
T21	Input Clock Period (6–16 Mhz)	63	167	nS
T22	Duration of CLK inactive	30	50	μS
T23	Duration of CLK active	30	50	μS
T24	Time from inactive CLK transition, used to time when the auxiliary device sample DATA	5	25	μS
T25	Time of inhibit mode	100	300	μS
T26	Time from rising edge of CLK to DATA transition	5	T28-5	μS
T27	Duration of CLK inactive	30	50	μS
T28	Duration of CLK active	30	50	μS
T29	Time from DATA transition to falling edge of CLK	5	25	μS

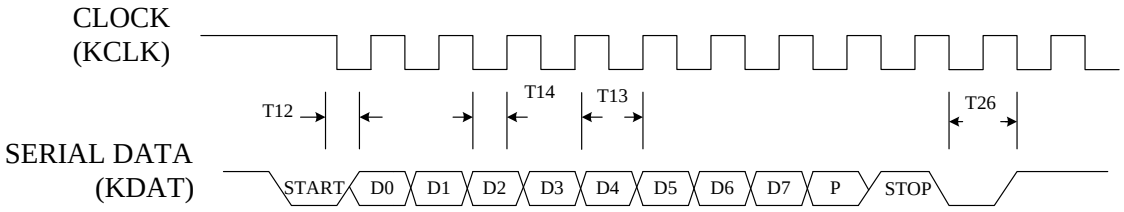
17.3.6.1. Writing Cycle Timing



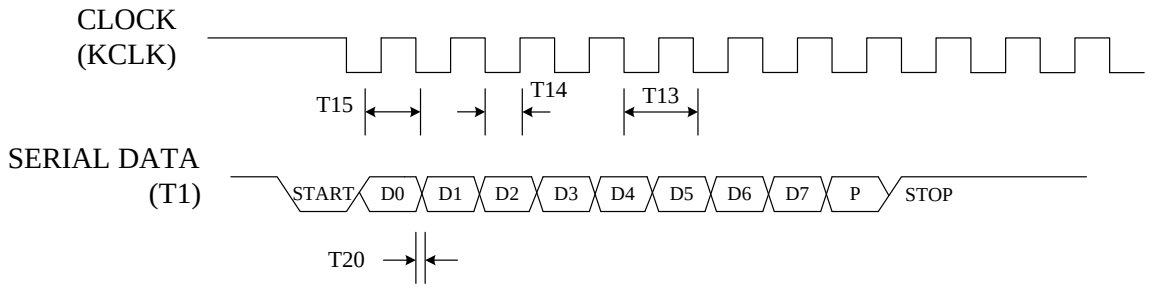
17.3.6.2. Read Cycle Timing



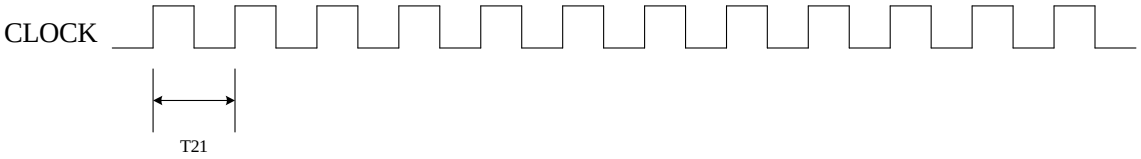
17.3.6.3. Send Data to K/B



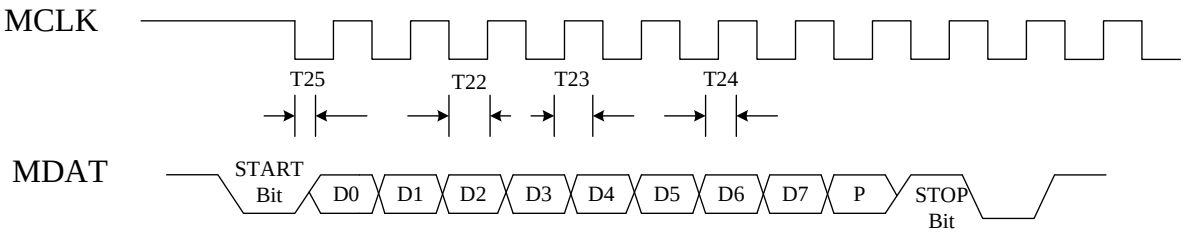
17.3.6.4. Receive Data from K/B



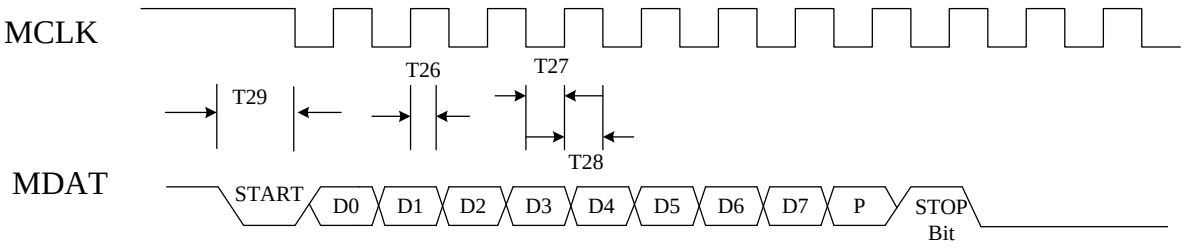
17.3.6.5. Input Clock



17.3.6.6. Send Data to Mouse



17.3.6.7. Receive Data from Mouse



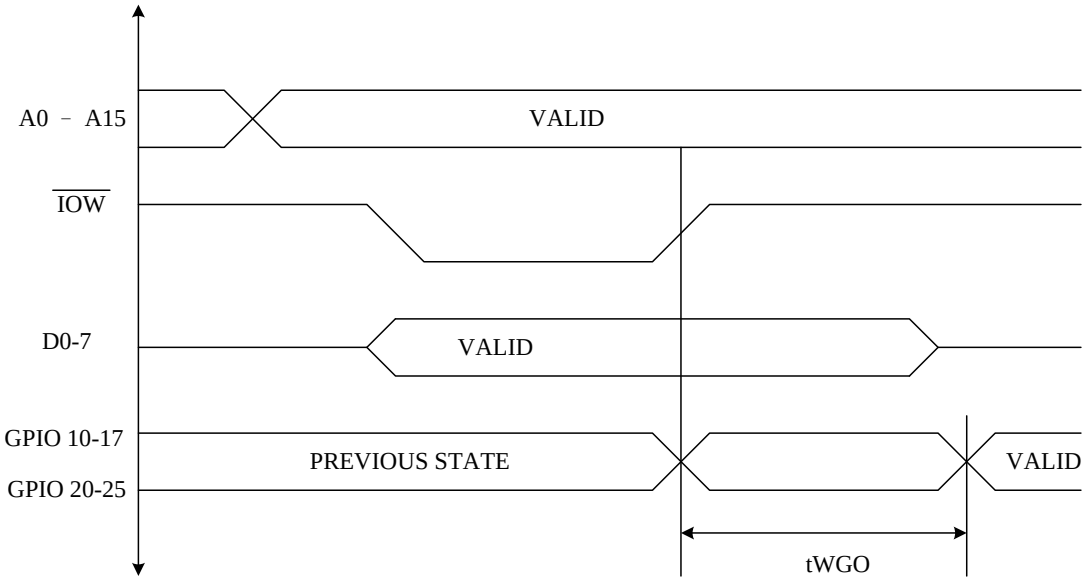
17.3.7 GPIO Timing Parameters

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WGO}	Write data to GPIO update		300(Note 1)	ns
t_{SWP}	SWITCH pulse width	16		msec

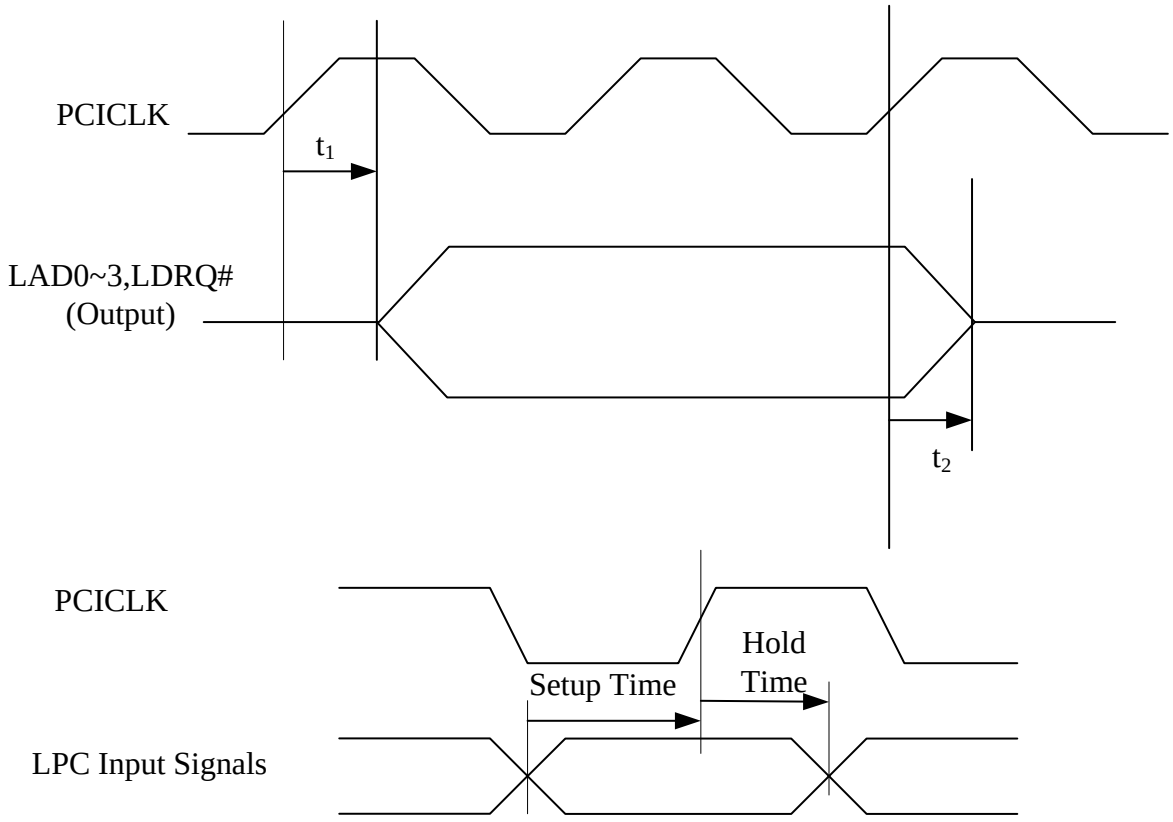
Note: Refer to Microprocessor Interface Timing for Read Timing.

17.3.7.1. GPIO Write Timing

GPIO Write Timing diagram



17.4 LPC Timing



SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
t_1	Output Valid Delay	4	11	nS
t_2	Float Delay	4	11	nS
t_3	LAD[3:0] Setup Time	14		nS
t_4	LAD[3:0] Hold Time	0		nS
t_5	LFRAME# Setup Time	12		nS
t_6	LFRAME# Hold Time	0		nS

18. TOP MARKING SPECIFICATIONS

The top marking of W83527HG

First Line	Nuvoton Logo.
Second Line	The chip part number: W83527HG
Third Line	Serial number
Fourth Line	Tracking Code: 8 12 G 9 C FA For Package information

8 Package was made in 2008

12 Week: 12

G Assembly house ID; G means Greatek; A means ASE; O means OSE

9 code version; 9 means code 009

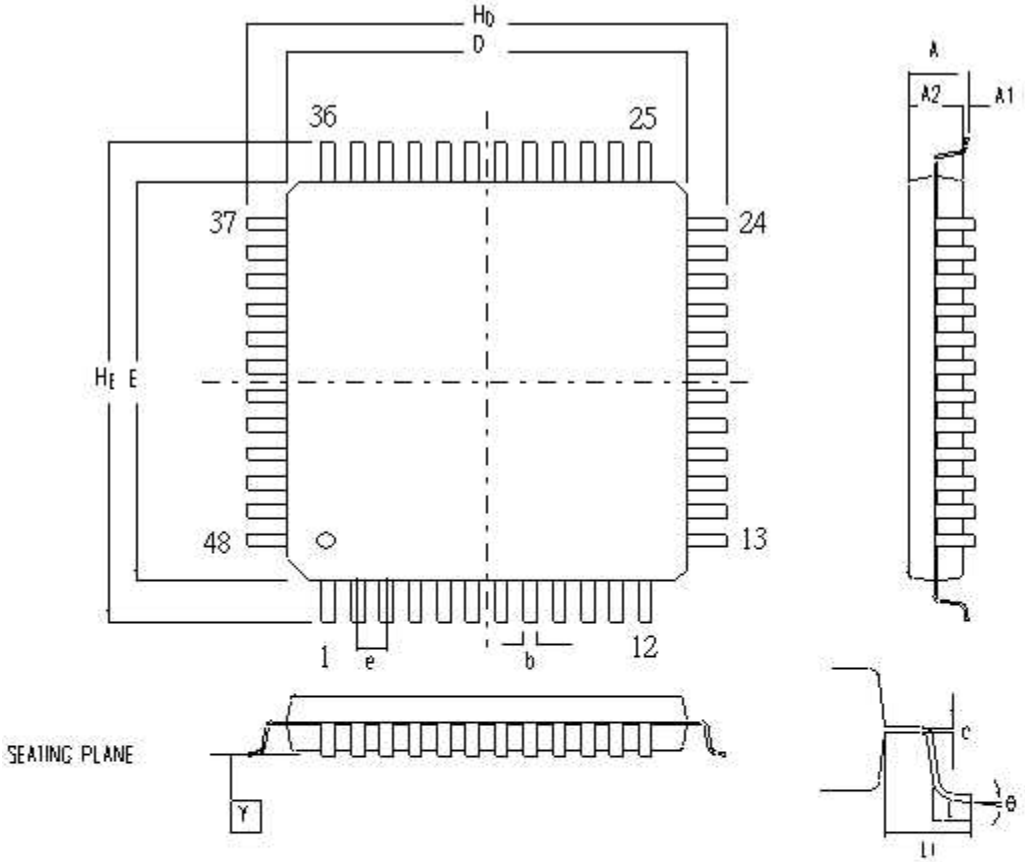
C The IC version

FA The Mask version

19. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83527HG	48-pin LQFP (Pb-free package)	Commercial 0℃ to +70℃

20. PACKAGE SPECIFICATION



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	0.004	0.006	0.05	0.10	0.15
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
HD	0.350	0.354	0.358	8.90	9.00	9.10
HE	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

48-pin (LQFP)

21. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
1.0	04/25/2008	N.A.	1. First published version.
1.1	06/10/2008	5, 7-12, 9, 127, 134	1. Add power sources to the pin layout. 2. Update the description of pin 25. 3. Specify the default of pin 18, 19, 21, 22, 23, 26, 28, 30, and 31. 4. Update CR[F0h] of 15.6 Logical Device B (Hardware Monitor). 5. Update the values in 16.1 Absolute Maximum Ratings.
1.2	06/19/2008	3, 13, 105, 127	1. Remove the description of PME# in Chapter 2 Features. 2. Modify the title of Chapter 6 to ACPI Glue Logic. 3. Update Chapter 13 General Purpose I/O. 4. Correct the default value of CRF0h in 15.6 Logical Device B (Hardware Monitor).
1.3	07/11/2008	5	1. Modify Chapter 4 Pin Layout.
1.4	10/14/2008	64, 66, 110, 123, 125, 126, 127, 147, 150	1. Modify the descriptions of 9.41 and 9.44. 2. Correct the description of bit 4 of CR[2Ch] of 16.1 Chip (Global) Control Register. 3. Update the descriptions of CR[30h], bit 7 of CR[E4h], bit 1 of CR[E5h], bits 3-1 of CR[E6h], and bit 4 of CR[E7h] of 16.5 Logical Device A (ACPI). 4. Correct the T4 timing of 17.3.1 Power On/ Off Timing. 5. Modify 17.3.2 AC Power Failure Resume Timing.
1.5	12/25/2009	63, 64, 79, 80	1. Correct the description of bit 3-1 of 9.86 FANCTRL6 SMART FAN™ III+ input source & output FAN select Register – Index 5Eh (Bank 1). 2. Update the descriptions of 9.41 and 9.44.

Important Notice

Nuvoton products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Furthermore, Nuvoton products are not intended for applications wherein failure of Nuvoton products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Nuvoton customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nuvoton for any damages resulting from such improper use or sales.