Winbond

W86C452

I/O CONTROL CHIP FOR IBM PC/AT

GENERAL DESCRIPTION

The W86C452 is an enhanced dual-channel version of the popular W86C450 asynchronous communication element (ACE) fabricated using WINBOND'S CMOS process. It is equivalent to VL16C452 of the VLSI Technology Inc.

The device surports two serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU.

The CPU can read the complete status of the UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the UART as well as any error conditions (parity, overrun, framing, or break interrupt).

The UART includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to (2^{16} -1), and producing a 16 × clock for driving the internal transmiter logic. Provisions are also included to use this 16 × clock to drive the receiver logic. The UART includes a complete MODEM-control capability and a processor-interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle the communications link.

In addition to its communication interface capabilities, the W86C452 provides the user with a fully bidirectional parallel Centronics type printer. This port allows information received from either serial communication port to be printed from the dual ACE.

FEATURES

- Easily interfaces to most popular microprocessors.
- Dual-channel version of W86C450
- Centronix printer interface
- Independently controlled transmit, receive, line status, and data set interrupts.
- Programmable baud generator allows division of any input clock by 1 to (2^{16} -1) and generates the internal 16 × clock.
- Independent receiver clock input.
- MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD).
- Fully programmable serial-interface characteristics:
  - -5, 6, 7, or 8-bit characters
  - -Even, odd, or no-parity bit generation and detection
  - -1, 1.5 or 2-stop bit generation
- False start bit detection.
- TRI-STATE TTL drive capabilities for bidirectional data bus and control bus on each channel
- Internal diagnostic capabilities:
  - -Loopback controls for communications link fault isolation
  - -Break, parity, overrun, framing error simulation.
- Fully prioritized interrupt system controls.

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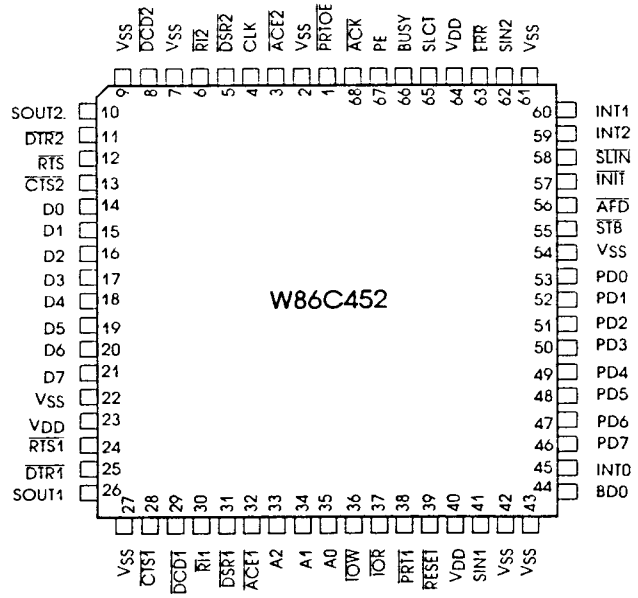
PIN CONFIGURATION



PIN DESCRIPTIONS

SINGAL NAME	PIN NO.	TYPE	SIGNAL DESCRIPTION
$\overline{IOR}$	37	I	Input/Output Read Strobe: This is an active low input which causes the selected channel to output data to the data bus (DB0-DB7). The data output depends upon the register selected by the address inputs A0, A1, A2. Chip select 0 ($\overline{ACE1}$) selects UART #1, chip select 1 ($\overline{ACE2}$) selects UART #2, and chip select 2 ($\overline{PRT1}$) selects the line printer part.
$\overline{IOW}$	36	I	Input/Output Write Strobe: This is an active low input which causes data from the data bus (DS0-DB7) to be input to either UART or to the parallel port. The data input depends upon the register selected by the address inputs A0, A1, A2. The chip select inputs ($\overline{ACE1}$, $\overline{ACE2}$, and $\overline{PRT1}$) enable UART #1,UART#2, and the parllel port (respectively).
DB0 / DB7	14 / 21	I/O	Data Bits DB0-DB7: The Data Bus provides eight, three-state I/O lines for the transfer of data, control and status information between the W86C452 and the CPU. These lines are normally in a high-impedance state except during read operations. D0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted.

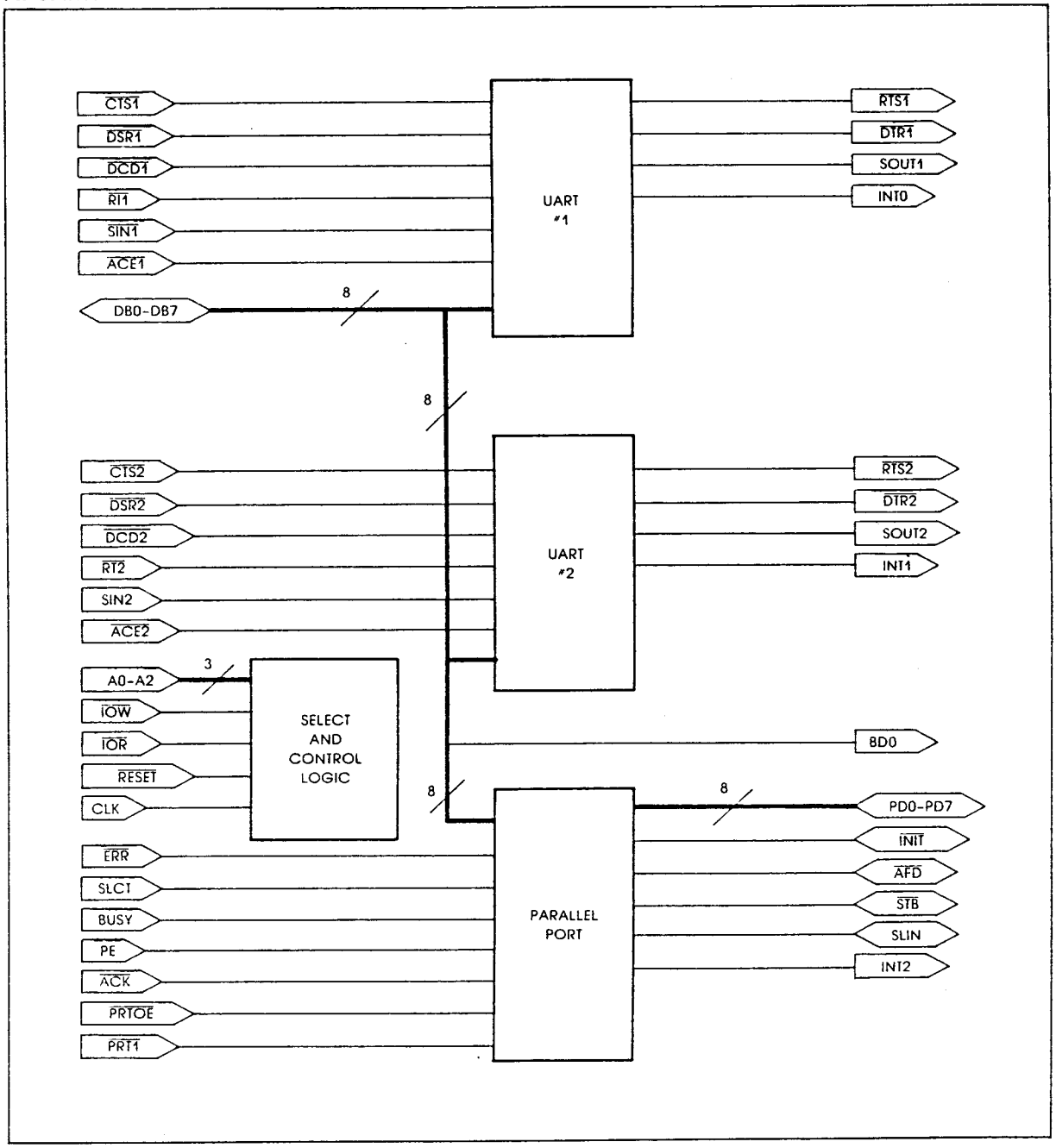
SINGAL NAME	PIN NO.	TYPE	SIGNAL DESCRIPTION
A0 A1 A2	35 34 33	I	Address Lines A0-A2: The address lines select the internal registers during CPU bus operations. See Table 1 for the decode of the serial channels. Table 5 for the decde of the parallel line printer port.
CLK	4	I	Clock Input:The external clock input.
SOUT1 SOUT2	26 10	O	Serial Data Outputs: These lines are the serial data outputs from the UARTs' transmitter circuitry. A mark (1) is a logic "one" (high) and space (0) is a logic "zero" (low). Each SOUT is held in the mark condition when the transmitter is disabled, Reset is true, the Transmitter Register is empty, or when in the Loop Mode.
$\overline{CTS1}$ $\overline{CTS2}$	28 13	I	Clear to Send Inputs: The logical state of each $\overline{CTS}$ pin is reflected in the CTS bit of the (MSR) Modem Status Register [CTS is bit 4 of the MSR, written MSR (4)] of each UART. A change of state in either CTS pin since the previous reading of the associated MSR causes the setting of DCTS [MSR(0)] of each Modem Status Register. When a CTS pin is active (low), the modem is indicating that data on the associated SOUT can be transmitted.
$\overline{DSR1}$ $\overline{DSR2}$	31 5	I	Data Set Ready Inputs: The logical state of the DSR pins is reflected in MSR(5) of its associated MODEM Status Register. DDSR [MSR(1)] indicates whether the associated DSR pin has changed state since the previous reading of the MSR. When a DSR pin is low, its modem is indicating that it is ready to exchange data with the associated UART.
$\overline{DTR1}$ $\overline{DTR2}$	25 11	O	Data Terminal Ready Lines: Each DTR pin can be set (low) by writing a logic 1 to MCR(0), Modem Control Register bit 0 of its associated UART. This signal is cleared (high) by writing a logic 0 to the DTR bit [MCR(0)] or whenever a reset occurs. When active (low), the DTR pin indicates to the DCE that its UART is ready to receiver data.
$\overline{RTS1}$ $\overline{RTS2}$	24 12	O	Request to Send Outputs: The $\overline{RTS}$ signal is an output on each UART used to enable the modem. An $\overline{RTS}$ pin is set low by writing a logic 1 to MCR(1) bit 1 of its UART's Modem Control Register. Both $\overline{RTS}$ pins are reset high by Reset. When active, an RTS pin indicates to the DCE that its UART has data ready to transmit. In half duplex operations, $\overline{RTS}$ is used to control the direction of the line.
$\overline{RI1}$ $\overline{RI2}$	30 6	I	Ring Indicator Inputs: When low, $\overline{RI}$ indicates that a telephone ringing signal has been received by the modem or data set. The $\overline{RI}$ signal is a modem control input whose condition is tested by reading MSR(6) (RI) of each UART. The Modem Status Register output TERI [MSR(2)] indicates whether the RI input has changed from high to low since the previous reading of the MSR. If the interrupt is enabled [IER(3)=1] and RI changes from a high to low, an interrupt is generated.

SINGAL NAME	PIN NO.	TYPE	SIGNAL DESCRIPTION
$\overline{PRTOE}$	1	I	Line Printer Output Enable: This input signal enables the parallel line printer when it is low. When this signal is high, the pins of the line printer are held in a high-impedence state. This line may be tied to ground for normal line printer operation.
V_{DD}	23 40 64	I	Power Supply: 5V ±5%
V_{SS}	2,7 9,22 27 42 43 54 61	I	Ground (0V): All pins must be tied to ground for proper operation.
$\overline{DCD1}$ $\overline{DCD2}$	29 8	I	Data Carry Detect: When active (low), $\overline{DCD}$ indicates that the data carrier has been detected by the modem or data set. $\overline{DCD}$ is a modem input whose condition can be tested by the CPU by reading MSR(7) (DCD) of the Modem Status Registers. MSR(3) (DDCD) of the Modem Status Register indicates whether the $\overline{DCD}$ input has changed since the previous reading of the MSR. $\overline{DCD}$ has no effect on the receiver. If the $\overline{DCD}$ changes state with the modem status interrupt enabled, an interrupt is generated.
$\overline{RESET}$	39	I	Reset: When low, the reset input forces the W86C452 into an idle mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The Line Status Register (LSR) is cleared except for the THRE and TEMT bits, which are set. All functions of the device remain in an idle state until programmed to resume serial data activities.
INT0 INT1	45 60	O	Serial Channel Interrupts: Each serial channel interrupt goes active (high) when one of the following interrupts has an active (high) condition and is enabled by the Interrupt Enable Register of its associated channel: Receiver Error flag. Received Data Available, Transmitter Holding Register Empty, and Modem Status. The interrupt is reset low upon appropriate service or a reset operation.
SIN1 SIN2	41 62	I	Serial Data Inputs: The serial data inputs move information from the communication line or moderm to the W85C452 receiver circuits. A mark (1) is high, and a space (0) is low. Data on serial data inputs is disabled when operating in the loop mode.
$\overline{ACE1}$ $\overline{ACE2}$ $\overline{PRT1}$	32 3 38	I	Chip Selects: Each Chip Select input acts as an enable for the write and read signals for the serial channels ($\overline{ACE1}$) and 2 ($\overline{ACE2}$). $\overline{PRT1}$ enables the the signals to the line printer port.

SINGAL NAME	PIN NO.	TYPE	SIGNAL DESCRIPTION
BD0	44	O	Bus Buffer Output: This active high output is asserted when either serial channel or the parallel port is selected as an output. This output can be used to control the system bus driver device (74LS245).
PD0 / PD7	53 / 46	I/O	Parallel Data Bits (0-7): These eight lines provide a byte-wide input or output port to the system. The eight lines are held in a high-impedance state when the port is not selected ($\overline{PRT1}$ is high).
$\overline{STB}$	55	I/O	Line Printer Strobe: This I/O line provides communication between the W86C452 and the line printer. When it is active low, it provides the line printer with a signal to latch the data currently on the parallel port.
$\overline{AFD}$	56	I/O	Line Printer Autofeed: This I/O line provides the line printer with an active low signal when continuous form paper is to be autofed to the printer.
$\overline{INIT}$	57	I/O	Line Printer Autofeed: This I/O line provides the line printer with an active low signal when continuous form paper is to be autofed to the printer.
$\overline{SLIN}$	58	I/O	Line Printer Select: This I/O line selects the printer when it is active low.
INT2	59	O	Interrupt Printer Port: This signal is an input line from the line printer that goes active high when an error signal is received. The interrupt is reset low upon a reset operation.
$\overline{ERR}$	63	I	Line Printer Error: This is an input line from the line printer. The line printer reports and error by holding this line low during the error condition. This causes INT2 to be asserted high.
SLCT	65	I	Line Printer Select: This is an input line from the line printer that goes high when the line printer has been selected.
BUSY	66	I	Line Printer Busy: This is an input line from the line printer that goes high when the line printer has a local operation in progress.
PE	67	I	Line Printer Paper Empty: This is an input line from the line printer that goes high when the printer runs out of paper, and causes INT2 to be asserted high.
$\overline{ACK}$	68	I	Line Printer Acknowledge: This input goes low to indicate a successful data transfer has taken place.

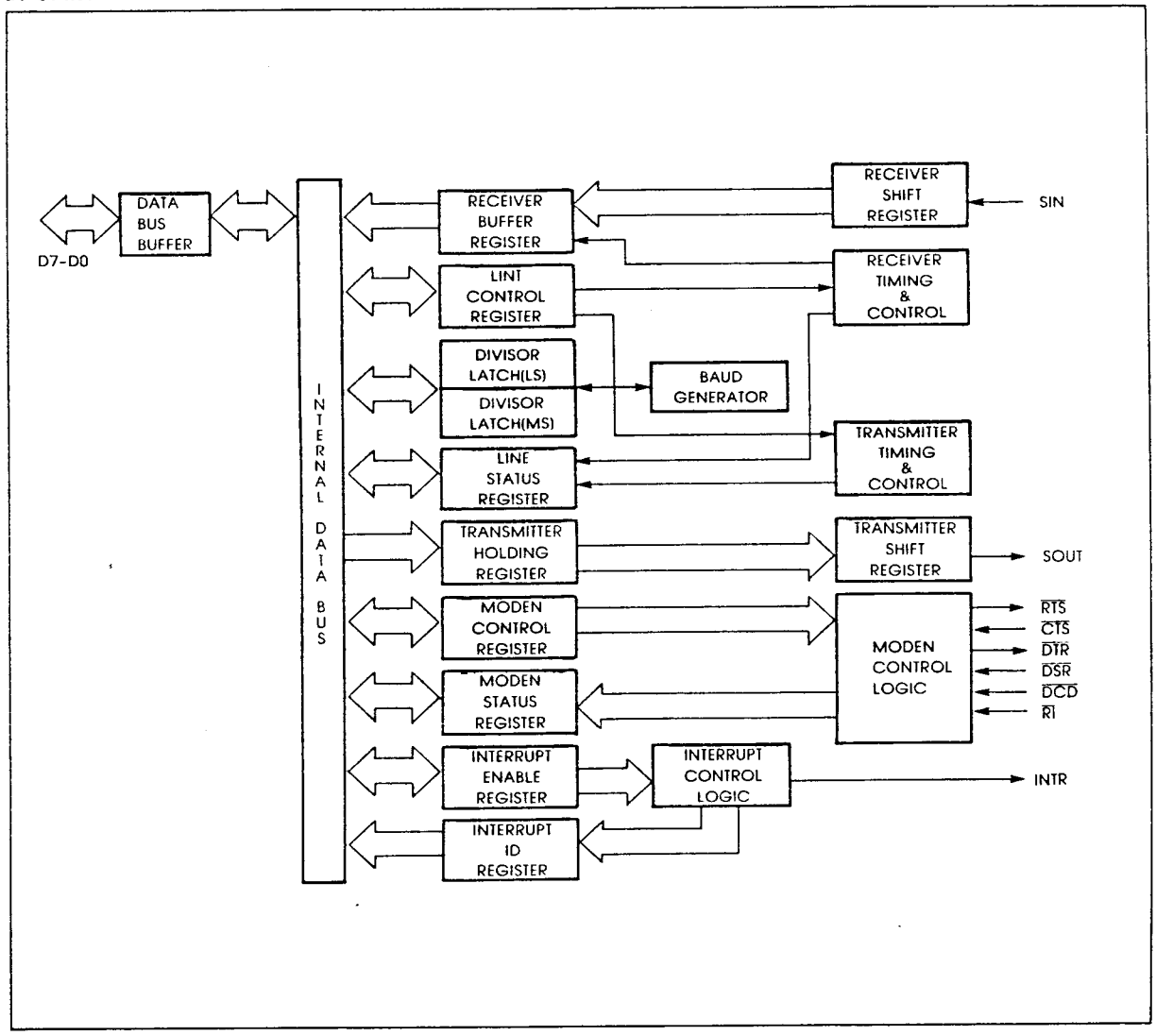
BLOCK DIAGRAM

A. UART/PARALLEL



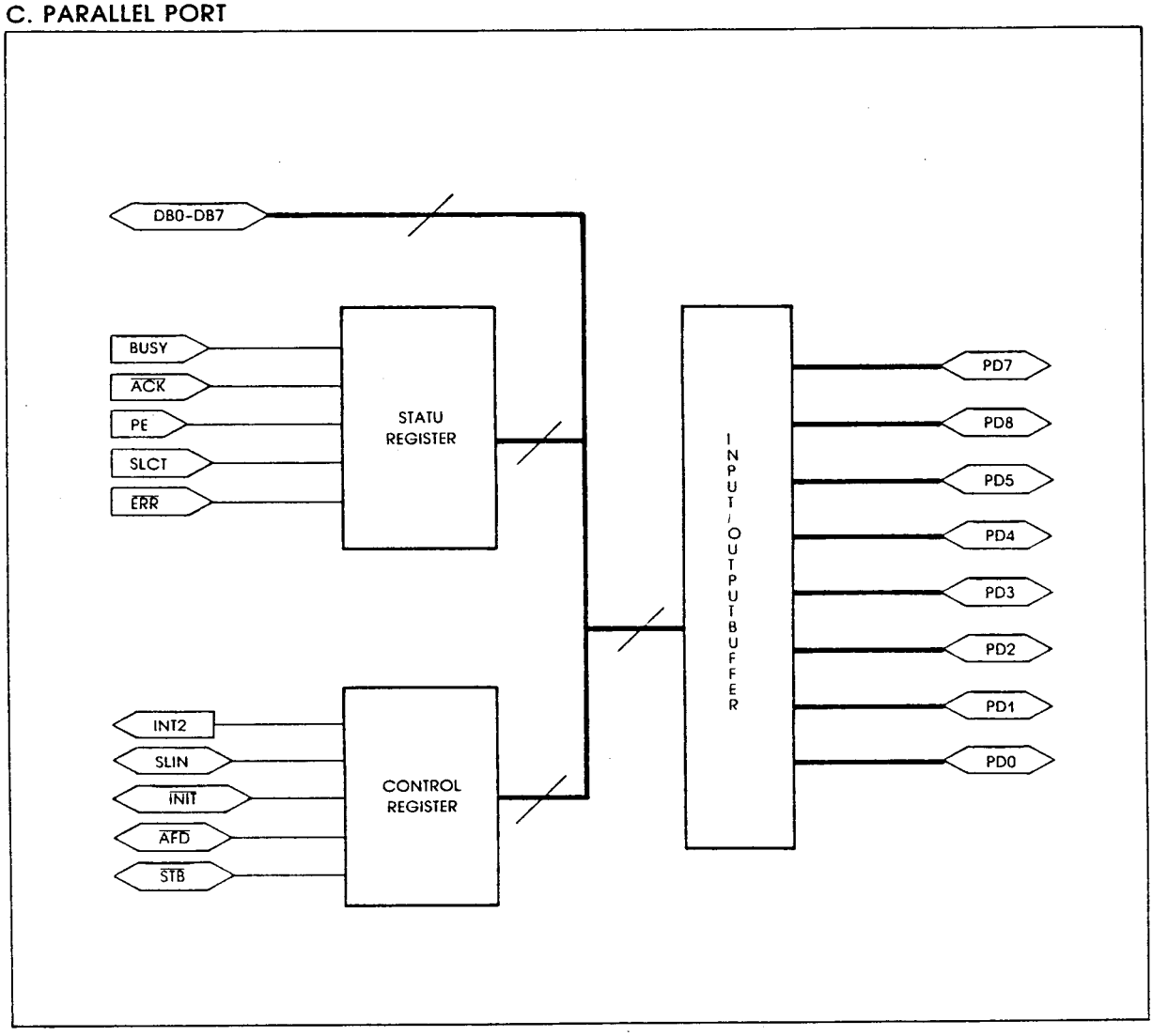
BLOCK DIAGRM (CONTINUE)

B. UART



BLOCK DIAGRAM (CONTINUE)

C. PARALLEL PORT



FUNCTIONAL DESCRIPTION

UART

The system programmer may access any of the UART registers summarized in Table 2 via the CPU. These registers control UART operations including tansmission and reception of data. Each register bit in Table 1 has it's name and reset state shown.

Table 1. **Summary of Registers**

BIT NO.	REGISTER ADDRESS										
	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	3	4	5	6	7	0 DLAB=1	1 DLAB=1
	RECEIVER BUFFER REGISTER (READ ONLY)	TRANSMITTER HOLDING REGISTER (WRITE ONLY)	INTERRUPT ENABLE REGISTER	INTERRUPT IDENT. REGISTER (READ ONLY)	LINE CONTROL REGISTER	MODEM CONTROL REGISTER	LINE STATUS REGISTER	MODEM STATUS REGISTER	SCRATCH REG-ISTER	DIVISOR LATCH (LS)	DIVISON LATCH (MS)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0 (Note 1)	Data Bit 0	Received Data Available	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta 0 Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Transmitter Holding Register Empty	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Daba Bit 2	Data Bit 2	Receiver Line Status	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bot 3	Data Bit 3	MODEM Status	0	Parity Enable (PEN)	Intea	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

a. Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange and sets the Divisor Latch Access bit via the Line Control Register (LCR). The programmer can also read the contents of the Line Control Register. The read capability simplifies system programming and eliminates the need for separate storage in system memory of the line memory of the line characteristics. Table 2 shows the contents of the LCR. Details on each bit follow:

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

BIT 1	BIT 0	CHARACTER LENGTH
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits transmitted and received in each serial character. If bit 2 is a logic 0, one Stop bit is generated or checked in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half Stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7- or 8-bit word length is selected, two Stop bits are generated. The Receiver checks the first Stop-bit only, regardless of the number of Stop bits selected.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bits 3,4 and 5 are logic 1 the Parity bit is transmitted and checked as a logic 0. If bits 3 and 5 are 1 and bit 4 is a logic 0 then the Parity bit is transmitted and checked as a logic 1. If bit 5 is a logic 0 Stick Parity is disabled.

Bit 6: This bit is the Break Control bit. It causes a break condition to be transmitted by the UART. When it is set to a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state. The break is disabled by clearing bit 6 to a logic 0. The Break Control bit acts only on SOUT and has no effect on the transmitter logic.

Note: This feature enables the CPU to alert a terminal in a computer communications system. If the following squence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0s, pad character, in response the TERE.
2. Set break after the next TERE.
3. Wait for the transmitter to be idle, (TEMT = 1), and clear break when normal transmisson has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator during a Read or Write operation.
It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the interrupt Enable Register.

b. Programmable Baud Generator

The UART contains a programmable Baud Generator that is capable of taking any clock input from DC to 3.1 MHz and dividing it by any divisor from 1 to $2^{76} - 1$. The output frequency of the Baud Generator is is 16 × the Baud [divisor # = (frequency input) (baud rate × 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure proper operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded.

Table 3 provide decimal divisors to use with crystal frequencies of 1.8432 MHz and 3.072 MHz respectively for common baud rates. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the of the desired baud rate is dependent on the crystal frequency chosen. Using a division of 0 is not recommended.

Note:
The maximum operating frequency of the Baud Generator is 3.1 MHz. However, when using divisors of 3 and below, the maximum frequency is equal to the divisor in MHz. For example, if the divisor is 1, then the maximum frequency is 1 MHz. In no case should the data rate be greater than 56K Baud.

Table 3. **Baud Rates Using 1.8432 MHz Crystal and 3.072 MHz Crystal**

DESIRED BAUD RATE	DECIMAL DIVISOR USED TO GENERATE 16 × CLOCK		PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL	
	1.8432M	3.072M	1.8432M	3.072M
50	2304	3840	—	—
75	1536	2560	—	—
110	1047	1745	0.026	0.026
134.5	857	1428	0.058	0.034
150	768	1280	—	—
300	384	640	—	—
600	192	320	—	—
1200	96	160	—	—
1800	64	107	—	0.312
2000	58	96	0.69	—
2400	48	80	—	—
3600	32	53	—	0.628
4800	24	40	—	—
7200	16	27	—	1.23
9600	12	20	—	—
19200	6	10	—	—
38400	3	5	—	—
56000	2	—	2.86	—

c. Line Status Register

This 8-bit register provides status information to the CPU concerning the date transfer. Table 2 shows the contents of the Line Status Register. Details on each bit follow:

Bit 0: This bit is the reciver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 is reset to a logic 0 by reading the data in the Receiver Buffer Register.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is set to a logic 1 upon detection of an overrun condition and reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE Bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is a logic 0 (Spacing level). The FE indicator is reset whenever the CPU reads the contens of the Line Status Register. The UART will try to resynchronize after a framing error. To do this it assumes that the framing error was due to the next start bit, so it samples this "STtart" bit twice and then takes in the "data".

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status Register. Restarting after a break is received, requires the SIN pin to be logical 1 for at least 1/s bit time.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5: This bit is the Transmitter Holding Register Empty (TERE) indicator. Bit 5 indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. Ths TERE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 whenever the CPU loads the Transmitter Holding Register.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character.

Bit 7: This bit is permanently set to logic 0.

Note: The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is not recommended as this operation is only used for factory testing.

d. Interrupt Indentification Register (IIR)

In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the Interrupt Identification Register. The four levels of interrupt conditions in order of priority are Receiver Line Status; Received Data Ready; Transmitter Holding Register Empty; and MODEM Status. When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is complete. Table 2 shows the contents of the IIR. Details on each bit follow:

Bit 0: This bit can be used in an interrupt environment to indicate whether an interrupt condition is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bit 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 4.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Table 4 **Interrupt Control Functions**

IIR				INTERRUPT SET AND RESET FUNCTIONS		
BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Receiver Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

e. Interrupt Enable Register

This register enables the four types of UART interrupts. Each interrupt can individually activate the interrupt (INTR) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register (IER). Similarly, setting bits of this register to a logic 1, enables the selected interrupt (s).

Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the INTR output signal. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. Table 2 shows the contents of the IER. Details on each bit follow.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.
Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.
Bit 2: This bit enables the receiver Line Status Interrupt when set to logic 1.
Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.
Bit 4 through 7: These four bits are always logic 0.

f. Modem Control Register

This register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register (MCR) are indicated in Table 2 and are described below. Table 2 shows the contents of the MCR. Details on each bit follow.
Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the DTR output is forced to a logic 0. When bit 0 is reset to a logic 0, the DTR output is forced to a logic 1.

Note: The DTR output of the UART may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output bit 1 affects the RTS output in a manner identical to that described above for bit 0.
Bit 2: This bit is not connected

Bit 3: This bit is set high, the INT output is enabled.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occur. the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$, and $\overline{DCD}$) are disconnected; and the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, OUT 1, and OUT 2) are internally connected to the four MODEM Control inputs. The MODEM Control output pins are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit-and-received-data paths of the UART.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.
Bit 5 through 7: These bits are permanently set to logic 0.

g. MODEM Status Register

This register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

Table 2 shows the contents of the MSR. Details on each bit follow.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the CTS input

Note: Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt os generated.

to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the RI input to the chip has changed from a low to a high state.

Bit 3: This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to INTEA 2 in the MCR.

h. Scratchpad Register

This 8-bit Read/Write Register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

B. PARALLEL PORT

The W86C452's parallel port interfaces the device to a Centronices-style printer. When ($\overline{PRT1}$) is low, the parallel is selected. Table 5 shows the registers associated with this parallel port. The read or write function of the register is controlled by the state of the read ($\overline{IOR}$) and write ($\overline{IOW}$) pin as shown. The top four registers are read-only registers, and the botton four are write-only registers. Table 6 shows the selection of PARALLEL PORT registers.

Table 5. Parallel Port Registers

REGISTER	REGISTER BITS							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read Port	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read Status	$\overline{BUSY}$	$\overline{ACK}$	PE	SLCT	$\overline{ERROR}$	1	1	1
Read Control	1	1	1	IRQ ENB	SLIN	$\overline{INIT}$	$\overline{AUTOFD}$	$\overline{STROBE}$
Write Port	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write Control	1	1	1	IRQ ENB	SLIN	$\overline{INIT}$	$\overline{AUTOFD}$	$\overline{STROBE}$

CONTROL PINS					REGISTER SELECTED
$\overline{IOR}$	$\overline{IOW}$	$\overline{PRT1}$	A1	A0	
0	1	0	0	0	Read Port
0	1	0	0	1	Read Status
0	1	0	1	0	Read Control
0	1	0	1	1	Invalid
1	0	0	1	0	Write Control
1	0	0	0	0	Write Port
1	0	0	0	1	Invalid
1	0	0	1	1	Invalid

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYM.	RATING	UNIT
Supply Voltage	$V_{DD} - V_{SS}$	−0.2 ~ 7	V
Input Voltage	V_{IN}	−0.2 ~ V_{DD}+0.2	V
Operating Temp.	T_{OP}	0 ~ 70	°C
Storage Temp.	T_{ST}	−20 ~ 150	°C
Power Dissipation	P	700	mW

D.C. CHARACTERISTICS

(V_{DD}=5.0V ±5%, V_{SS}=0V, T_A=0°C to 70°C)

PARAMETER	SYM.	CONDITIONS	MIN.	MAX.	UNIT
Input Voltage	V_{ILX}	Clock input	−0.5	0.8	V
	V_{IHX}		2.0	V_{CC}	V
Input Voltage	V_{IL}	Other inputs	−0.5	0.8	V
	V_{IH}		2.0	V_{CC}	V

PARAMETER	SYM.	CONDITIONS	MIN.	MAX.	UNIT
Output Voltage	V_{OL}	I_{OL}=4.0mA on all DB0-DB7, 12mA on PD0-PD7, 2mA on all other outputs	—	0.4	V
	V_{OH}	I_{OH}=−0.4mA on all DB0-DB7, −0.2mA on PD0-PD7, −0.2mA on all other outputs	2.4	—	V
Average Power Supply Current (V_{CC})	I_{CCA}	V_{DD}=5.25V, T_A=25°C No load on output SIN, DSR, DCD, CTS, RI=2.0V All other inputs = 0.8V Baud Rate Generator is 4 MHz Baud Rate is 56k	—	50	mA
Input Leakage	I_{IL}	V_{DD}=5.25V, V_{SS}=0V All other pins floating V_{IN}=0V, 5.25V	—	±10	μA
Clock Leakage	I_{CL}		—	±10	μA
Tri-state Lekage	I_{OZ}	V_{DD}=5.25V, V_{SS}=0V V_{OUT}=0V, 5.25V 1) Chip deselected 2) WRITE mode, chip selected	—	±20	μA
Reset Schmitt V_{IL}	V_{IL} (res)		—	0.8	V
Reset Schmitt V_{IH}	V_{IH} (res)		2.0	—	V

A.C. CHARACTERISTICS

(V_{DD}=5.0V ±5%, V_{SS}=0V, T_A=0°C TO 70°C)

PARAMETER	SYM.	CONDITIONS	MIN.	MAX.	UNIT
$\overline{IOR}$ Delay From Address	T_{AR}	(Note 2)	60	—	nS
$\overline{IOW}$ Delay from Address	T_{AW}	(Note 2)	60	—	nS
$\overline{IOR}$ Delay from Chip Select	T_{CSR}	(Note 2)	50	—	nS
$\overline{IOW}$ Delay from Select	T_{CSW}	(Note 2)	50	—	nS
Data Hold Time	T_{DH}		40	—	nS
Data Setup Time	T_{DS}		40	—	nS
$\overline{IOR}$ to Floating Data Delay	T_{HZ}	100pF loading (Note 4)	0	100	nS
Address Hold Time from $\overline{IOR}$	T_{RA}	(Note 2)	20	—	nS

PARAMETER	SYM.	CONDITIONS	MIN.	MAX.	UNIT
$\overline{IOR}$ Strobe Width	T_{RD}		125	—	nS
Delay from $\overline{IOR}$ to Data	T_{RVD}	@100pF loading	—	125	nS
Address Hold Time form $\overline{IOW}$	T_{WA}	(Note 2)	20	—	nS
Chip Select Hold Time from $\overline{IOW}$	T_{WCS}	(Note 2)	20	—	nS
Chip Select Hold Time from $\overline{IOR}$	T_{RCS}	(Note 2)	20	—	nS
$\overline{IOW}$ Strobe Width	T_{WR}		100	—	nS
Duration of Clock High Pulse	T_{XH}	External Clock	140	—	nS
Duration of Clock Low Pulse	T_{XL}	External Clock	140	—	nS
Reset Pulse WIDTH	T_{RW}		5		nS
Read Cycle	RC		360	—	nS
Write Cycle	WC		360	—	nS

Note 1: All timing specifications apply to pin on both serial channels.

2: The internal address strobe is always active.

3: RCLK = T_{XL} and T_{XL}.

4: Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.

CHARACTERISTICS (Continue)

(V_{DD} = 5.0V ±5%, V_{SS} = 0V, T_A = 0°C to 70°C)

PARAMETER	SYM.	CONDITIONS	MIN.	MAX.	UNIT
Receiver					
Delay from $\overline{IOR}$ (RD RBR or RD LSR) to Reset Interrupt	T_{RINT}	100pF loading	—	1	μS
Delay from Stop to Set Interrupt	T_{SINT}		1	1	RCLK Cycle
Transmitter					
Delay from $\overline{IOW}$ (WR THR) to Reset Interrupt	T_{HR}	100pF Load	—	175	nS
Delay from $\overline{IOR}$ (RD IIR) to Reset Interrupt (THRE)	T_{IR}	100pF Load	—	250	nS
Delay from Initial INTR Reset to Transmit Start	T_{IRS}		1	8	B.C.
Delay from Initial Write to Interrupt	T_{SI}		9	16	B.C.
Delay from Stop to Interrupt (THRE)	T_{STI}		8	8	B.C.

PARAMETER	SYM.	CONDITIONS	MIN.	MAX.	UNIT
Modem Control					
Delay from $\overline{IOW}$ (WR MCR) to Output	T_{MDO}	100pF Load	—	200	nS
Delay to Reset Interrupt from $\overline{IOR}$ (RD MSR)	T_{RIM}	100pF Load	—	250	nS
Delay to Reset Interrupt from MODEM input	T_{SIM}	100pF Load	—	200	nS
Parallel Port					
Data Time	T_{DT}		0.5	—	μS
Strobe Time	T_{SB}		1	500	μS
Acknowledge Delay (Busy Start to Acknowledge)	T_{AD}	(Note 5)			μS
Acknowledge Delay (Busy End to Acknowledge)	T_{AKD}	(Note 5)			μS
Acknowledge Duration time	T_{AK}	(Note 5)			μS
Busy Duration Time	T_{BSY}	(Note 5)			μS
Busy Delay Time	T_{BSD}	(Note 5)			μS

Note 1: All timing specifications apply to pin on both serial channels.

2: The internal address strobe is always active.

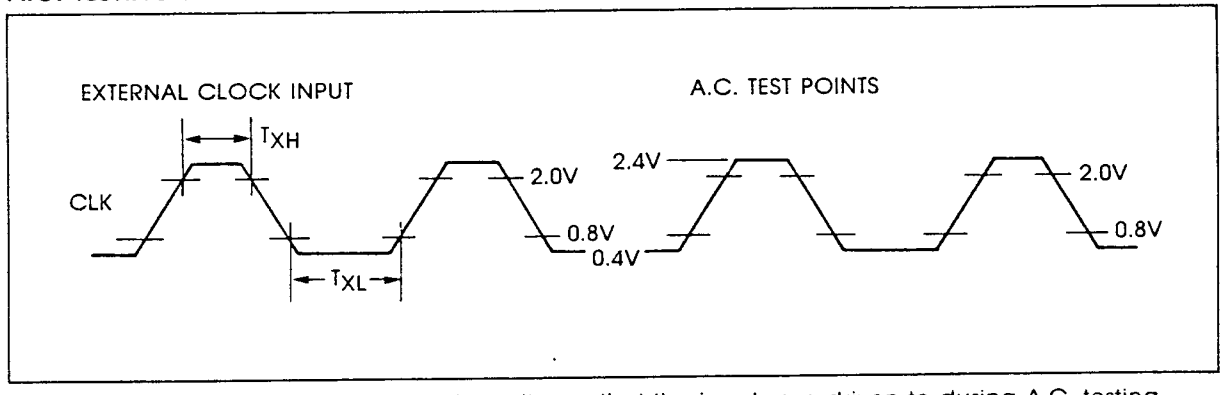
3: RCLK = T_{XL} and T_{XL}.

4: Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.

5: Defined by Printer.

TIMING WAVEFORM (All timings are referenced to valid 0 and valid 1)

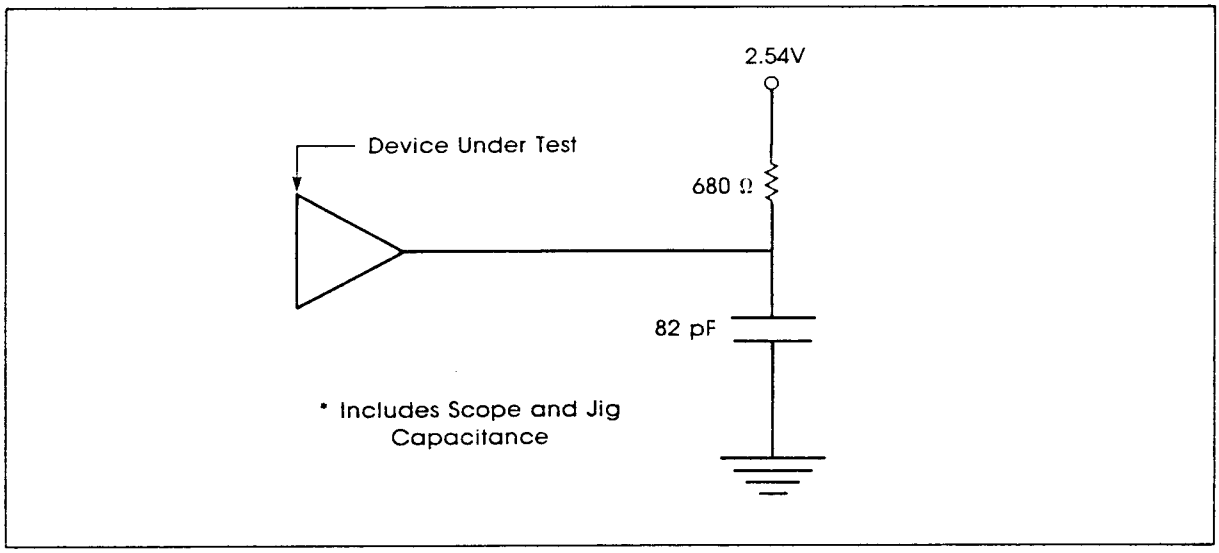
A.C. TESTING INPUT/OUTPUT WAVEFORMS



Note 1: The 2.4V and 0.4V levels are the voltages that the inputs are driven to during A.C. testing.

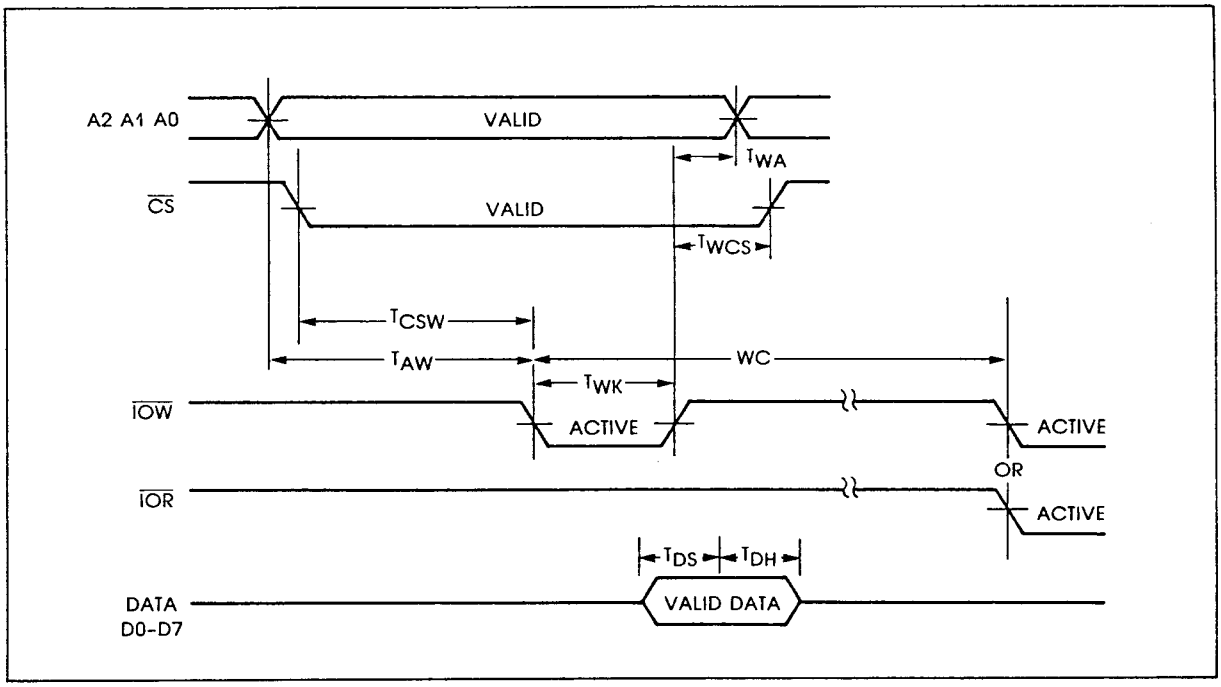
2: The 2.0V and 0.8V levels are the voltages at which the timing tests are made.

A.C. TEST LOAD

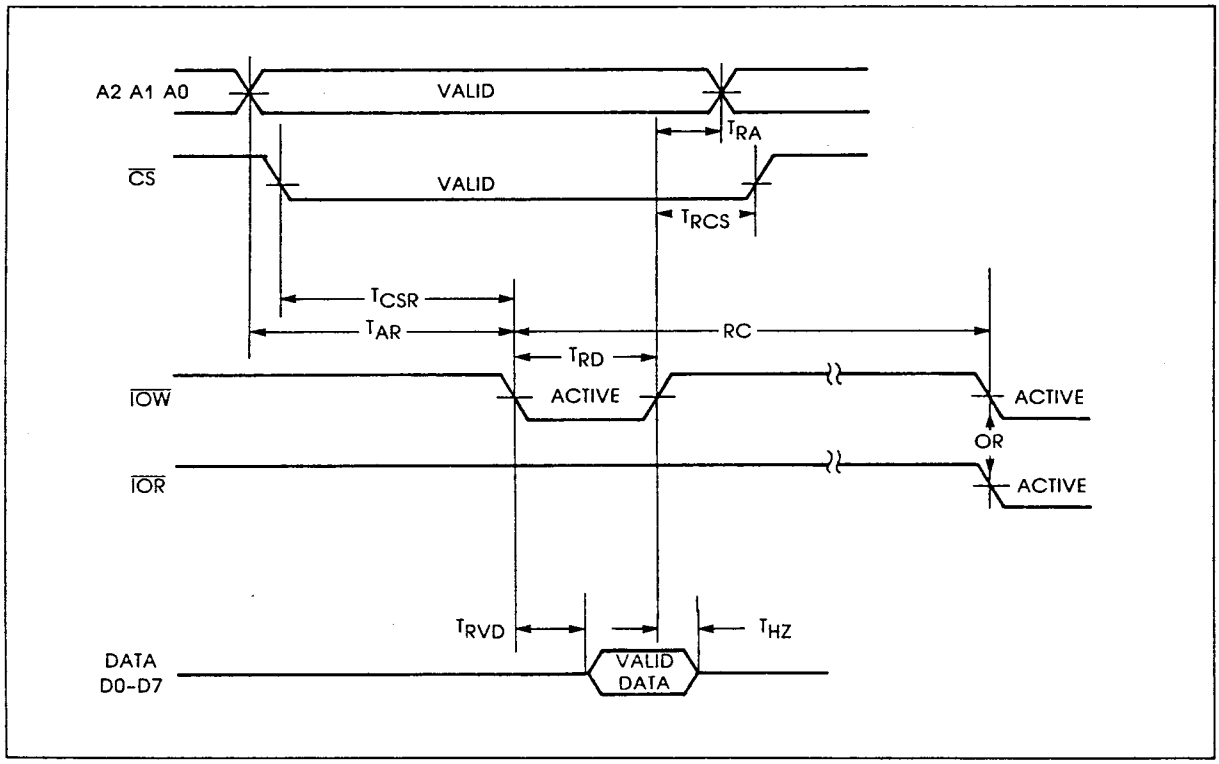


TIMING WAVEFORM (Continue)

WRITE CYCLE TIMING

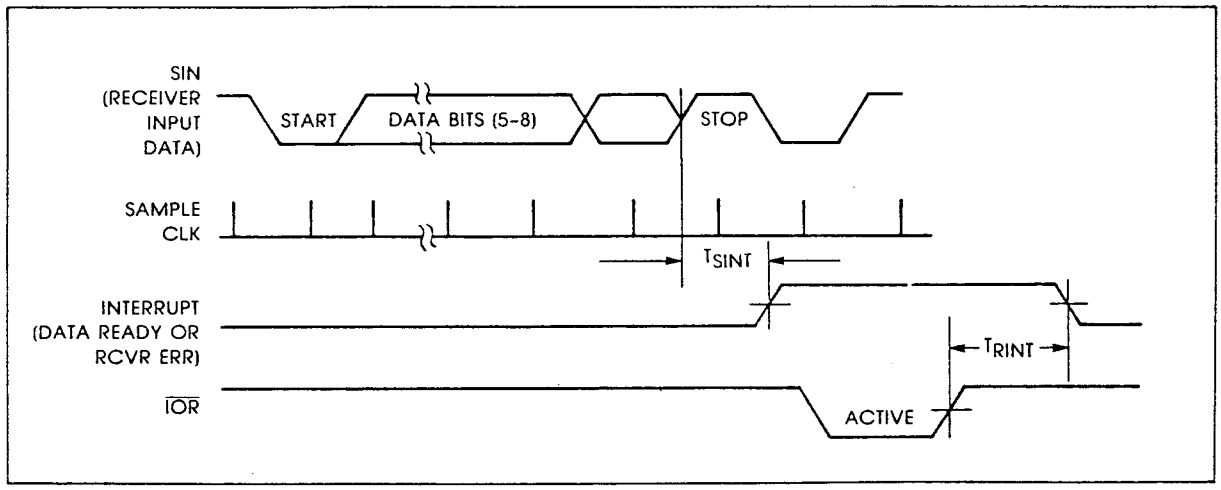


READ CYCLE TIMING

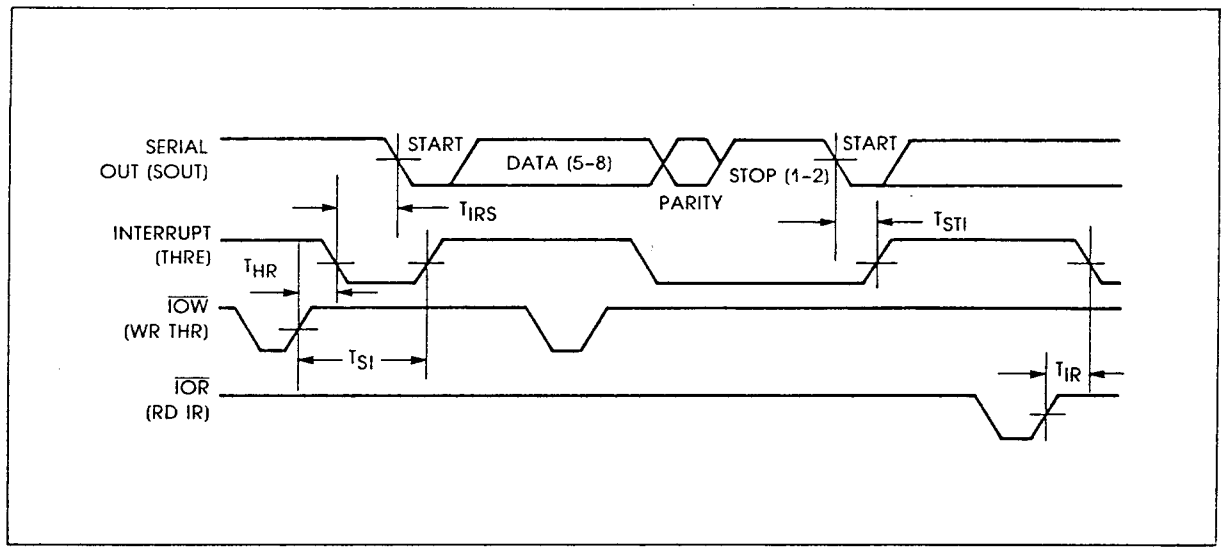


TIMING WAVEFORM (Continue)

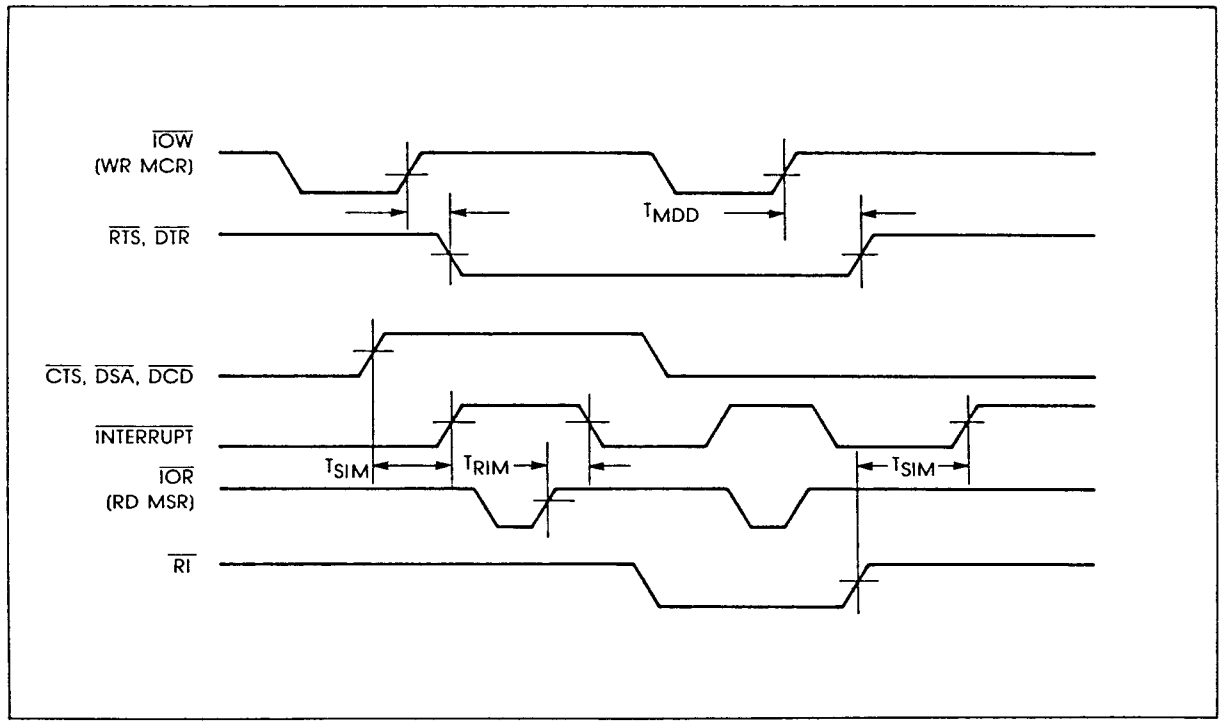
RECEIVER TIMING



TRANSMITTER TIMING

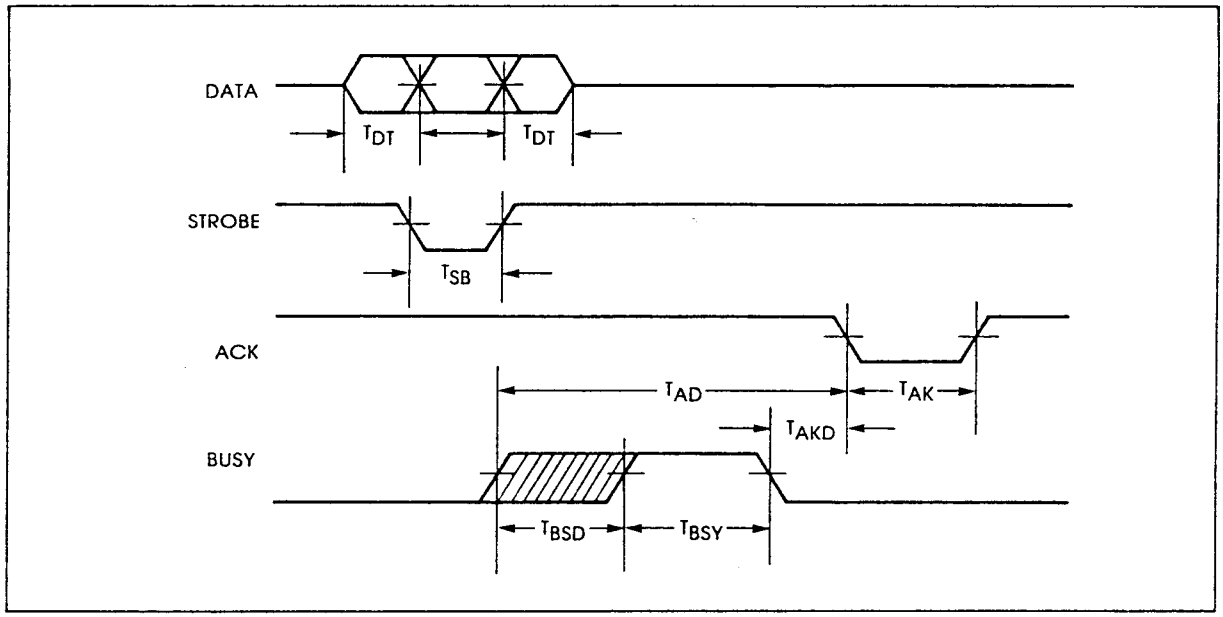


MODEM TIMING

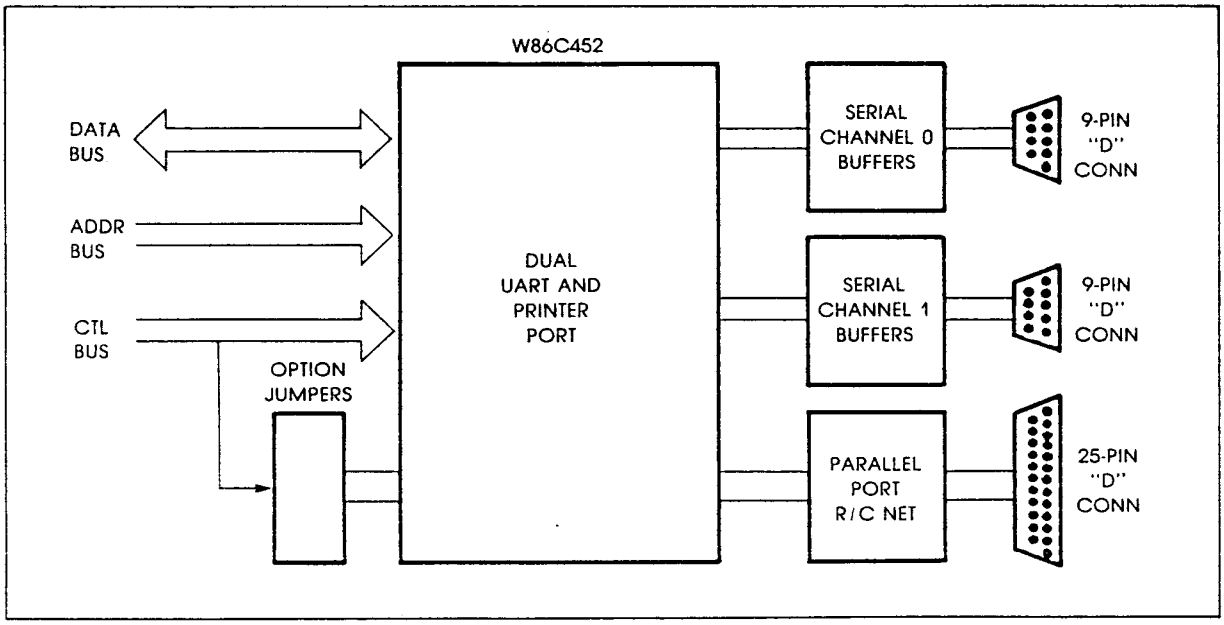


TIMING WAVEFORMS (Continue)

PARALLEL PORT TIMING



TYPICAL APPLICATION



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