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Winbond Electronics Corp.

512K × 4 BANKS × 32 BITS DDR SDRAM

GENERAL DESCRIPTION

The W946432AD is a high-speed CMOS Double Data Rate synchronous dynamic random access memory organized as 512K words x 4 banks x 32 bits.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

The W946432AD operates from a differential clock (CLK and $\overline{CLK}$ the crossing of CLK going HIGH and $\overline{CLK}$ going LOW will be referred to as the postive edge of CLK). Commands (address and control signals) are registered at every positive edge of CLK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CLK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable READ or WRITE burst lengths of 2, 4 or 8 locations. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

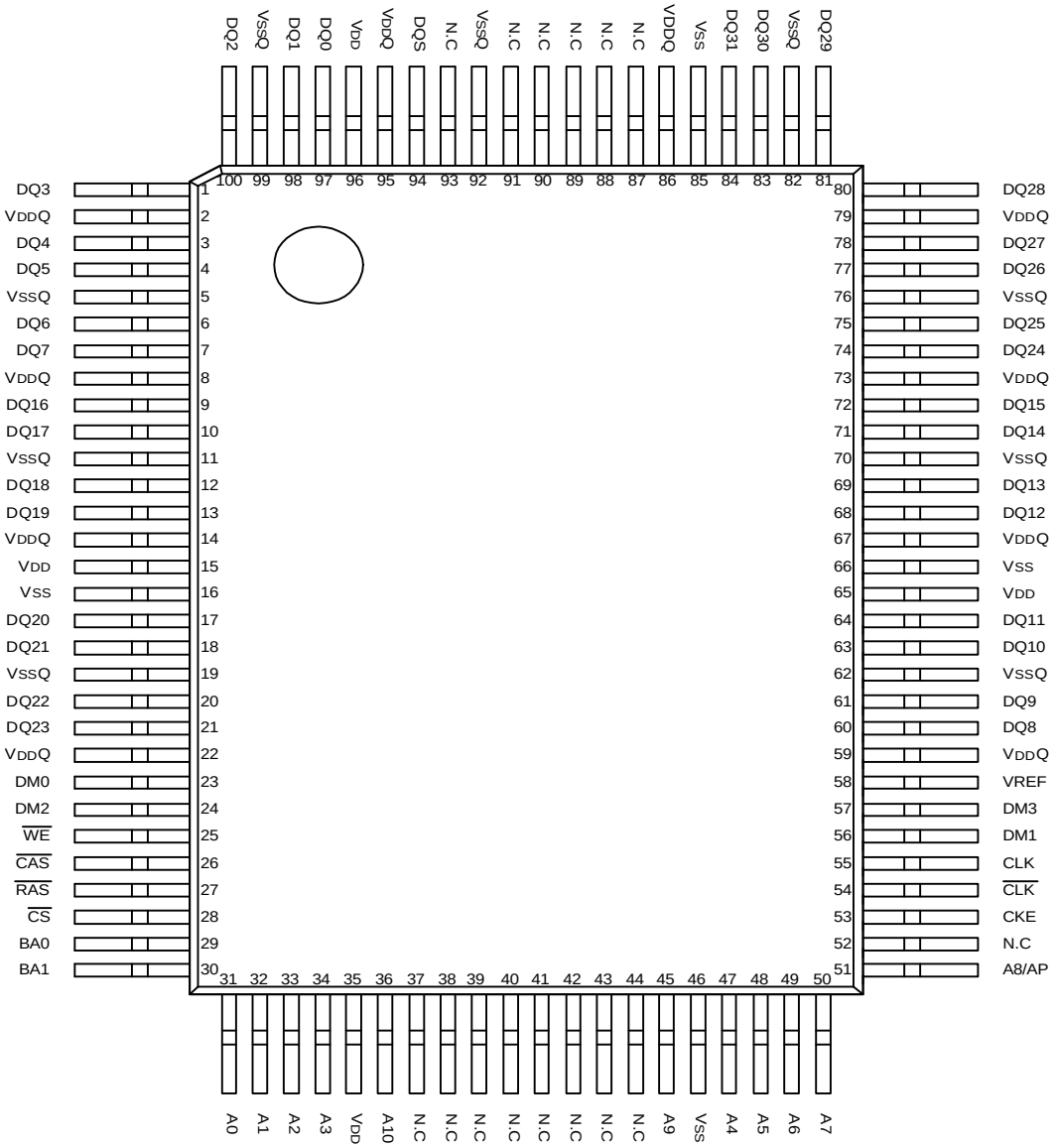
As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

FEATURES

- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional, data strobe (DQS) is transmitted/ received with data, to be used in capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CLK and $\overline{CLK}$)
- DLL aligns DQ and DQS transitions with CLK transitions
- Programmable DLL on or DLL off mode
- Commands entered on each positive CLK edge; data and data mask referenced to both edges of DQS
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- Burst lengths: 2, 4, or 8
- CAS Latency: 3
- AUTO PRECHARGE option for each burst access
- Auto Refresh and Self Refresh Modes
- 15.6us Maximum Average Periodic Refresh Interval
- 2.5V (SSTL_2 compatible) I/O
- $V_{DD}Q$ = 2.5V ± 0.2V
- V_{DD} = 2.5V ± 0.2V

512K × 4 BANKS × 32 BITS DDR SDRAM

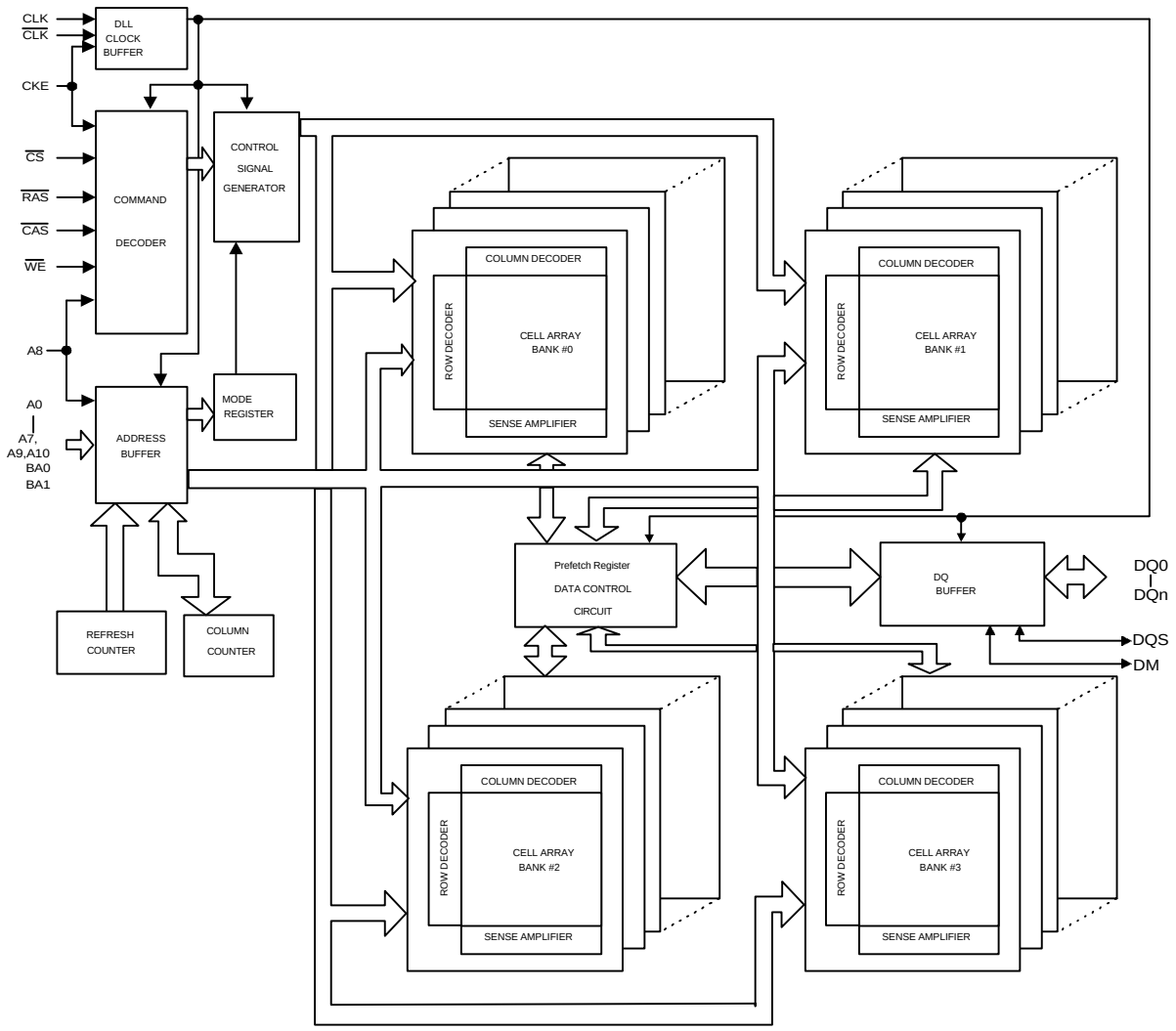
PIN CONFIGURATION



PIN DESCRIPTION

PIN NAME	FUNCTION	DESCRIPTION
CLK, $\overline{CLK}$	Differential clock input	All address and control input signals are sampled on the crossing of the positive edge of CLK and negative edge of $\overline{CLK}$. Output (read) data is referenced to the crossings of CLK and $\overline{CLK}$ (both directions of crossing).
CKE	Clock Enable	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit, and for output disable. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CLK, $\overline{CLK}$ and CKE are disabled during POWER-DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH.
$\overline{CS}$	Chip Select	All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Command Inputs	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM	Input Data Mask	DM is an input mask signal for writes data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
BA0, BA1	Bank Address	BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A0-A10	Address Input	Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A8 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A8 LOW) or all banks (A8 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS).
DQ	Data Input/Output	Data bus
DQS	Data Strobe	Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data.
$V_{DD}Q$	DQ Power	2.5V ± 0.2V.
$V_{SS}Q$	DQ Ground	Ground.
V_{DD}	Supply Power	2.5V ± 0.2V
V_{SS}		Ground.
NC	No Connection	No connection
V_{REF}		SSTL_2 reference voltage.

BLOCK DIAGRAM



NOTE:
The cell array configuration is 2048 * 256 * 32

ABSOLUTE MAXIMUM RATINGS*

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-0.3~ V_{DD} +0.3	V	1
V_{OUT}	Output Voltage	-0.3~ $V_{DD}Q$+0.3	V	1
V_{DD}	Power Supply Voltage	-0.3~4.6	V	1
$V_{DD}Q$	I/O Power Supply Voltage	-0.3~3.6	V	1
T_{OPR}	Operating Temperature	0~70	°C	1
T_{STG}	Storage Temperature	-55~150	°C	1
T_{SOLDER}	Soldering Temperature(10s)	260	°C	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

*Conditions outside the limits listed under “Absolute Maxi-mum Ratings” may cause permanent damage to the device.

CAPACITANCE ($V_{DD}Q$ = 2.5V, V_{DD} = 2.5 ± 0.2, f 100 MHz, T_A = 25 °C)

PARMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: CK, $\overline{CK}$	CI1	2.5	3.5	pF	
Input Capacitance: All other input-only pins	CI2	2.5	3.5	pF	
Input/Output Capacitance: DQ, DQS, DM	CI0	4.0	5.5	pF	

Note: These parameters are periodically sampled and not 100% tested.

ELECTRICAL CHARACTERISTICS AND DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; $V_{DD}Q$ = +2.5V ±0.2V, V_{DD} = +2.5V ±0.2V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage (for devices with V_{DD} of 2.5V)	V_{DD}	2.3	2.7	V	
I/O Supply Voltage	$V_{DD}Q$	2.3	2.7	V	
I/O Reference Voltage	V_{REF}	1.15	1.35	V	3
I/O Termination Voltage (system)	V_{TT}	V_{REF} -0.04	V_{REF} + 0.04	V	4
Input High (Logic 1) Voltage	$V_{IH(DC)}$	V_{REF} +0.18	V_{DD} + 0.3	V	
Input Low (Logic 0) Voltage	$V_{IL(DC)}$	-0.3	V_{REF} -0.18	V	
Input Voltage Level, CK and $\overline{CK}$ inputs	$V_{IN(DC)}$	-0.3	$V_{DD}Q$ + 0.3	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	$V_{ID(DC)}$	0.36	$V_{DD}Q$ + 0.6	V	5
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	I_I	-5	5	uA	
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ V_{OUT} ≤ $V_{DD}Q$)	I_{OZ}	-5	5	uA	
OUTPUT LEVELS Output High Current (V_{OUT} = 1.95V) Output Low Current (V_{OUT} = 0.35V)	 I_{OH} I_{OL}	 -15.2 15.2		 mA mA	

AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; $V_{DD}Q$ = +2.5V ± 0.2V, V_{DD} = +2.5V ± 0.2V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage, DQ, DQS and DM signals	V_{IH}(AC)	V_{REF} + 0.35		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	V_{IL}(AC)		V_{REF} - 0.35	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	V_{ID}(AC)	0.7	$V_{DD}Q$ + 0.6	V	5
Input Crossing Point Voltage, CK and $\overline{CK}$ inputs	V_{IX}(AC)	0.5*$V_{DD}Q$-0.2	0.5*$V_{DD}Q$+0.2	V	7

I_{DD} SPECIFICATIONS AND CONDITIONS

(0°C ≤ T_A ≤ 70°C; $V_{DD}Q$ = +2.5V ± 0.2V, V_{DD} = +2.5V ± 0.2V)

		MAX		
	SYMBOL		UNITS	NOTES
OPERATING CURRENT: One Bank; Active-Precharge; tRC = tRC MIN; tCK = tCK MIN; DQ, DM and DQS inputs changing twice per clock cyle; address and control inputs changing once per clock cycle	$I_{DD}0$	TBD	mA	
OPERATING CURRENT: One Bank; Active-Read-Precharge; Burst = 2; tRC = tRC MIN; CL = 3 ; tCK = tCK MIN; I_{OUT}= 0 mA; Address and control inputs changing once per clock cycle	$I_{DD}1$	TBD	mA	
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; power-down mode; CKE ≤ V_{IL} (MAX); tCK = tCK MIN	$I_{DD}2P$	TBD	mA	
IDLE STANDBY CURRENT: $\overline{CS}$ ≥ V_{IH} (MIN); All banks idle; CKE ≥ V_{IH} (MIN); tCK = tCK MIN; Address and other control inputs changing once per clock cycle	$I_{DD}2N$	TBD	mA	
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; power-down mode; CKE ≤ V_{IL} (MAX); tCK = tCK MIN	$I_{DD}3P$	TBD	mA	
ACTIVE STANDBY CURRENT: $\overline{CS}$ ≥ V_{IH} (MIN); CKE ≥ V_{IH} (MIN); One bank; Active-Precharge; tRC = tRAS MAX; tCK = tCK MIN; DQ, DM and DQS inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	$I_{DD}3N$	TBD	mA	
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; CL = 3 ; tCK = tCK MIN; I_{OUT} = 0 mA	$I_{DD}4R$	TBD	mA	
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; CL = 3 ; tCK = tCK MIN; DQ, DM and DQS inputs changing twice per clock cycle	$I_{DD}4W$	TBD	mA	
AUTO REFRESH CURRENT: tRC = tRFC (MIN)	$I_{DD}5$	TBD	mA	
SELF REFRESH CURRENT: CKE ≤ 0.2V	$I_{DD}6$	TBD	mA	

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512K × 4 BANKS × 32 BITS DDR SDRAM

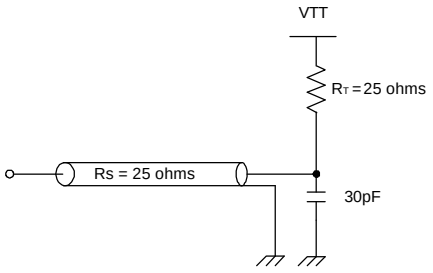
AC CHARACTERISTICS

(0°C ≤ TA ≤ 70°C; VDDQ = +2.5V ± 0.2V, VDD = +2.5V ± 0.2V)

PARAMETER		-4		-5		-6		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
DQ output access time from CLK/ $\overline{CLK}$	tAC	-0.1	0.1	-0.1	0.1	-0.1	0.1	tCK	
DQS output access time from CLK/ $\overline{CLK}$	tDQSCK	-0.1	0.1	-0.1	0.1	-0.1	0.1	tCK	
CLK high-level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CLK low-level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
Clock cycle time	tCLK	4	8	5	8	6	8	ns	8
DQ and DM input hold time	tDH	0.5		0.5		0.5		ns	
DQ and DM input setup time	tDS	0.5		0.5		0.5		ns	
DQ and DM input pulse width (for each input)	tDIPW	1		1.6		1.6		ns	
Data-out high-impedance time from CLK/ $\overline{CLK}$	tHZ	-0.1	0.1					tCK	
Data-out low-impedance time from CLK/ $\overline{CLK}$	tLZ	-0.1	0.1					tCK	
DQS-DQ Skew (for DQS and associated DQ signals)	tDQSQ	-0.5	0.5	-0.5	0.5	-0.5	0.5	ns	
DQS-DQ Skew (for DQS and all DQ signals)	tDQSQA	-0.5	0.5					ns	
DQ/DQS output valid time	tDV	0.35		0.35		0.35		tCK	
Write command to first DQS latching transition	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
DQS input high pulse width	tDQSH	0.35		0.4	0.6	0.4	0.6	tCK	
DQS input low pulse width	tDQSL	0.35		0.4	0.6	0.4	0.6	tCK	
DQS falling edge to CLK setup time	tDSS	0.2						tCK	
DQS falling edge hold time from CLK	tDSH	0.2						tCK	
MODE REGISTER SET command cycle time	tMRD	2						tCK	
Write postamble	tWPST	0.4	0.6					tCK	
Write preamble	tWPRE	0.25						tCK	
Address and Control input hold time	TIH	1						ns	
Address and Control input setup time	TIS	1						ns	
Read preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6					tCK	
ACTIVE to PRECHARGE command	tRAS	35		35	120K	42	120K	ns	
ACTIVE to ACTIVE/Auto Refresh command period	tRC	47		55		60		ns	
Auto Refresh to Active/Auto Refresh command period	tRFC	47		66		72		ns	
ACTIVE to READ or WRITE delay	tRCD	3		15		18		tCK	
PRECHARGE command period	tRP	3		15		18		tCK	
ACTIVE bank A to ACTIVE bank B command	tRRD	2		11		12		tCK	
Write recovery time	tWR	2		10		12		tCK	
Auto Precharge write recovery + precharge time	tDAL	5		25		30		tCK	
Internal Write to Read Command Delay	tWTR	2						tCK	9
Exit SELF REFRESH to non-READ command	tXSNR	47						ns	
Exit SELF REFRESH to READ command	tXSRD	200		200		200		tCK	
Average Periodic Refresh Interval	tREFI		15.6		15.6		15.6	us	

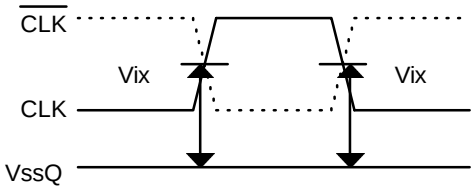
NOTES

1. All voltages referenced to V_{SS}.
2. Outputs measured with equivalent load:



A.C TEST LOAD

3. V_{REF} is expected to be equal to 0.5*V_{DD}Q of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed +/-2% of the DC value.
4. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
5. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
6. I_{DD} specifications are tested after the device is properly initialized.
7. VIX is the differential clock cross point voltage where input timing measurement is referenced.



8. Beyond 8ns tCK, chip maybe in "DLL off" mode
9. WRITE interrupted by READ is not allowed.

Note:

FUNCTIONAL DESCRIPTION

The W946432AD is a high speed CMOS, dynamic random access memory containing 67,108,864 bits. The W946432AD is internally configured as a quad bank DRAM.

The W946432AD uses a double data rate architecture to achieve high speed operation. The double data rate architecture is essentially a 32 prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the W946432AD consists of a single 32bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding 32bit wide, one half clock cycle data transfers at the I/O pins.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A10 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the DDR SDRAM must be initialized. The following sections provide etailed information covering device initialization, register definition, command descriptions and device operation.

INITIALIZATION

W986432AD must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must first be applied to V_{DD}, then to $V_{DD}Q$, and finally to V_{REF} (and to the system V_{TT}). V_{TT} must be applied after $V_{DD}Q$ to avoid device latch up, which may cause permanent damage to the device. V_{REF} can be applied any time after $V_{DD}Q$, but is expected to be nominally coincident with V_{TT}. Except for CKE, inputs are not recognized as valid until after V_{REF} is applied. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after V_{DD} is applied. Maintaining an LVCMOS LOW level on CKE during power up is required to guarantee that the DQ and DQS outputs will be in the High-Z state, where they will remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200µs delay prior to applying an executable command.

Once the 200µs delay has been satisfied, a DESELECT or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a PRECHARGE ALL command should be applied. Next a MODE REGISTER SET command should be issued for the Extended Mode Register, to enable the DLL, then a MODE REGISTER SET command should be issued for the Mode Register, to reset the DLL, and to program the operating parameters. 200 clock cycles are required between the DLL reset and any read command. A PRECHARGE ALL command should be applied, placing the device in the “all banks idle” state.

Once in the idle state, two AUTO REFRESH cycles must be performed. Additionally, a MODE REGISTER SET command for the Mode Register, with the reset DLL bit deactivated (i.e. to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

REGISTER DEFINITION

MODE REGISTER

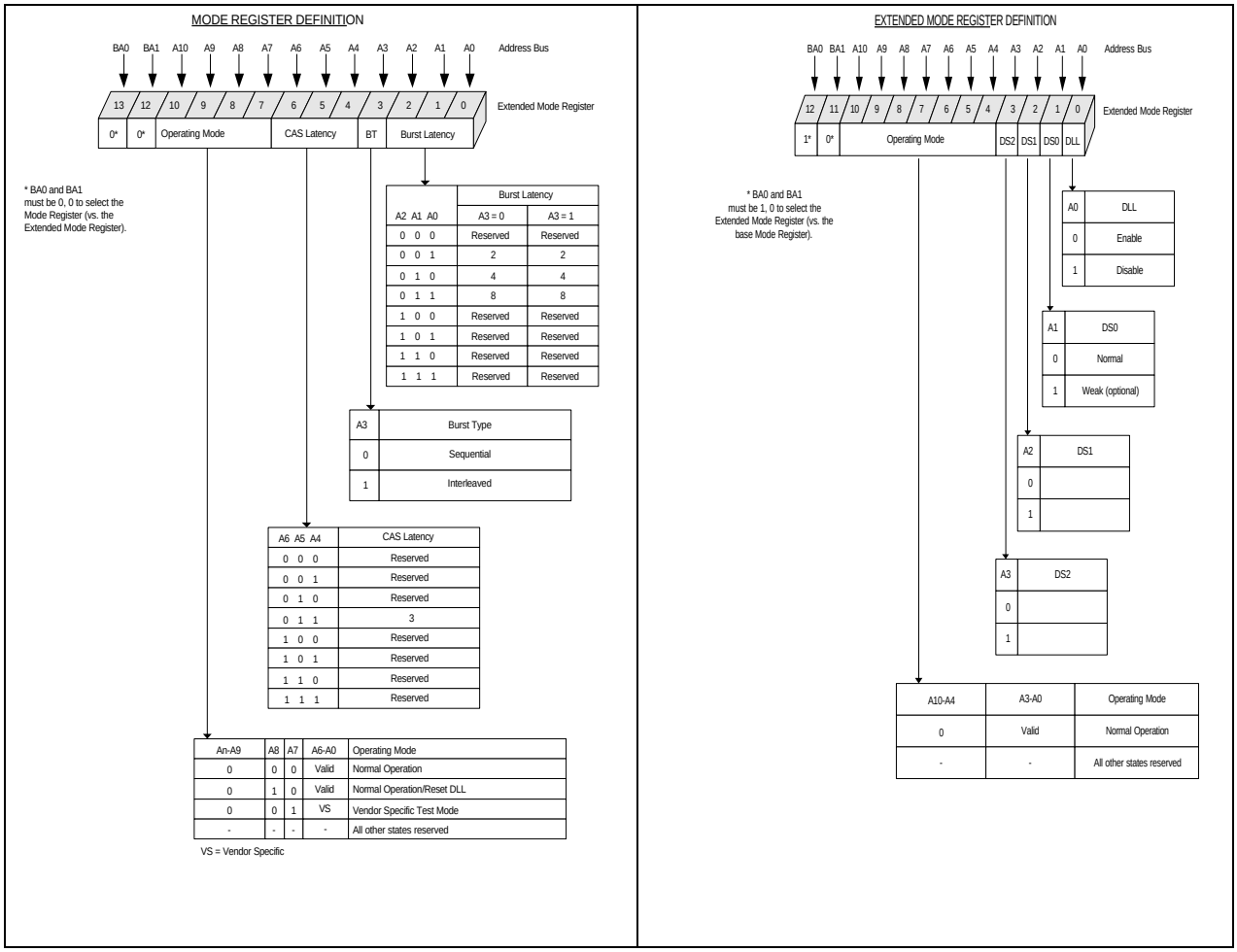
The Mode Register is programmed by the MODE REGISTER SET command (MRS/EMRS) when all banks are idle and no bursts are in progress.

The Mode Register is used to define the operation specific mode of of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a $\overline{\text{CAS}}$ latency, and an operating mode, as shown in Figure1:

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functionsinclude DLL enable/disable,output drive strength selection. These functions as shown inFigure1:.

Mode Register must be loaded, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Figure1:Mode Register Definition



Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Table 1: The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.
When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place with in this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-A7 when the burst length is set to two, by A2-A7 when the burst length is set to four and by A3-A7 when the burst length is set to eight. The remaining address bit is used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected by bit A3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 1:.

Table 1:BURST DEFINITION

Burst Length	Starting Column Address:			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			**A0**		
			0	0 - 1	0 - 1
			1	1 – 0	1 – 0
4		**A1**	**A0**		
		0	0	0–1–2-3	0-1-2-3
		0	1	1–2–3–0	1-0-3-2
		1	0	2–3–0–1	2-3-0-1
		1	1	3–0–1–2	3-2-1-0
8	**A2**	**A1**	**A0**		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

NOTE:

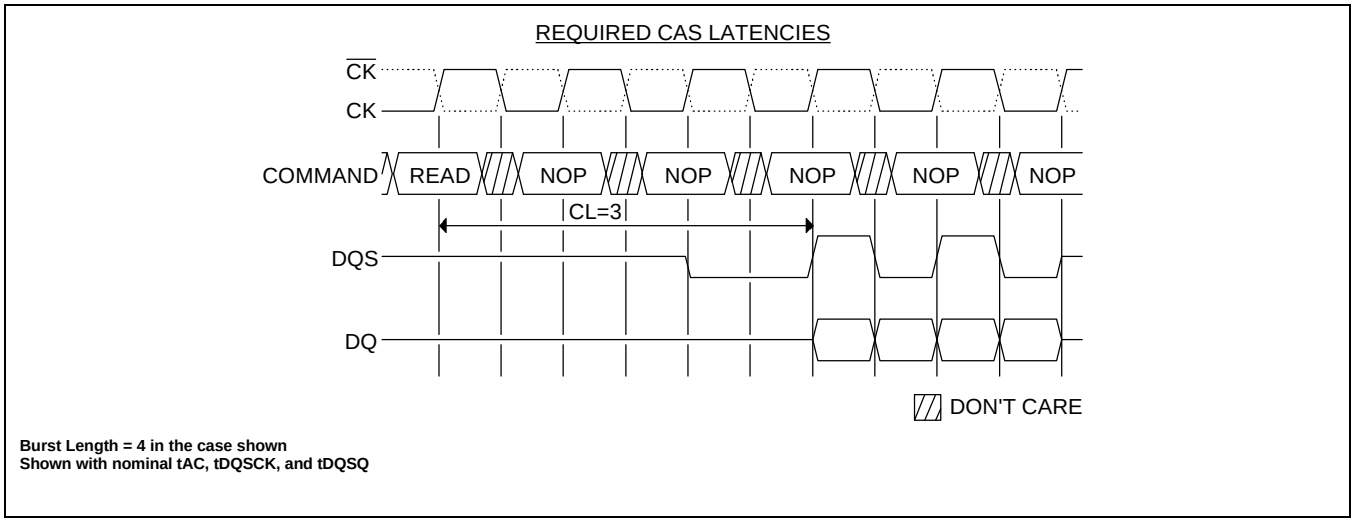
1. For a burst length of two, A1-A7 selects the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2-A7 selects the four-data-element block; A0-A1 selects the first access within the block.
3. For a burst length of eight, A3-A7 selects the eight-data- element block; A0-A2 selects the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency is set to 3 clocks.

If a READ command is registered at clock edge n, and the latency is 3 clocks, the data will be available nominally coincident with clock edge n + 3.

Figure2:REQUIRED CAS LATENCIES



Operating Mode

The normal operating mode is selected by issuing a Mode Register Set command with bits A7-A10 each set to zero, and bits A0-A6 set to the desired values. A DLL reset is inititated by issuing a Mode Register Set command with bits A7 and A9-A10 each set to zero, bit A8 set to one, and bits A0-A6 set to the desired values. A Mode Register Set command issued to reset the DLL should always be followed by a Mode Register Set command to select normal operating mode.

All other combinations of values for A7-A10 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable isrequiredduringpower-upinitialization,andupon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation (upon exiting Self Refresh Mode, the DLL is enabled automatically). Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

Output Drive Strength

DS0, DS1, DS2, **TBD**

COMMANDS

Truth Table provides a quick reference of available commands. This is followed by a verbal description of each command. The additional Function Truth Tables provide current state/ next state information.

TRUTH TABLE (NOTE 1, 2)

Symbol	Command	Device State	CKEn-1	CKEn	DM	BA0,1	A8	A10, A9-0	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
ACT	Bank Active	Idle (3)	H	X	X	V	V	V	L	L	H	H
PRE	Bank Precharge	Any (3)	H	X	X	V	L	X	L	L	H	L
PREA	Precharge All	Any	H	X	X	X	H	X	L	L	H	L
WRIT	Write	Active (3)	H	X	X	V	L	V	L	H	L	L
WRITA	Write with Autoprecharge	Active (3)	H	X	X	V	H	V	L	H	L	L
READ	Read	Active (3)	H	X	X	V	L	V	L	H	L	H
READA	Read with Autoprecharge	Active (3)	H	X	X	V	H	V	L	H	L	H
MRS	Mode Register Set	Idle	H	X	X	L,L	V	V	L	L	L	L
EMRS	Extended Mode Register Set		H	X	X	H,L	V	V	L	L	L	L
NOP	No-Operation	Any	H	X	X	X	X	X	L	H	H	H
BST	Burst Read Stop	Active (4)	H	X	X	X	X	X	L	H	H	L
DSL	Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
AREF	Auto-Refresh	Idle	H	H	X	X	X	X	L	L	L	H
SELF	Self-Refresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
SELEX	Self-Refresh Exit	Idle (S.R)	L	H	X	X	X	X	H L	X H	X H	X X
PD	Power Down Mode Entry	Idle Active (5)	H	L	X	X	X	X	H L	X H	X H	X X
PDEX	Power Down Mode Exit	Any (Power down)	L	H	X	X	X	X	H L	X H	X H	X X
WDE	Data Write Enable	Active	H	X	L	X	X	X	X	X	X	X
WDD	Data Write Disable	Active	H	X	H	X	X	X	X	X	X	X

Notes:

(1) V = Valid, X = Don't care, L = Low Level, H = High Level

(2) CKEn signal is input level when commands are provided.
CKEn-1 signal is input level one clock cycle before the command provided.

(3) These are state of bank designated by BA0 BA1 signals.

(4) Applies only to read bursts with autoprecharge disabled; this command should not be used for read bursts with autoprecharge enabled, and for write bursts.

(5) Power Down Mode can not be entered in the burst cycle.

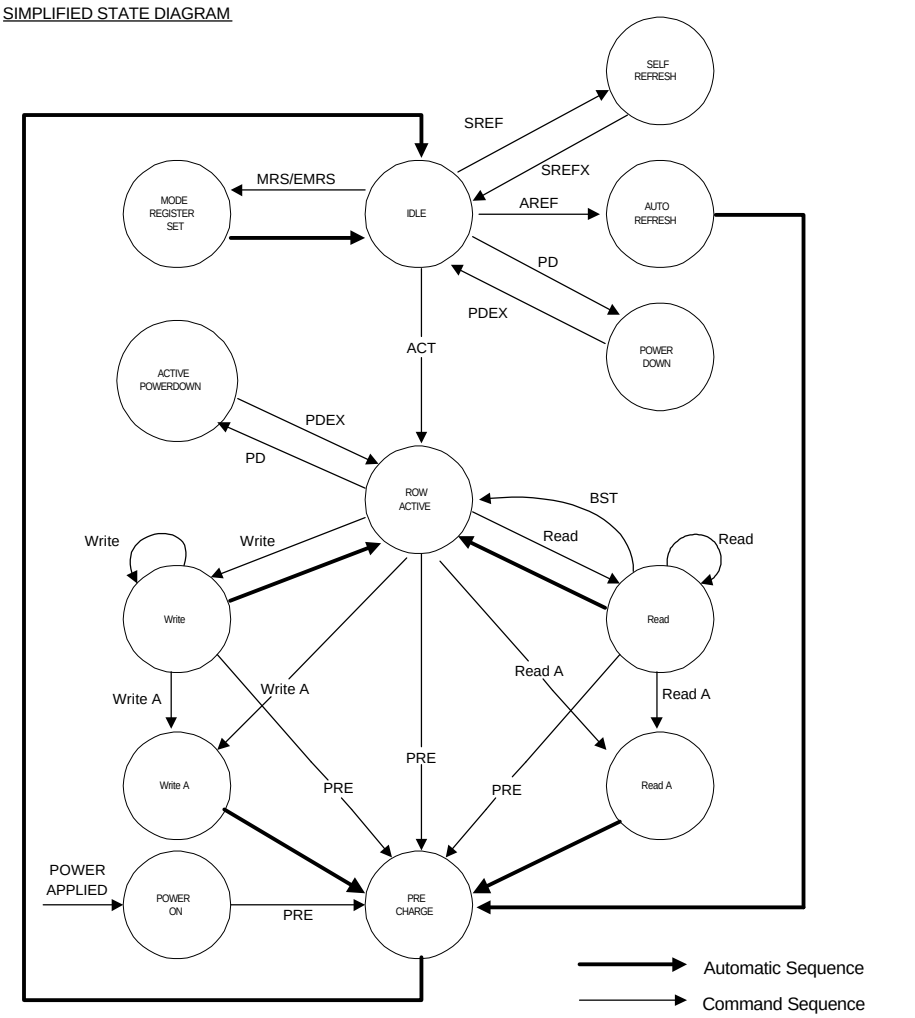
Function TRUTH TABLE (NOTE 1)

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	ACTION	NOTE
Idle	H	X	X	X	X	DSL	NOP	
	L	H	H	X	X	NOP, BST	NOP	
	L	H	L	H	BA, CA,A8	Read, Read A	ILLEGAL	3
	L	H	L	L	BA, CA,A8	Write, Write A	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ACTIVE (select and activate row)	
	L	L	H	L	BA, A8	PRE, PRE A	NOP	
	L	L	L	H	X	AREF, SREF	Refresh or Self refresh	2
	L	L	L	L	Op-Code	MRS, EMRS	Mode register accessing	2
Row Active	H	X	X	X	X	DSL	NOP	
	L	H	H	X	X	NOP, BST	NOP	
	L	H	L	H	BA, CA,A8	Read, Read A	READ (start READ burst)	4
	L	H	L	L	BA, CA,A8	Write, Write A	WRITE (start WRITE burst)	4
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A8	PRE, PRE A	PRECHARGE	5
	L	L	L	H	X	AREF, SREF	ILLEGAL	
	L	L	L	L	Op-Code	MRS, EMRS	ILLEGAL	
Read	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	Burst stop	
	L	H	L	H	BA, CA,A8	Read, Read A	Term burst, start new READ burst	6
	L	H	L	L	BA, CA,A8	Write, Write A	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A8	PRE, PRE A	Term burst, PRECHARGE	
	L	L	L	H	X	AREF, SREF	ILLEGAL	
	L	L	L	L	Op-Code	MRS, EMRS	ILLEGAL	
Write	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA, CA,A8	Read, Read A	ILLEGAL	3
	L	H	L	L	BA, CA,A8	Write, Write A	Term burst, start new READ burst	6,7
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A8	PRE, PRE A	Term burst, PRECHARGE	
	L	L	L	H	X	AREF, SREF	ILLEGAL	8
	L	L	L	L	Op-Code	MRS, EMRS	ILLEGAL	
Read with Auto rpecharge	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA, CA,A8	Read, Read A	ILLEGAL	
	L	H	L	L	BA, CA,A8	Write, Write A	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A8	PRE, PRE A	ILLEGAL	
	L	L	L	H	X	AREF, SREF	ILLEGAL	
	L	L	L	L	Op-Code	MRS, EMRS	ILLEGAL	
Write with Auto precharge	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA, CA,A8	Read, Read A	ILLEGAL	
	L	H	L	L	BA, CA,A8	Write, Write A	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A8	PRE, PRE A	ILLEGAL	
	L	L	L	H	X	AREF, SREF	ILLEGAL	
	L	L	L	L	Op-Code	MRS, EMRS	ILLEGAL	

NOTE:

1. This table applies when CKE n-1 was HIGH and CKE n is HIGH.
2. ILLEGAL if any bank is not idle.
3. ILLEGAL to bank in specified states; Function may be legal in the bank indicated by Bank Address(BA), depending on the state of that bank.
4. ILLEGAL if tRCD is not satisfied.
5. ILLEGAL if tRAS is not satisfied.
6. Must satisfy bust interrupt condition.
7. Must satisfy bus contention, bus turn around, and/ or write recovery requirements
8. Must mask preceding data, which don't satisfy tWR

Figure3:Simplified State Diagram



MRS = Mode Register Set
EMRS = Extended Mode Register Set
SREF = Enter Self Refresh
SREFX = Exit Self Refresh
AREF = Auto Refresh
PD = Enter Power Down
PDEX = Exit Power Down

ACT = Active
Write A = Write with Autoprecharge
Read A = Read with Autoprecharge
PRE = Precharge
BST = B nst Read Stpop

DESELECT

The Device Deselect command disables the command decoder so that the $\overline{RAS}$ $\overline{CAS}$ $\overline{WE}$ and Address inputs are ignored. This command is similar to the No-Operation command.

NO OPERATION (NOP)

The No Operation Command should be used in cases when the DDR SDRAM is in an idle or a wait state to prevent the DDR SDRAM from registering any unwanted commands between operations. A No Operation Command is registered when $\overline{CS}$ is low with $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ held high at the rising edge of the clock. A No Operation Command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

MODE REGISTER SET

Command is registered when $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ is at the rising edge of the clock. The mode registers are loaded by inputs A0-A10. See mode register descriptions in the Register Definition section. The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress, and a subsequent executable command cannot be issued until tMRD is met.

ACTIVE

The ACTIVE command is registered when $\overline{CS}$, $\overline{RAS}$ is low with $\overline{CAS}$, and $\overline{WE}$ held high at the rising edge of the clock, used to open a row in a particular bank for a subsequent access.

READ

The READ command is registered when $\overline{CS}$, $\overline{CAS}$ is low with $\overline{RAS}$, and $\overline{WE}$ held high at the rising edge of the clock, used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A7 selects the starting column location.

WRITE

The WRITE command is registered when $\overline{CS}$, $\overline{CAS}$, $\overline{WE}$ is low with $\overline{RAS}$, held high at the rising edge of the clock, used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A7 selects the starting column location

PRECHARGE

The PRECHARGE command is registered when $\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ is low with $\overline{CAS}$ held high at the rising edge of the clock, used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the PRECHARGE command is issued. Input A8 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank.

BURST READ STOP

The BURST READ STOP command register when $\overline{CS}$ $\overline{WE}$ is low with RAS CAS held high is used to truncate read bursts (with autoprecharge disabled).

AUTO REFRESH

The Auto Refresh command is register when $\overline{CS}$ $\overline{RAS}$ $\overline{CAS}$ low with $\overline{WE}$ high.

The refresh addressing is generated by the internal refresh controller. This makes the address bits “Don’t Care” during an AUTO REFRESH command. The W946432AD requires AUTO REFRESH cycles at an average periodic interval of 15.6µs (maximum).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM, meaning that the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 9 * 15.6us (140.4us). This maximum absolute interval is short enough to allow for DLL updates internal to the DDR SDRAM to be restricted to AUTO REFRESH cycles, without allowing too much drift in tAC between updates.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). The DLL is automatically disabled upon entering SELF REFRESH, and is automatically enabled upon exiting SELF REFRESH (200 clock cycles must then occur before a READ command can be issued). Input signals except CKE are “Don’t Care” during SELF REFRESH.

The procedure for exiting self refresh requires a sequence of commands. First, CK must be stable prior to CKE going back HIGH. Once CKE is HIGH, the DDR SDRAM must have NOP commands issued for tXSNR because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for 200 clock cycles before applying any other command.

OPERATIONS

BANK/ROW ACTIVATION

Before any READ or WRITE commands can be issued to a bank within the DDR SDRAM, a row in that bank must be “opened.” This is accomplished by the ACTIVE command, which selects both the bank and the row to be activated.

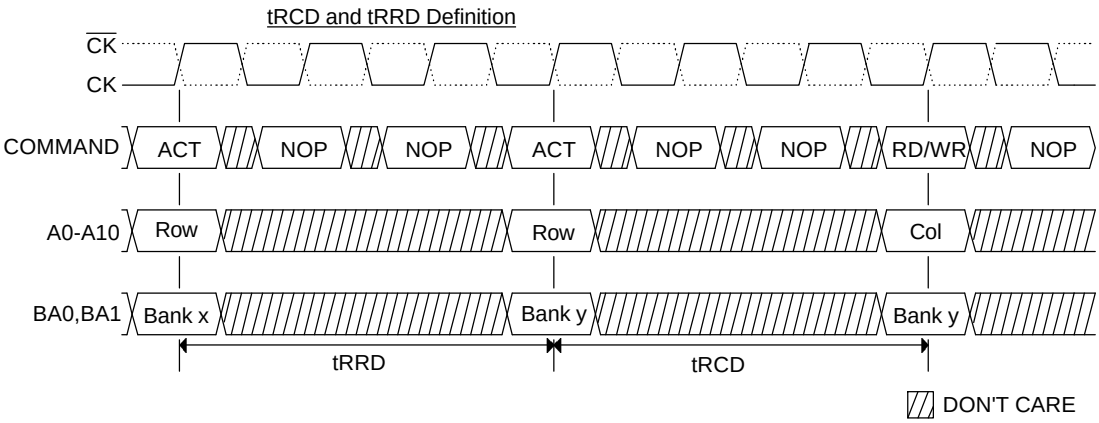
The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A10 selects the row. The maximum time that each bank can be held in the active state is specified as tRAS (max). After this command is issued, Read or Write operation can be executed.

After opening a row, a READ or WRITE command may be issued to that row, subject to the tRCD specification.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been “closed” (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by tRC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by tRRD.

Figure4:tRCD and tRRD Definition



READs

The starting column and bank addresses are provided with the READ command and AUTO PRECHARGE is either enabled or disabled for that burst access. If AUTO PRECHARGE is enabled (A8 = high), the row that is accessed will start precharge at the completion of the burst. This command cannot be interrupted by any other command. For the generic READ commands used in the following illustrations, AUTO PRECHARGE is disabled (A8 = low).

During READ bursts, the valid data-out element from the starting column address will be available following the $\overline{CAS}$ latency after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge. Figure5: shows general timing. DQS is driven by the DDR SDRAM along with output data. The initial LOW state on DQS is known as the read preamble; the LOW state coincident with the last data-out element is known as the read post amble. Upon completion of a burst, assuming no other commands have been initiated, the DQS will go High-Z.

Data from any READ burst may be concatenated with or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new READ command should be issued *x* cycles after the first READ command, where *x* equals the number of desired data element pairs (pairs are required by the *32* prefects architecture). This is shown in Figure6:. A READ command can be initiated on any clock cycle following a previous READ command. Non-consecutive READ data is shown for illustration in Figure7:. Full-speed random read accesses within a page (or pages) can be performed as shown in Figure8:.

Data from any READ burst may be truncated with a BURST READ STOP command, as shown in Figure9:The BURST READ STOP latency is equal to the read ($\overline{CAS}$) latency.

Data from any READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST READ STOP command must be used, as shown in Figure10:.

A READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that AUTO PRECHARGE was not activated). The PRECHARGE command should be issued *x* cycles after the READ command, where *x* equals the number of desired data element pairs. Note that part of the row precharge time is hidden during the access of the last data elements.

In the case of a READ being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same READ burst with AUTO PRECHARGE enabled. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate bursts.

Figure5:READ BURST – REQUIRED CAS LATENCIES

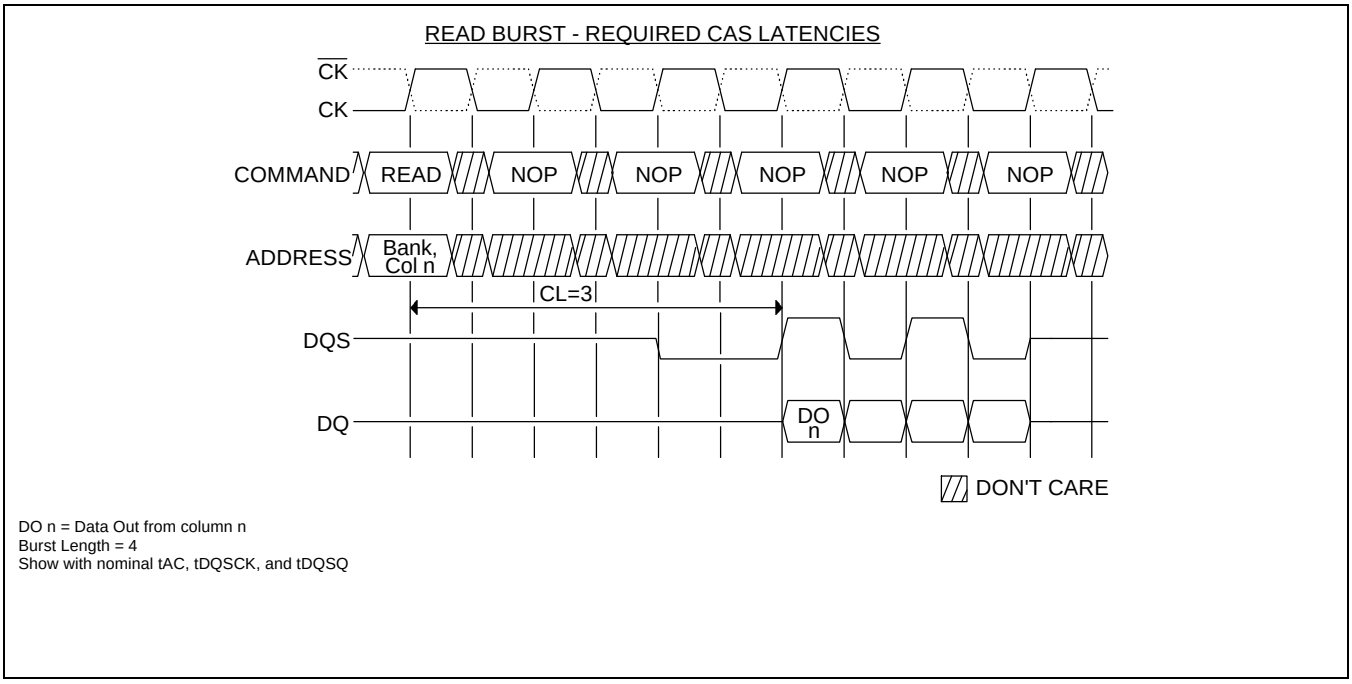
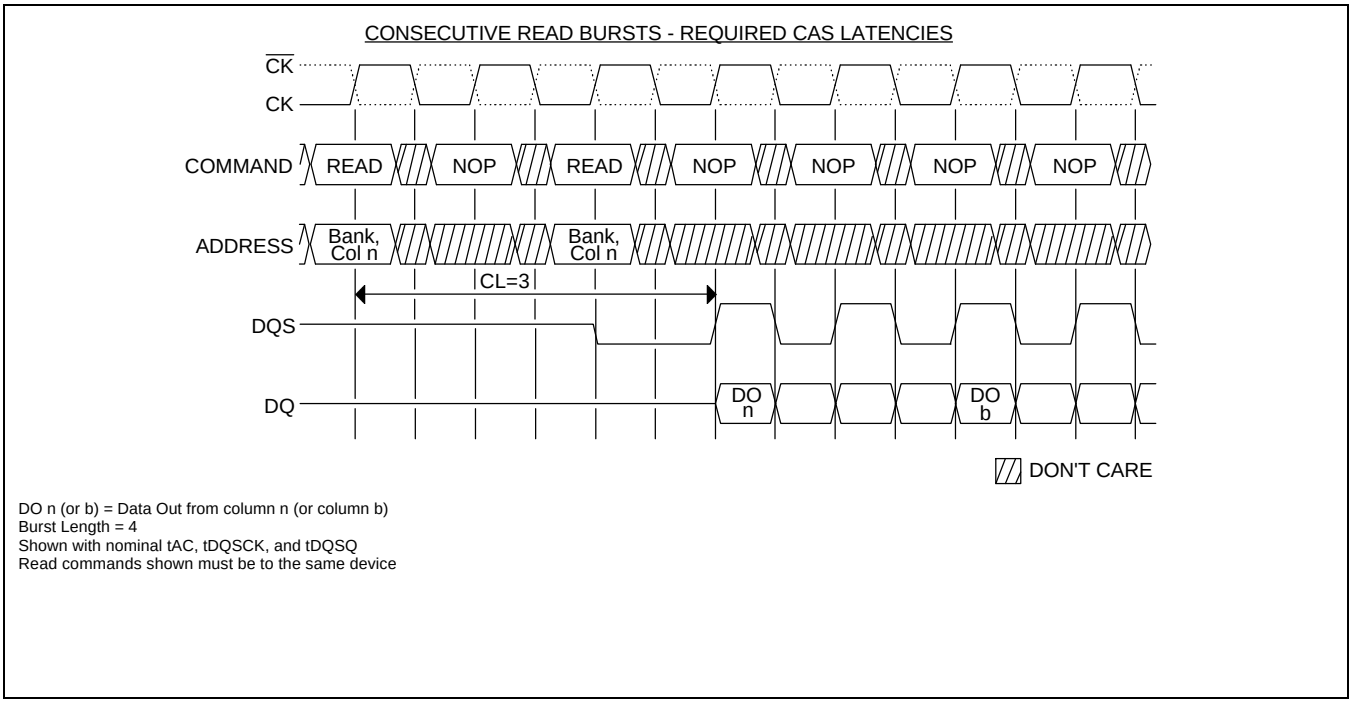
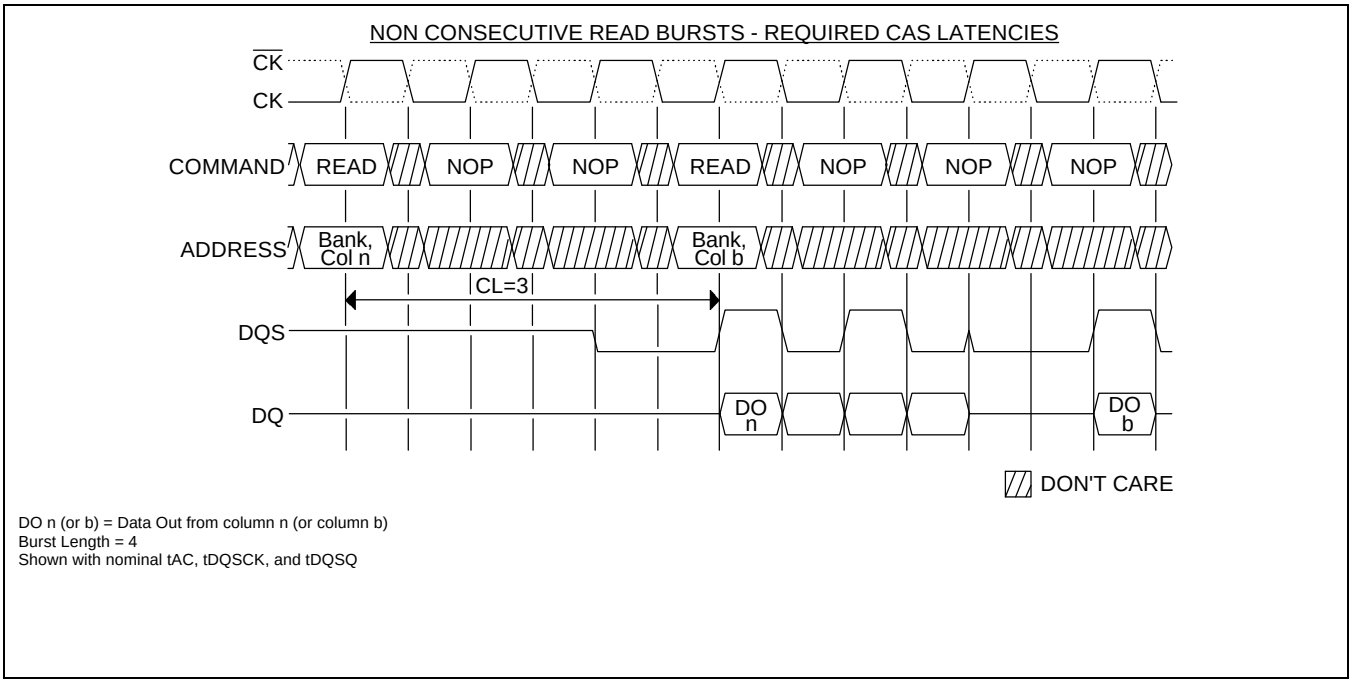


Figure6:CONSECUTIVE READ BURSTS – REQUIRED CAS LATENCIES



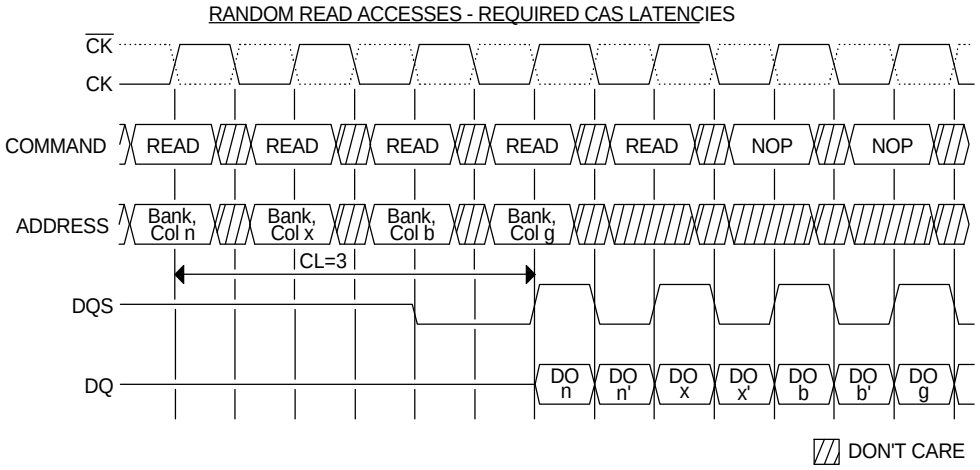
DO n (or b) = Data Out from column n (or column b)
Burst Length = 4
Shown with nominal tAC, tDQSCK, and tDQSQ
Read commands shown must be to the same device

Figure7:NON – CONSECUTIVE READ BURSTS – REQUIRED CAS LATENCIES



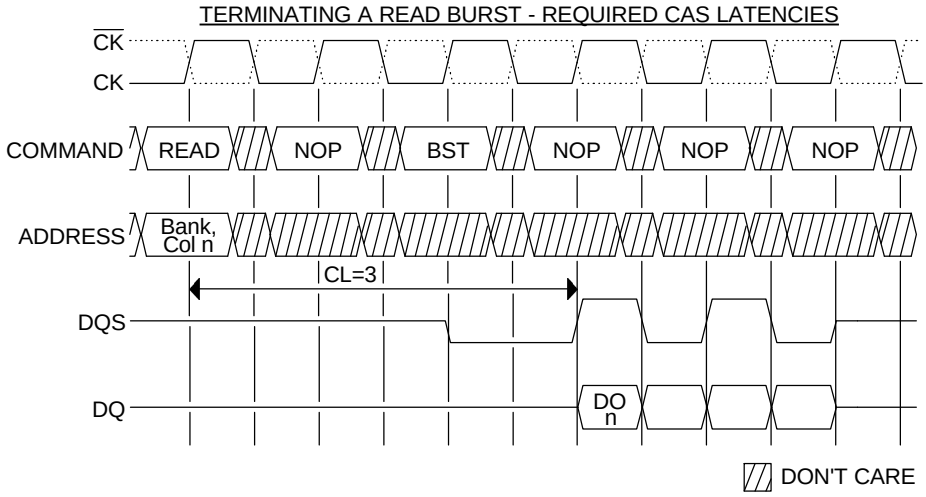
DO n (or b) = Data Out from column n (or column b)
Burst Length = 4
Shown with nominal tAC, tDQSCK, and tDQSQ

Figure8:RANDOM READ ACCESSES – REQUIRED CAS LATENCIES



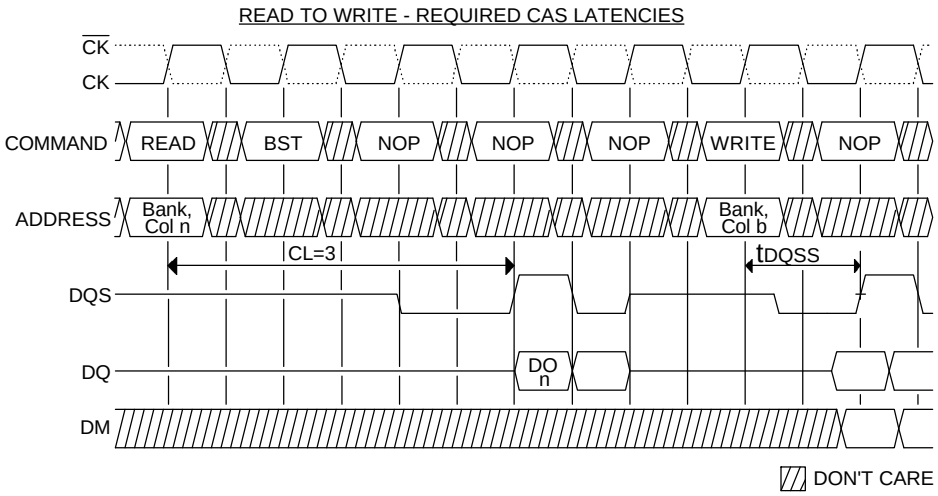
DO n, etc. = Data Out from column n, etc.
n', etc. = the next Data Out following DO n, etc. according to the programmed burst order
Burst Length = 4
Reads are to active rows in any banks
Shown with nominal tAC, tDQSCK, and tDQSQ

Figure9:BURST READ STOP– REQUIRED CAS LATENCIES



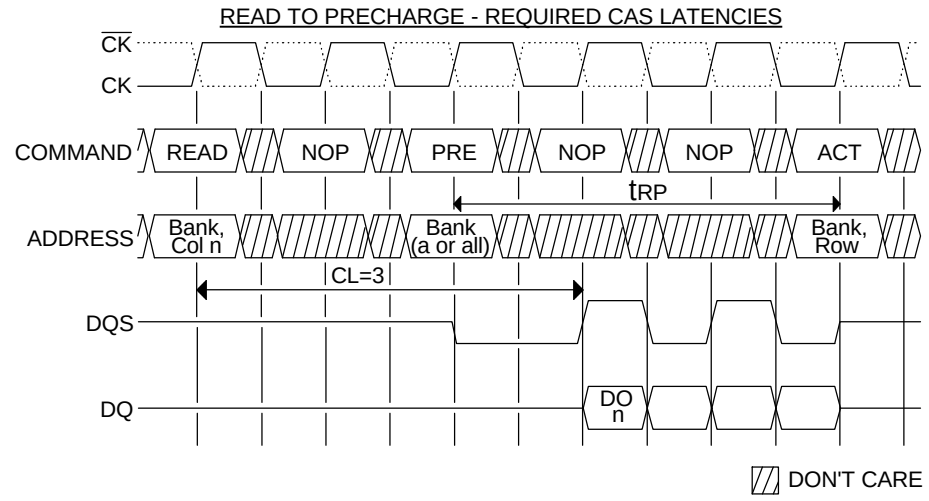
DO n = Data Out from column n
Cases shown are bursts of 8 terminated after 4 data elements
Shown with nominal tAC, tDQSCK, and tDQSQ

Figure10:READ TO WRITE – REQUIRED CAS LATENCIES



DO n (or b) = Data Out from column n (or column b)
Burst Length = 4
Data In elements are applied following DI b in the programmed order
Shown with nominal tAC, tDQSCK, and tDQSQ

Figure11:READ TO PRECHARGE – REQUIRED CAS LATENCIES



DO n (or b) = Data Out from column n Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8
Shown with nominal tAC, tDQSCK, and tDQSQ

WRITEs

The starting column and bank addresses are provided with the WRITE command, and AUTO PRECHARGE is either enabled or disabled for that access. If AUTO PRECHARGE is enabled (A8=HIGH), the row being accessed will be precharged at the end of the WRITE burst; if AUTO PRECHARGE is disabled (A8=LOW), the row will remain open for subsequent accesses.

During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the write command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write post amble. The time between the WRITE command and the first corresponding rising edge of DQS (tDQSS) is specified with a relatively wide range (from 75% to 125% of 1 clock cycle), Figure12: show the two extremes of tDQSS for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQS will remain High-Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data can be maintained. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst, which is being truncated. The new WRITE command should be issued *x* cycles after the first WRITE command, where *x* equals the number of desired data element pairs Figure13: show concatenated bursts of 4. An example of non-consecutive WRITEs is shown in. 0 Full-speed random write accesses within a page or pages can be performed as shown in. Figure15: Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE without truncating the write burst, tWTR should be met as shown in Figure16:.

Data for any WRITE burst may be followed by a subsequent PRECHARGE command. To follow a WRITE without truncating the write burst, tWR should be met as shown in 0.

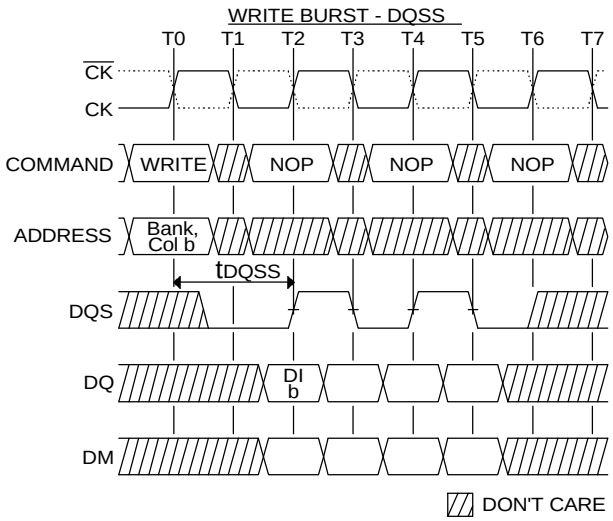
Data for any WRITE burst may be truncated by a subsequent PRECHARGE command, as shown in Figure18: Figure19:. Note that only the data-in pairs that are registered prior to the tWR period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in Figure18: Figure19:. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until t RP is met.

POWER-DOWN

Power-down is entered when CKE is registered LOW (no accesses can be in progress). If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$ and CKE. For maximum power savings, the user has the option of disabling the DLL prior to entering power-down. In that case, the DLL must be enabled after exiting power-down, and 200 clock cycles must occur before a READ command can be issued. However, power-down duration is limited by the refresh requirements of the device, so in most applications, the self-refresh mode is preferred over the DLL-disabled power-down mode.

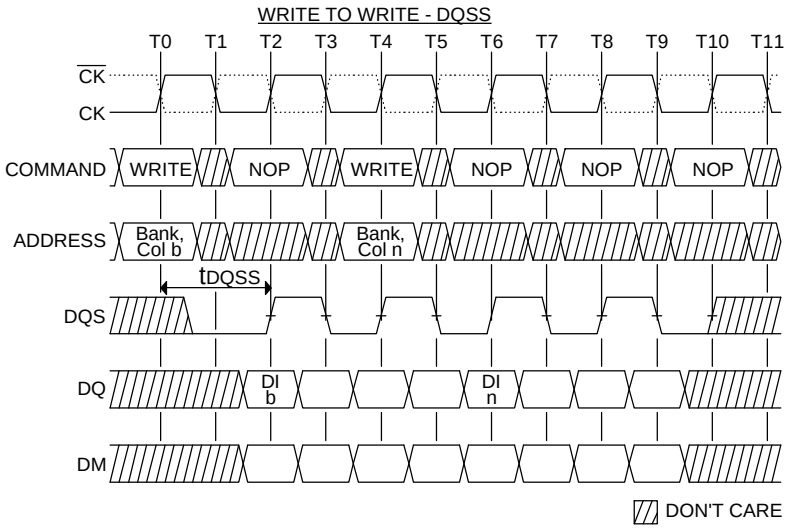
In power-down, CKE LOW and a stable clock signal must be maintained at the inputs of the DDR SDRAM, and all other input signals are “Don’t Care”. The power-down state is synchronously exited when CKE is registered HIGH (along with a NOP or DESELECT command). A valid executable command may be applied one clock cycle later.

Figure12:WRITE BURST – DQSS



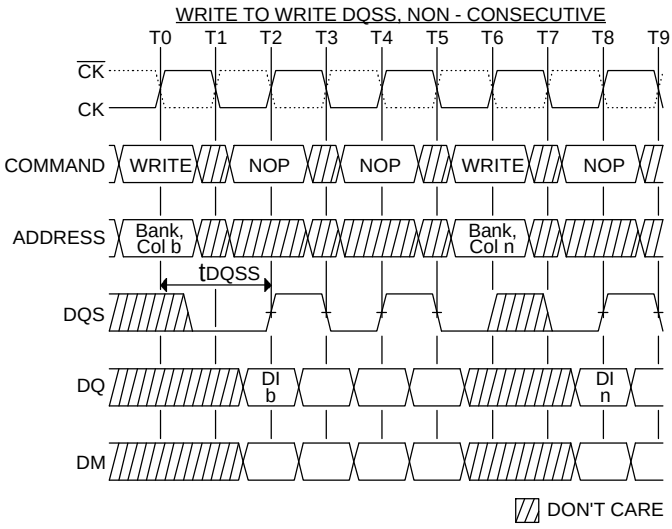
DI b, etc. = Data In for column b, etc.
A non-interrupted burst of 4 is shown
A8 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

Figure13:WRITE TO WRITE – DQSS



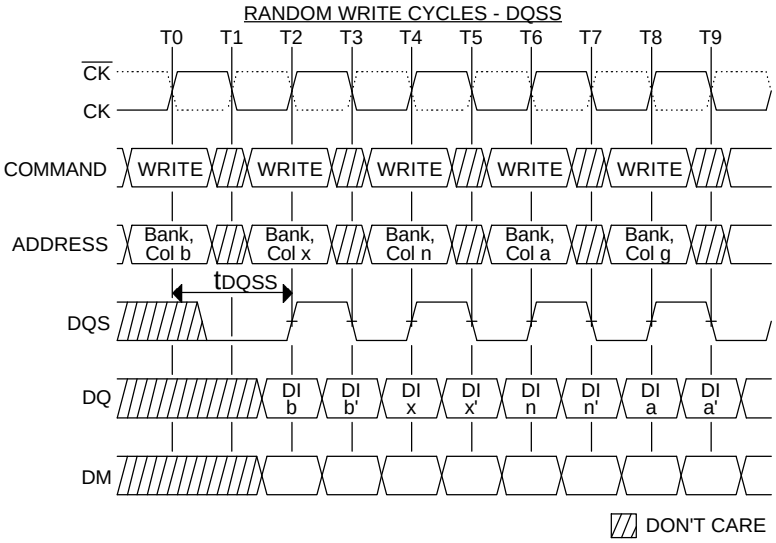
DI b, etc. = Data In for column b, etc.
A non-interrupted burst of 4 is shown

Figure14:WRITE TO WRITE DQSS, NON – CONSECUTIVE



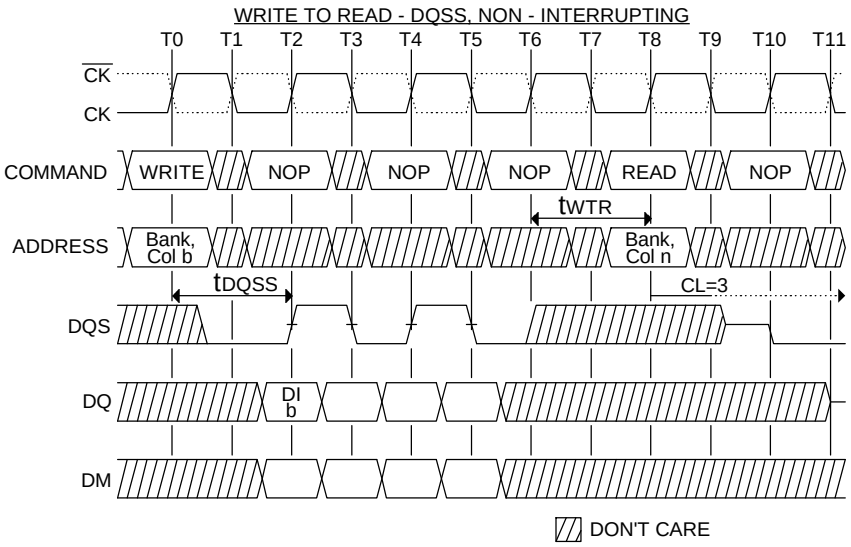
DI b, etc. = Data In for column b, etc.
A non-interrupted burst of 4 is shown
Each Write command may be to any bank, and may be to the same or different devices
Depending on external components

Figure15:RANDOM WRITE CYCLES – DQSS



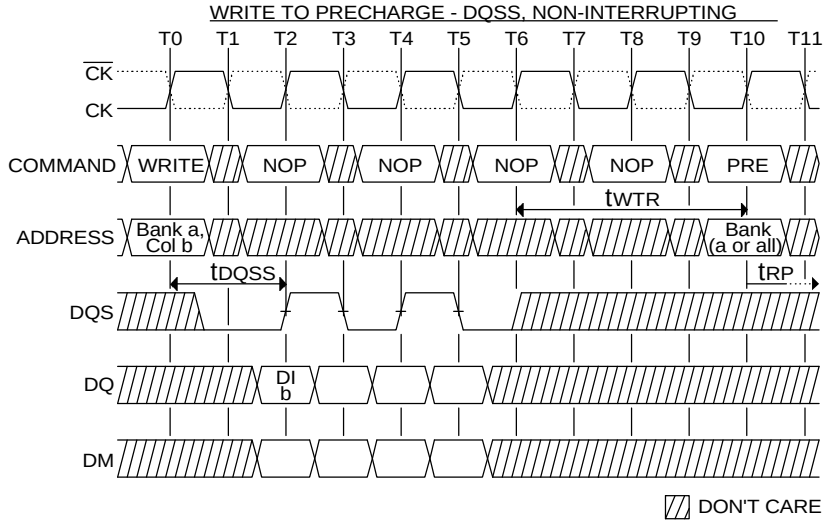
DI b, etc. = Data In for column b, etc.
b', etc. = the next Data In following DI b, etc. according to the programmed burst order
Programmed Burst Length = 2, 4 or 8 in cases shown

Figure16:WRITE TO READ – DQSS, NON – INTERRUPTING



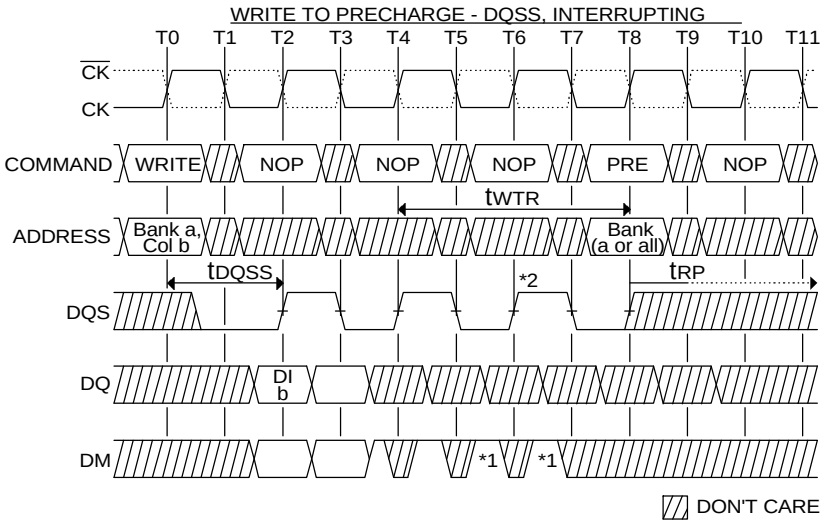
DI b, etc. = Data In for column b, etc.
A non-interrupted burst of 4 is shown
tWTR is referenced from the first postive CK edge after the last Data In pair
A8 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
The READ andWRITE commands may be to any bank, and may be to the same or different devices
In the case where the READ and WRITE commands are to different devices, tWTR need not be met, and the READ command can be applied earlier
tWTR = 2 tCK for optional CL = 1.5 (otherwise tWTR = 1 Tck)

Figure17:WRITE TO PRECHARGE - DQSS, NON - INTERRUPTING



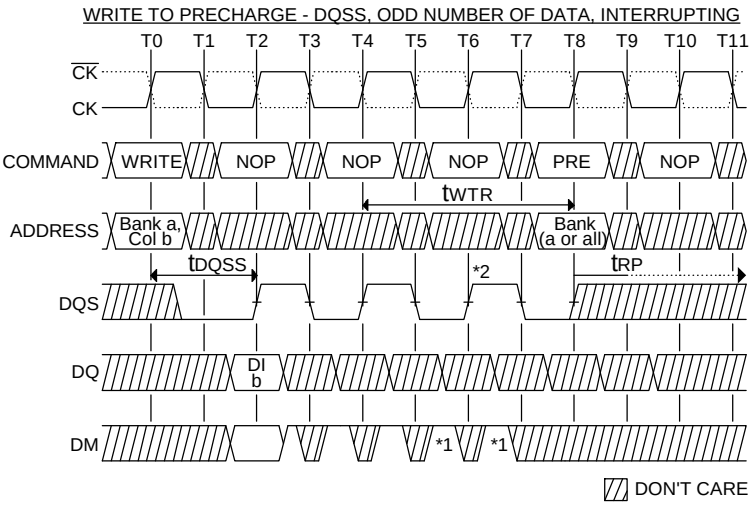
DI b, etc. = Data In for column b, etc.
A non-interrupted burst of 4 is shown
tWTR is referenced from the first postive CK edge after the last Data In pair
A8 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

Figure18:WRITE TO PRECHARGE – DQSS, INTERRUPTING



DI b = Data In for column b
A interrupted burst of 4 or 8 is shown, 2 data elements are written
1 subsequent element of Data In is applied in the programmed order following DI b
tWTR is referenced from the first postive CK edge after the last desired Data In pair
The PRECHARGE command masks the last two data elements in the burst
A8 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
*1 = can be don't care for programmed burst length of 4
*2 = for programmed burst length of 4, DQS becomes don't care at this point

Figure19:WRITE TO PRECHARGE – DQSS, ODD NUMBER OF DATA, INTERRUPTING



DI b = Data In for column b
A interrupted burst of 4 or 8 is shown, 1 data element is written
tWTR is referenced from the first postive CK edge after the last desired Data In pair
The PRECHARGE command masks the last two data elements in the burst
A8 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
*1 = can be don't care for programmed burst length of 4
*2 = for programmed burst length of 4, DQS becomes don't care at this point

Figure20:POWER - DOWN

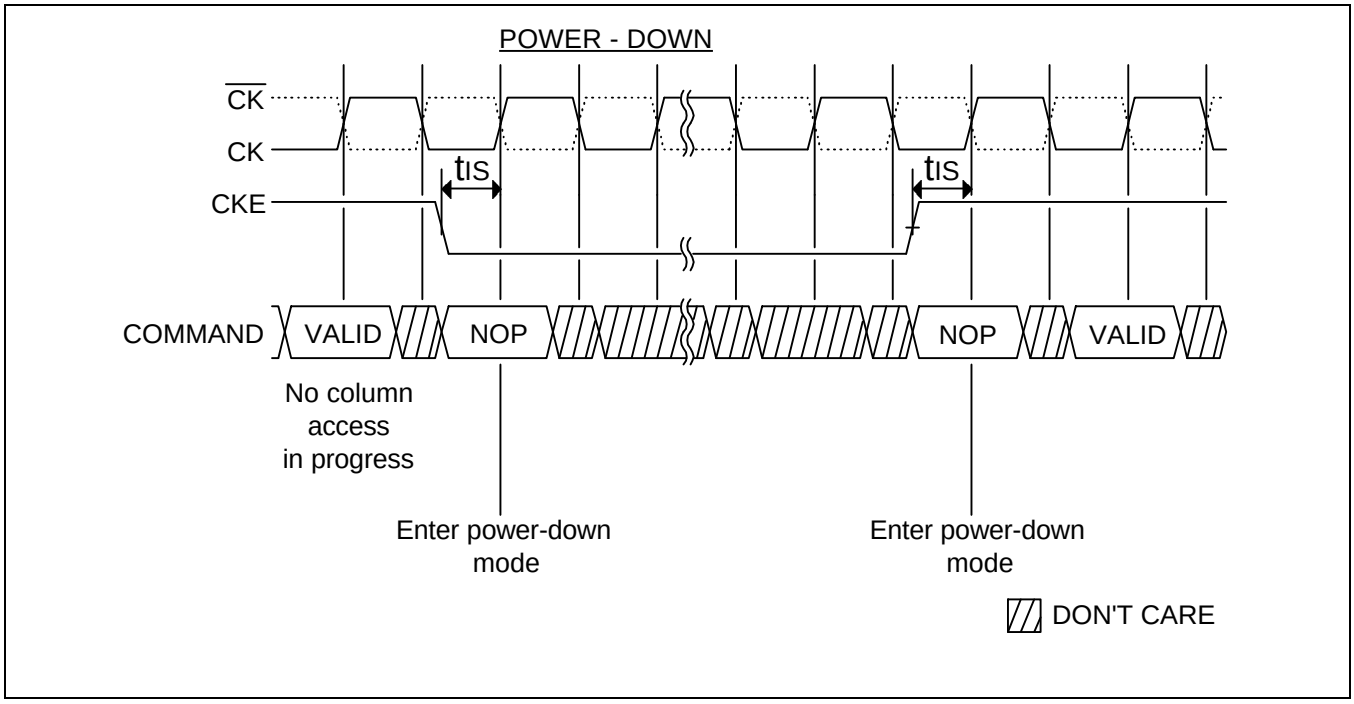


Figure21:DATA INPUT (WRITE) TIMING

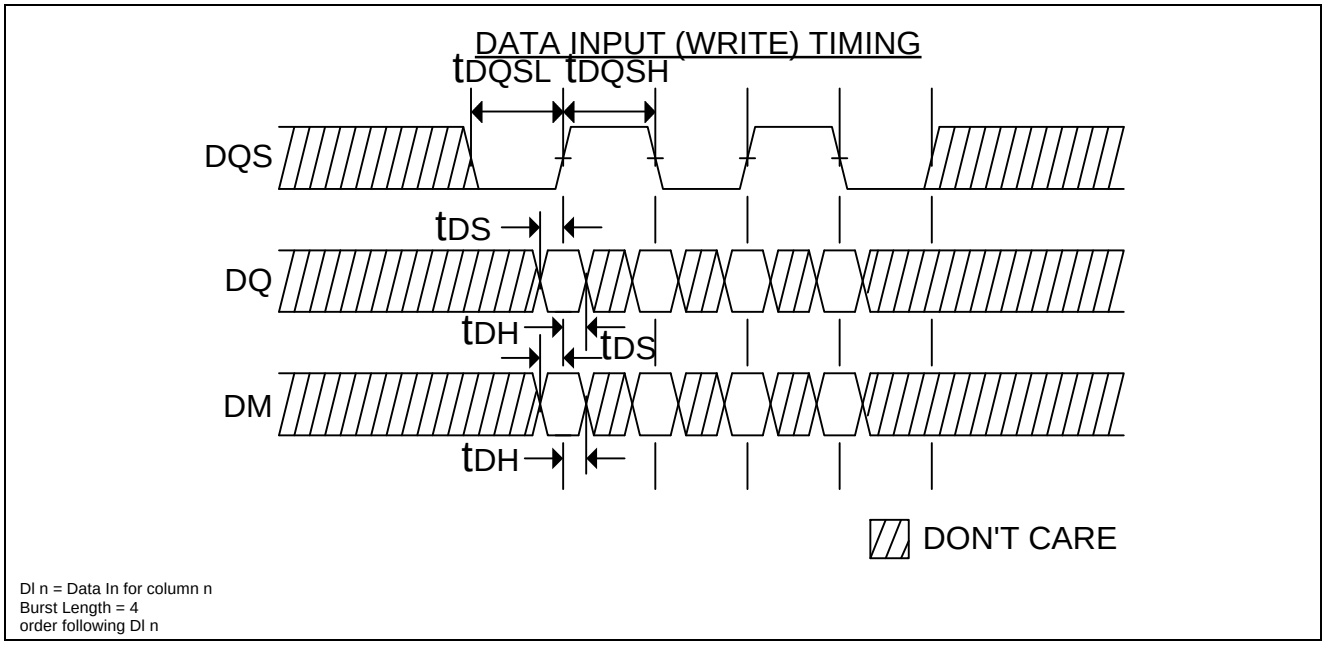
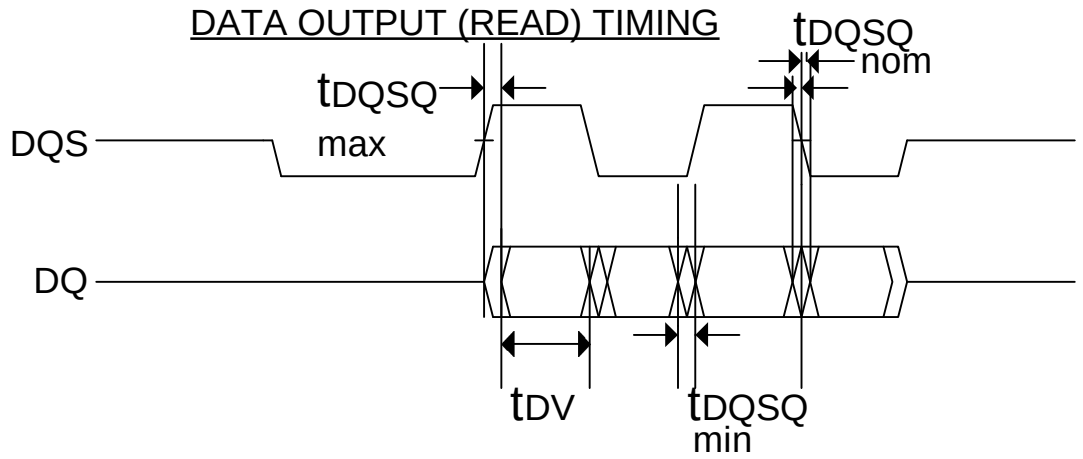
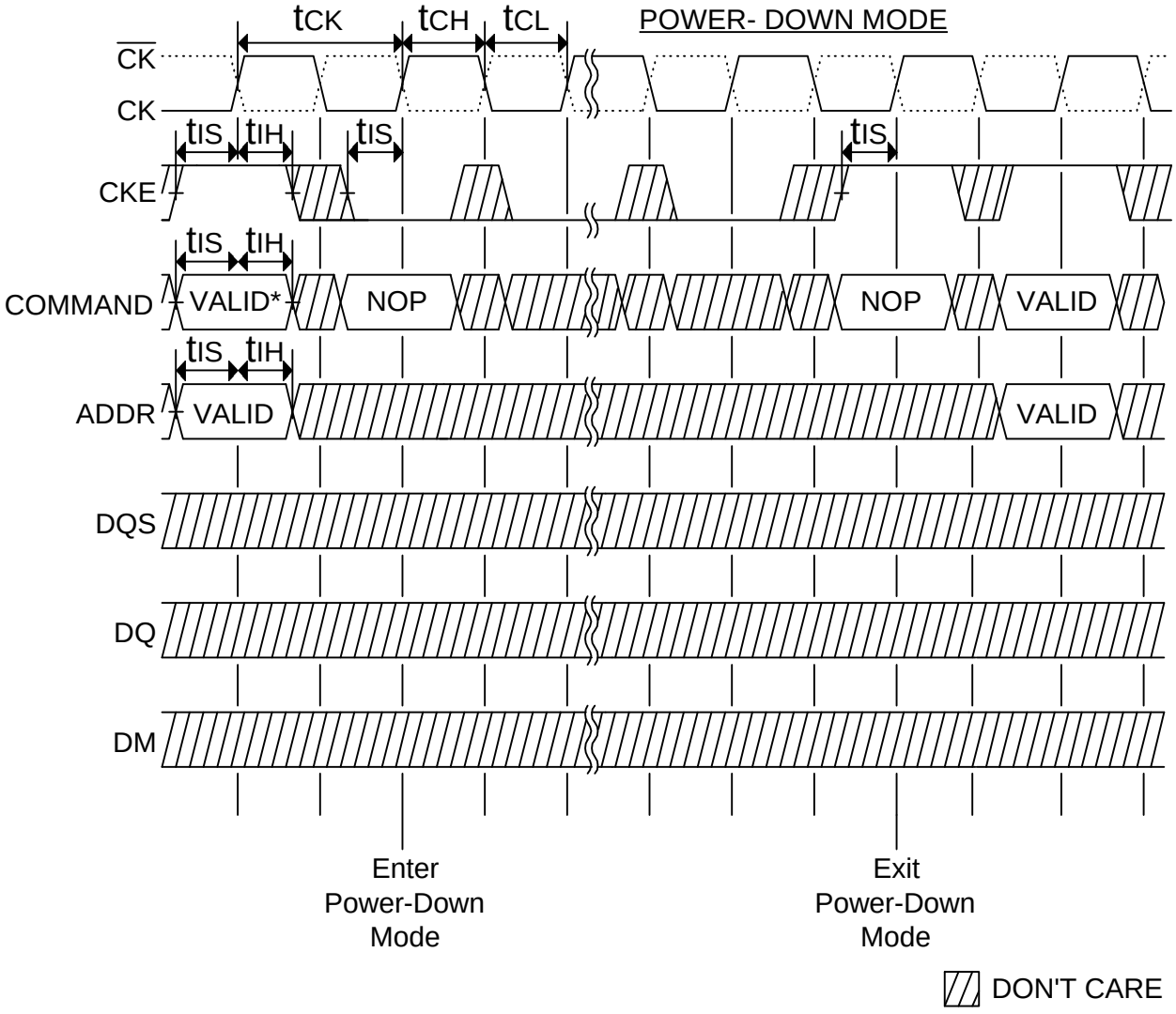


Figure22:DATA OUTPUT (READ) TIMING



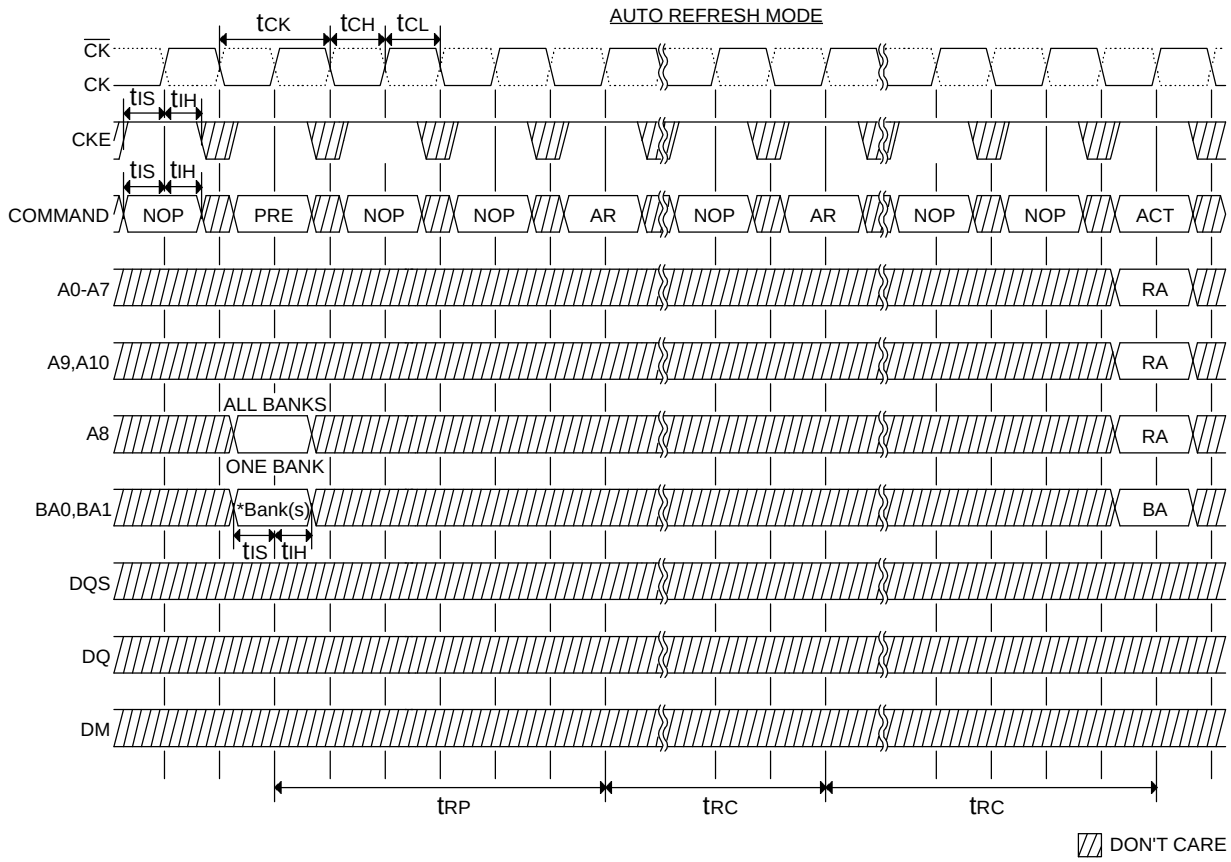
1.tDQSQ max occurs when DQS is earliest among DQS signals to transition.
2.tDQSQ min occurs when DQS is the latest among DQS and DQ signals to transition.
3.tDQSQ nom, shown for reference, occurs when DQS transitions in the center among DQ signal transitions.
4.Burst Length = 4

Figure23:POWER – DOWN MODE



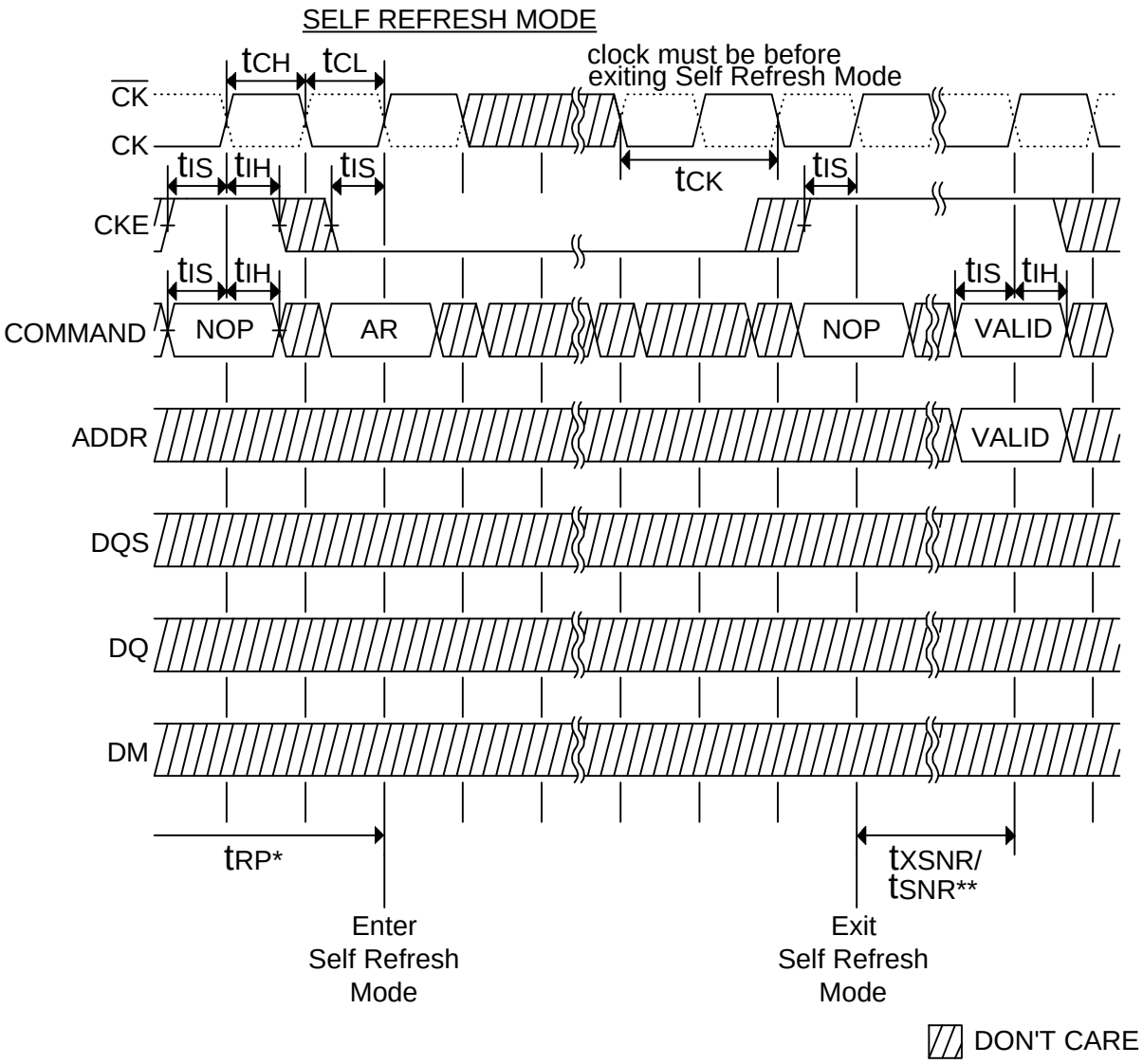
No column accresses are allowed to be in progress at the Power-Down is entered
* = If this command is a PRECHARGE (or if the device is already in the idle state) then the Power-Down mode shown is Precharge Power Down. If this command is an ACTIVE (or if at least one row is already active) then the Power-Down mode shown is Active Power Down

Figure24:AUTO REFRESH MODE



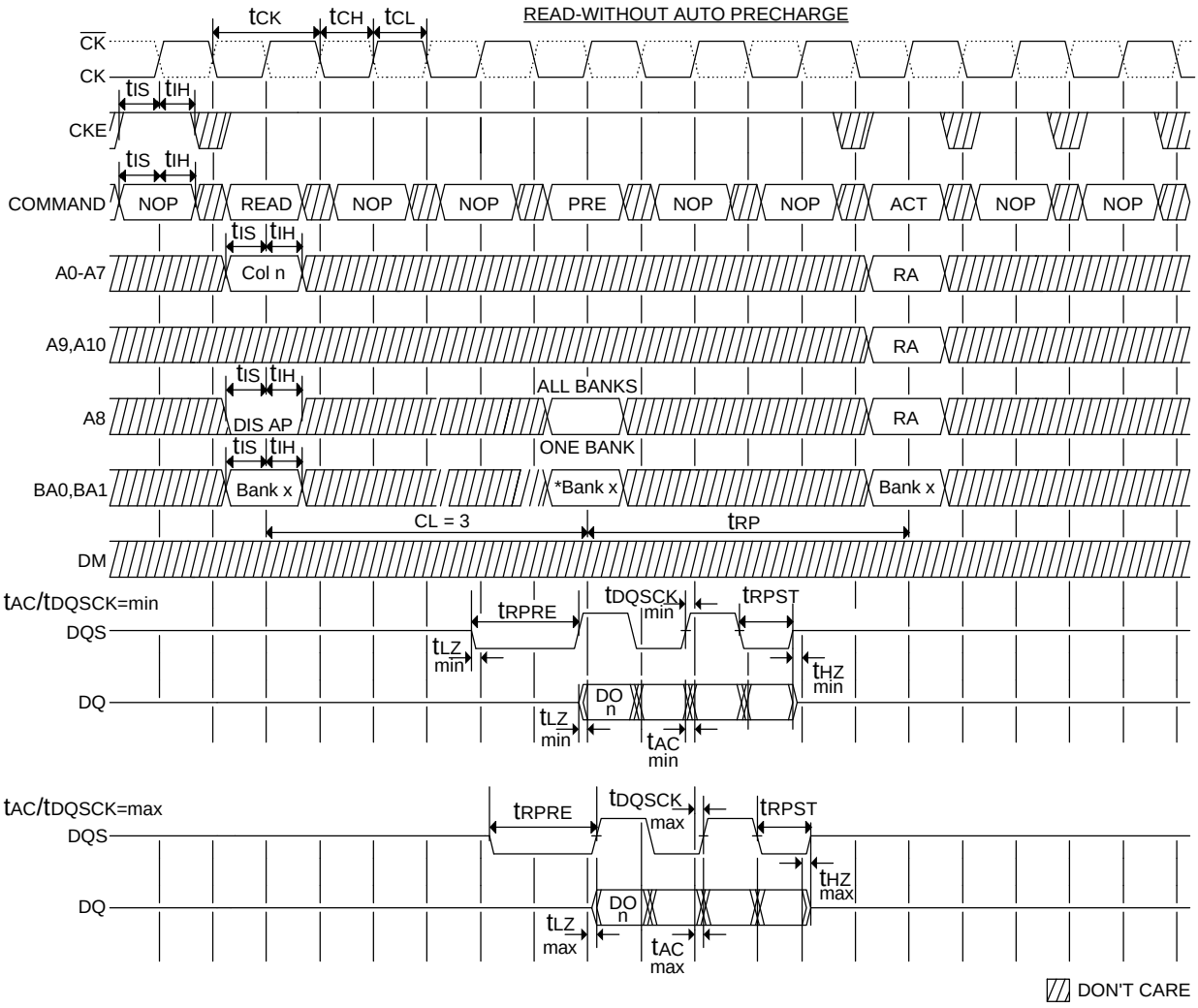
* = "Don't Care", if A8 is HIGH at this point; A8 must be HIGH if more than one bank is active (i.e. must precharge all active banks)
PRE = PRECHARGE, ACT = ACTIVE, RA ROW Address, BA = BANK Address, AR = AUTOREFRESH
NOP commands are shown for ease of illustration; other valid commands may be possible at these time
DM, DQ and DQS signals are all "Do'nt Care"/High-z for operations shown

Figure25:SELF REFRESH MODE



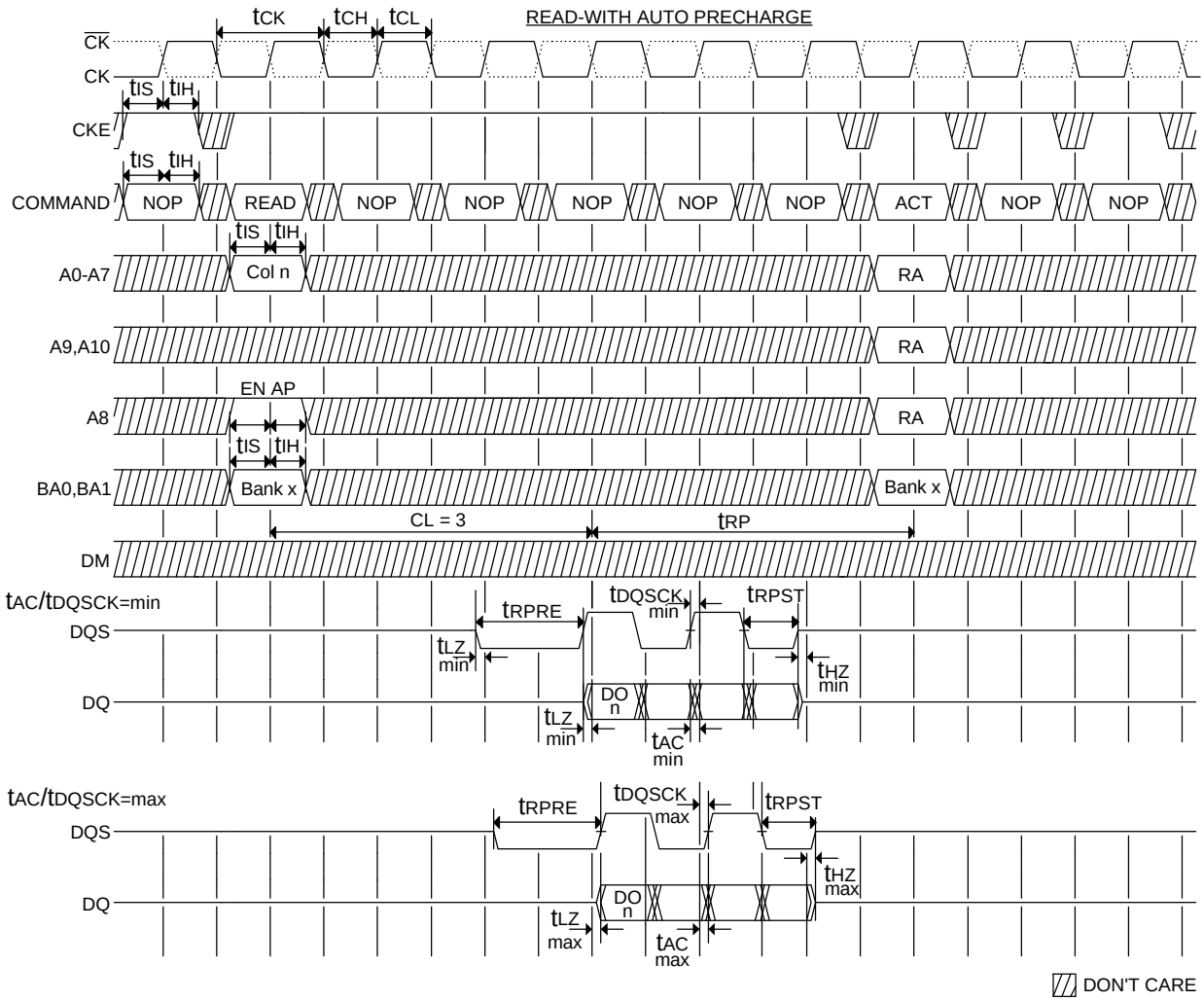
* = Device must be in tje "All banks idle" state prior to entering Self Refresh Mode
** = tXNR is required before any non-READ command can be applied, and tSNRD (200 cycles of CLK) are required befor READ command can be applied.

Figure26:READ – WITHOUT AUTO PRECHARGE



DO n = Data Out from column n
Burst Length = 4
DIS AP = Disable Autoprecharge
* = "Don't Care", if A8 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times

Figure27:READ - WITH AUTO PRECHARGE



DO n = Data Out from column n
Burst Length = 4
EN AP = Enable Autoprecharge
ACT = ACTIVE, RA = Row Address
NOP commands are shown for ease of illustration; other commands may be valid at these times

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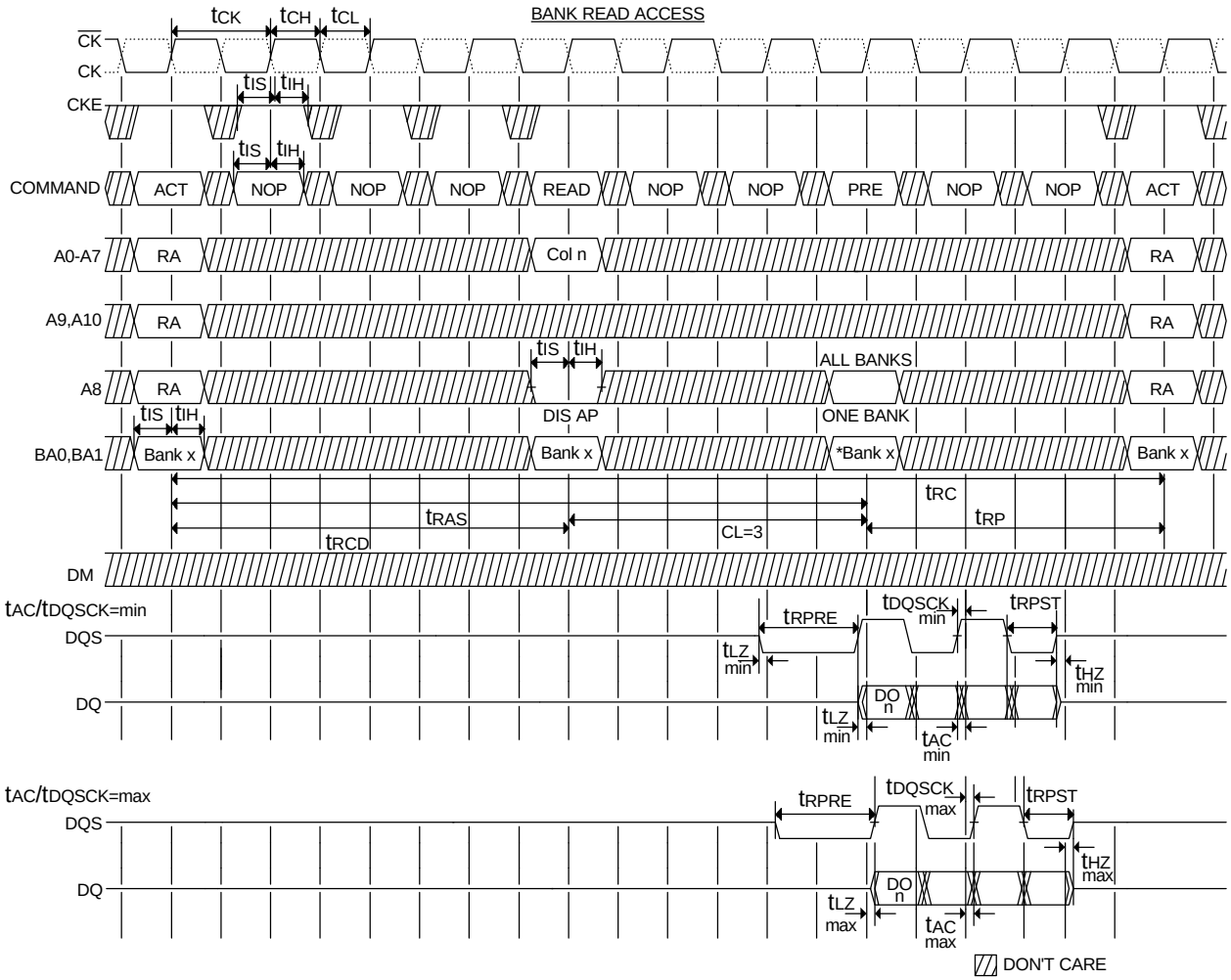
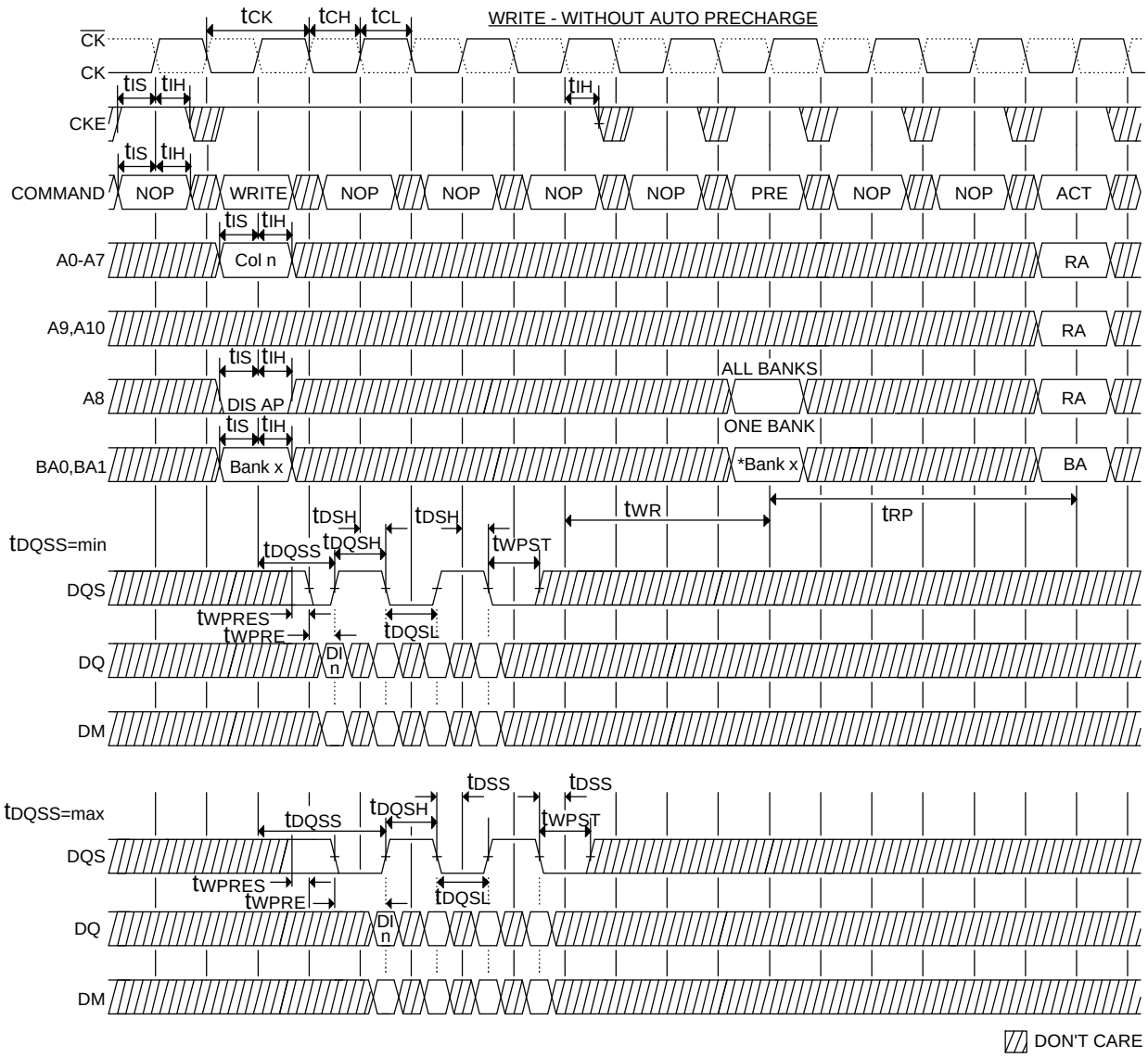
Figure28:BANK READ ACCESS



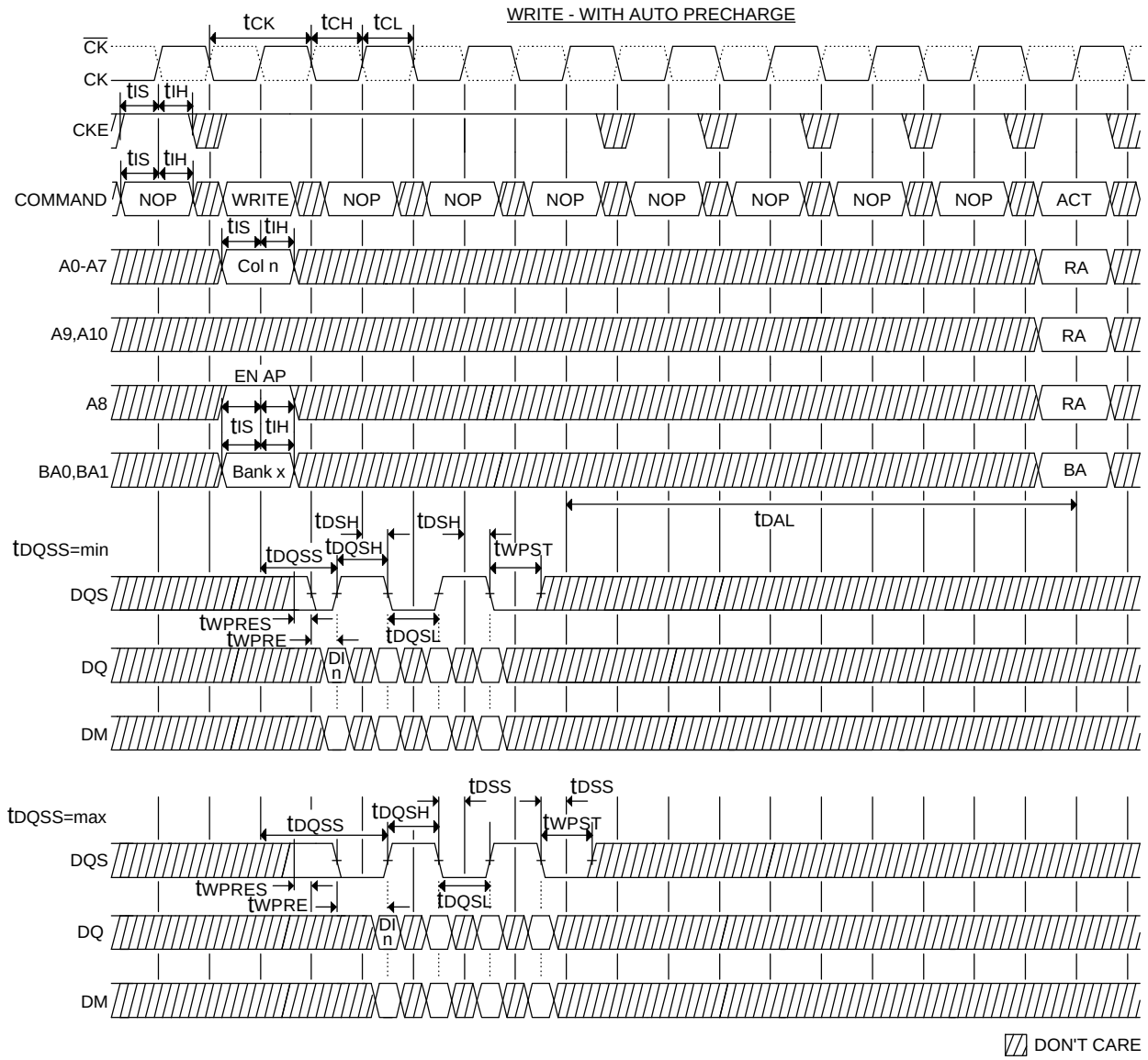
DO n = Data Out from column n
Burst Length = 4
DIS AP = Disable Autoprecharge
* = "Don't Care", if A8 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times
Note that tRCD MIN so that the same timing applies if Autoprecharge is enabled (in which case tRAS would be limiting)

Figure29:WRITE – WITHOUT AUTO PRECHARGE



DI n = Data IN from column n
Burst Length = 4
DIS AP = Disable Autoprecharge
* = "Don't Care", if A8 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times

Figure30:WRITE – WITH AUTO PRECHARGE



DI n = Data IN from column n
Burst Length = 4
EN AP = Disable Autoprecharge
ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times

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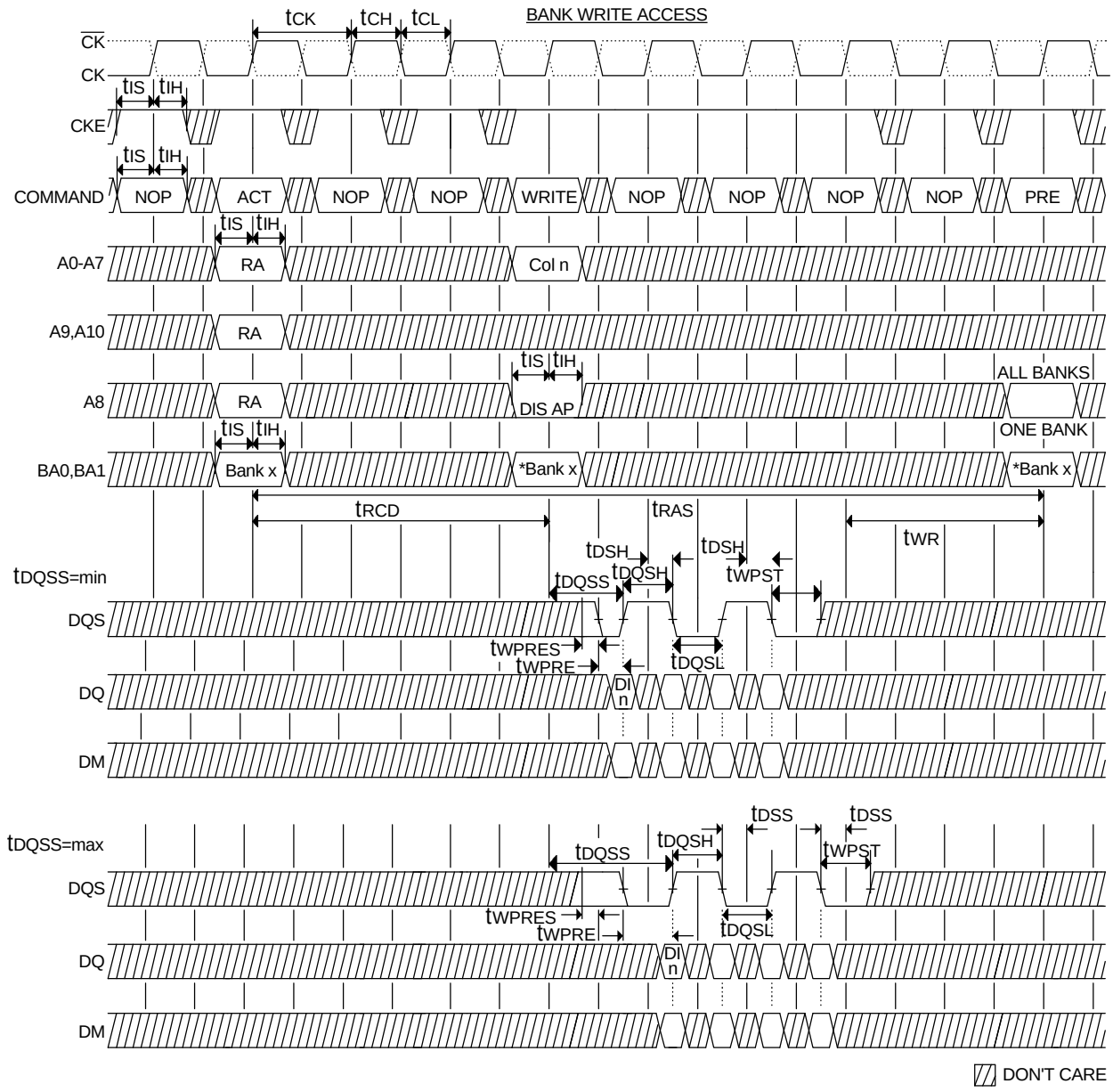
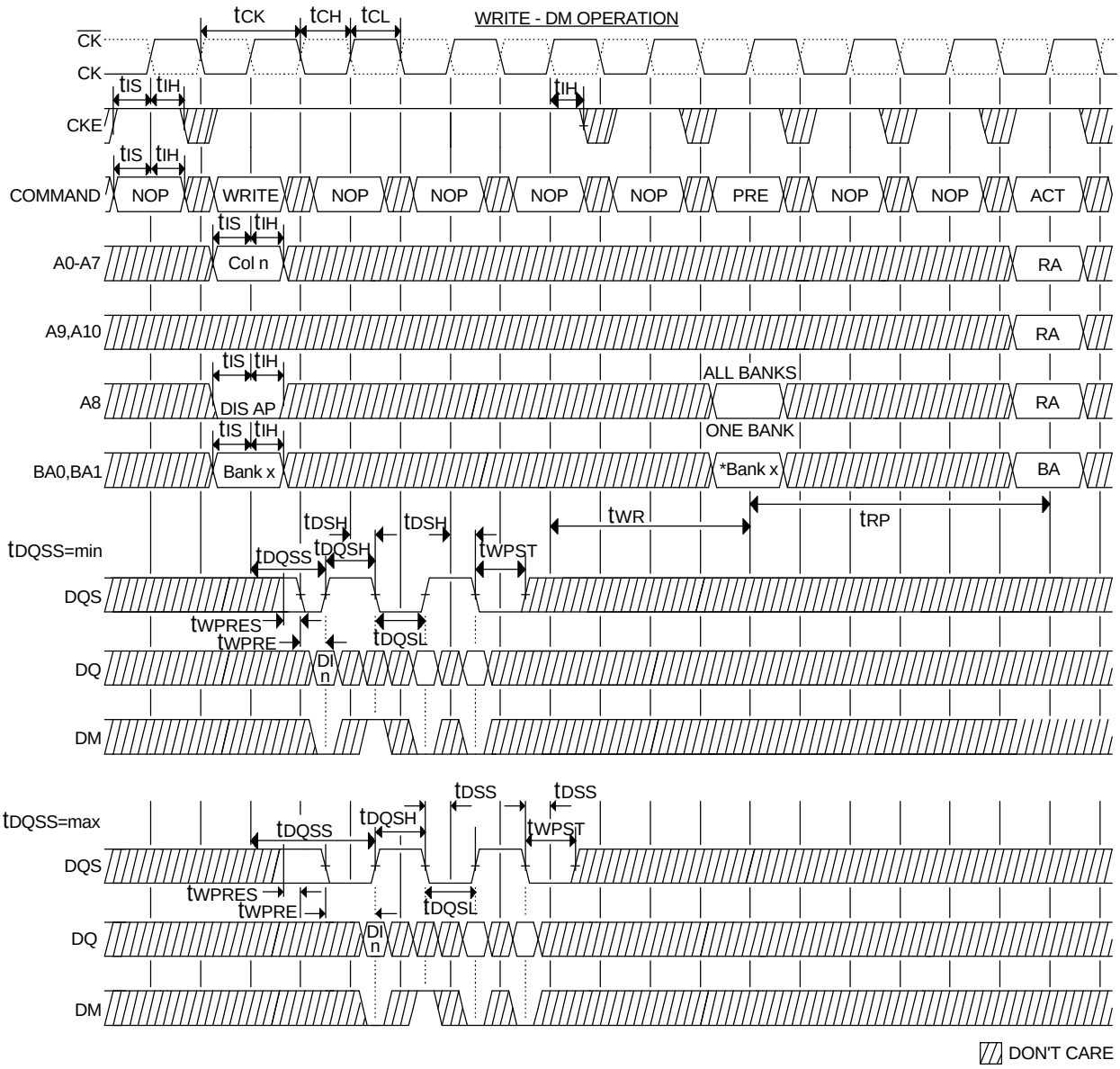
Figure31:BANK WRITE ACCESS



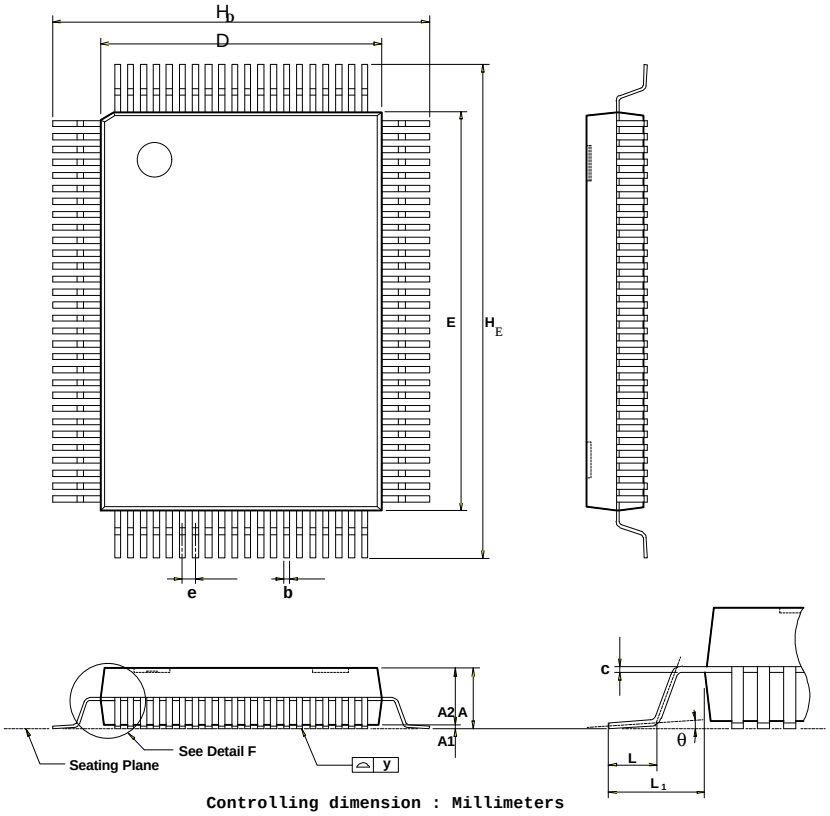
DI n = Data IN from column n
Burst Length = 4
DIS AP = Disable Autoprecharge
* = "Don't Care", if A8 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times

Figure32:WRITE – DM OPERATION



DI n = Data IN from column n
Burst Length = 4
DIS AP = Disable Autoprecharge
* = "Don't Care", if A8 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times

PACKAGE DIMENSIONS



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.009	0.013	0.015	0.22	0.32	0.38
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.783	0.787	0.791	19.90	20.00	20.10
e	0.020	0.026	0.032	0.498	0.65	0.802
H_D	0.626	0.630	0.634	15.90	16.00	16.10
H_E	0.862	0.866	0.870	21.90	22.00	22.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1		0.039			1.00	
y	—	—	0.003	—	—	0.08
θ	0°	—	7 °	0°	—	7 °