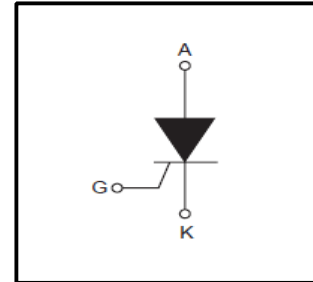


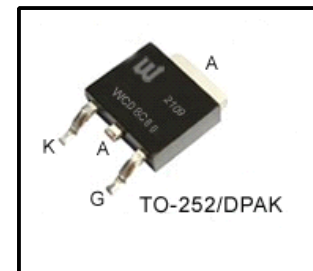
Features

- Repetitive Peak Off-State Voltage:600V
- R.M.S On-State Current ($I_{T(RMS)}$)=8A
- Low On-State Voltage(1.4(Typ.)@ITM)
- Isolation Voltage(V_{ISO} =1500V AC)



General Description

Standard gate triggering SCR is fully isolated package suitable for the application where requiring high bidirectional blocking voltage capability and also suitable for over voltage protection ,motor control circuit in power tool, inrush current limit circuit and heating control system.



Absolute Maximum Ratings ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter		Value	Units
V_{DRM}/V_{RRM}	Repetitive Peak Off-State Voltage (Note(1))		600	V
$I_{T(AV)}$	Average On-State Current(180° Conduction Angle)	$T_J = 85^\circ\text{C}$	5	A
$I_{T(RMS)}$	R.M.S On-State Current(180° Conduction Angle)	$T_J = 85^\circ\text{C}$	8	A
I_{TSM}	Non Repetitive Surge Peak on-state Current	$t_p = 8.3\text{ms}$	73	A
		$t_p = 10\text{ms}$	70	
I^2t	I^2t Value for Fusing	$t_p = 8.3\text{ms}$	24.5	A^2s
di/dt	Critical rate of rise of on-state current $I_{TM} = 2\text{A}; I_G = 10\text{mA}; dI_G/dt = 100\text{A}/\mu\text{s}$	$T_J = 125^\circ\text{C}$	50	$\text{A}/\mu\text{s}$
$P_{G(AV)}$	Average Gate Power Dissipation	$T_J = 125^\circ\text{C}$	1	W
I_{FGM}	Peak Gate Current	$T_J = 125^\circ\text{C}$	4	A
V_{RGM}	Reverse Peak Gate Voltage	$T_J = 125^\circ\text{C}$	5	V
V_{ISO}	Isolation Breakdown voltage(R.M..S)	A.C. 1minute	1500	V
T_J	Junction Temperature		-40~125	$^\circ\text{C}$
T_{STG}	Storage Temperature		-40~150	$^\circ\text{C}$

Note1: Although not recommended, off-state Voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed $15\text{A}/\mu\text{s}$.

Thermal Characteristics

Symbol	Parameter	Value			Units
		Min	Typ	Max	
$R_{\theta Jc}$	Thermal Resistance Junction to Case	-	-	20	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	-	-	70	$^\circ\text{C}/\text{W}$

Electrical Characteristics ($T_J=25^{\circ}\text{C}$, $R_{GK}=1\text{K}\Omega$ unless otherwise specified)

Symbol			Value			Units
			Min	Typ	Max	
$I_{\text{DRM}}/I_{\text{RRM}}$	Off-state leakage current ($V_{\text{AK}}=V_{\text{DRM}}/V_{\text{RRM}}$)	$T_C=25^{\circ}\text{C}$	-	-	5	μA
		$T_C=125^{\circ}\text{C}$			2	mA
V_{TM}	Forward "On" voltage ($I_{\text{TM}}=16\text{A}$ $t_p=380\mu\text{s}$) (Note2.1)		-	1.4	1.6	V
I_{GT}	Gate Trigger Current(continuous dc) ($V_{\text{AK}}=12\text{Vdc}$, $R_L=140\Omega$) (Note2.2)		-	-	15	mA
V_{GT}	Gate Trigger Voltage (continuous dc) ($V_{\text{AK}}=12\text{Vdc}$, $R_L=140\Omega$) (Note2.2)		-	-	1.5	V
V_{GD}	Gate threshold Voltage ($V_D=12V_{\text{DRM}}$ $R_L=3.3\text{K}\Omega$ $R_{GK}=220\Omega$) (Note2.1)		0.1	-	-	V
dv/dt	Critical Rate of Rise Off-State Voltage ($V_D=0.67V_{\text{DRM}}$; $R_{GK}=220\Omega$)	$T_J=125^{\circ}\text{C}$	200	-	-	$\text{V}/\mu\text{s}$
I_{H}	Holding Current($V_D=12\text{V}$; $I_{\text{GT}}=0.5\text{mA}$)		-	-	20	mA
I_{L}	Latching Current($V_D=12\text{V}$; $I_{\text{GT}}=0.5\text{mA}$)		-	2	6	mA
R_d	Dynamic resistance	$T_J=125^{\circ}\text{C}$	-	-	46	$\text{m}\Omega$

*Notes:

2.1 Pulse Width $\leq 1.0\text{ms}$, Duty cycle $\leq 1\%$

2.2 R_{GK} Current is not Included in measurement.

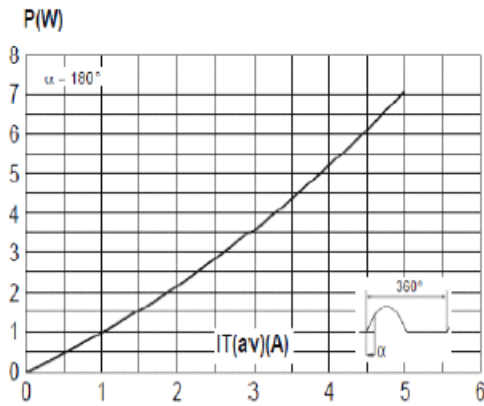


Fig. 1 Maximum average power dissipation versus average on-state current

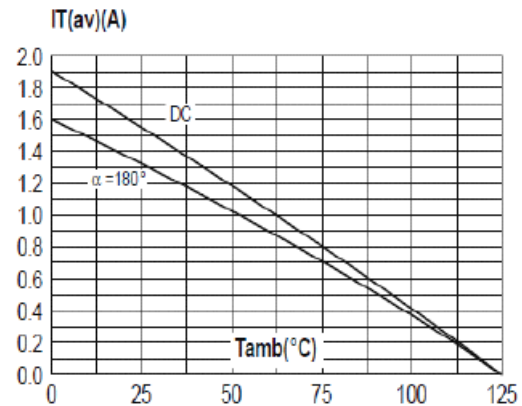


Fig. 2 Average and D.C. on-state current versus ambient temperature (device mounted on FR4 with recommended pad layout)

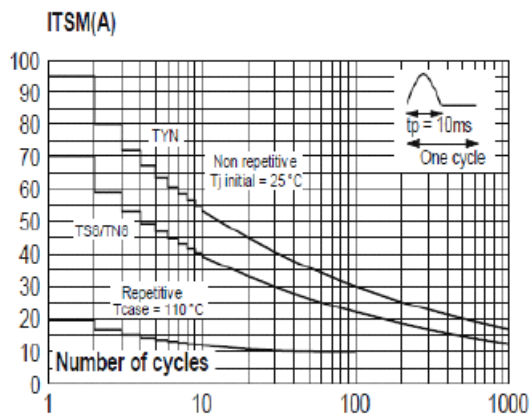


Fig. 3 Surge peak on-state current versus Number of cycles.

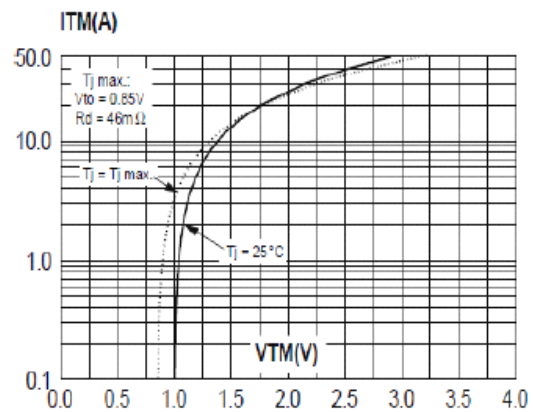


Fig. 4 On-state Characteristics (maximum values)

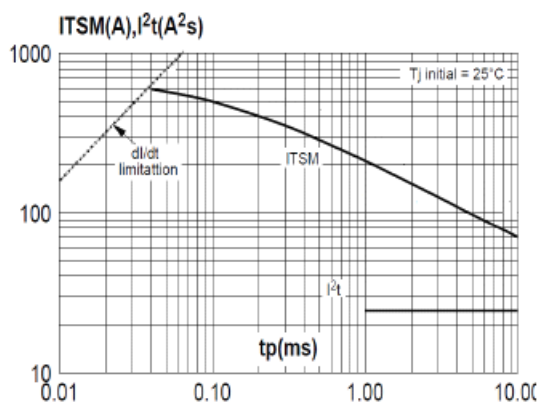


Fig. 5 Non-repetitive surge peak on-state current for a sinusoidal pulse with width $T_p < 10\text{ms}$ and corresponding value of I^2t

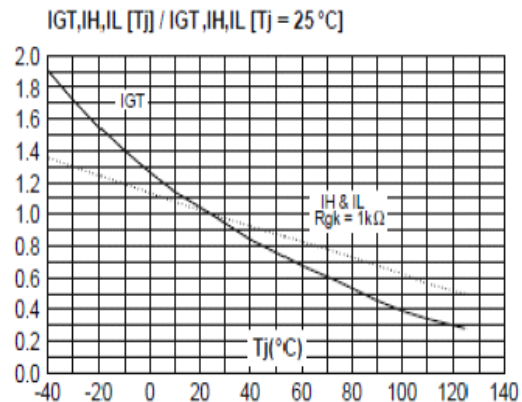


Fig. 6 Relative variation of gate trigger current and holding versus junction temperature

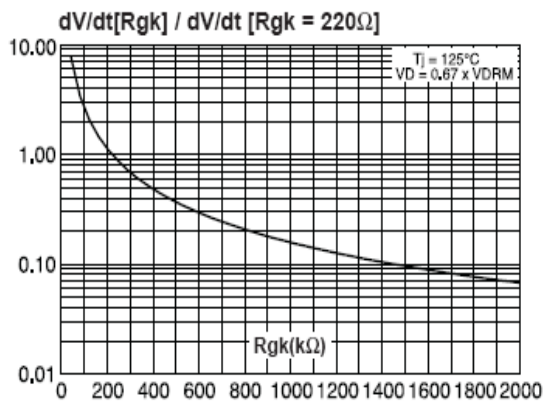


Fig.7 Relative variation of dv/dt immunity versus gate-cathode resistance (typical values)

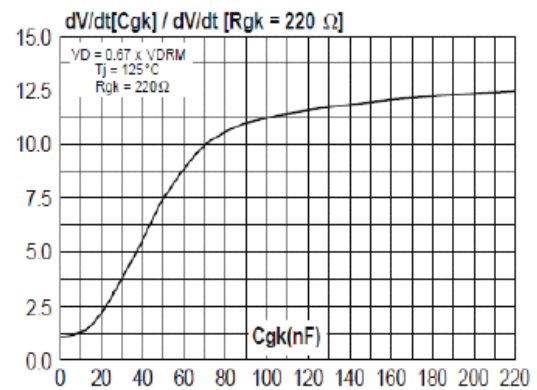


Fig.8 Relative variation of dv/dt immunity versus gate-cathode capacitance (typical values)

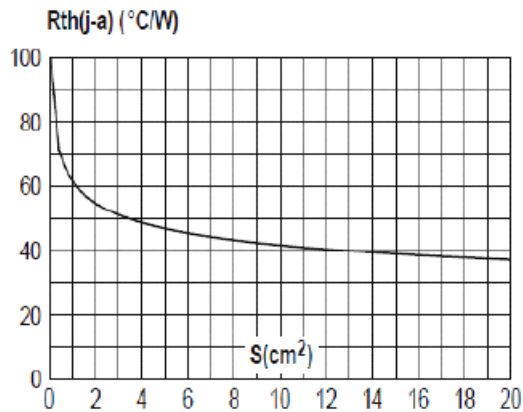


Fig.8 Thermal Resistance junction to ambient Versus copper surface under tab (Epoxy printed Circuit board FR4, copper thickness: 35μm)

TO-252 Package Dimension

Unit: mm

