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WCMA1008C1X

128K x 8 Static RAM

Features

- **Voltage Range**
  - **4.5V–5.5V**
- **Low active power**
  - **Typical active current: 6 mA @ f = f_{max} (70 ns speed)**
- **Low standby current**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE_1}$, CE_2, and $\overline{OE}$ features**
- **CMOS for optimum speed/power**

Functional Description

The WCMA1008C1X is a high-performance CMOS static RAM organized as 128K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE_1}$), an active HIGH Chip Enable (CE_2), an active LOW Output Enable ($\overline{OE}$), and three-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

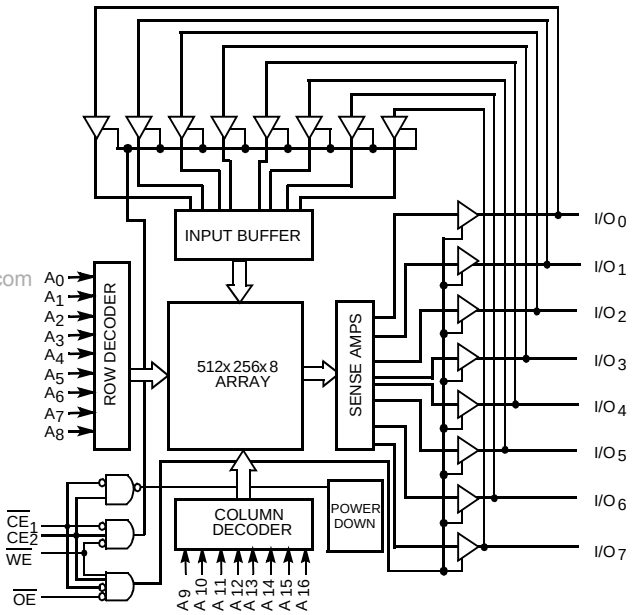
Writing to the device is accomplished by taking Chip Enable 1 ($\overline{CE_1}$) and Write Enable ($\overline{WE}$) inputs LOW and Chip Enable 2 (CE_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable 1 ($\overline{CE_1}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) and Chip Enable 2 (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE_1}$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE_1}$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW)

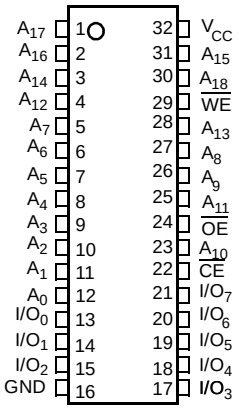
The WCMA1008C1X is available in a standard 32-pin 450-mil-wide body width SOIC and 32-pin TSOP type I.

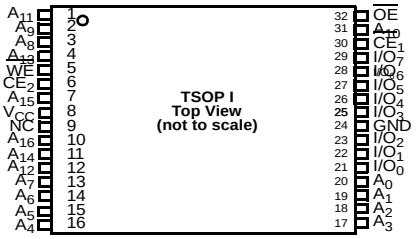
Logic Block Diagram



Pin Configuration

Top View
SOIC





Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{CC} to Relative GND .....–0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1].....–0.5V to V_{CC} +0.5V

DC Input Voltage[1].....–0.5V to V_{CC} +0.5V

Current into Outputs (LOW).....20 mA

Static Discharge Voltage.....2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .....>200 mA

Product Portfolio

Product	V_{CC} Range			Speed	Temp.	Power Dissipation			
						Operating, Icc		Standby (I_{SB2})	
						$f = f_{max}$			
	Min.	Typ.[2]	Max.			Typ.[2]	Max.	Typ.[2]	Max.
WCMA1008C1X	4.5 V	5.0V	5.5V	70 ns	Ind'l	6 mA	15 mA	4 μA	20 μA
				55 ns		7.5 mA	20 mA		

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40°C to +85°C	4.5V–5.5V

Notes:

1. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
2. Typical values are measured at V_{CC} = 5V, T_A = 25°C, and are included for reference only and are not tested or guaranteed.

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Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	WCMA1008C1X-55			WCMA1008C1X-70			Units
			Min.	Typ.[2]	Max.	Min.	Typ.[2]	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 1 mA	2.4			2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA			0.4			0.4	V
V_{IH}	Input HIGH Voltage		2.2		V_{CC} +0.3	2.2		V_{CC} +0.3	V
V_{IL}	Input LOW Voltage		–0.3		0.8	–0.3		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	–1		+1	–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	–1		+1	–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	f=f_{MAX}=1/t_{RC} | I_{OUT} =0 mA V_{CC} = Max.,		7.5	20		6	15	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC},$\overline{CE}_1$≥V_{IH},CE_2<V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		0.1	2		0.1	1	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} – 0.3V,CE_2 <0.3 V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f =0		2.5	15			15	µA

Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	9	pF
C_{OUT}	Output Capacitance		9	pF

AC Test Loads and Waveforms

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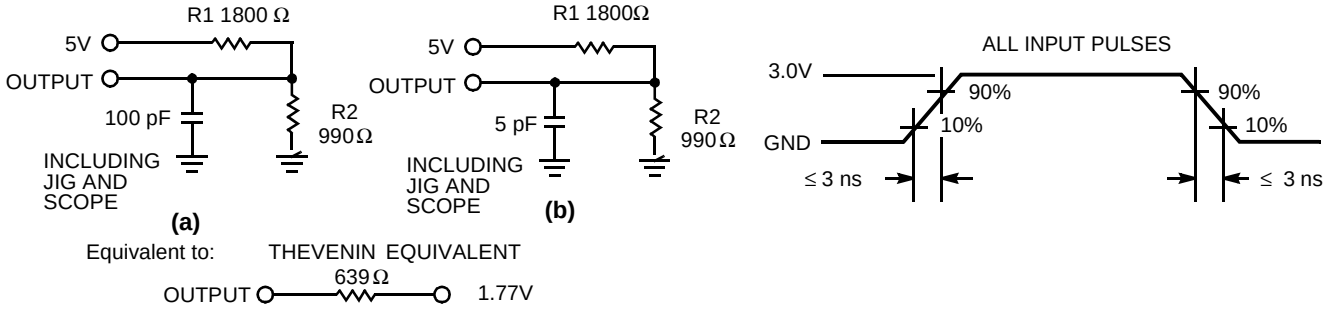

Note:

3. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics[4] Over the Operating Range

Parameter	Description	55		70		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	5		5		ns
t_{ACE}	$\overline{CE}_1$ LOW to Data Valid, CE_2 HIGH to Data Valid		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		20		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[5]	0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[5, 6]		20		25	ns
t_{LZCE}	$\overline{CE}_1$ LOW to Low Z, CE_2 HIGH to Low Z[5]	5		5		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z, CE_2 LOW to High Z[5, 6]		20		25	ns
t_{PU}	$\overline{CE}_1$ LOW to Power-Up, CE_2 HIGH to Power-Up	0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down, CE_2 LOW to Power-Down		55		70	ns
WRITE CYCLE[7]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	$\overline{CE}_1$ LOW to Write End, CE_2 HIGH to Write End	45		60		ns
t_{AW}	Address Set-Up to Write End	45		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	45		50		ns
t_{SD}	Data Set-Up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[5, 6]	5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]		20		25	ns

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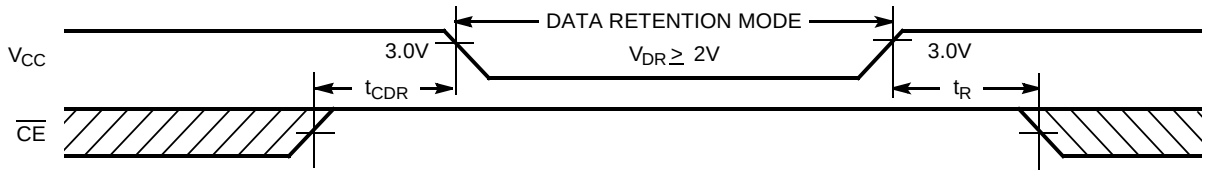
Notes:

4. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
5. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
7. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW and CE_2 HIGH, and $\overline{WE}$ LOW. $\overline{CE}_1$ and $\overline{WE}$ must be LOW and CE_2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ.[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		2.0			V
I_{CCDR}	Data Retention Current	$\overline{V_{CC}} = V_{DR} = 3.0V$, $\overline{CE_1} \geq V_{CC} - 0.3V$, $CE_2 < 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or, $V_{IN} \leq 0.3V$		1.5	20	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time		0			ns
t_R[8]	Operation Recovery Time		70			ns

Data Retention Waveform



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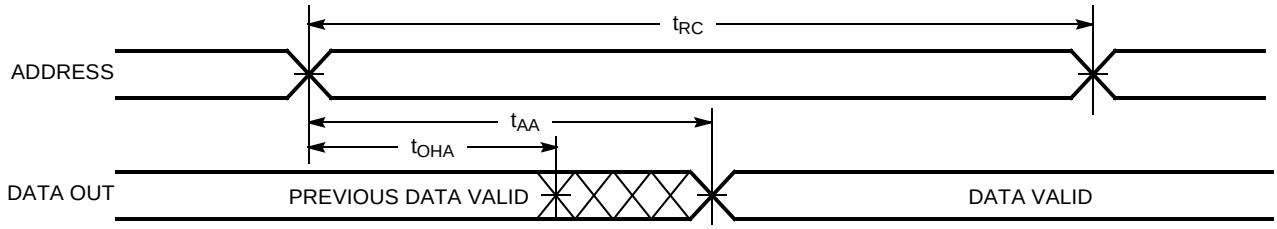
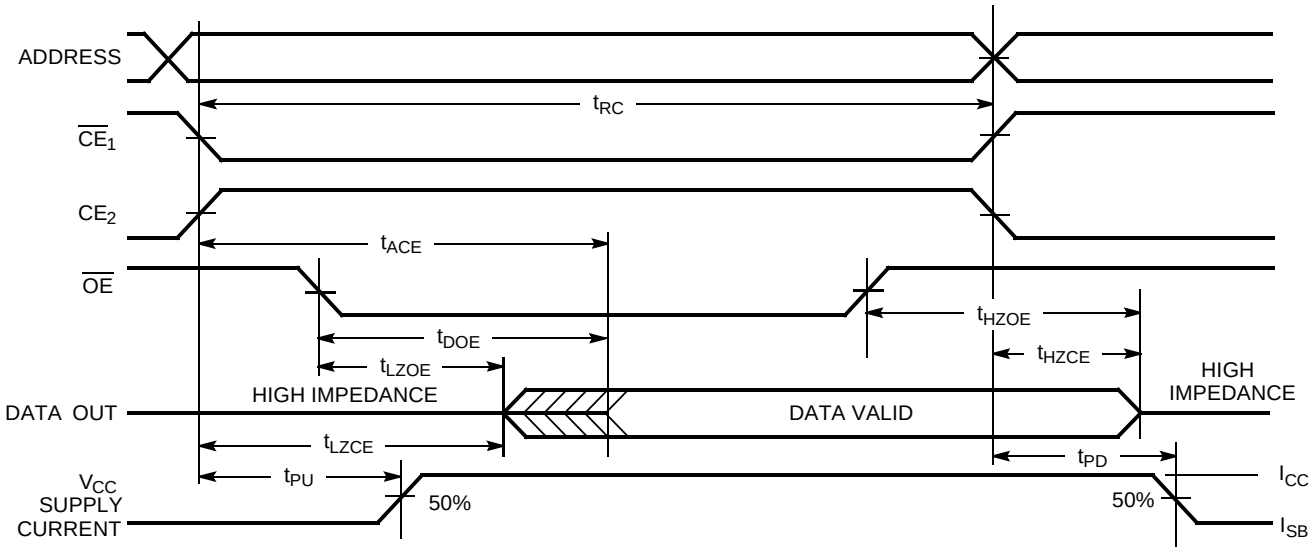
Switching Waveforms

Read Cycle No.1[9, 10]



Read Cycle No. 2 ($\overline{OE}$ Controlled)[10, 11]



Notes:

8. Full Device operatin requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100\ \mu s$ or stable at $V_{cc(min)} \geq 100\ \mu s$.
9. Device is continuously selected. $\overline{OE}$, $\overline{CE_1} = V_{IL}$, $CE_2 = V_{IH}$
10. $\overline{WE}$ is HIGH for read cycle.
11. Address valid prior to or coincident with $\overline{CE_1}$ transition LOW and CE_2 transition HIGH.

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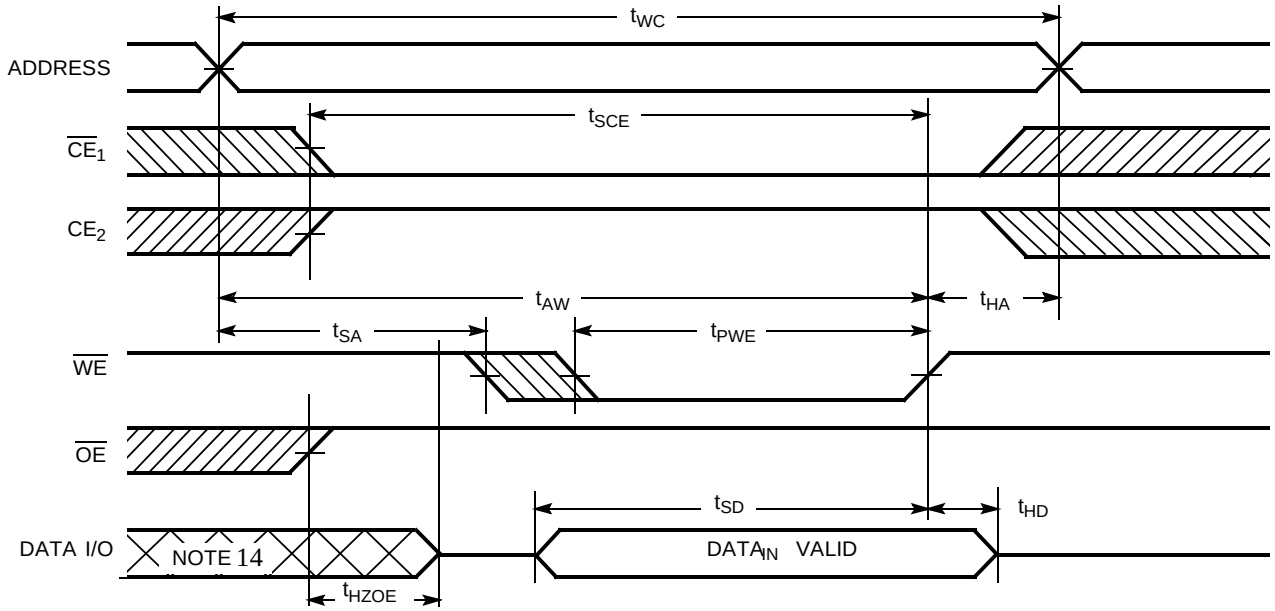
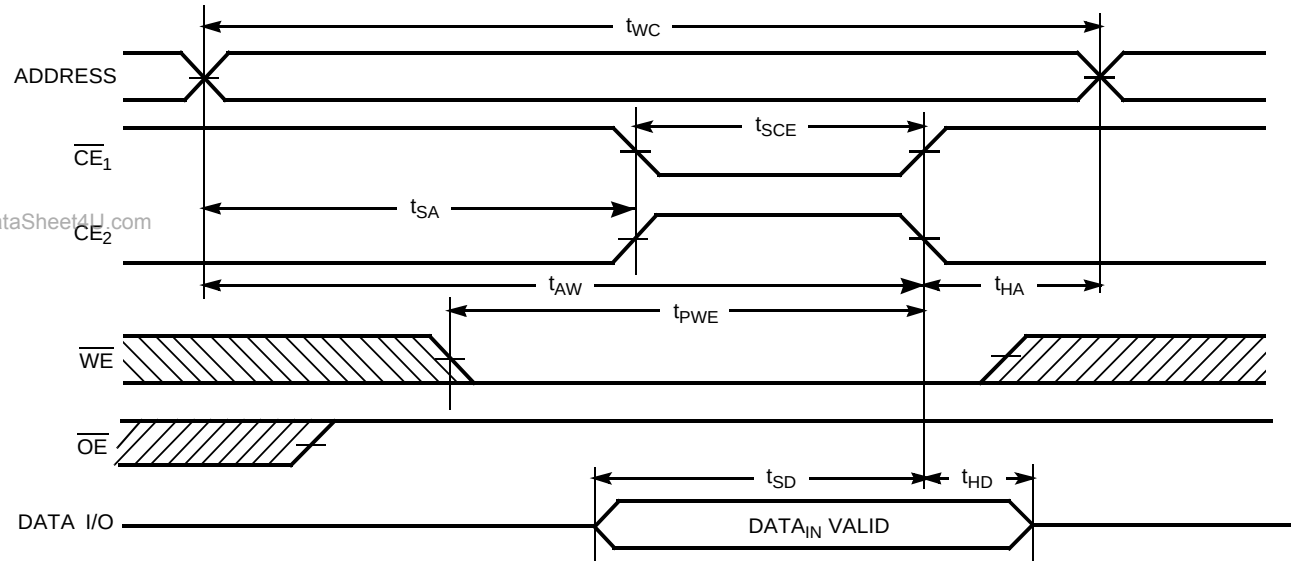
Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{WE}$ Controlled)[7. 12, 13]



Write Cycle No. 2 ($\overline{CE_1}$ or CE_2 Controlled)[7, 12, 13]



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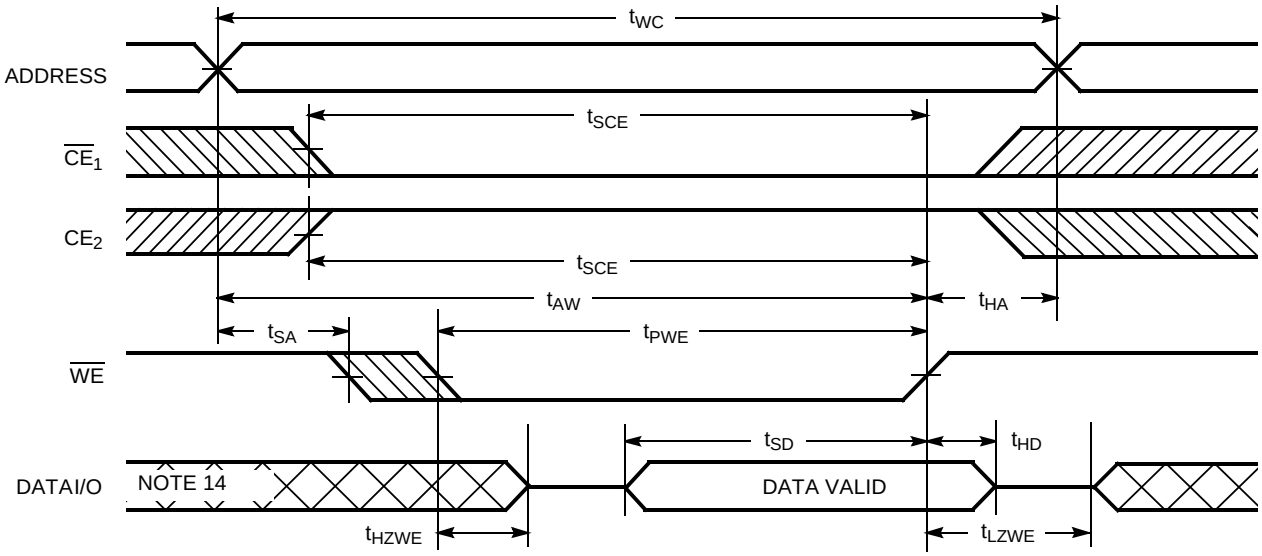
Notes:
12. If $\overline{CE_1}$ goes HIGH and CE_2 LOW simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
13. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
14. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No.3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[12]



Truth Table

$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	$I/O_0 - I/O_7$	Mode	Power
H	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	L	X	X	High Z	Power-Down	Standby (I_{SB})
L	H	L	H	Data Out	Read	Active (I_{CC})
L	H	X	L	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

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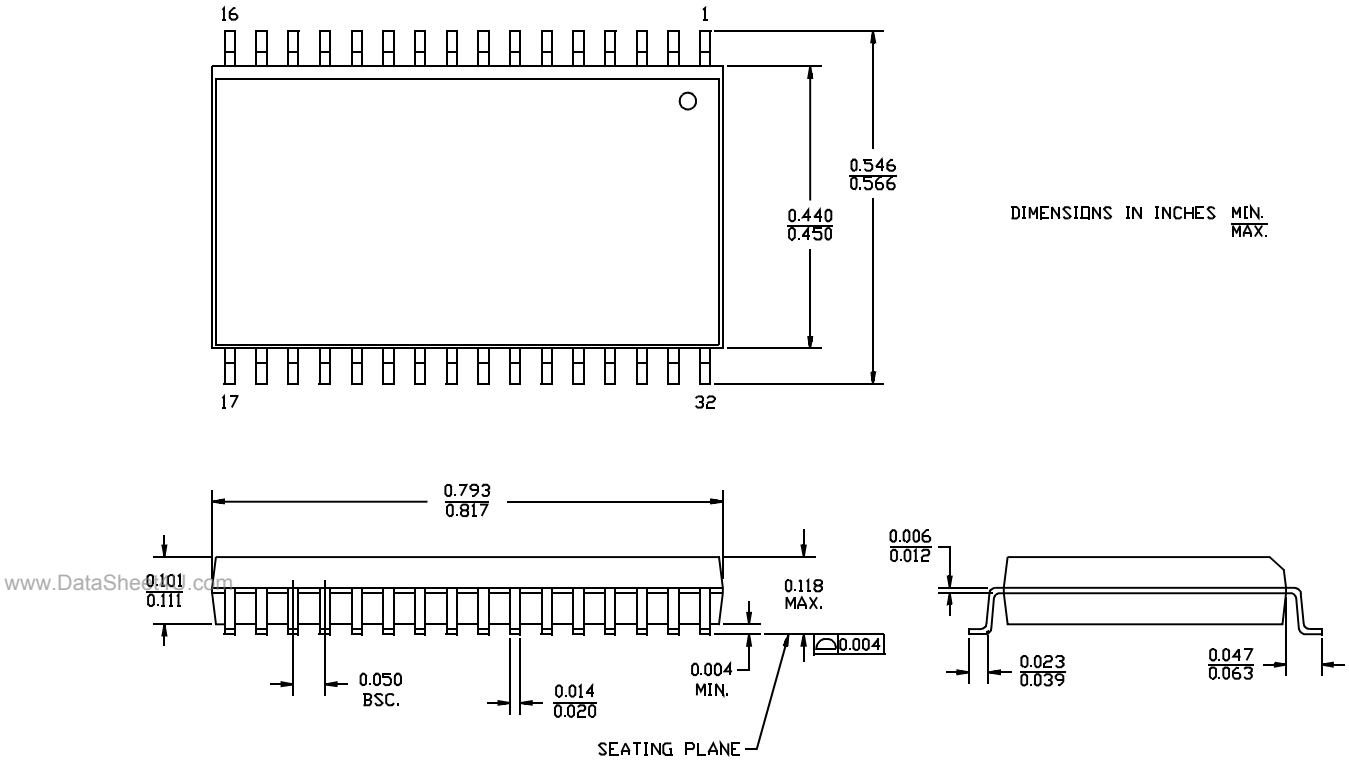
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	WCMA1008C1X-GF70	G32	32-Lead (450-Mil) Molded SOIC	Industrial
	WCMA1008C1X-TF70	T32	32-Lead TSOP	
55	WCMA1008C1X-GF55	G32	32-Lead (450-Mil) Molded SOIC	
	WCMA1008C1X-TF55	T32	32-Lead TSOP	

Package Diagrams

32-Lead (450 MIL) Molded SOIC, G32



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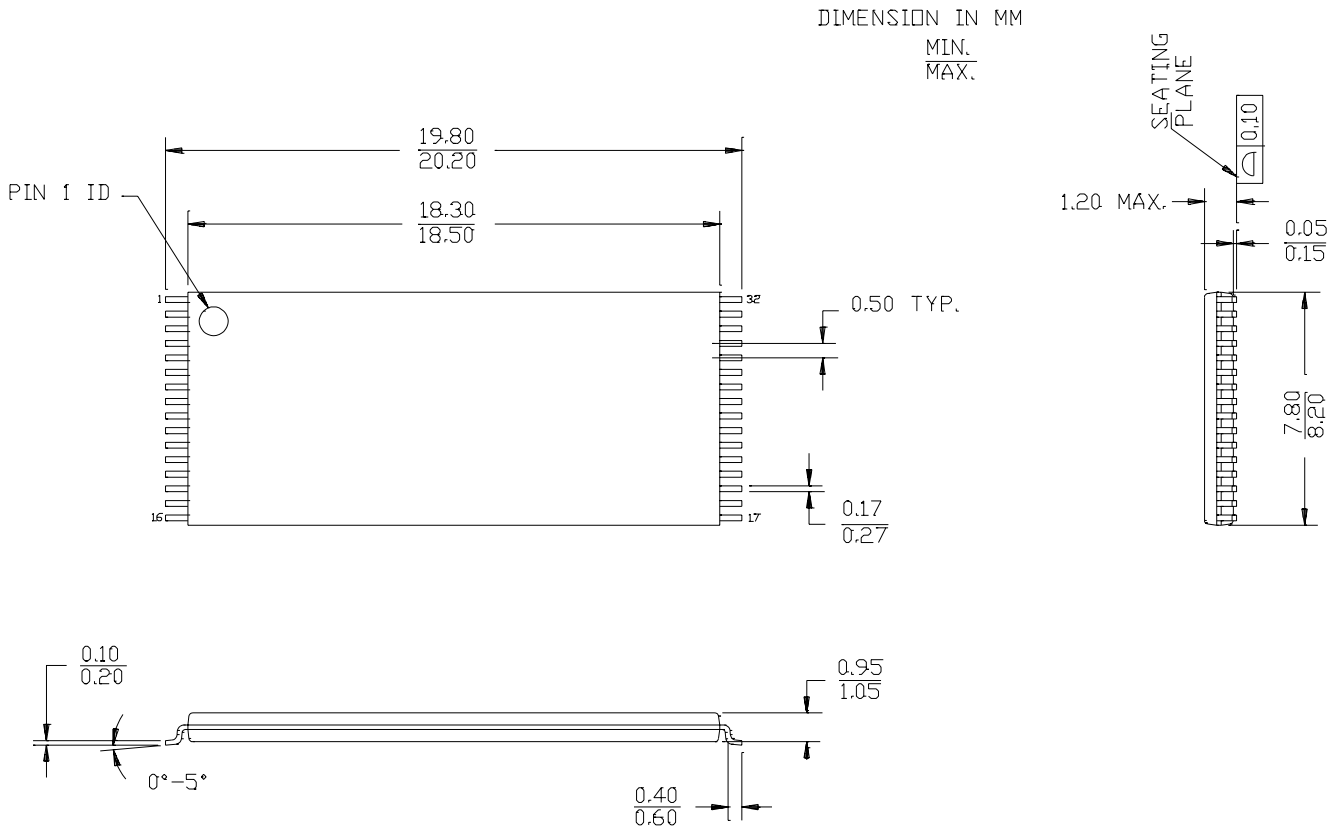
Package Diagrams (continued)

32-Lead Thin Small Outline Package T32



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Document Title: WCMA1008C1X, 128K x 8 Static RAM					
REV.	**Spec #**	**ECN #**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	38-14022	115241	4/24/2002	MGN	New Datasheet

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