

WCMA1016U4X

64K x 16 Static RAM

Features

- High Speed
 - 55ns and 70ns availability
- Low voltage range
 - 2.7V–3.6V
- Ultra-low active power
- Low standby power
- Easy memory expansion with \overline{CE} and \overline{OE} features
- Automatic power-down when deselected
- CMOS for optimum speed/power

Functional Description

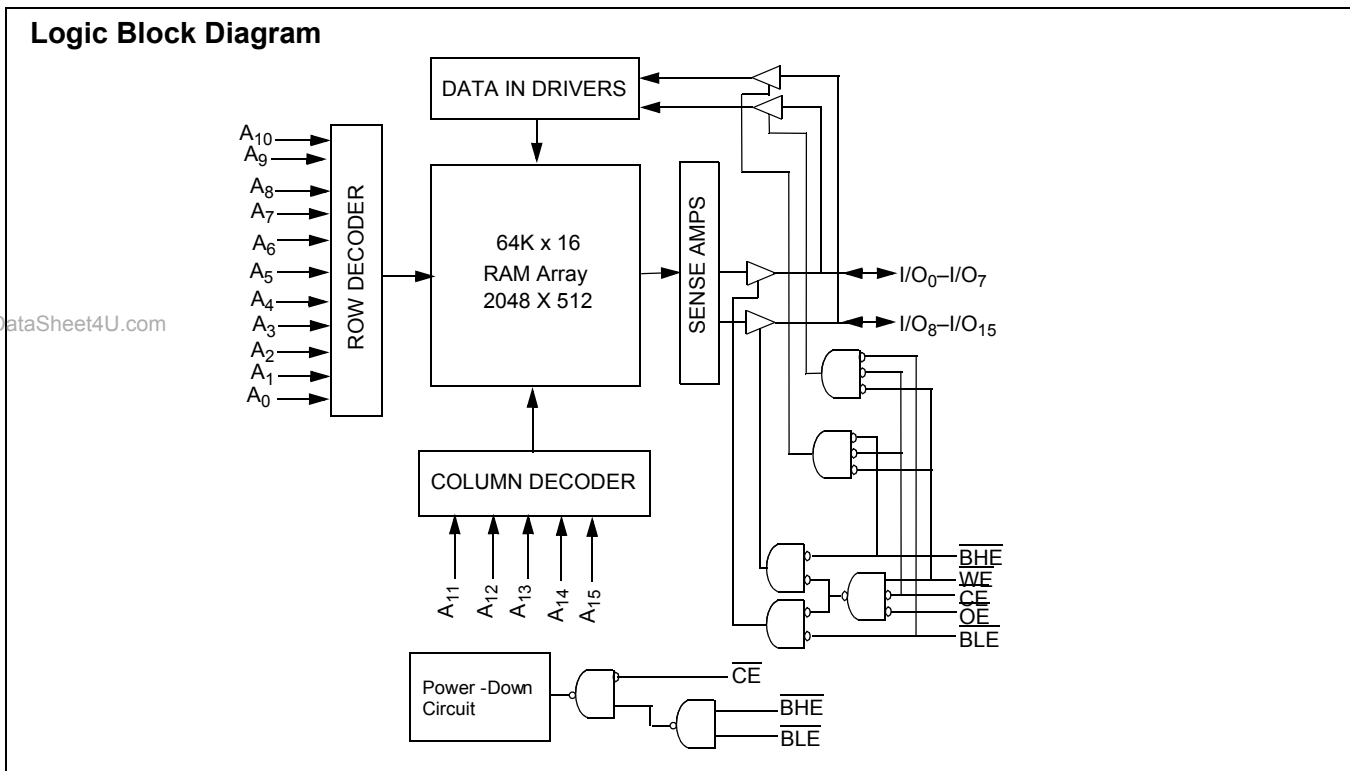
The WCMA1016U4X is a high-performance CMOS static RAM organized as 64K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This device is ideal for portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected (\overline{CE} HIGH or both BLE

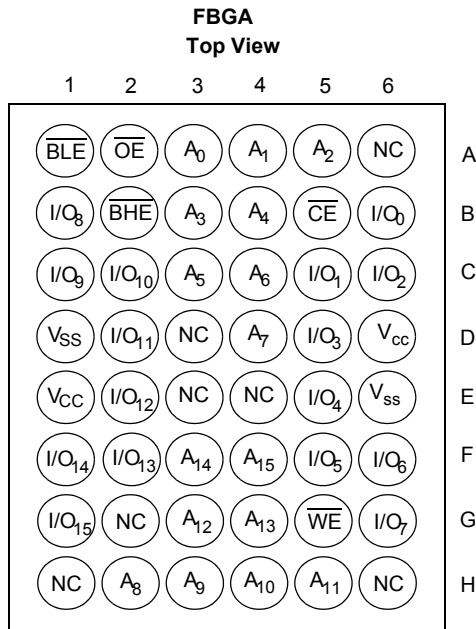
and \overline{BHE} are HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected (\overline{CE} HIGH), outputs are disabled (\overline{OE} HIGH), both Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , BLE HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{15}).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7 . If Byte High Enable (\overline{BHE}) is LOW, then data from memory will appear on I/O_8 to I/O_{15} . See the Truth Table at the back of this data sheet for a complete description of read and write modes.

The WCMA1016U4X is available in a 48-ball FBGA package.



Pin Configuration^[1]

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied.....	-55°C to +125°C
Supply Voltage to Ground Potential	-0.5V to +4.6V

DC Voltage Applied to Outputs

in High Z State ^[2]	-0.5V to V _{CC} + 0.5V
DC Input Voltage ^[2]	-0.5V to V _{CC} + 0.5V
Output Current into Outputs (LOW).....	20 mA
Static Discharge Voltage.....	>2001V (per MIL-STD-883, Method 3015)
Latch-Up Current.....	>200 mA

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Operating Range

Device	Range	Ambient Temperature	V _{CC}
WCMA1016U4X	Industrial	-40°C to +85°C	2.7V to 3.6V

Product Portfolio

Product	V _{CC} Range			Speed	Power Dissipation (Industrial)	
	V _{CC} (min.)	V _{CC} (typ.) ^[3]	V _{CC} (max.)		Operating, I _{CC} (f=f _{max})	Standby (I _{SB2})
					Max.	Max.
WCMA1016U4X	2.7V	3.0V	3.6V	70 ns	15 mA	15 μA
				55 ns	20 mA	

Notes:

1. NC pins are not connected to the die.
2. V_{IL}(min) = -2.0V for pulse durations less than 20 ns.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC}(typ), T_A = 25°C.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	WCMA1016U4X-70/55			Unit
			Min.	Typ. ^[3]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA V _{CC} = 2.7V	2.2			V
V _{OL}	Output LOW Voltage	I _{OL} = 2.1 mA V _{CC} = 2.7V			0.4	V
V _{IH}	Input HIGH Voltage		2.0		V _{CC} + 0.3V	V
V _{IL}	Input LOW Voltage		-0.3		0.4	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC} V _{CC} = 3.6V I _{OUT} = 0 mA CMOS levels	70ns		15	mA
			55ns		20	
I _{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V _{CC} , $\overline{CE} \geq V_{IH}$ V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}			2	μA
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$ V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = 0		0.5	15	

Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = V _{CC(typ)}	6	pF
C _{OUT}	Output Capacitance		8	pF

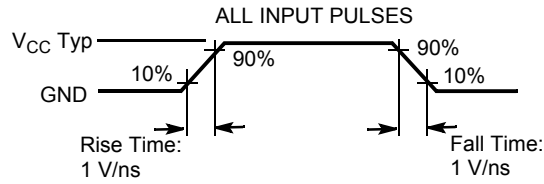
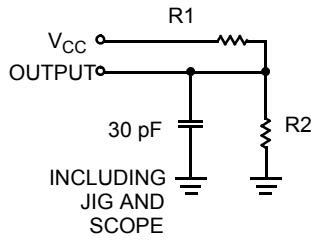
Thermal Resistance

Description	Test Conditions	Symbol	BGA	Units
Thermal Resistance (Junction to Ambient) ^[4]	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	θ _{JA}	55	°C/W
Thermal Resistance (Junction to Case) ^[4]		θ _{JC}	16	°C/W

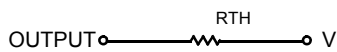
Note:

4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

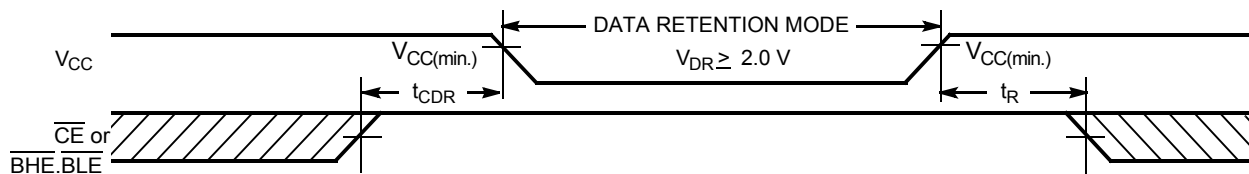


Parameters	3.3V	UNIT
R1	1213	Ohms
R2	1378	Ohms
R _{TH}	645	Ohms
V _{TH}	1.75	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. ^[3]	Max.	Unit
V _{DR}	V _{CC} for Data Retention		2.0		3.6	V
I _{CCDR}	Data Retention Current	V _{CC} = 2.0V CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		0.5	15	μA
t _{CDR} ^[4]	Chip Deselect to Data Retention Time		0			ns
t _R ^[5]	Operation Recovery Time		t _{RC}			ns

Data Retention Waveform^[6]



Notes:

- Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min)} ≥ 100 μs or stable at V_{CC(min)} ≥ 100 μs.
- BHE.BLE is the AND of both BHE and BLE. Chip can be deselected by either disabling the chip enable signals or by disabling both BHE and BLE.

Switching Characteristics Over the Operating Range^[7]

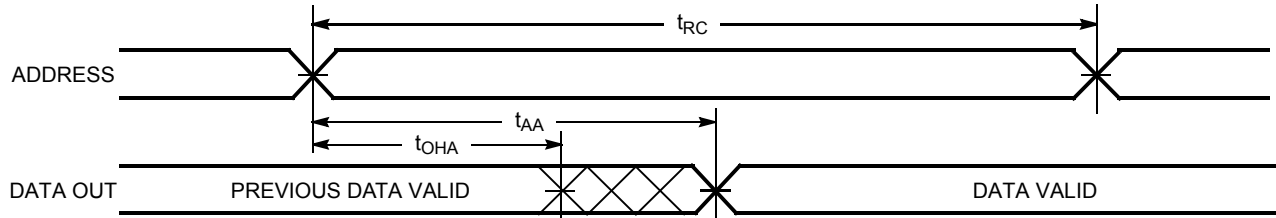
Parameter	Description	WCMA1016U4X-55		WCMA1016U4X-70		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t _{RC}	Read Cycle Time	55		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	10		10		ns
t _{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		55		70	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		25		35	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low Z ^[8]	5		5		ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High Z ^[8, 9]		20		25	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to Low Z ^[8]	10		10		ns
t _{HZCE}	$\overline{\text{CE}}$ HIGH to High Z ^[8, 9]		20		25	ns
t _{PU}	$\overline{\text{CE}}$ LOW to Power-Up	0		0		ns
t _{PD}	$\overline{\text{CE}}$ HIGH to Power-Down		55		70	ns
t _{DBE}	$\overline{\text{BLE}} / \overline{\text{BHE}}$ LOW to Data Valid		55		70	ns
t _{LZBE}	$\overline{\text{BLE}} / \overline{\text{BHE}}$ LOW to Low Z ^[8]	5		5		ns
t _{HZBE}	$\overline{\text{BLE}} / \overline{\text{BHE}}$ HIGH to High Z ^[8, 9]		20		25	ns
WRITE CYCLE^[10]						
t _{WC}	Write Cycle Time	55		70		ns
t _{SCE}	$\overline{\text{CE}}$ LOW to Write End	45		60		ns
t _{AW}	Address Set-Up to Write End	45		60		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width	40		50		ns
t _{BW}	$\overline{\text{BLE}} / \overline{\text{BHE}}$ LOW to Write End	45		60		ns
t _{SD}	Data Set-Up to Write End	25		30		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High Z ^[8, 9]		25		25	ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z ^[8]	5		5		ns

Note:

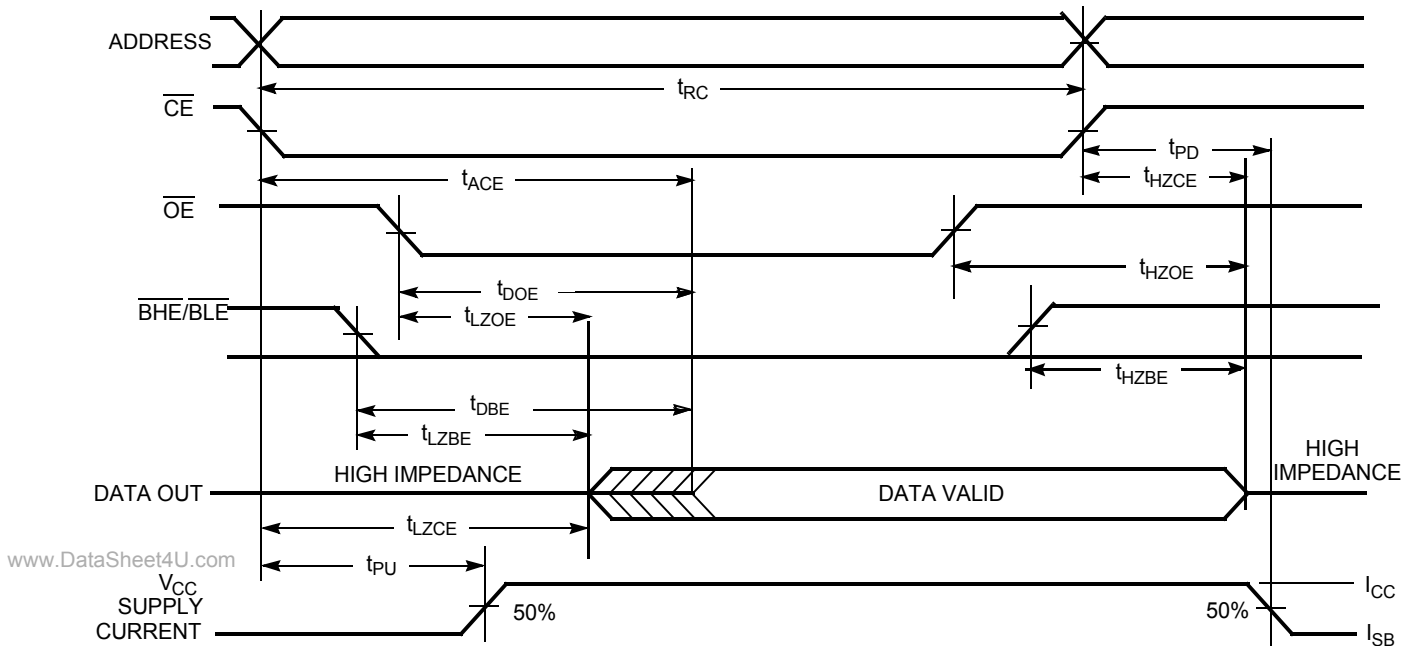
7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. t_{HZOE}, t_{HZCE}, t_{HZBE} and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
10. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}}$, $\overline{\text{CE}} = V_{IL}$, $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled) [11, 12]



Read Cycle No. 2 (\overline{OE} Controlled) [12, 13]

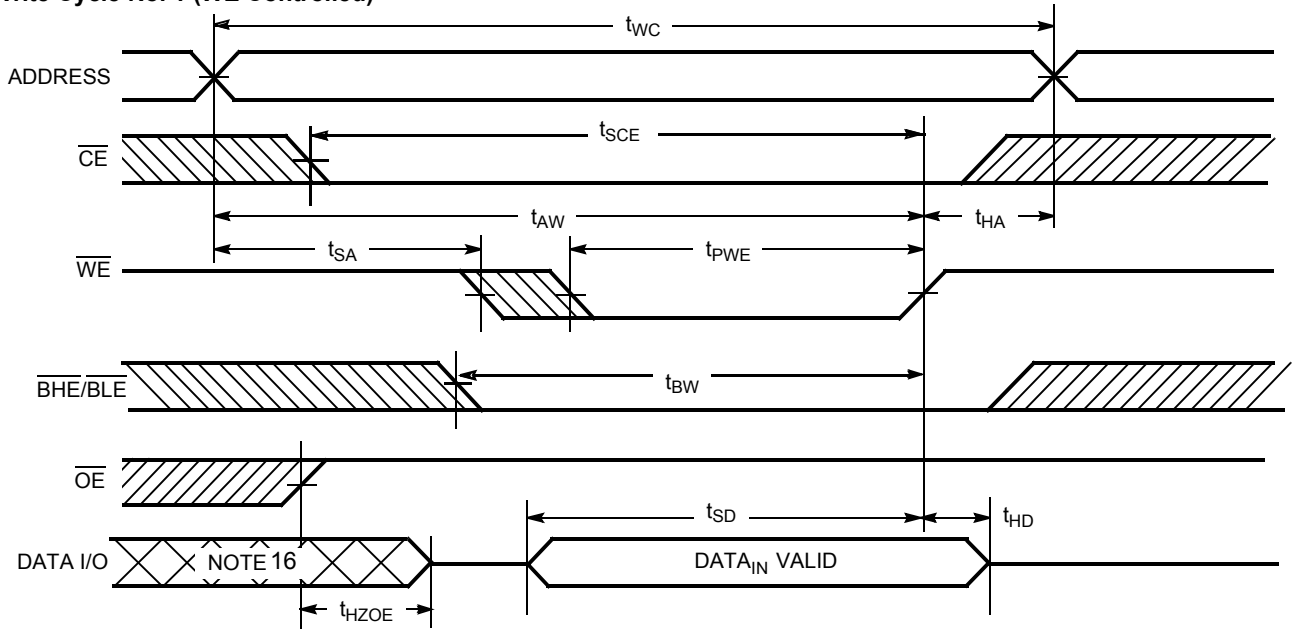


Notes:

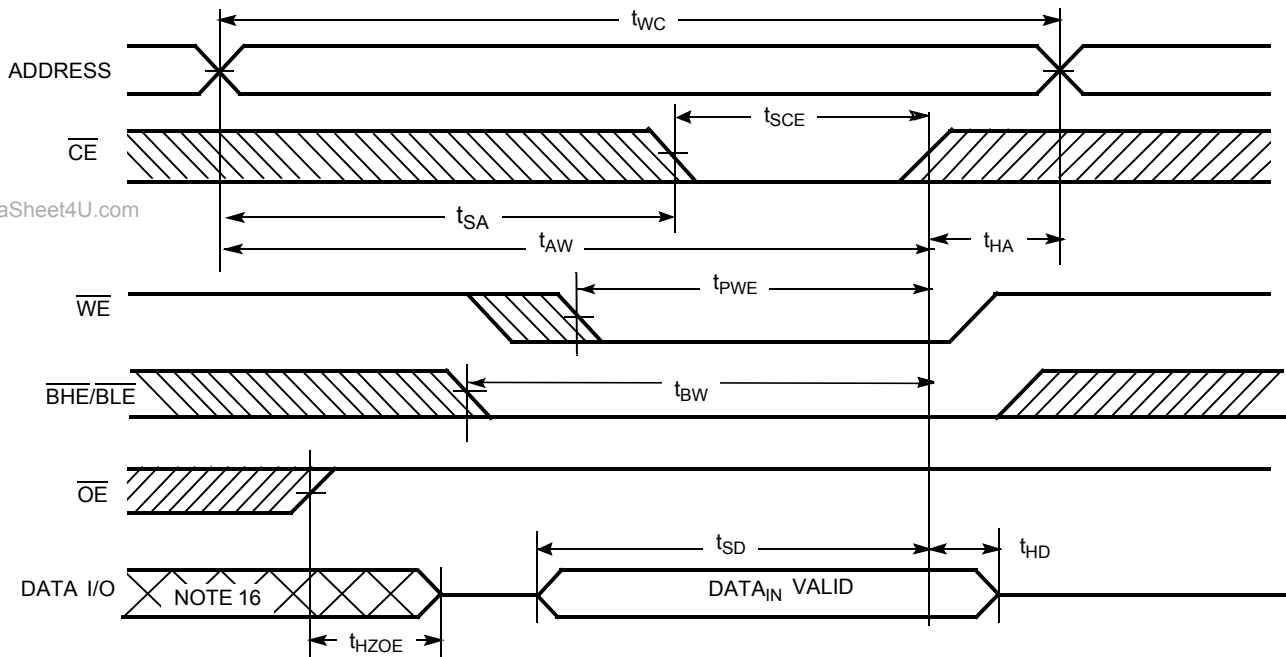
11. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$.
12. WE is HIGH for read cycle.
13. Address valid prior to or coincident with \overline{CE} , \overline{BHE} , \overline{BLE} , transition LOW.

Switching Waveforms

Write Cycle No. 1 (\overline{WE} Controlled) [10, 14, 15]



Write Cycle No. 2 (\overline{CE} Controlled) [10, 14, 15]

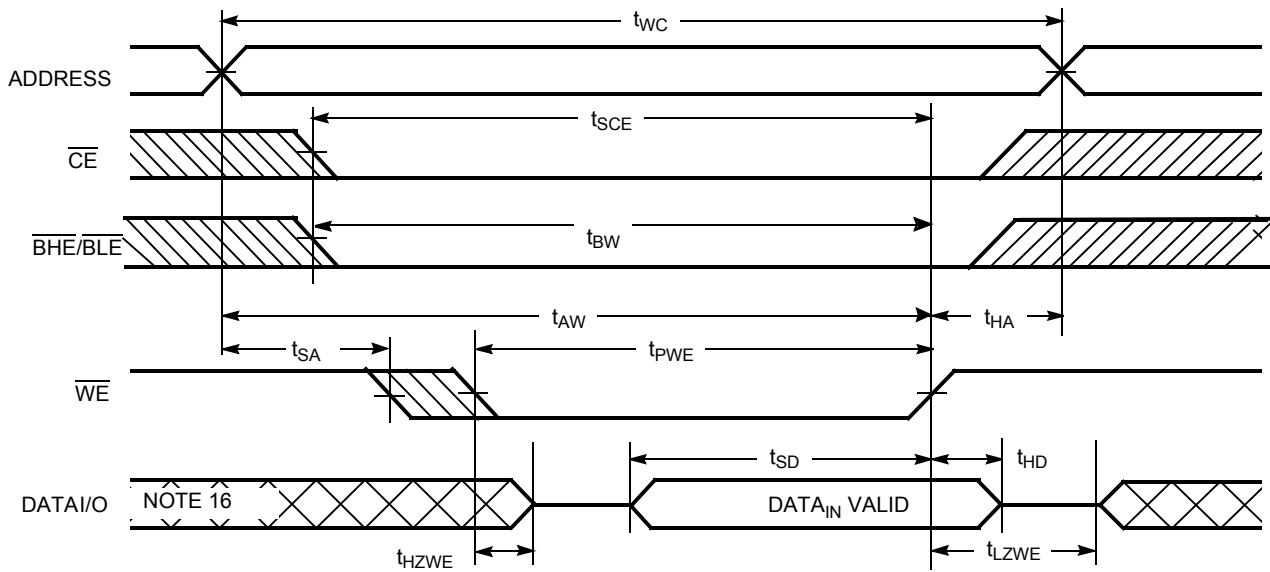


Note:

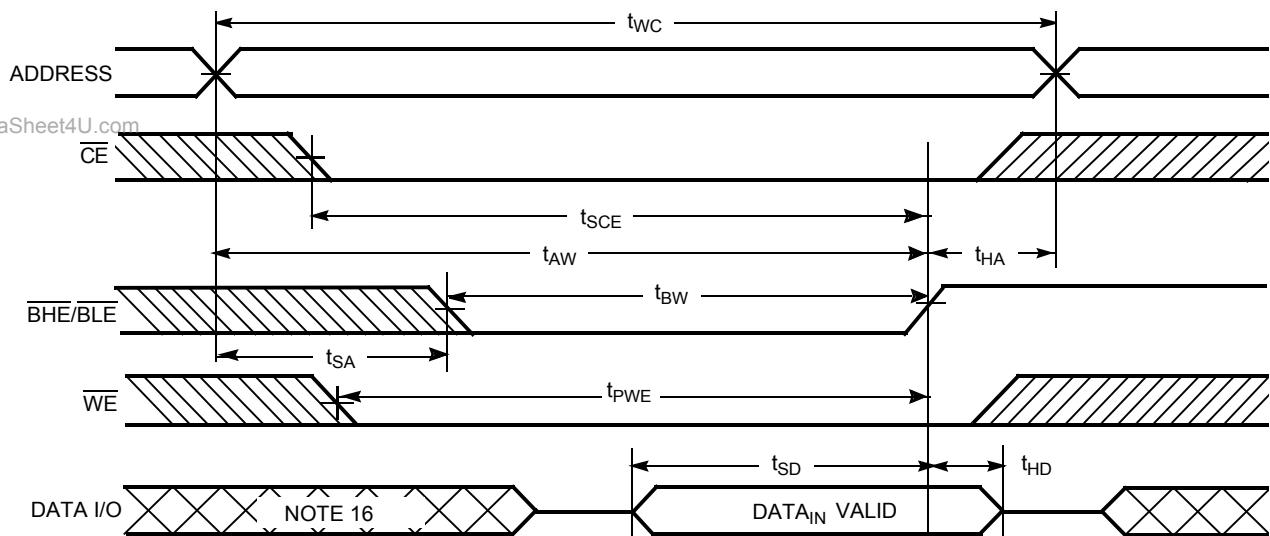
- 14. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 15. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
- 16. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[15]



Write Cycle No. 4 ($\overline{BHE}/\overline{BLE}$ Controlled, \overline{OE} LOW)^[15]





WCMA1016U4X

Truth Table

CE	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby (I _{SB})
X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I _{SB})
L	H	L	L	L	Data Out (I/O ₀ -I/O ₁₅)	Read	Active (I _{CC})
L	H	L	H	L	Data Out (I/O ₀ -I/O ₇); I/O ₈ -I/O ₁₅ in High Z	Read	Active (I _{CC})
L	H	L	L	H	Data Out (I/O ₈ -I/O ₁₅); I/O ₀ -I/O ₇ in High Z	Read	Active (I _{CC})
L	H	H	L	L	High Z	Output Disabled	Active (I _{CC})
L	H	H	H	L	High Z	Output Disabled	Active (I _{CC})
L	H	H	L	H	High Z	Output Disabled	Active (I _{CC})
L	L	X	L	L	Data In (I/O ₀ -I/O ₁₅)	Write	Active (I _{CC})
L	L	X	H	L	Data In (I/O ₀ -I/O ₇); I/O ₈ -I/O ₁₅ in High Z	Write	Active (I _{CC})
L	L	X	L	H	Data In (I/O ₈ -I/O ₁₅); I/O ₀ -I/O ₇ in High Z	Write	Active (I _{CC})

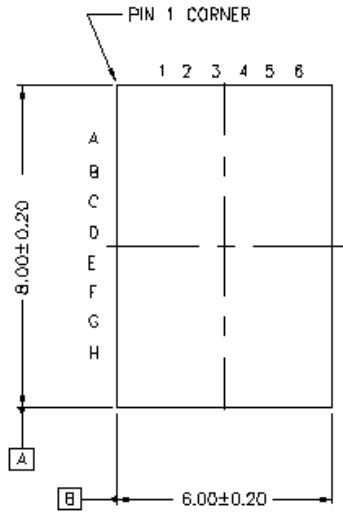
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	WCMA1016U4X-FF70	FB48A	48-Ball Fine Pitch BGA	Industrial
55	WCMA1016U4X-FF55			

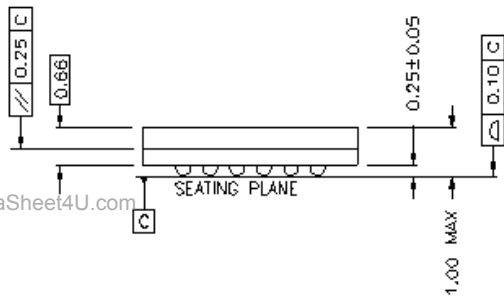
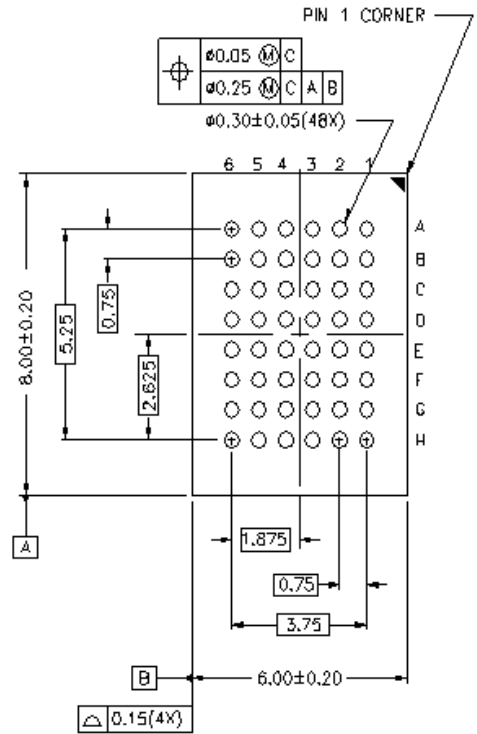
Package Diagrams

48-Ball (6.0 mm x 8.0 mm x 1.0 mm) Fine Pitch BGA, FB48A

Top View



Bottom View





WCMA1016U4X

Document Title: WCMA1016U4X, 64K x 16 Static RAM					
REV.	Spec #	ECN #	Issue Date	Orig. of Change	Description of Change
**	38-14024	115247	1/17/02	MGN	New Data Sheet