

WCMA2008U1B

256K x 8 Static RAM

Features

- **High Speed**
— 70ns availability
- **Voltage range**
— 2.7V–3.3V
- **Ultra low active power**
— Typical active current: 1 mA @ f = 1MHz
— Typical active current: 7 mA @ f = f_{max} (70ns speed)
- **Low standby power**
- **Easy memory expansion with \overline{CE}_1 , \overline{CE}_2 , and \overline{OE} features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

Functional Description

The WCMA2008U1B is a high-performance CMOS static RAM organized as 256K words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This device is ideal for portable applications. The device also has an automatic power-down feature that significantly

reduces power consumption by 80% when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected (\overline{CE}_1 HIGH or \overline{CE}_2 LOW).

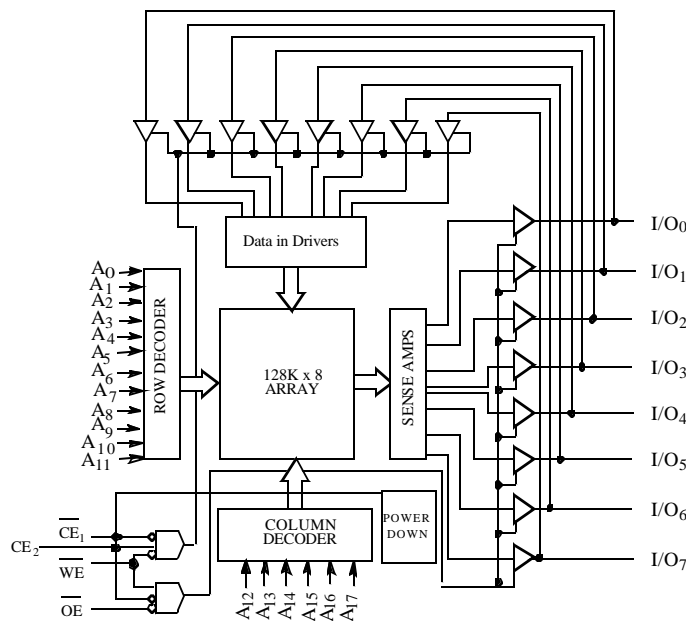
Writing to the device is accomplished by taking Chip Enable (\overline{CE}_1) and Write Enable (WE) inputs LOW and Chip Enable 2 (\overline{CE}_2) HIGH. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₁₇).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}_1) and Output Enable (\overline{OE}) LOW while forcing Write Enable (WE) and Chip Enable 2 (\overline{CE}_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

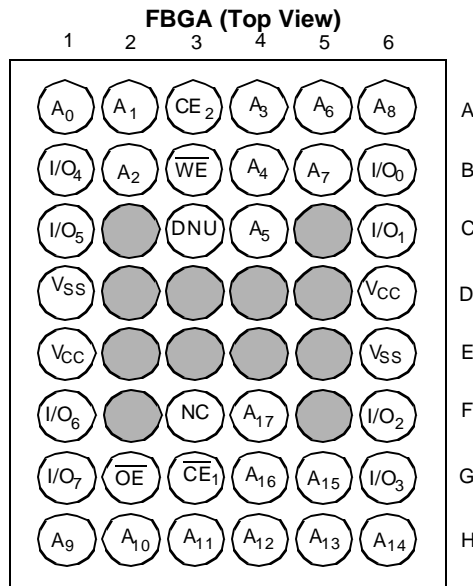
The eight input/output pins (I/O₀ through I/O₇) are placed in a high-impedance state when the device is deselected (\overline{CE}_1 HIGH or \overline{CE}_2 LOW), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE}_1 LOW and \overline{CE}_2 HIGH and WE LOW).

The WCMA2008U1B is available in a 36-ball FBGA package.

Logic Block Diagram



Pin Configurations



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	55°C to +125°C
Supply Voltage to Ground Potential	-0.5V to +4.6V

DC Voltage Applied to Outputs

in High Z State ^[1]	0.5V to V _{CC} + 0.5V
DC Input Voltage ^[1]	-0.5V to V _{CC} + 0.5V
Output Current into Outputs (LOW)	20 mA
Static Discharge Voltage	>2001V (per MIL-STD-883, Method 3015)
Latch-Up Current	>200 mA

Operating Range

Product	Range	Ambient Temperature	V _{CC}
WCMA2008U1B	Industrial	-40°C to +85°C	2.7V to 3.3V

Product Portfolio

Product	V _{CC} Range			Speed	Power Dissipation (Industrial)					
					Operating, I _{CC}				Standby (I _{SB2})	
	f = 1 MHz		f = f _{max}							
	Min.	Typ. ^[2]	Max.		Typ. ^[2]	Max.	Typ. ^[2]	Max.	Typ. ^[2]	Max.
WCMA2008U1B	2.7V	3.0V	3.3V	70 ns	1.5 mA	3 mA	7 mA	15 mA	2 μA	10 μA

Notes:

- V_{IL(min.)} = -2.0V for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25°C.



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Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	WCMA2008U1B-70			Unit
			Min.	Typ. ^[2]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -1.0 mA V _{CC} = 2.7V	2.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 2.1 mA V _{CC} = 2.7V			0.4	V
V _{IH}	Input HIGH Voltage		2.2		V _{CC} + 0.3V	V
V _{IL}	Input LOW Voltage		-0.3		0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC} V _{CC} = 3.3V I _{OUT} = 0 mA CMOS Levels		7	15	mA
		f = 1 MHz		1.5	3	
I _{SB1}	Automatic CE Power-Down Current—CMOS Inputs	CE ₁ ≥ V _{CC} - 0.2V or CE ₂ ≤ 0.2V V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = f _{max} (Address and Data Only), f = 0 (OE, WE)		2	10	μA
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	CE ₁ ≥ V _{CC} - 0.2V or CE ₂ ≤ 0.2V V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0, V _{CC} = 3.3V				

Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = V _{CC} (typ)	6	pF
C _{OUT}	Output Capacitance		8	pF

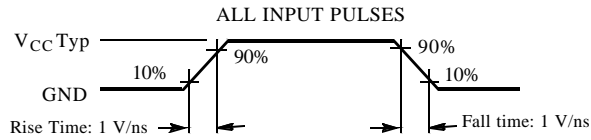
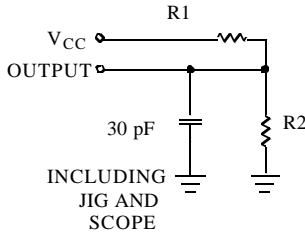
Thermal Resistance

Description	Test Conditions	Symbol	BGA	Unit
Thermal Resistance ^[3] (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	Θ _{JA}	55	°C/W
Thermal Resistance ^[3] (Junction to Case)		Θ _{JC}	16	°C/W

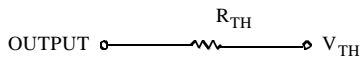
Note:

3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENINEQUIVALENT

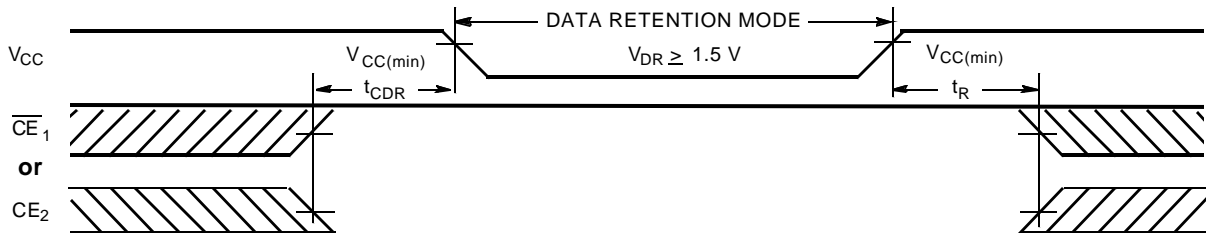


Parameters	3.3V	Unit
R1	1105	Ohms
R2	1550	Ohms
R _{TH}	645	Ohms
V _{TH}	1.75	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. ^[2]	Max.	Unit
V _{DR}	V _{CC} for Data Retention		1.5		V _{CCmax}	V
I _{CCDR}	Data Retention Current	V _{CC} = 1.5V CE ₁ ≥ V _{CC} - 0.2V or CE ₂ ≤ 0.2V V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V		1	6	μA
t _{CDR} ^[3]	Chip Deselect to Data Retention Time		0			ns
t _R ^[4]	Operation Recovery Time		t _{RC}			ns

Data Retention Waveform



Note:

4. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min.)} ≥ 100 μs or stable at V_{CC(min.)} ≥ 100 μs.



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Switching Characteristics Over the Operating Range^[5]

Parameter	Description	WCMA2008U1B-70		Unit
		Min.	Max.	
READ CYCLE				
t_{RC}	Read Cycle Time	70		ns
t_{AA}	Address to Data Valid		70	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	\overline{CE}_1 LOW and CE_2 HIGH to Data Valid		70	ns
t_{DOE}	\overline{OE} LOW to Data Valid		35	ns
t_{LZOE}	\overline{OE} LOW to Low $Z^{[6]}$	5		ns
t_{HZOE}	\overline{OE} HIGH to High $Z^{[6, 7]}$		25	ns
t_{LZCE}	\overline{CE}_1 LOW and CE_2 HIGH to Low $Z^{[6]}$	10		ns
t_{HZCE}	\overline{CE}_1 HIGH or CE_2 LOW to High $Z^{[6, 7]}$		25	ns
t_{PU}	\overline{CE}_1 LOW and CE_2 HIGH to Power-Up	0		ns
t_{PD}	\overline{CE}_1 HIGH or CE_2 LOW to Power-Down		70	ns
WRITE CYCLE^[8,]				
t_{WC}	Write Cycle Time	70		ns
t_{SCE}	\overline{CE}_1 LOW and CE_2 HIGH to Write End	60		ns
t_{AW}	Address Set-Up to Write End	60		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-Up to Write Start	0		ns
t_{PWE}	\overline{WE} Pulse Width	50		ns
t_{SD}	Data Set-Up to Write End	30		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	\overline{WE} LOW to High $Z^{[6, 7]}$		25	ns
t_{LZWE}	\overline{WE} HIGH to Low $Z^{[6]}$	10		ns

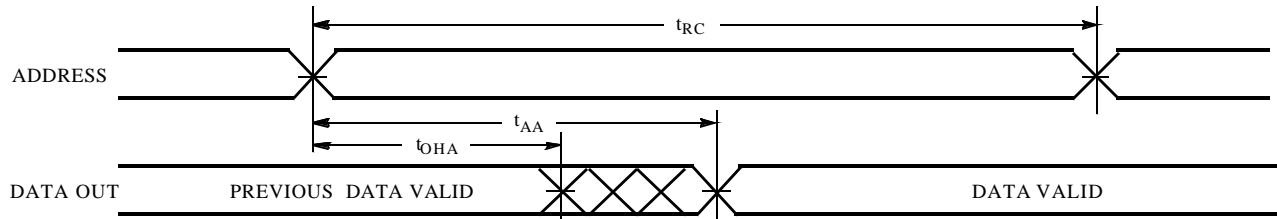
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Notes:

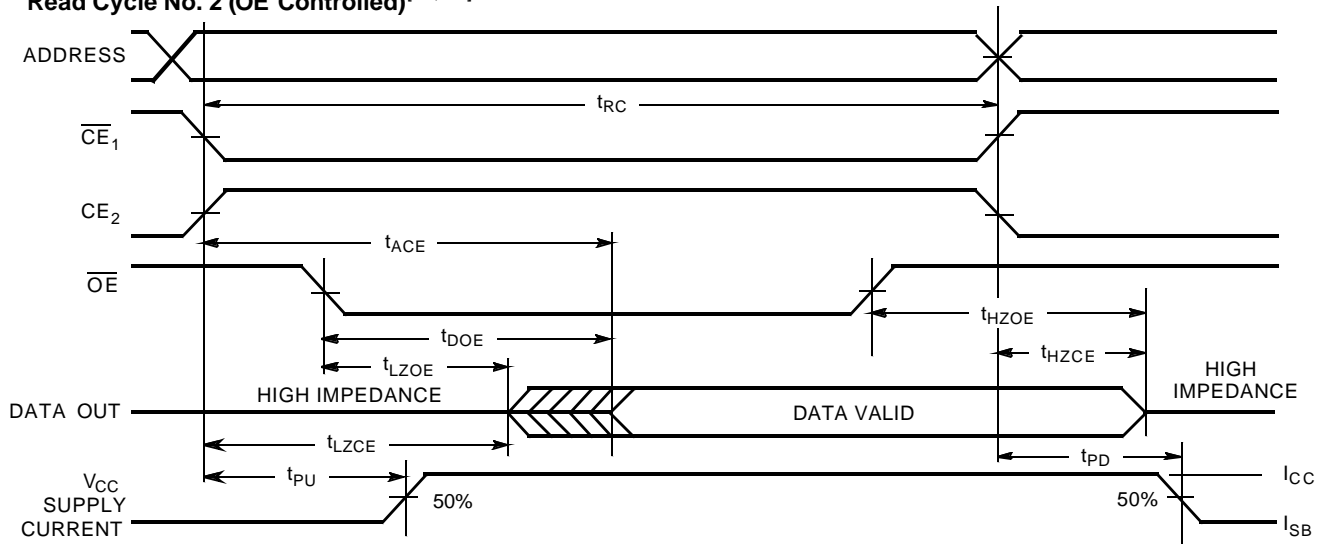
5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE} , t_{HZCE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
8. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled) [9, 10]



Read Cycle No. 2 (\overline{OE} Controlled) [10, 11]

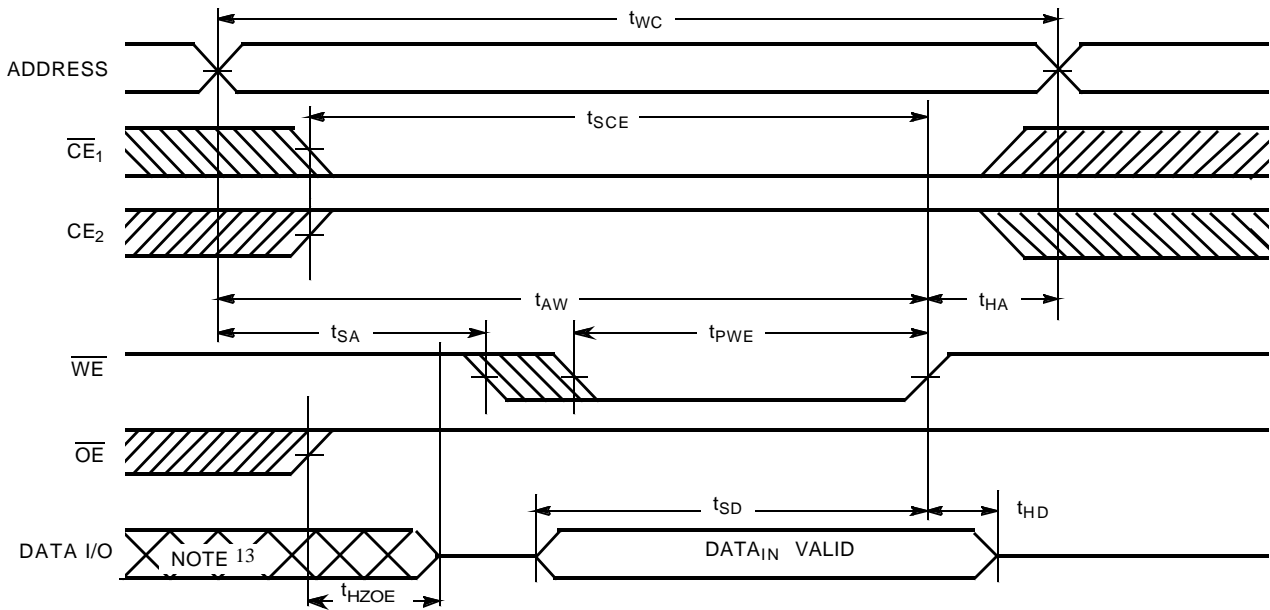


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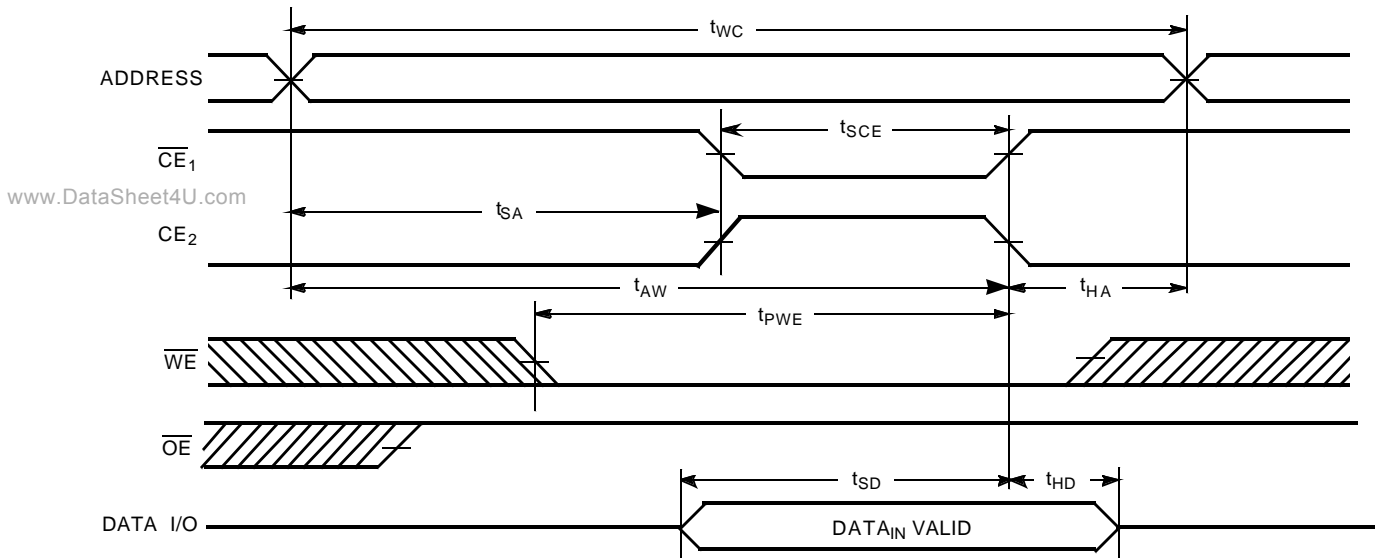
- 9. Device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.
- 10. \overline{WE} is HIGH for read cycle.
- 11. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 (\overline{WE} Controlled) [8, 12, 14]



Write Cycle No. 2 (\overline{CE}_1 or \overline{CE}_2 Controlled) [8, 12, 14]

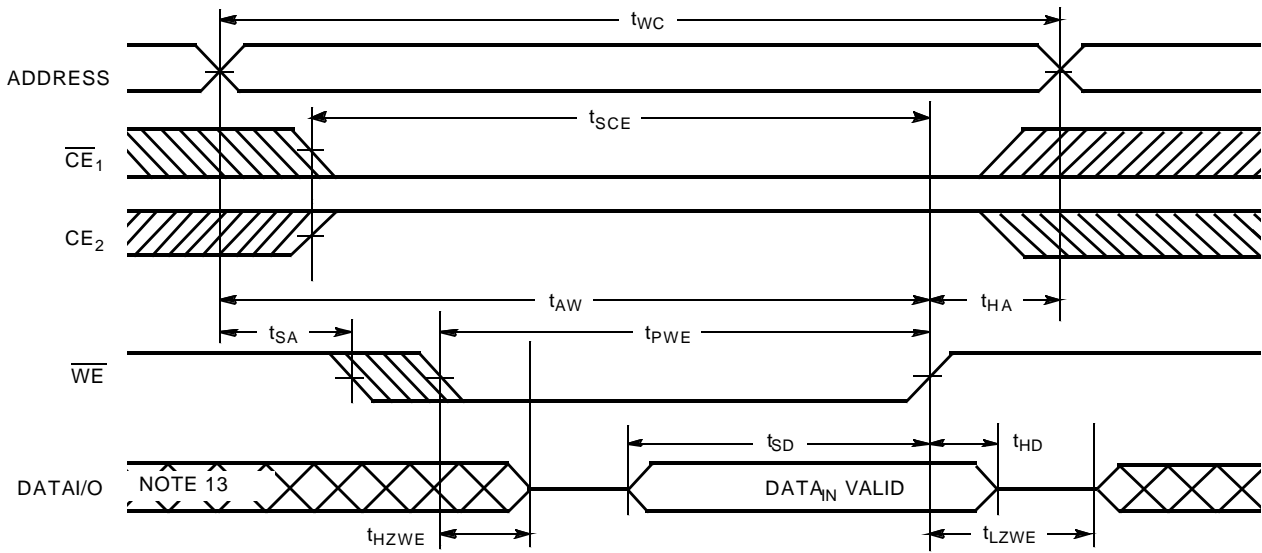


Notes:

- 12. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 13. During this period, the I/Os are in output state and input signals should not be applied.
- 14. If \overline{CE}_1 goes HIGH or \overline{CE}_2 goes LOW simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) ^[14]





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Truth Table

\overline{CE}_1	CE_2	\overline{WE}	\overline{OE}	Inputs/Outputs	Mode	Power
H	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	L	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	H	L	Data Out	Read	Active (I_{CC})
L	H	L	X	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Output Disabled	Active (I_{CC})

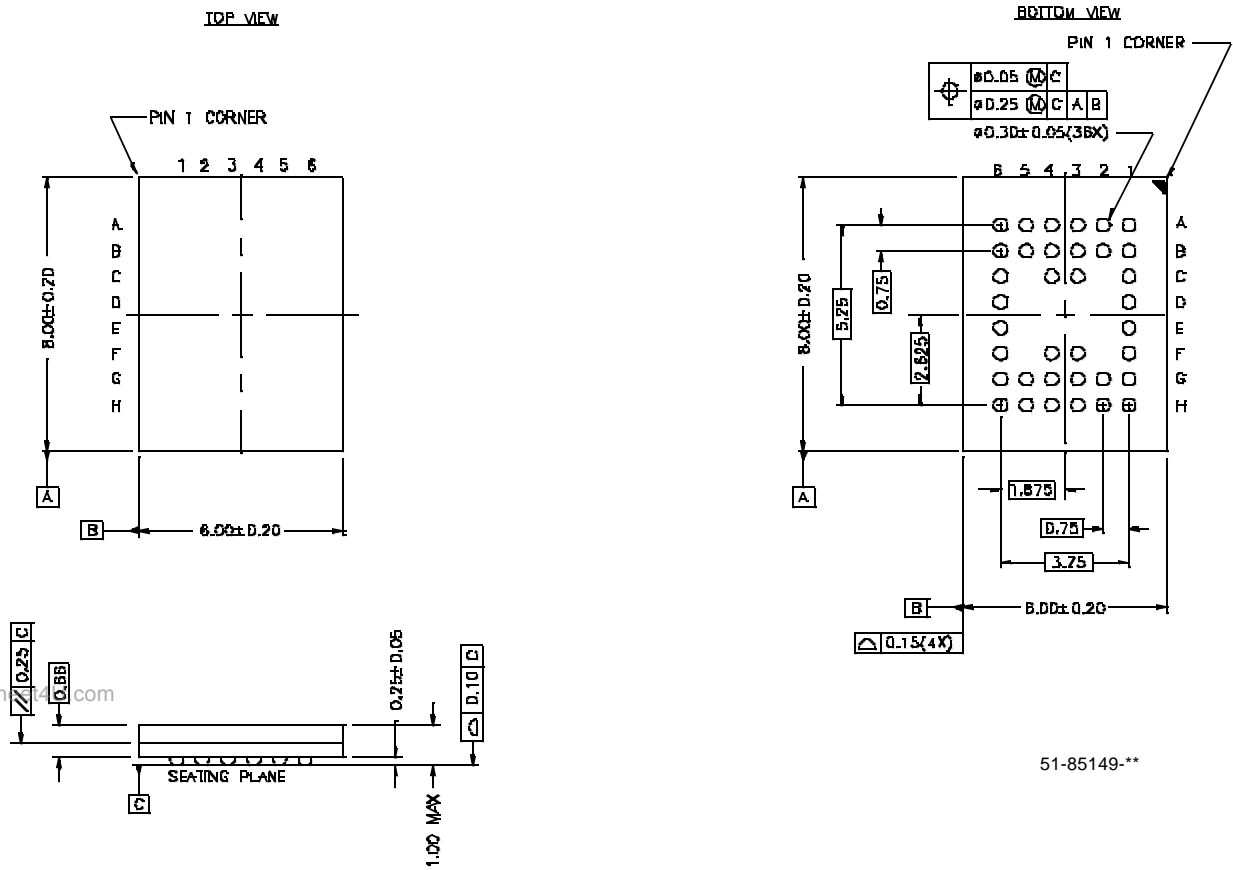
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Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	WCMA2008U1B-FF70	FB36A	36-ball Fine Pitch BGA (6.0 mm x 8.0 mm x 1.0 mm)	Industrial

Package Diagrams

36-Lead VFBGA (6.0 mm x 8.0 mm x 1.0 mm) FB36A



51-85149-**



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Document Title: WCMA2008U1B, 256K x 8 Static RAM					
REV.	Spec #	ECN #	Issue Date	Orig. of Change	Description of Change
**	38-05321	117495	3/18/2002	CBD	New Data Sheet