



Preliminary

WCMA4016U1X

256K x 16 Static RAM

Features

- Low voltage range: 2.7V–3.6V
- Ultra-low active, standby power
- Easy memory expansion with  $\overline{CE}_1$  and  $\overline{CE}_2$  and  $\overline{OE}$  features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected
- CMOS for optimum speed/power

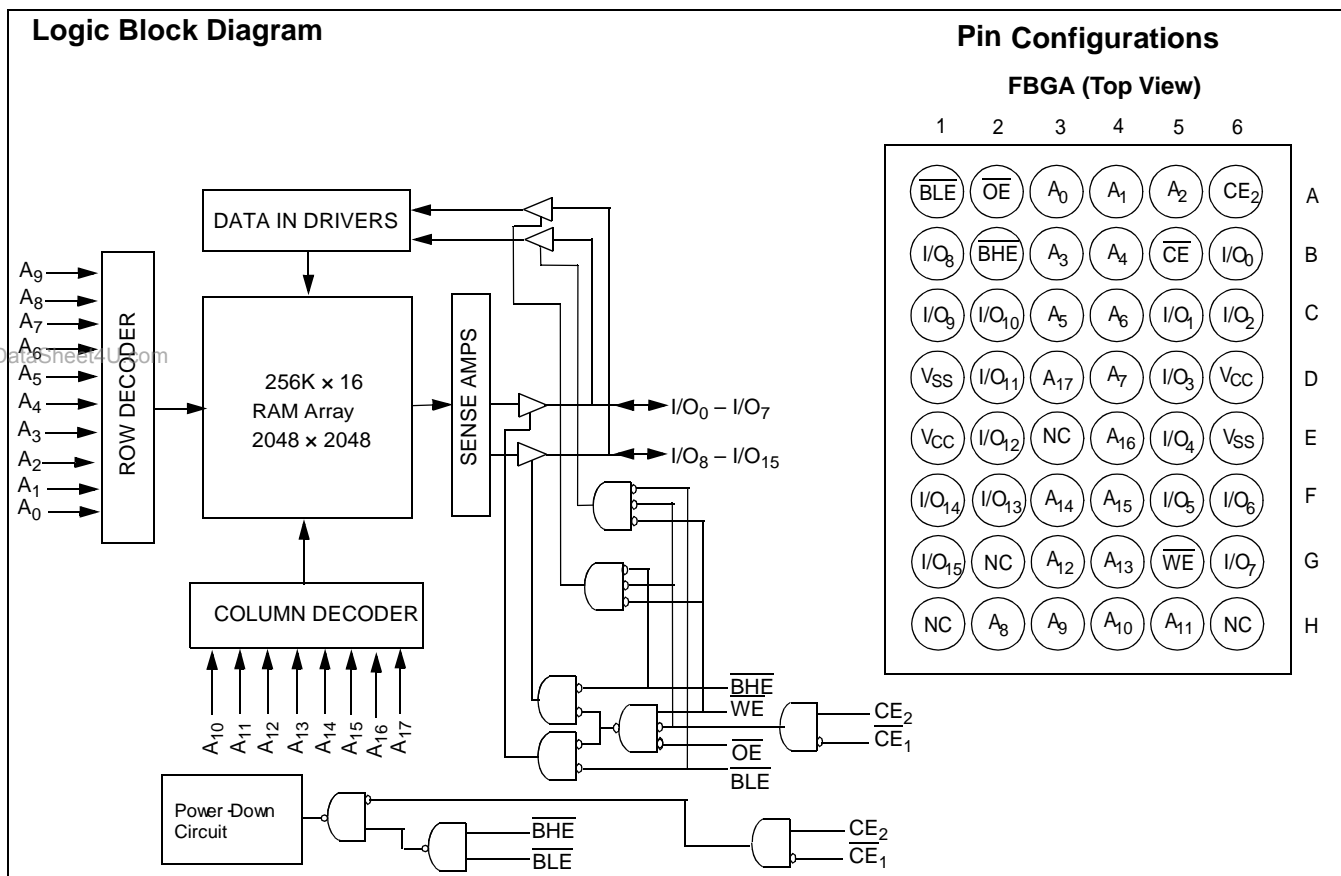
Functional Description<sup>[1]</sup>

The WCMA4016U1X is a high-performance CMOS static RAM organized as 262,144 words by 16 bits. This device features advanced circuit design to provide ultra-low active current and standby current. This is ideal for providing more battery life in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ( $\overline{CE}_1$  HIGH or  $\overline{CE}_2$  LOW or

both  $\overline{BHE}$  and  $\overline{BLE}$  are HIGH). The input/output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high-impedance state when: deselected ( $\overline{CE}_1$  HIGH or  $\overline{CE}_2$  LOW), outputs are disabled ( $\overline{OE}$  HIGH), both Byte High Enable and Byte Low Enable are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}_1$  LOW,  $\overline{CE}_2$  HIGH and WE LOW).

Writing to the device is accomplished by taking Chip Enables ( $\overline{CE}_1$  LOW and  $\overline{CE}_2$  HIGH) and Write Enable (WE) input LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_0$  through  $I/O_7$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ).

Reading from the device is accomplished by taking Chip Enables ( $\overline{CE}_1$  LOW and  $\overline{CE}_2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_8$  to  $I/O_{15}$ . See the truth table at the back of this datasheet for a complete description of read and write modes.



# WCMA4016U1X

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied..... -55°C to +125°C  
 Supply Voltage to Ground Potential ..... -0.5V to +4.6V  
 DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V  
 DC Input Voltage<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

Output Current into Outputs (LOW)..... 20 mA  
 Static Discharge Voltage..... >2100V (per MIL-STD-883, Method 3015)  
 Latch-Up Current..... >200 mA

## Operating Range

Device	Range	Ambient Temperature	V <sub>CC</sub>
WCMA4016U1X	Industrial	-40°C to +85°C	2.7V to 3.6V

## Product Portfolio

Product	V <sub>CC</sub> Range			Power	Speed (ns)	Power Dissipation (Industrial)			
	V <sub>CC(min.)</sub>	V <sub>CC(typ.)</sub> <sup>[2]</sup>	V <sub>CC(max.)</sub>			Operating (I <sub>CC</sub> )		Standby (I <sub>SB2</sub> )	
						Typ. <sup>[2]</sup>	Maximum	Typ. <sup>[2]</sup>	Maximum
WCMA4016U1X	2.7V	3.0V	3.6V	LL	70	7 mA	15 mA	2 μA	20 μA

## Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	WCMA4016U1X			Unit
			Min.	Typ. <sup>[2]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA, V <sub>CC</sub> = 2.7V	2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA, V <sub>CC</sub> = 2.7V			0.4	V
V <sub>IH</sub>	Input HIGH Voltage	V <sub>CC</sub> = 3.6V	2.2		V <sub>CC</sub> + 0.5V	V
V <sub>IL</sub>	Input LOW Voltage	V <sub>CC</sub> = 2.7V	-0.5		0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	±1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-1	+1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub> , CMOS Levels, V <sub>CC</sub> = 3.6V		7	15	mA
		I <sub>OUT</sub> = 0 mA, f = 1 MHz, CMOS Levels		1	2	mA
I <sub>SB1</sub>	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.3V$ , $CE_2 \leq 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ , $V_{IN} \leq 0.3V$ , f = f <sub>MAX</sub> (Address and Data Only), f = 0 (OE, WE, BHE and BLE), V <sub>CC</sub> = 3.60V	LL	2	20	μA
I <sub>SB2</sub>	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.3V$ or $CE_2 \leq 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , f = 0, V <sub>CC</sub> = 3.60V	LL	2	20	μA

**Notes:**

- V<sub>IL(min.)</sub> = -2.0V for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25°C.

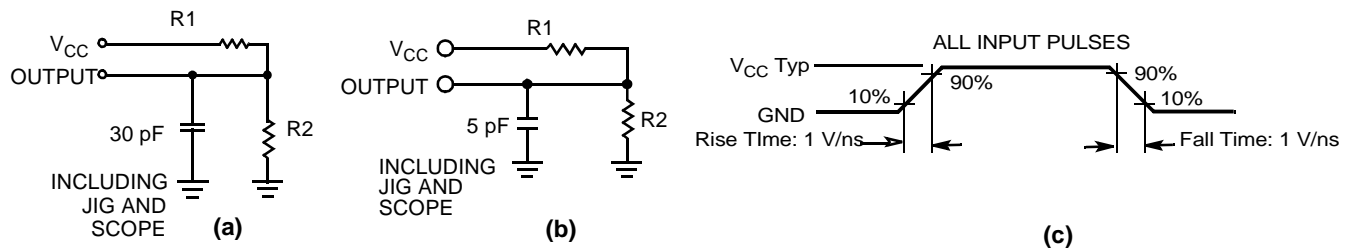
**Capacitance<sup>[3]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC</sub> (typ.)	6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

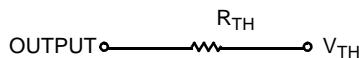
**Thermal Resistance**

Description	Test Conditions	Symbol	BGA	Units
Thermal Resistance (Junction to Ambient) <sup>[3]</sup>	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	Θ <sub>JA</sub>	55	°C/W
Thermal Resistance (Junction to Case) <sup>[3]</sup>		Θ <sub>JC</sub>	16	°C/W

**AC Test Loads and Waveforms**



Equivalent to: THÉVENIN EQUIVALENT



Parameters	3.0V	Unit
R1	1103	Ω
R2	1554	Ω
R <sub>TH</sub>	645	Ω
V <sub>TH</sub>	1.75V	V

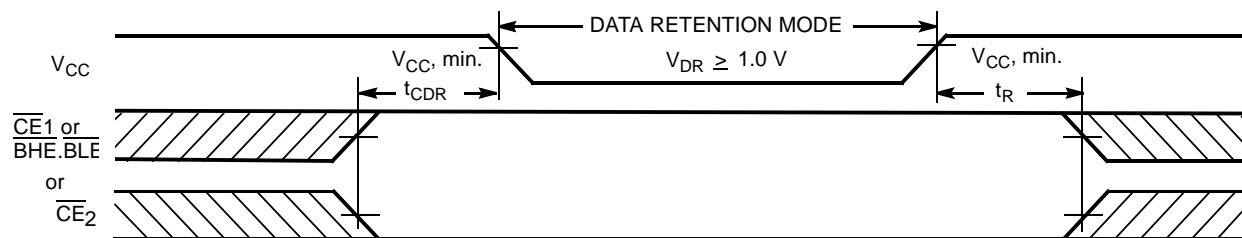
**Data Retention Characteristics (Over the Operating Range)**

Parameter	Description	Conditions	Min.	Typ. <sup>[2]</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		1.0		3.6	V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = 1.0V CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.3V, CE <sub>2</sub> ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V	L	1	10	μA
			LL			
t <sub>CDR</sub> <sup>[3]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub> <sup>[4]</sup>	Operation Recovery Time		70			ns

**Note:**

- Tested initially and after any design or process changes that may affect these parameters.
- Full Device AC operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC</sub>(min.) > 10 μs or stable at V<sub>CC</sub>(min.) > 10 μs.

**Data Retention Waveform<sup>[5]</sup>**



**Switching Characteristics Over the Operating Range<sup>[6]</sup>**

Parameter	Description	70 ns		Unit
		Min.	Max.	
<b>READ CYCLE</b>				
t <sub>RC</sub>	Read Cycle Time	70		ns
t <sub>AA</sub>	Address to Data Valid		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		ns
t <sub>ACE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Data Valid		70	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		35	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[7, 9]</sup>	5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[9]</sup>		25	ns
t <sub>LZCE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Low Z <sup>[7]</sup>	10		ns
t <sub>HZCE</sub>	$\overline{CE}_1$ HIGH and CE <sub>2</sub> LOW to High Z <sup>[7, 9]</sup>		25	ns
t <sub>PU</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Power-Up	0		ns
t <sub>PD</sub>	$\overline{CE}_1$ HIGH and CE <sub>2</sub> LOW to Power-Down		70	ns
t <sub>DBE</sub>	$\overline{BHE} / \overline{BLE}$ LOW to Data Valid		70	ns
t <sub>LZBE</sub> <sup>[8]</sup>	$\overline{BHE} / \overline{BLE}$ LOW to Low Z	5		ns
t <sub>HZBE</sub>	$\overline{BHE} / \overline{BLE}$ HIGH to High Z		25	ns
<b>WRITE CYCLE<sup>[10, 11]</sup></b>				
t <sub>WC</sub>	Write Cycle Time	70		ns
t <sub>SCE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Write End	60		ns
t <sub>AW</sub>	Address Set-Up to Write End	60		ns
t <sub>HA</sub>	Address Hold from Write End	0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	50		ns

**Notes:**

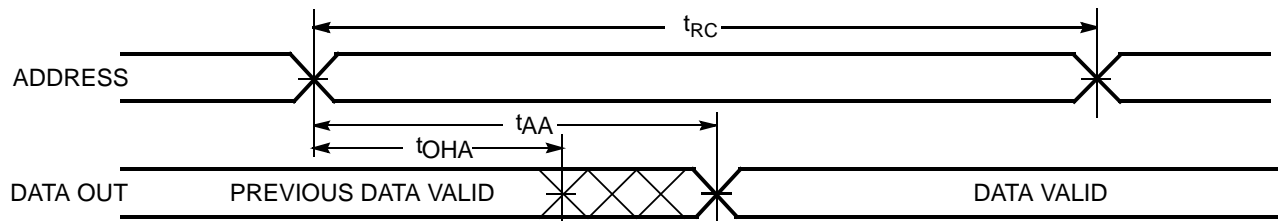
- $\overline{BHE} / \overline{BLE}$  is the AND of both  $\overline{BHE}$  and  $\overline{BLE}$ . Chip can be deselected by either disabling the chip enable signals or by disabling both  $\overline{BHE}$  and  $\overline{BLE}$ .
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to V<sub>CC(typ.)</sub>, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
- If both byte enables are toggled together this value is 10ns
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle #3 (WE controlled, OE LOW) is the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.

**Switching Characteristics** Over the Operating Range<sup>[6]</sup> (continued)

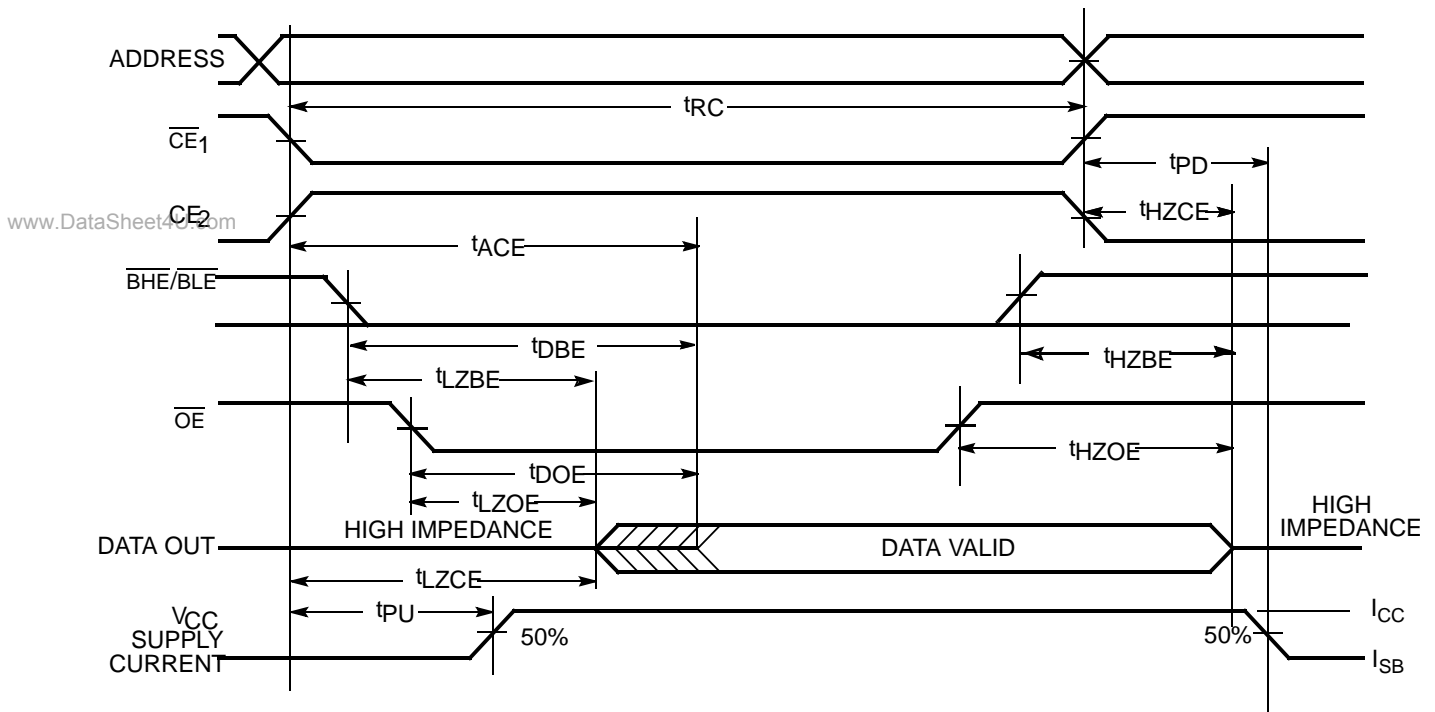
Parameter	Description	70 ns		Unit
		Min.	Max.	
$t_{BW}$	$\overline{BHE}$ / $\overline{BLE}$ Pulse Width	60		ns
$t_{SD}$	Data Set-Up to Write End	30		ns
$t_{HD}$	Data Hold from Write End	0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[7, 9]</sup>		25	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup>	10		ns

**Switching Waveforms**

**Read Cycle 1 (Address Transition Controlled)**<sup>[12, 13]</sup>



**Read Cycle 2 ( $\overline{OE}$  Controlled)**<sup>[13, 14]</sup>

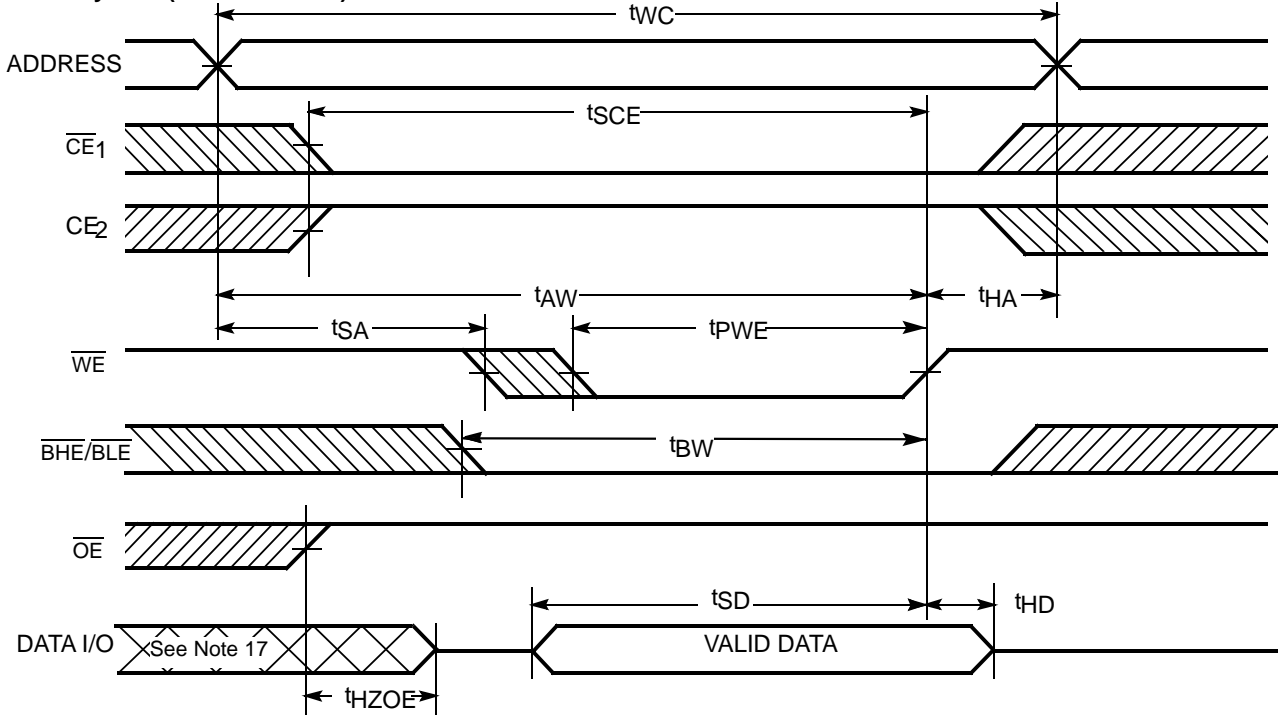


**Notes:**

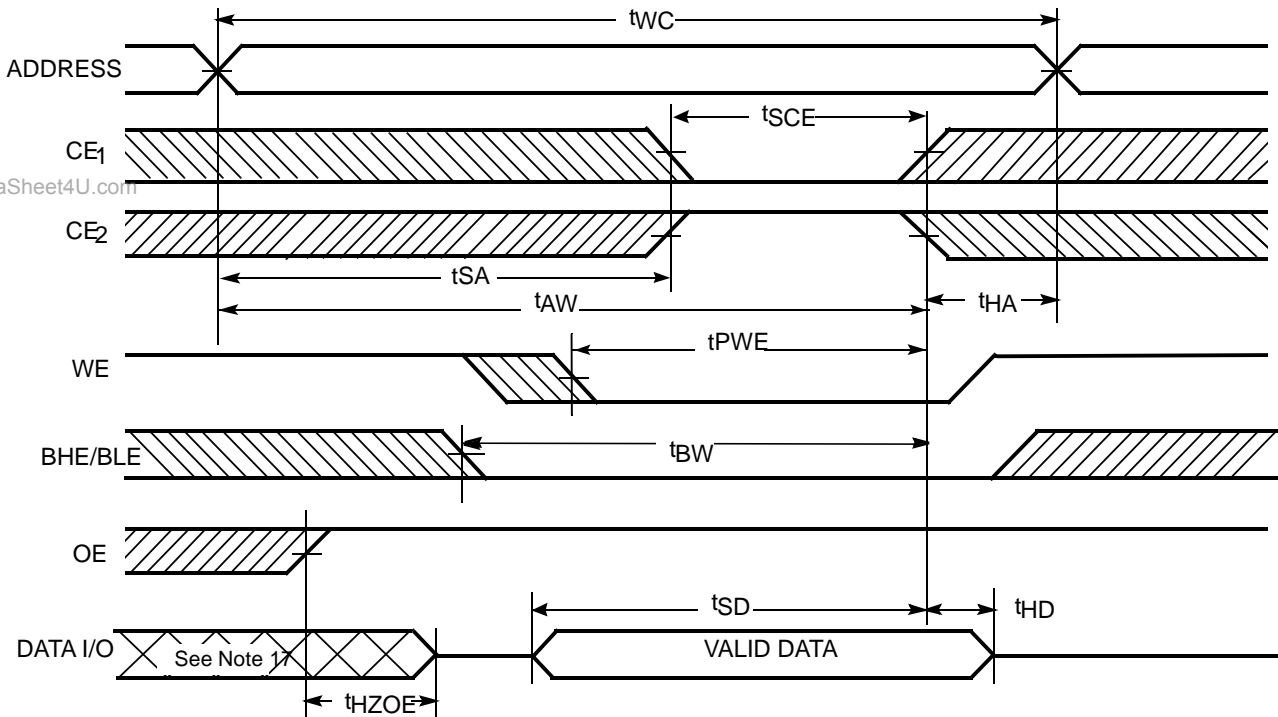
- 12. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ , and  $CE_2 = V_{IH}$ .
- 13.  $\overline{WE}$  is HIGH for read cycle.
- 14. Address valid prior to or coincident with  $\overline{CE}_1$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW and  $CE_2$  transition HIGH.

**Switching Waveforms (continued)**

**Write Cycle 1 ( $\overline{WE}$  Controlled)** [10, 15, 16, 17]



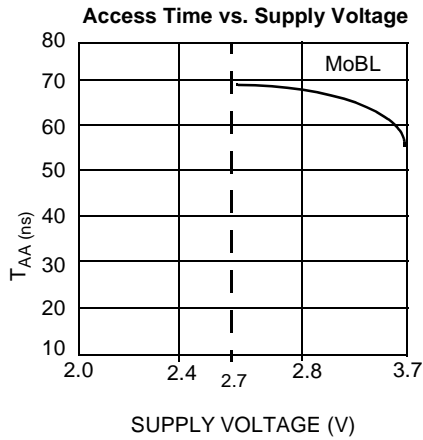
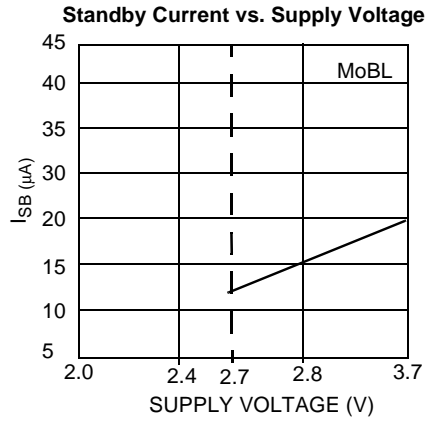
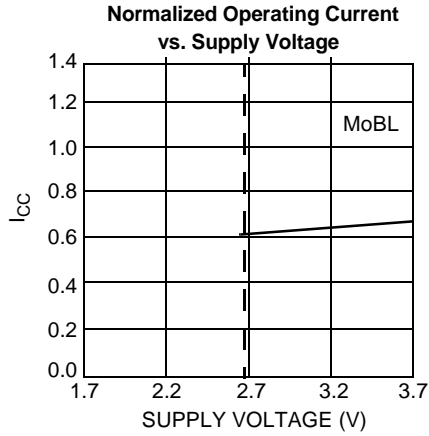
**Write Cycle 2 ( $\overline{CE}_1$  or  $CE_2$  Controlled)** [10, 15, 16, 17]



**Notes:**

- 15. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 16. If  $\overline{CE}_1$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high-impedance state.
- 17. During this period, the I/Os are in output state and input signals should not be applied.

**Typical DC and AC Characteristics**



**Truth Table**

CE <sub>1</sub>	CE <sub>2</sub>	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-Down	Standby (I <sub>SB</sub> )
X	L	X	X	X	X	High Z	Deselect/Power-Down	Standby (I <sub>SB</sub> )
X	X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I <sub>SB</sub> )
L	H	H	L	L	L	Data Out (I/O0 – I/O15)	Read	Active (I <sub>CC</sub> )
L	H	H	L	H	L	Data Out (I/O0 – I/O7); High Z (I/O8 – I/O15)	Read	Active (I <sub>CC</sub> )
L	H	H	L	L	H	High Z (I/O0 – I/O7); Data Out (I/O8 – I/O15)	Read	Active (I <sub>CC</sub> )
L	H	H	H	L	H	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	H	H	H	H	L	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	H	H	H	L	L	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	H	L	X	L	L	Data In (I/O0 – I/O15)	Write	Active (I <sub>CC</sub> )
L	H	L	X	H	L	Data In (I/O0 – I/O7); High Z (I/O8 – I/O15)	Write	Active (I <sub>CC</sub> )

# WCMA4016U1X

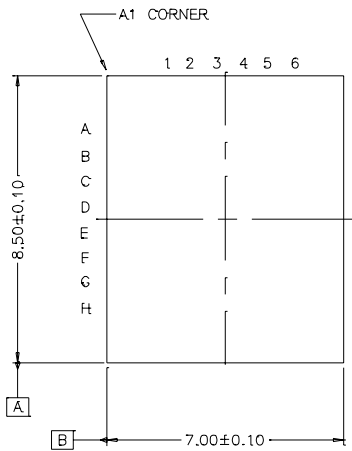
## Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	WCMA4016U1X-FF70	BA48	48-Ball Fine Pitch BGA	Industrial

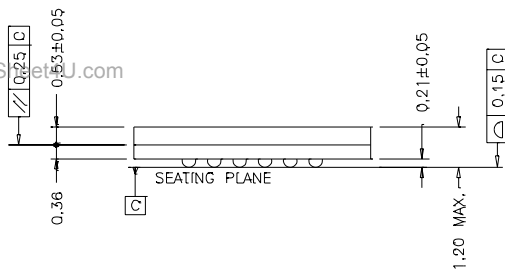
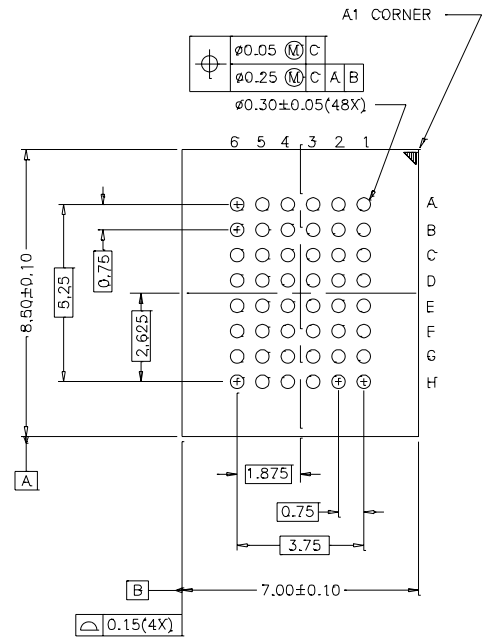
## Package Diagrams

### 48-Ball (7.00 mm x 8.5 mm x 1.2 mm) FBGA BA48B

TOP VIEW



BOTTOM VIEW



51-85106-\*D





**Document History Page**

<b>Document Title: WCMA4016U1X 256K x 16 STATIC RAM</b>				
<b>Document Number:</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**		See ECN	AJU	New Data Sheet