**WEIDA**

# WCMB4016R4X

## 256K x 16 Static RAM

### Features

- **Low voltage range:**
  — **1.65V–1.95V**
- **Ultra-low active power**
  — **Typical Active Current: 0.5 mA @ f = 1 MHz**
  — **Typical Active Current: 2 mA @ f = $f_{max}$ (70 ns speed)**
- **Low standby power**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

### Functional Description

The WCMB4016R4X is a high-performance CMOS static RAM organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This device is ideal for portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{CE}$ HIGH or both $\overline{BLE}$
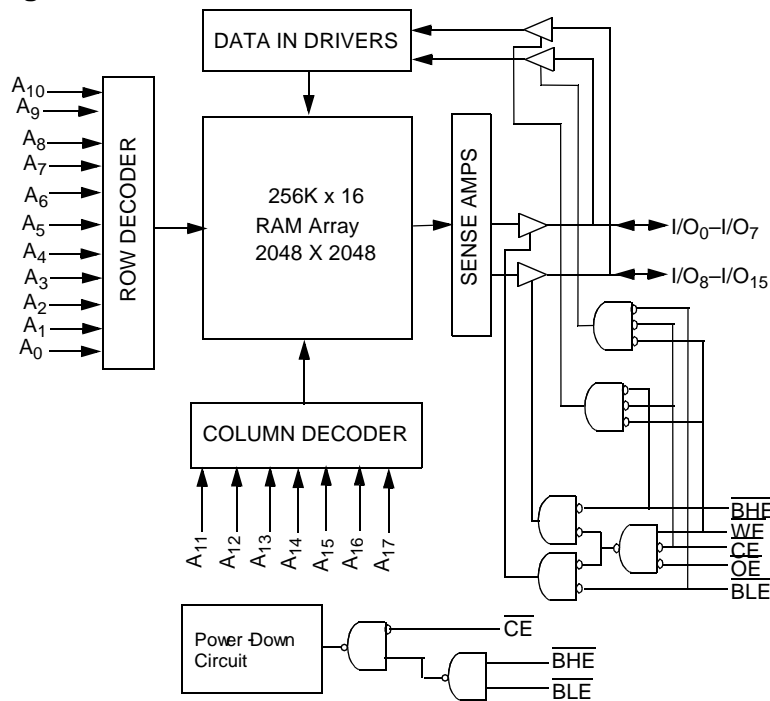
and $\overline{BHE}$ are HIGH). The input/output pins (I/O$_0$ through I/O$_{15}$) are placed in a high-impedance state when: deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O$_0$ through I/O$_7$), is written into the location specified on the address pins (A$_0$ through A$_{17}$). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O$_8$ through I/O$_{15}$) is written into the location specified on the address pins (A$_0$ through A$_{17}$).
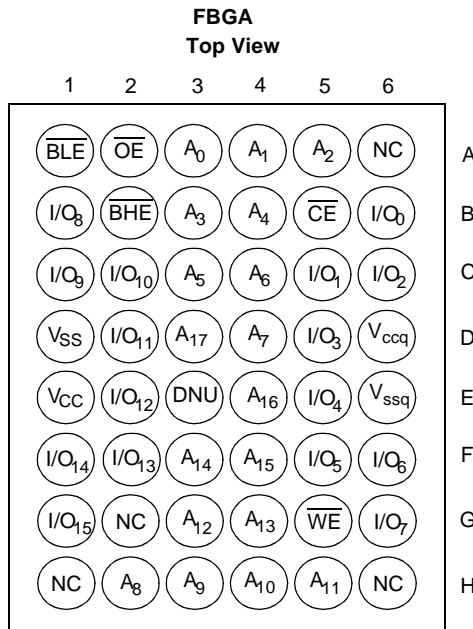
Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O$_0$ to I/O$_7$. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O$_8$ to I/O$_{15}$. See the Truth Table at the back of this data sheet for a complete description of read and write modes.

The WCMB4016R4X is available in a 48-ball FBGA package.



Logic Block Diagram

## Pin Configuration[1, 2]

**FBGA**
**Top View**

|   | 1 | 2 | 3 | 4 | 5 | 6 |   |
|---|---|---|---|---|---|---|---|
| A | $\overline{BLE}$ | $\overline{OE}$ | $A_0$ | $A_1$ | $A_2$ | NC | A |
| B | $I/O_8$ | $\overline{BHE}$ | $A_3$ | $A_4$ | $\overline{CE}$ | $I/O_0$ | B |
| C | $I/O_9$ | $I/O_{10}$ | $A_5$ | $A_6$ | $I/O_1$ | $I/O_2$ | C |
| D | $V_{SS}$ | $I/O_{11}$ | $A_{17}$ | $A_7$ | $I/O_3$ | $V_{ccq}$ | D |
| E | $V_{CC}$ | $I/O_{12}$ | DNU | $A_{16}$ | $I/O_4$ | $V_{ssq}$ | E |
| F | $I/O_{14}$ | $I/O_{13}$ | $A_{14}$ | $A_{15}$ | $I/O_5$ | $I/O_6$ | F |
| G | $I/O_{15}$ | NC | $A_{12}$ | $A_{13}$ | $\overline{WE}$ | $I/O_7$ | G |
| H | NC | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | NC | H |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ...................................... −65°C to +150°C

Ambient Temperature with
Power Applied................................................. −55°C to +125°C

Supply Voltage to Ground Potential ................. −0.2V to +2.4V

DC Voltage Applied to Outputs
in High Z State[3] ........................................ −0.2V to $V_{CC}$ + 0.2V

DC Input Voltage[3] ................................... −0.2V to $V_{CC}$ + 0.2V

Output Current into Outputs (LOW)............................ 20 mA

Static Discharge Voltage........................................... >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current .................................................... >200 mA

## Operating Range

| Device | Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|---|
| WCMB4016R4X | Industrial | −40°C to +85°C | 1.65V to 1.95V |

## Product Portfolio

|  |  |  |  |  | Power Dissipation (Industrial) | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
|  | $V_{CC}$ Range | | |  | Operating ($I_{CC}$) | | | | Standby ($I_{SB2}$) | |
|  |  |  |  |  | f = 1 MHz | | f = $f_{max}$ | | | |
| Product | $V_{CC(min.)}$ | $V_{CC(typ.)}$[4] | $V_{CC(max.)}$ | Speed | Typ.[4] | Max. | Typ.[4] | Max. | Typ.[4] | Max. |
| WCMB4016R4X | 1.65V | 1.80V | 1.95V | 70 ns | 0.5 mA | 3 mA | 2 mA | 6 mA | 1 μA | 10 μA |

**Notes:**
1. NC pins are not connected to the die.
2. E3 (DNU) can be left as NC or $V_{SS}$ to ensure proper application.
3. $V_{IL}$(min) = −2.0V for pulse durations less than 20 ns.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$ Typ, $T_A$ = 25°C.

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | | WCMB4016R4X Min. | WCMB4016R4X Typ.[4] | WCMB4016R4X Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = -0.1 mA | $V_{CC}$ = 1.65V | 1.4 | | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 0.1 mA | $V_{CC}$ = 1.65V | | | 0.2 | V |
| $V_{IH}$ | Input HIGH Voltage | | | 1.4 | | $V_{CC}$ + 0.2V | V |
| $V_{IL}$ | Input LOW Voltage | | | −0.2 | | 0.4 | V |
| $I_{IX}$ | Input Leakage Current | GND $\leq V_I \leq V_{CC}$ | | −1 | | +1 | μA |
| $I_{OZ}$ | Output Leakage Current | GND $\leq V_O \leq V_{CC}$, Output Disabled | | −1 | | +1 | μA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | f = $f_{MAX}$ = 1/$t_{RC}$ | $V_{CC}$ = 1.95V $I_{OUT}$ = 0 mA CMOS levels | | 2 | 6 | mA |
| | | f = 1 MHz | | | 0.5 | 3 | mA |
| $I_{SB1}$ | Automatic CE Power-Down Current— CMOS Inputs | $\overline{CE} \geq V_{CC}$ – 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V, $V_{IN} \leq$ 0.2V f = $f_{MAX}$ (Address and Data Only), f = 0 ($\overline{OE}$, $\overline{WE}$, $\overline{BHE}$, and $\overline{BLE}$) | | | 1 | 10 | μA |
| $I_{SB2}$ | Automatic CE Power-Down Current— CMOS Inputs | $\overline{CE} \geq V_{CC}$ – 0.2V $V_{IN} \geq V_{CC}$ – 0.2V or $V_{IN} \leq$ 0.2V, f = 0, $V_{CC}$ = 1.95V | | | | | |

## Capacitance[5]

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = $V_{CC(typ)}$ | 6 | pF |
| $C_{OUT}$ | Output Capacitance | | 8 | pF |

## Thermal Resistance

| Description | Test Conditions | Symbol | BGA | Unit |
|---|---|---|---|---|
| Thermal Resistance (Junction to Ambient)[5] | Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board | $\Theta_{JA}$ | 55 | °C/W |
| Thermal Resistance (Junction to Case)[5] | | $\Theta_{JC}$ | 16 | °C/W |

**Note:**
5. Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms
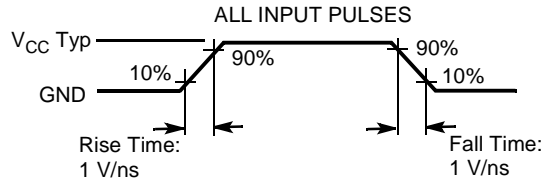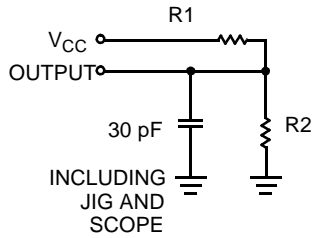


**Equivalent to:** THÉVENIN EQUIVALENT
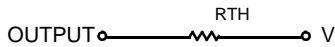
| Parameters | 1.8V | UNIT |
|---|---|---|
| R1 | 13500 | Ohms |
| R2 | 10800 | Ohms |
| $R_{TH}$ | 6000 | Ohms |
| $V_{TH}$ | 0.80 | Volts |

## Data Retention Characteristics (Over the Operating Range)

| Parameter | Description | Conditions | Min. | Typ.[4] | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | | 1.0 | | 1.95 | V |
| $I_{CCDR}$ | Data Retention Current | $V_{CC} = 1.0V$<br>$\overline{CE} \geq V_{CC} - 0.2V$,<br>$V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ | | 1 | 8 | µA |
| $t_{CDR}$[5] | Chip Deselect to Data Retention Time | | 0 | | | ns |
| $t_R$[6] | Operation Recovery Time | | $t_{RC}$ | | | ns |

## Data Retention Waveform[7]
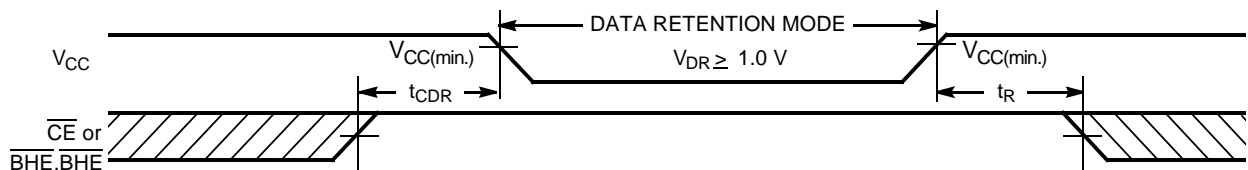


**Notes:**

6. Full device operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
7. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

## Switching Characteristics Over the Operating Range[8]

| Parameter | Description | 70 ns | | Unit |
| | | Min. | Max. | |
|---|---|---|---|---|
| **READ CYCLE** | | | | |
| $t_{RC}$ | Read Cycle Time | 70 | | ns |
| $t_{AA}$ | Address to Data Valid | | 70 | ns |
| $t_{OHA}$ | Data Hold from Address Change | 10 | | ns |
| $t_{ACE}$ | $\overline{CE}$ LOW to Data Valid | | 70 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 35 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low Z[9] | 5 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z[9, 10] | | 25 | ns |
| $t_{LZCE}$ | $\overline{CE}$ LOW to Low Z[9] | 10 | | ns |
| $t_{HZCE}$ | $\overline{CE}$ HIGH to High Z[9, 10] | | 25 | ns |
| $t_{PU}$ | $\overline{CE}$ LOW to Power-Up | 0 | | ns |
| $t_{PD}$ | $\overline{CE}$ HIGH to Power-Down | | 70 | ns |
| $t_{DBE}$ | $\overline{BLE}/\overline{BHE}$ LOW to Data Valid | | 70 | ns |
| $t_{LZBE}$ | $\overline{BLE}/\overline{BHE}$ LOW to Low Z[9] | 5 | | ns |
| $t_{HZBE}$ | $\overline{BLE}/\overline{BHE}$ HIGH to High Z[9, 10] | | 25 | ns |
| **WRITE CYCLE[11]** | | | | |
| $t_{WC}$ | Write Cycle Time | 70 | | ns |
| $t_{SCE}$ | $\overline{CE}$ LOW to Write End | 60 | | ns |
| $t_{AW}$ | Address Set-Up to Write End | 60 | | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | | ns |
| $t_{SA}$ | Address Set-Up to Write Start | 0 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 50 | | ns |
| $t_{BW}$ | $\overline{BLE}/\overline{BHE}$ LOW to Write End | 60 | | ns |
| $t_{SD}$ | Data Set-Up to Write End | 30 | | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High Z[9, 10] | | 25 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low Z[9] | 10 | | ns |

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**Notes:**
8. Test conditions assume signal transition time of 3ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified $I_{OL}/I_{OH}$ and 30-pF load capacitance.
9. At any given temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZBE}$ is less than $t_{LZBE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any given device.
10. $t_{HZOE}$, $t_{HZCE}$, $t_{HZBE}$, and $t_{HZWE}$ transitions are measured when the outputs enter a high impedance state.
11. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write

## Switching Waveforms

**Read Cycle No. 1 (Address Transition Controlled)**[12, 13]
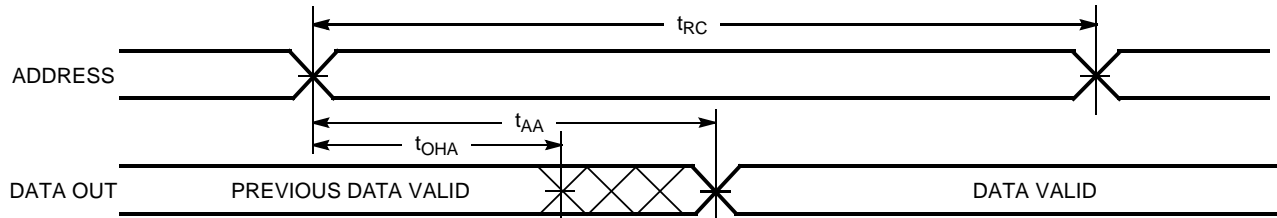


**Read Cycle No. 2 ($\overline{OE}$ Controlled)**[13, 14]



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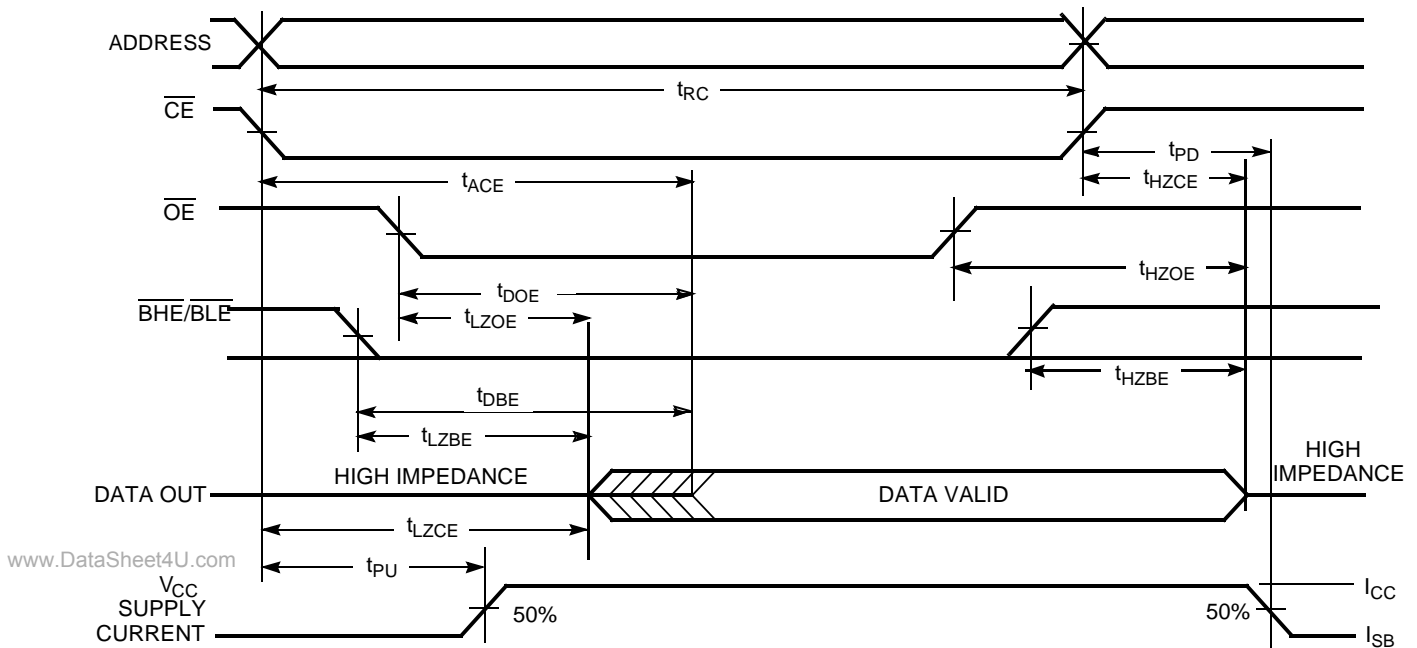
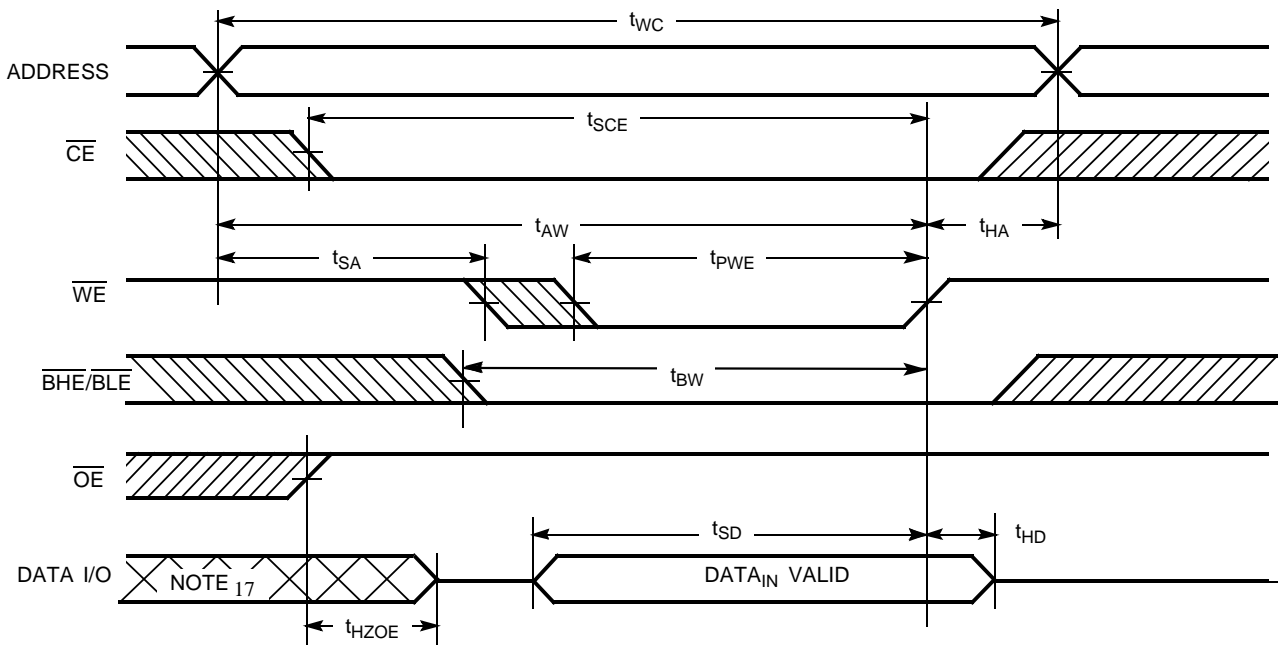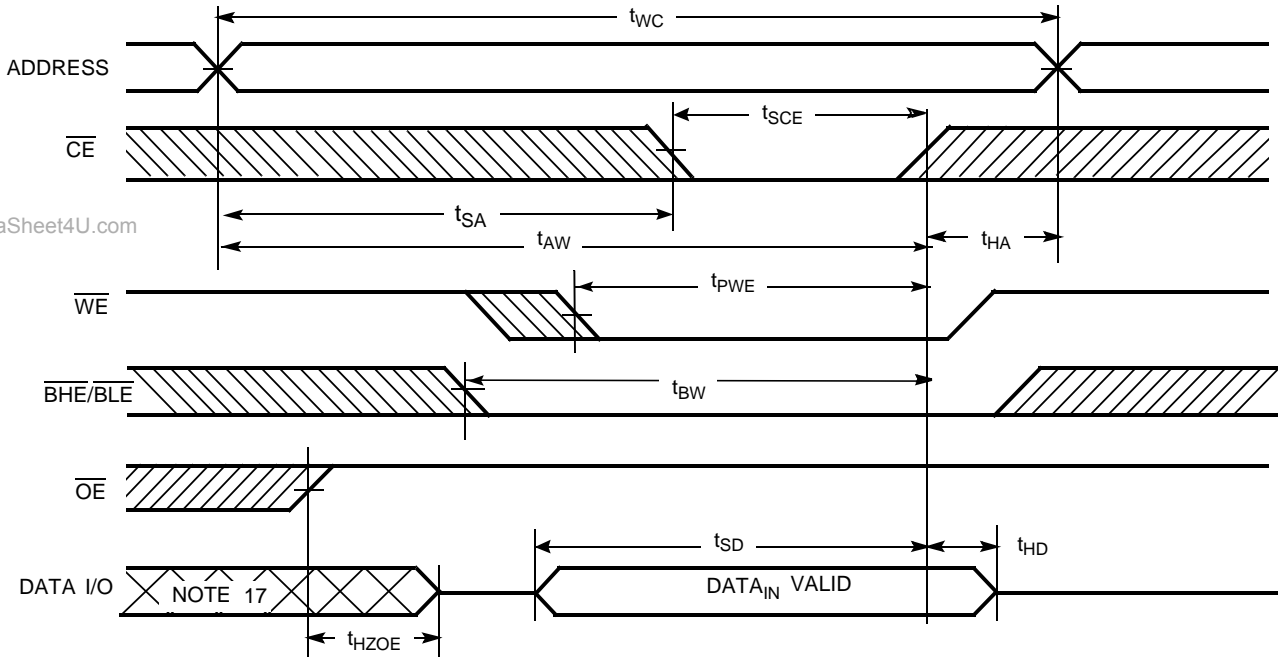**Notes:**
12. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE}$, $\overline{BHE}$, $\overline{BLE}$, transition LOW.

## Switching Waveforms

### Write Cycle No. 1($\overline{\text{WE}}$ Controlled)[11, 15, 16]



### Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled)[11, 15, 16]



**Notes:**
15. Data I/O is high impedance if $\overline{\text{OE}} = V_{IH}$.
16. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state.
17. During this period, the I/Os are in output state and input signals should not be applied.

## Switching Waveforms

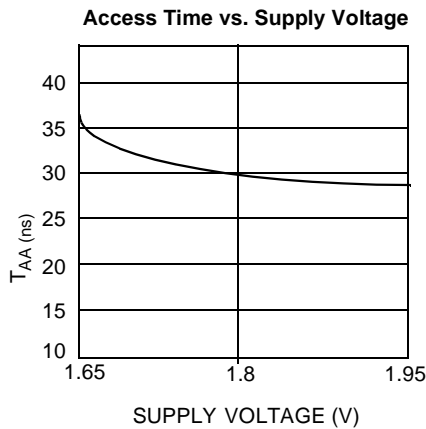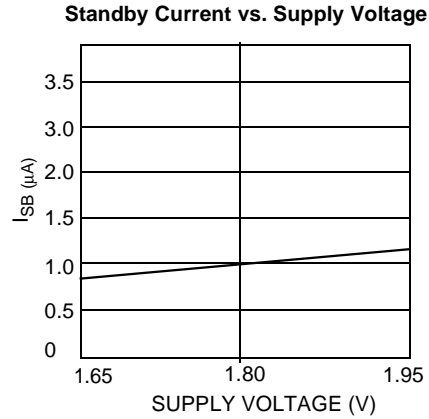### Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[16]
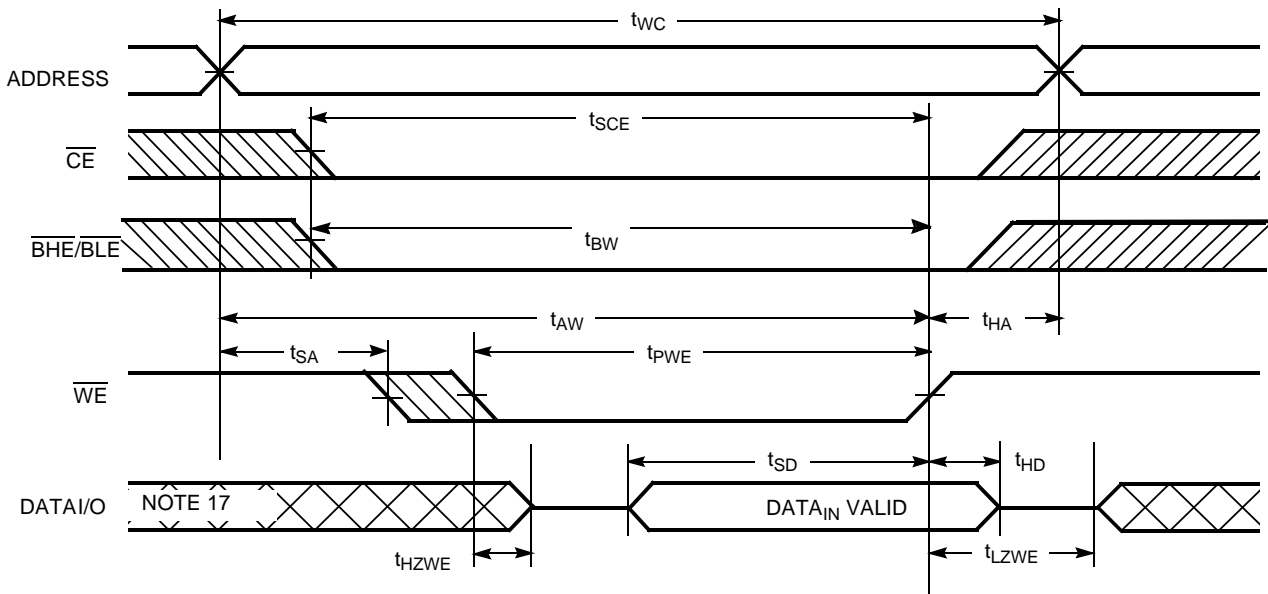


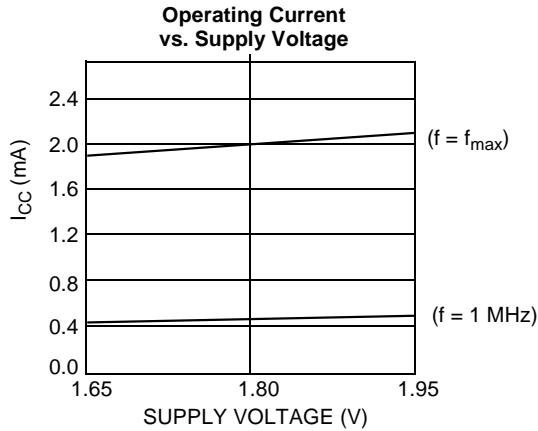### Write Cycle No. 4 ($\overline{BHE}/\overline{BLE}$ Controlled, $\overline{OE}$ LOW)[16]
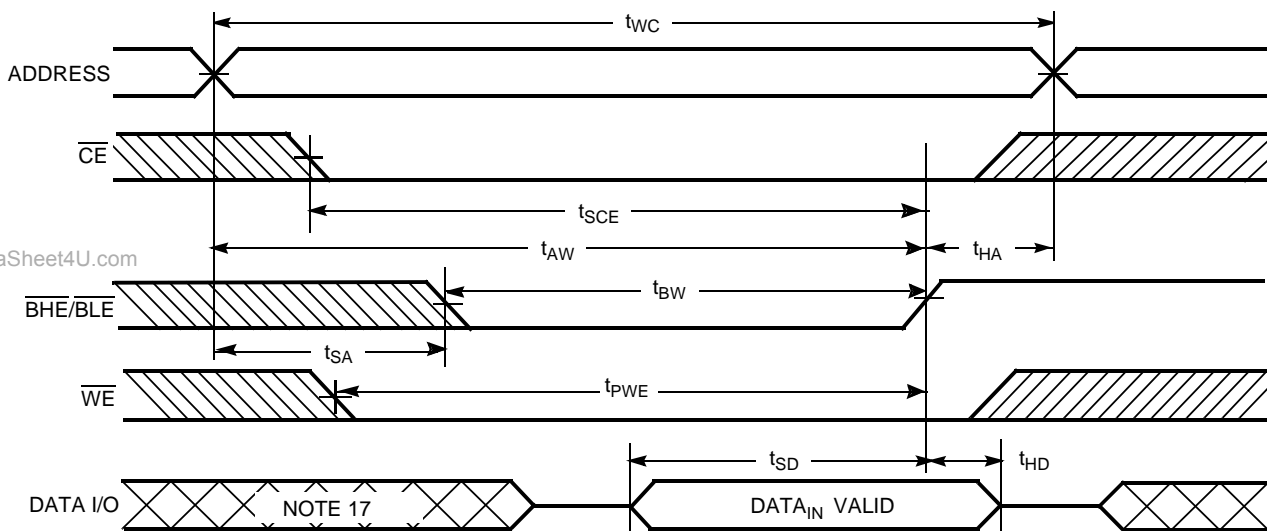


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## Typical DC and AC Characteristics

(Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC}$ Typ, $T_A = 25°C$.)

**Operating Current vs. Supply Voltage**

(f = $f_{max}$)

(f = 1 MHz)

**Standby Current vs. Supply Voltage**

**Access Time vs. Supply Voltage**

## Truth Table

| CE | WE | OE | BHE | BLE | Inputs/Outputs | Mode | Power |
|----|----|----|-----|-----|----------------|------|-------|
| H | X | X | X | X | High Z | Deselect/Power-Down | Standby ($I_{SB}$) |
| X | X | X | H | H | High Z | Deselect/Power-Down | Standby ($I_{SB}$) |
| L | H | L | L | L | Data Out (I/O$_O$–I/O$_{15}$) | Read | Active ($I_{CC}$) |
| L | H | L | H | L | Data Out (I/O$_O$–I/O$_7$); I/O$_8$–I/O$_{15}$ in High Z | Read | Active ($I_{CC}$) |
| L | H | L | L | H | Data Out (I/O$_8$–I/O$_{15}$); I/O$_0$–I/O$_7$ in High Z | Read | Active ($I_{CC}$) |
| L | H | H | L | L | High Z | Output Disabled | Active ($I_{CC}$) |
| L | H | H | H | L | High Z | Output Disabled | Active ($I_{CC}$) |
| L | H | H | L | H | High Z | Output Disabled | Active ($I_{CC}$) |
| L | L | X | L | L | Data In (I/O$_O$–I/O$_{15}$) | Write | Active ($I_{CC}$) |
| L | L | X | H | L | Data In (I/O$_O$–I/O$_7$); I/O$_8$–I/O$_{15}$ in High Z | Write | Active ($I_{CC}$) |
| L | L | X | L | H | Data In (I/O$_8$–I/O$_{15}$); I/O$_0$ –I/O$_7$ in High Z | Write | Active ($I_{CC}$) |

## Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 70 | WCMB4016R4X-FF70 | FB48A | 48-Ball Fine Pitch BGA | Industrial |

## Package Diagrams

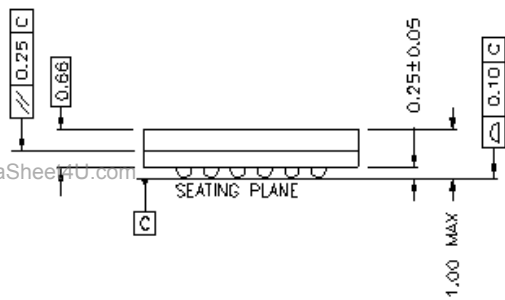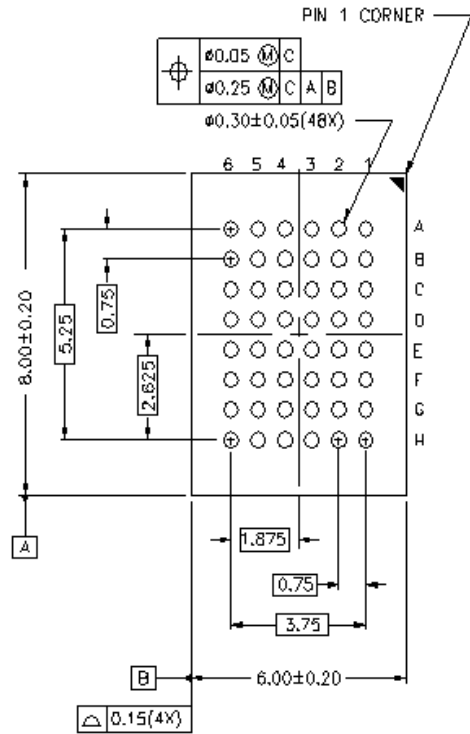### 48-Ball (6.0 mm x 8.0 mm x 1.0 mm) Fine Pitch BGA, FB48A

Top View                                                                                    Bottom View
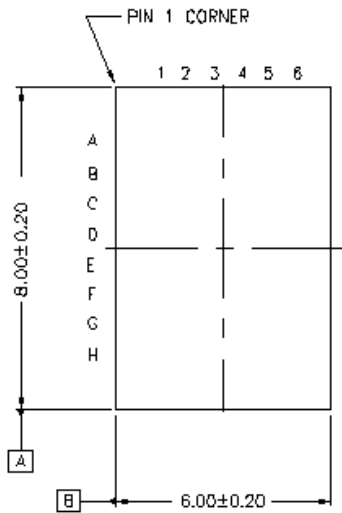
| Document Title: WCMB4016R4X, 256K x 16 Static RAM | | | | | |
|---|---|---|---|---|---|
| **REV.** | **Spec #** | **ECN #** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 38-14012 | 115228 | 1/17/02 | MGN | New Data Sheet |

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